Implementation of an open-source design Flow for nano scale Chip Design/Manufacturing Process at Universidad del valle de Guatemala

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***Abstract*—This paper carries out the Tiny Tapeout initiative with 4 verilog designs,() with the intention to fully utilize and comprehend this open-source design flow for chip design/manufacturing and to leave proper documentation for future students to take advantages of this new and innovative processes to enter in the semiconductor realm. We had the opportunity to receive the courses required to be eligible for**

***Index Terms*—IEEE, IEEEtran, journal, LaTeX, paper, template.**

I. Introduction

The semiconductor industry -chip/microchip industry- holds a significant share in the market owing to its rapid strides in technological advancement. Over the years, there has been a noticeable trend of various companies pushing the limits of nanoscale technology, driving innovation within the sector [1]. This remarkable progress has been made possible primarily by two major aspects: on one hand there are super specialised chip manufacturing hardware, that bring to life the digital representation of the chip. On the other hand there are very specialised software tools that are made by very specific software developing companies, who are responsible for making said digital representation of the chip.

Intel, Apple, AMD, Samsung and similar semiconductor industry giants have the financial resources to invest in these specialised tools and software, which are often costly due to their advanced capabilities and precision engineering [7-8]. These tools facilitate tasks such as layout design, simulation, verification, and manufacturing of semiconductor chips. By utilising such tools, these companies can explore innovative concepts, test them in virtual as well as physical environments, and fine-tune their designs before misproduction.

Additionally, software development companies like Synopsys, Cadence, and Mentor Graphics play a crucial role in shaping the semiconductor landscape [11]. They continuously develop and refine software that cater to the intricate needs of chip designers and manufacturers [12]. These tools streamline workflows, improve design accuracy, and optimise manufacturing processes, ultimately leading to the production of high-quality chips that power a wide array of electronic devices, from smartphones, laptops, autonomous vehicles to sophisticated industrial equipment, all the way to life-critical biomedical equipment, satellites, and space shuttles [10].

However, it's worth acknowledging that while the semiconductor industry thrives on innovation, learning about the intricacies of integrated circuit design and manufacturing processes can be very difficult [13,15]. This challenge is one of the key hurdles that stems from the gap in access to chip design and manufacturing processes between industry and academia. The tools and resources used by technology giants already mentioned are often proprietary and come with substantial financial barriers. This fination challenge creates a division between the cutting-edge practices employed in the industry and the educational resources available in academic settings [13].

Students and researchers in academia might encounter difficulties in gaining hands-on experience with the most up-to-date tools and techniques used in the semiconductor industry. Moreover, access to advanced fabrication facilities and sophisticated design software can be limited, potentially hindering their ability to fully grasp the complexities of modern chip design. The rapid pace of innovation in the industry can also make it challenging for academic curricula to keep up with the latest developments, further emphasising the disparity between theoretical knowledge and practical application.

Efforts are being made to bridge this gap by fostering collaborations between industry and academia [16]. Some companies offer educational programs, internships, and partnerships with universities, enabling students and researchers to gain exposure to state-of-the-art tools and real-world design challenges [19]. Moreover, open-source initiatives and shared research facilities aim to provide broader access to resources that were once exclusive to industry giants. By narrowing the division between industry and academia, aspiring chip designers and researchers can better prepare themselves for the demands of the semiconductor landscape [18].

As the semiconductor industry propels forward with innovation, the challenge lies in ensuring that the knowledge and expertise surrounding integrated circuit design and manufacturing are accessible to all. Bridging the gap between the tools and processes utilised in industry and those available in academic settings will be crucial for nurturing the next generation of skilled professionals who can contribute to the ongoing advancements in the semiconductor field. In this work, an open-source environment for a design flow for chip

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manufacturing will be deployed at Universidad del Valle de Guatemala to shorten the gap between industry and academia.

II. Experimental

In the following figured (1), the main stepes of this work are portrayed.

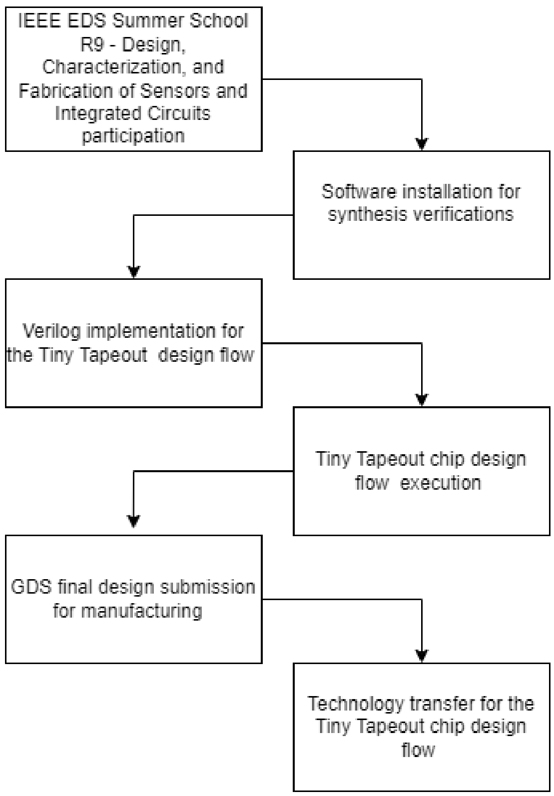


Fig. 1: Experimental Model Blocks

A. IEEE EDS Summer School R9 - Design, Characterization, and Fabrication of Sensors and Integrated Circuits participation

In June 2023 two senior students from the Electronics Engineering department at Universidad del Valle de Guatemala were granted scholarships to attend the ”2023 IEEE EDS Summer School R9” in Puebla, Mexico Throughout this enlightening summer program, a wide array of topics were addressed, ranging from insights of former students who work in the field, to several educational tools provided by one of the industry leaders; Synopsys. A significant message stood out: Microchip design and fabrication industry is so complex, so dynamic, and so expensive due to infrastructure, human resources, etc. so that it becomes extremely challenging to almost impossible for academia to keep up with it. During the program, the gap between industry capability and academic resources became evident as the alumni shared their experiences. Some of the former students highlighted that they had encountered setbacks in their projects due to challenges in installation or upkeep of some tools within the expansive realm of semiconductor technology. Notably, a few even mentioned that a lack of infrastructure and limited time had led to the unfortunate loss of grants they had secured for their projects. In the program, there were also discussions about new open-source tools such as Wokwi, designed to facilitate learning about logical circuitry. The Efabless initiative was another topic, that was introduce as a private semiconductor fabrication company, but the one that left the most significant impact was Tiny Tapeout because it closes de gap between the complexity behind the chip design and manufacturing in industry and the resources, time, and knowledge typically available in academia. This tool stood out for its adoption is further supported by a multi-purpose wafer and the cost-effectiveness of chip production. Typically, one of the challenges in academia involves acquiring the necessary computing power to run complex design tools. However, Tiny Tapeout has tackled this issue by providing its own cloud computing infrastructure, effectively reducing the demand for high computational resources. On the other hand, the installation of some of the highly advanced programs use in the industry are very complex using authentication servers to secure their tools, however Tiny Tapeout has manage to set their installation tool process very straightforward using only three steps. It's worth mentioning that Tiny Tapeout has its own website where you can consult any doubt its installer might have, and it has several channels of communication. The aim of the Tiny Tapeout initiative is not to take over the semiconductor industry but to give students the knowledge and experience of working in this ample field, moreover, offer students the experience of taking a digital design all the way to semiconductor fabrication.

B. Software installation for synthesis verifications

To verify that both logical and physical synthesis align with the Verilog files, the installation of an open-source integrated circuit design flow called OpenLane was performed. To use it, a virtual machine with Ubuntu 22 was set up, and the necessary prerequisites, including Python 3, git, make, and Docker, were installed. The GitHub repository containing OpenLane was cloned and compiled. It was confirmed that OpenLane operated correctly by synthesizing a 4-bit adder.

C. Verilog implementation for the Tiny Tapeout design flow

This section introduces the Verilog implementation within the framework of Tiny Tapeout, a project dedicated to generating chip layouts from Verilog files. In this context, we will delineate the four distinct designs produced, providing comprehensive descriptions of the modules and their respective behaviors.

1) Multi stage path for delay measurements: The core of the module featured an approach to creating a ring oscillator. Although it was initially intended to utilize cascaded NOT gates, it was observed that the synthesizer, under the constraints of the Tiny Tapeout design flow, may replace these gates with buffers. As a result, the oscillatory behavior was expectedly altered. Nevertheless, the module's ring oscillator function was realized through a sequence of logical operations involving AND gates and inverters, forming a feedback loop. The logical signals EN and EN_2 served as inputs to an AND_2 module, generating a waveform represented by W_1. Subsequently, this waveform traversed a series of inverters (tt_prim_inv modules), resulting in the generation of W_2, W_3, and cyclically returning to W_1. While this configuration may not conform precisely to the original design intent, it offers a valuable educational opportunity to explore gate delays and their implications in digital circuitry when compared to theoretical calculations.

2) ASCII Text Printer Circuit: A Verilog module was designed to function as a text printing system capable of displaying two distinct texts, which are selected through an external signal. The module employs an internal counter synchronized with the clock to determine the specific ASCII character displayed based on the selection signal and the counter value. The output is provided through the output pins in ASCII format.

3) Implementation of the Pong game: The Verilog code, pong_neopixel.v, with the main module ”tt_um_pong_neopixel”, has been developed with the purpose of implementing a version of the Pong game on a Neopixel pixel matrix. This design has been conceived as an example of an interactive and playful application of programmable digital hardware. The ”tt_um_pong_neopixel” module consists of several inputs and outputs intended to control the game, including player input signals, start signals, and outputs to manage the Neopixel matrix, along with clock and reset signals. To ensure the stability of the input signals, ”debounce” modules have been implemented. The game logic includes the management of the movement of the players’ paddles and the ball, as well as collision detection and game reset when appropriate. In addition, logic has been developed to generate Neopixel signals that control the display on the matrix, allowing player interaction. This design also incorporates counters to track the sending of data to the matrix and appropriately selects whether LEDs should be turned on or off based on the position of the ball and paddles.

4) Pulse Width Modulation Generator: The Verilog code, pwm_generator.v, with the main module ”tt_um_pwm”, is designed to generate a pulse width modulation (PWM) signal controlled by buttons. The module allows the duty cycle of the PWM signal to be increased or decreased via buttons. To ensure a reliable reading of the buttons, debounce logic is implemented that generates a slow clock signal (slow_clk_enable).

D. Tiny Tapeout chip design flow execution

The execution of the Tiny Tapeout chip design flow begins with a series of essential steps. First it is necessary to fork the example repository provided by the Tiny Tapeout project. Once this step is completed, enabling the repository’s capability to perform actions is crucial, as it allows for the automation of subsequent processes. To ensure the project’s proper execution, several key tasks must be carried out. First all Verilog files must be located in the ”src” folder. Additionally, the ”info.yaml” file must be filled out with relevant information, including the Verilog files that constitute the design, the main design module, the authors, a project description, and, if applicable, the clock frequency. These steps are fundamental to ensuring an effective design flow and the correct implementation of chips in Tiny Tapeout.

E. GDS final design submission for manufacturing

In the final submission phase of the GDS design for manufacturing, a series of crucial steps were undertaken to ensure the integrity and accuracy of the delivered information. First a comprehensive review of all relevant repositories was conducted with the aim of identifying and rectifying any errors that may have existed in their execution. Subsequently, the provided form by Latin Practice was completed, requiring essential details about the repositories, including author names and direct links to the referred repositories. It is noteworthy that this form-filling process was rigorously carried out before the stipulated deadline, which was September 5th. These steps were taken to ensure the consistency and precision of the information provided in this critical stage of the GDS design project.

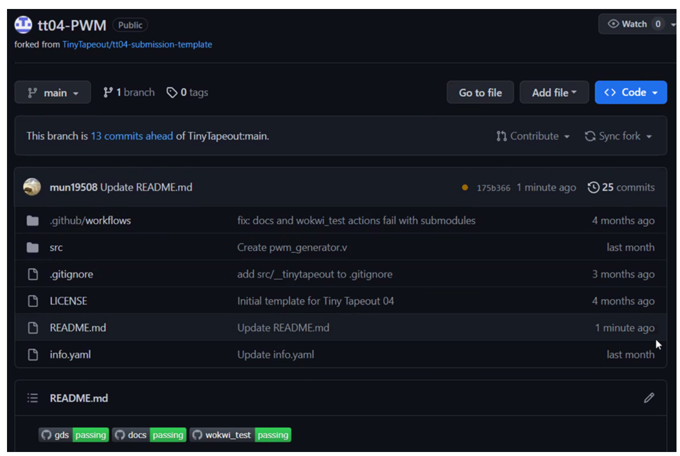


Fig. 2: Verified Pulse Width Modulation Generator Verilog

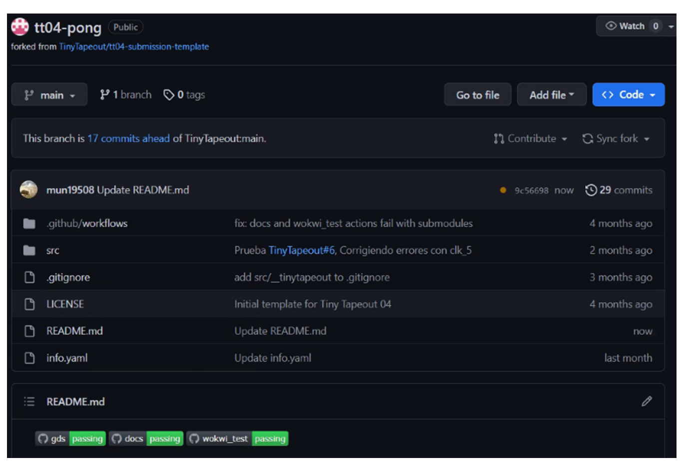


Fig. 3: Verified Pong game Verilog

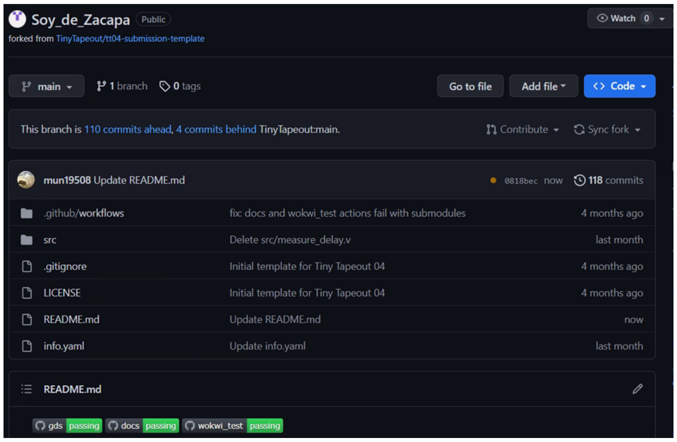


Fig. 4: Verified ASCII Text Printer Circuit Verilog

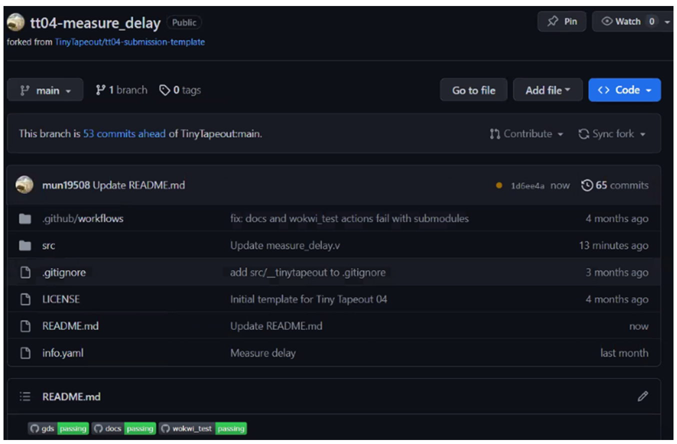


Fig. 5: Verified Multi stage path for delay measurements Verilog

F. Technology transfer for the Tiny Tapeout chip design flow

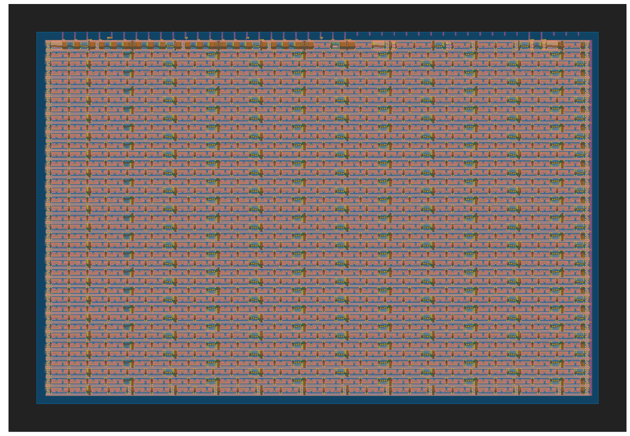
The true purpose behind this paper is to push the boundaries of understanding the semiconductor fabrication field at Universidad del Valle de Guatemala. The proper documentation of the knowledge acquired by all the members that were involved on this work is essential for future students. Therefore, Video tutorials and documents were made for students to replicate the Tiny tapeout program to take any design from a fully digital verilog implemented circuit all the way to a physical integrated circuit.

III. Results

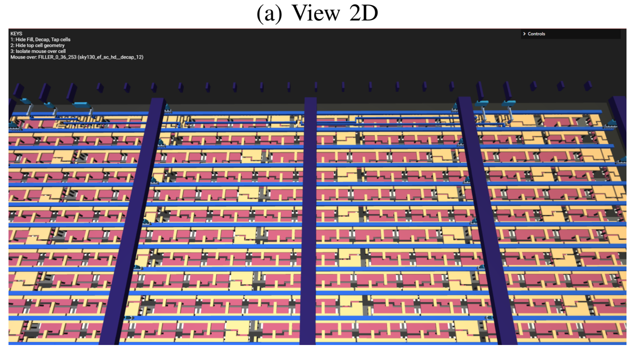
In this section, we present the final results for each individual verilog filed we have submitted:

A. Multi stage path for delay measurements

The multi stage path was submitted with no errors, and the final layout is shown in figure 6. The final layout is composed of 4 stages, each stage has 4 inverters and 4 transmission gates.



(a) View 2D

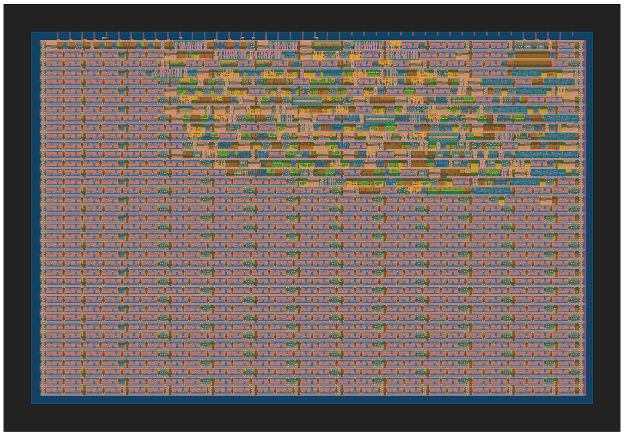


(b) View 3D

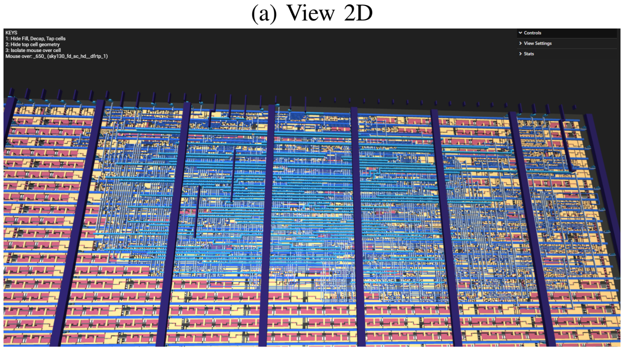
Fig. 6: Multi stage path for delay measurements layout

B. ASCII Text Printer Circuit

The circuit ASCII text printer was submitted with no errors, and the final layout is shown in figure 7.



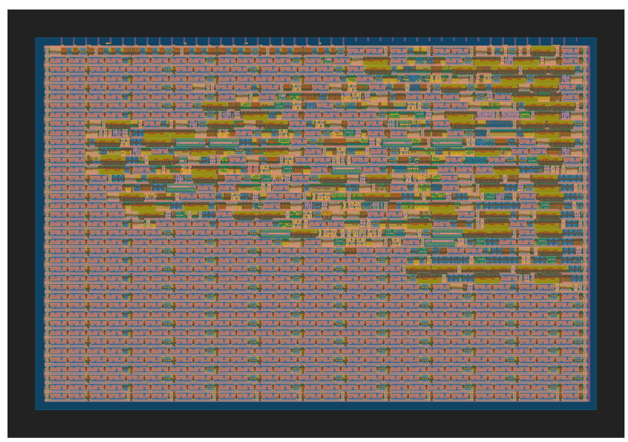
(a) View 2D



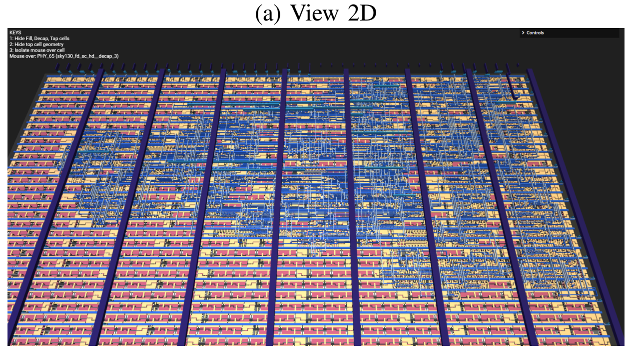
(b) View 3D

Fig. 7: ASCII text printer circuit layout

C. Implementation of the Pong game



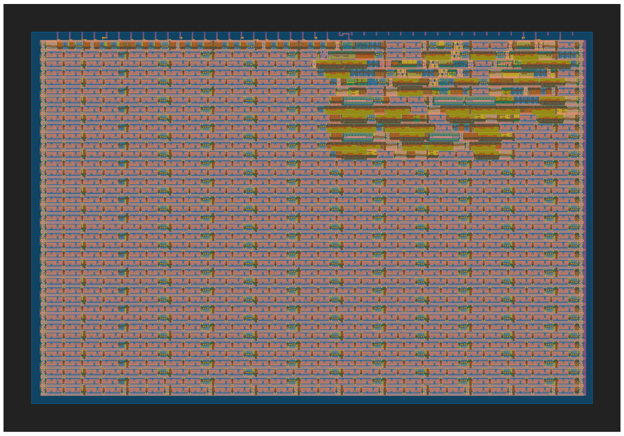
(a) View 2D



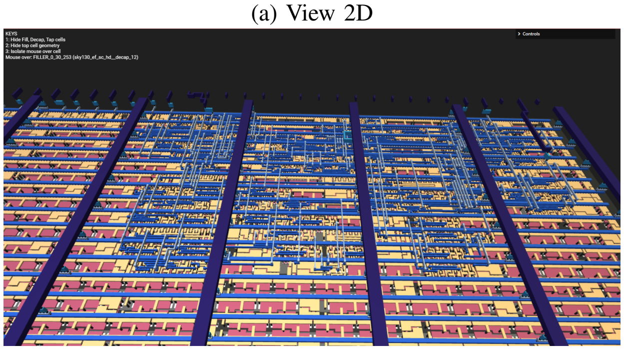
(b) View 3D

Fig. 8: The Pong game layout

D. Pulse Width Modulation Generator



(a) View 2D



(b) View 3D

Fig. 9: Pulse Width Modulation generator layout

Circuit	Porcentage utilize(%)
Multi stage path for delay measurements	0.63
ASCII Text Printer Circuit	17.87
Implementation of the Pong game	28.82
Pulse Width Modulation Generator	9.59

TABLE I: Porcentaje utilize in length of waver per circuit

IV. Conclusion

Appendix A
Proof of the First Zonklar Equation

Appendix one text goes here.

Appendix B

Appendix two text goes here.

Acknowledgment

The authors would like to thank...

References

[1] H. Kopka and P. W. Daly, *A Guide to LATEX*, 3rd ed. Harlow, England: Addison-Wesley, 1999.

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Michael Shell Biography text here.

John Doe Biography text here.

Jane Doe Biography text here.