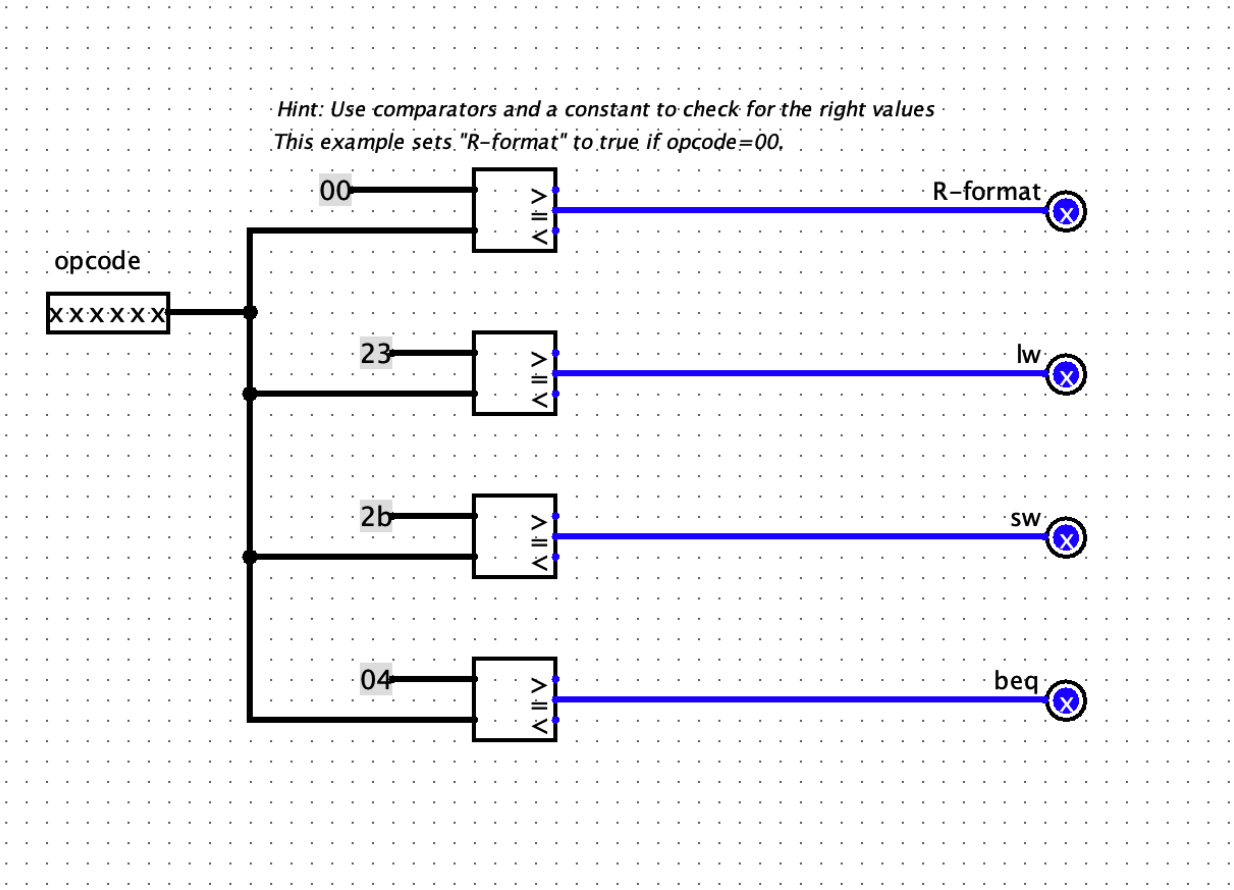
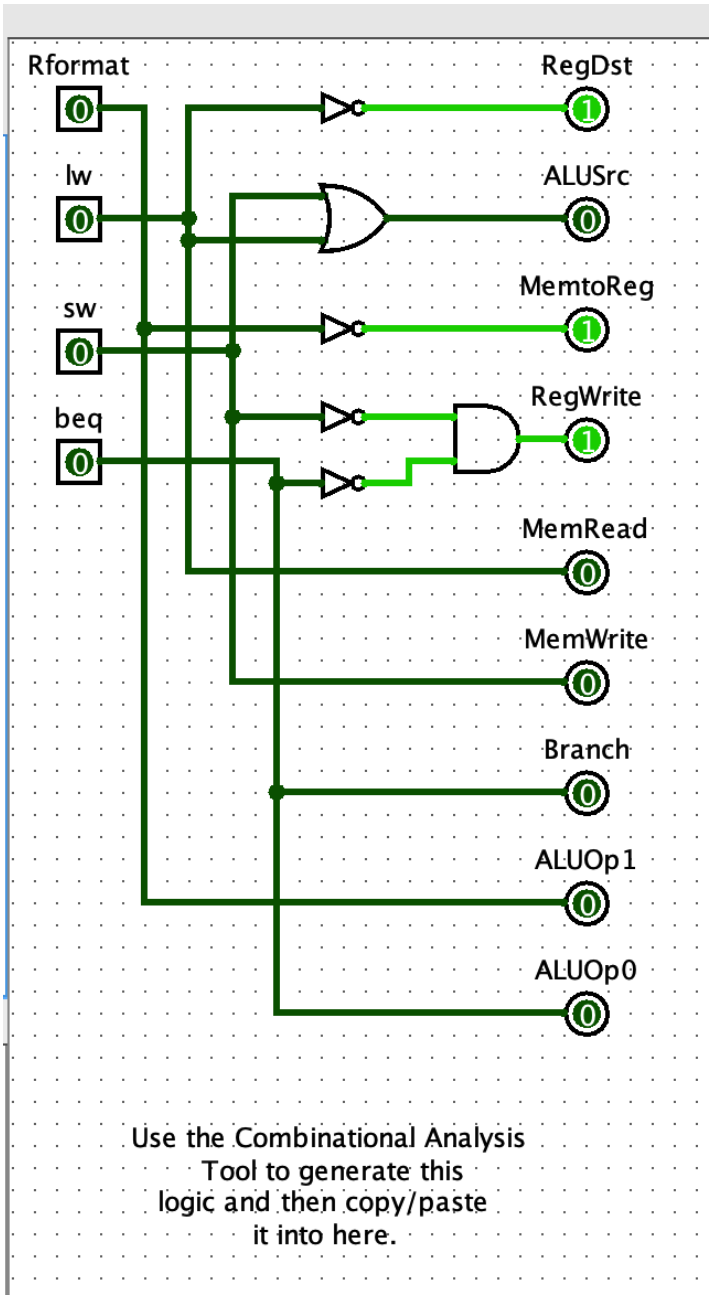
TODO 1:



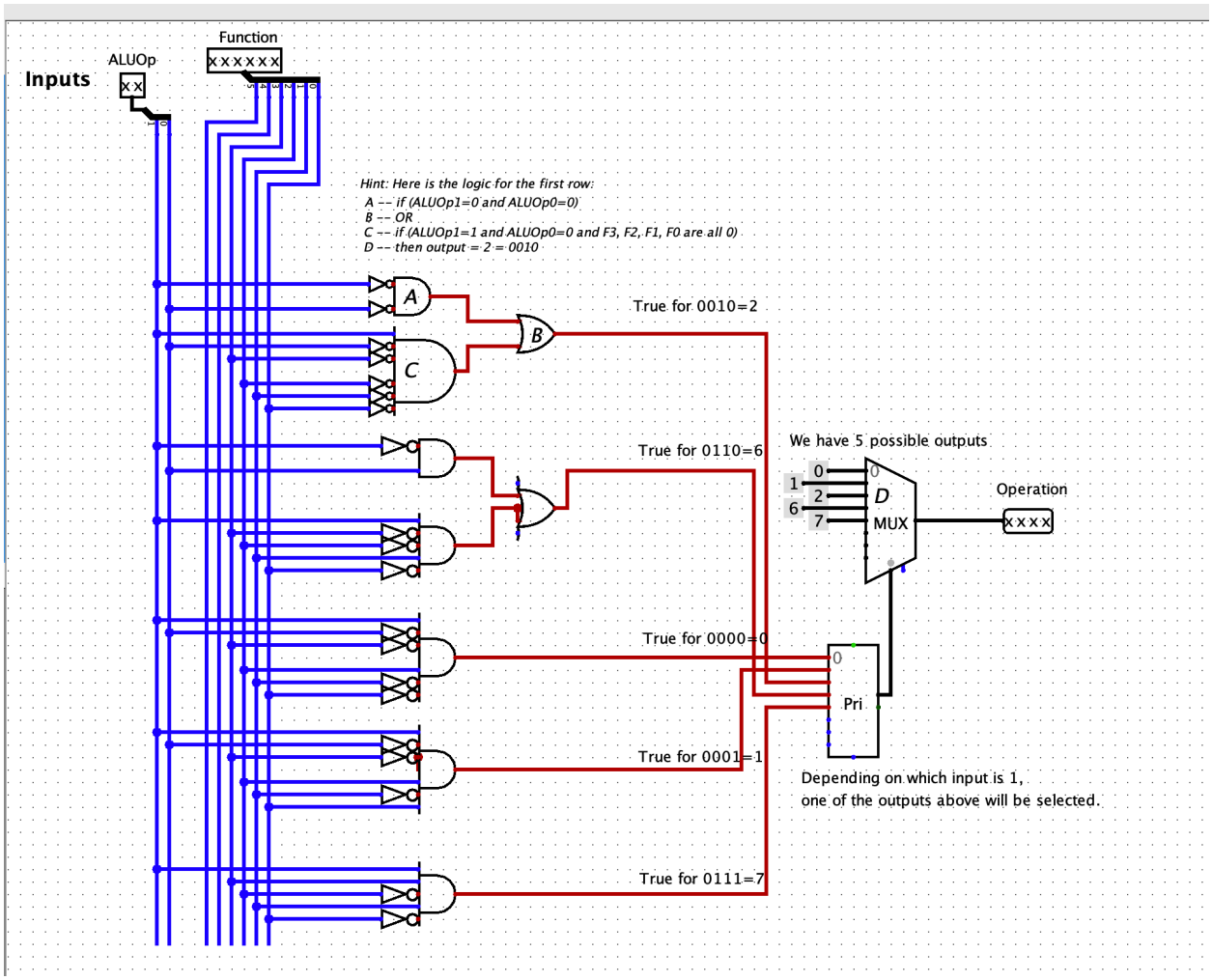
TODO 2:

Output	R-format	Lw	Sw	Beq
RegDst	1	0	X	X
ALUSrc	0	1	1	0
MemtoReg	0	1	X	X
RegWrite	1	1	0	0
MemRead	0	1	0	0
MemWrite	0	0	1	0
Branch	0	0	0	1
ALUOp1	1	0	0	1
ALUOp0	0	0	0	1

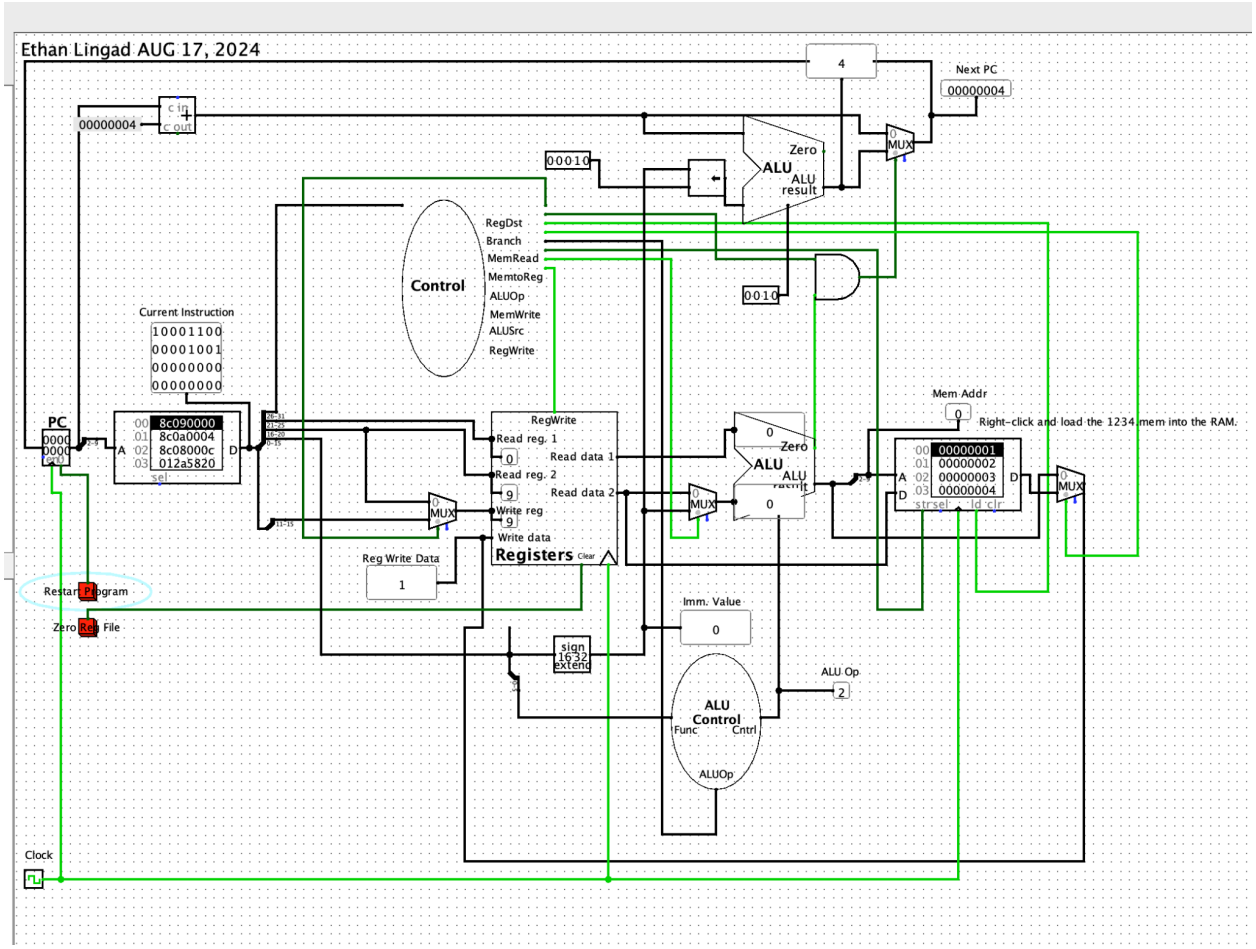
TODO 3:


Rformat
lw
sw
beq
RegDst
ALUSrc
MemtoReg
RegWrite
MemRead
MemWrite
Branch
ALUOp1
ALUOp0
Use the Combinational Analysis
Tool to generate this
logic and then copy/paste
it into here.

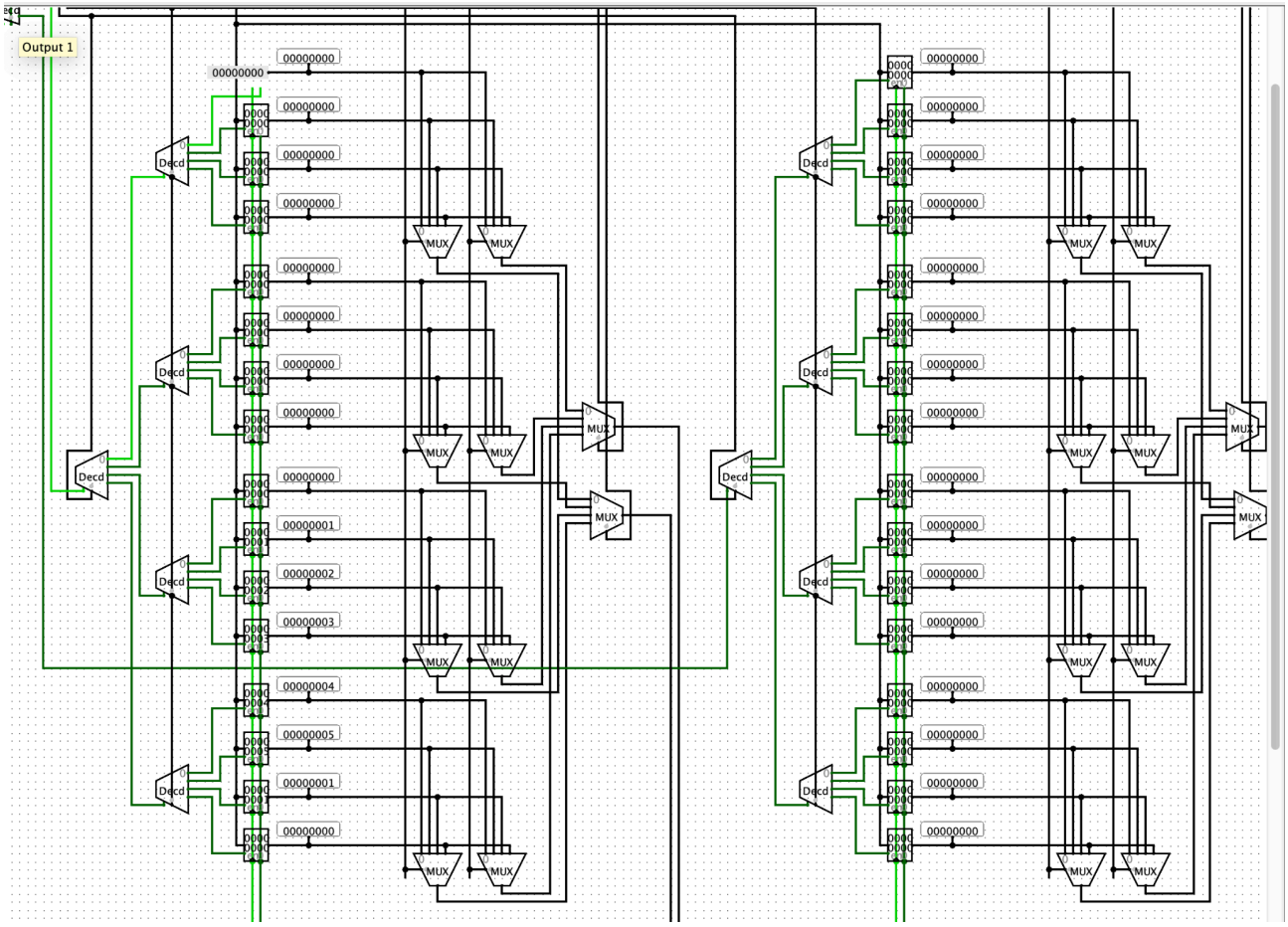
TODO 4:


Inputs
ALUOp
xx
Function
xxxxxx
Hint: Here is the logic for the first row:
A -- if (ALUOp1=0 and ALUOp0=0)
B -- OR
C -- if (ALUOp1=1 and ALUOp0=0 and F3, F2, F1, F0 are all 0)
D -- then output = 2 = 0010
A
B
C
True for 0010=2
True for 0110=6
True for 0000=0
True for 0001=1
True for 0111=7
We have 5 possible outputs
0
1
2
6
7
D
MUX
Operation
xxxx
Pri
Depending on which input is 1,
one of the outputs above will be selected.

TODO 5:


Ethan Lingad AUG 17, 2024
4
Next PC
00000004
00000004
c_in
c_out
00010
Zero
ALU
ALU result
MUX
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Control
0010
Current Instruction
10001100
00001001
00000000
00000000
Mem Addr
0
Right-click and load the 1234 mem into the RAM.
PC
0000
0000
clock
00 8c090000
01 8c0a0004
02 8c08000c
03 012a5820
A
D
sel
RegWrite
Read reg. 1
0
Read data 1
Read reg. 2
9
Read data 2
Write reg
9
Write data
Registers
Clear
Reg Write Data
1
Restart Program
Zero Reg File
Imm. Value
0
sign 16 32 extend
ALU Op
2
ALU Control
Func
Cntrl
ALUOp
00 00000001
01 00000002
02 00000003
03 00000004
strsel
ld
clr
Clock

TODO 6:


Output 1
Decd
MUX
00000000
00000001
00000002
00000003
00000004
00000005