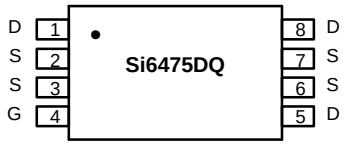
P-Channel 12-V (D-S) MOSFET

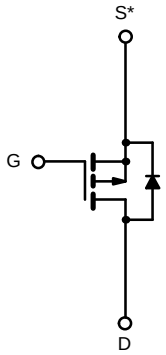
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–12	0.011 @ V_{GS} = –4.5 V	–10
	0.0135 @ V_{GS} = –2.5 V	–9
	0.017 @ V_{GS} = –1.8 V	–8

TrenchFET® Power MOSFETs

TSSOP-8



Top View



P-Channel MOSFET

* Source Pins 2, 3, 6 and 7 must be tied common.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		**Symbol**	**10 secs**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	–12		V
Gate-Source Voltage		V_{GS}	±8		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	–10	–7.8	A
	T_A = 70°C		–8	–6.2	
Pulsed Drain Current (10 μs Pulse Width)		I_{DM}	–30		
Continuous Source Current (Diode Conduction)[a]		I_S	–1.5	–0.95	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.75	1.08	W
	T_A = 70°C		1.14	0.69	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	55	70	°C/W
	Steady State		95	115	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	35	45	

Notes
a. Surface Mounted on 1” x 1” FR4 Board.

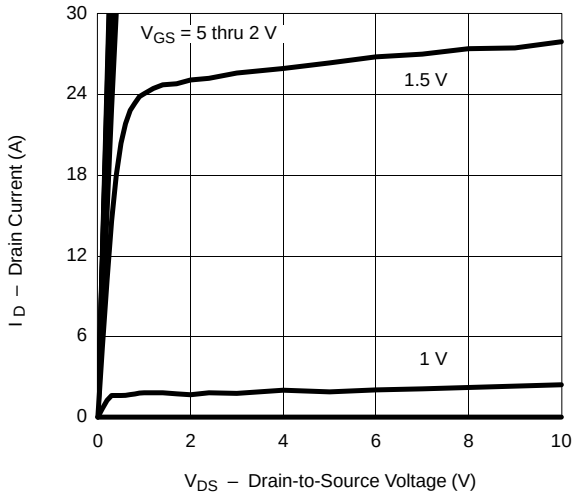
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –5 mA	–0.45			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –9.6 V, V_{GS} = 0 V			–1	µA
		V_{DS} = –9.6 V, V_{GS} = 0 V, T_J = 70°C			–10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = –5 V, V_{GS} = –4.5 V	20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = –4.5 V, I_D = –10 A		0.009	0.011	Ω
		V_{GS} = –2.5 V, I_D = –9 A		0.011	0.0135	
		V_{GS} = –1.8 V, I_D = –8 A		0.014	0.017	Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = –15 V, I_D = –10 A		50		S
Diode Forward Voltage[a]	V_{SD}	I_S = –1.5 A, V_{GS} = 0 V		–0.68	–1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –10 A		49.5	70	nC
Gate-Source Charge	Q_{gs}			7.7		
Gate-Drain Charge	Q_{gd}			8.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –6 V, R_L = 6 Ω I_D ≅ –1 A, V_{GEN} = –4.5 V, R_G = 6 Ω		56	85	ns
Rise Time	t_r			62	100	
Turn-Off Delay Time	$t_{d(off)}$			300	450	
Fall Time	t_f			185	270	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –1.5 A, di/dt = 100 A/µs		90	150	

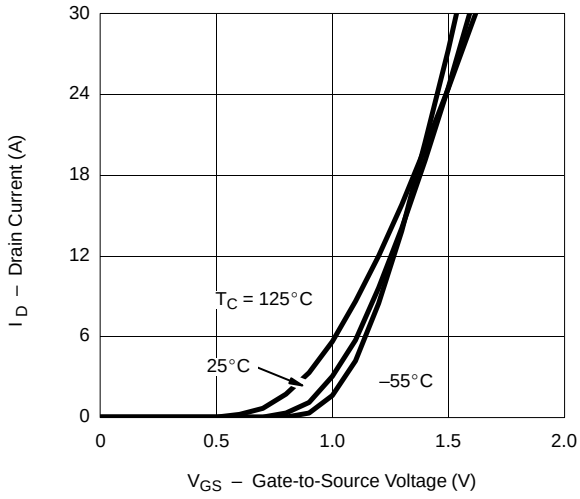
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

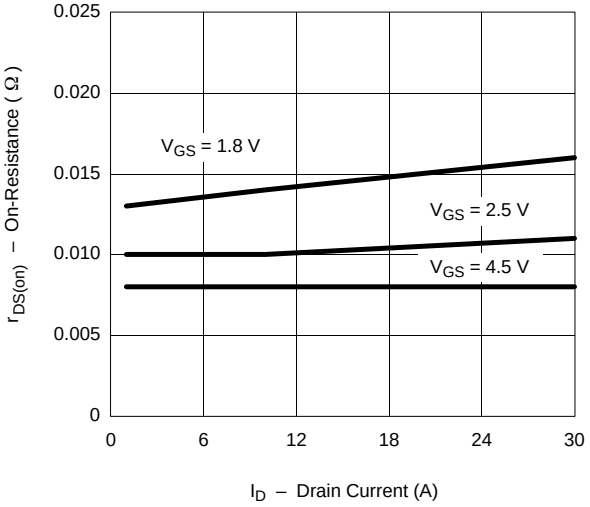


Transfer Characteristics

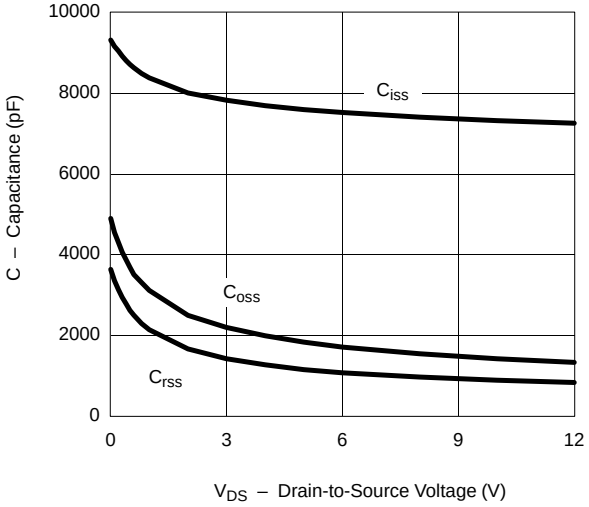


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

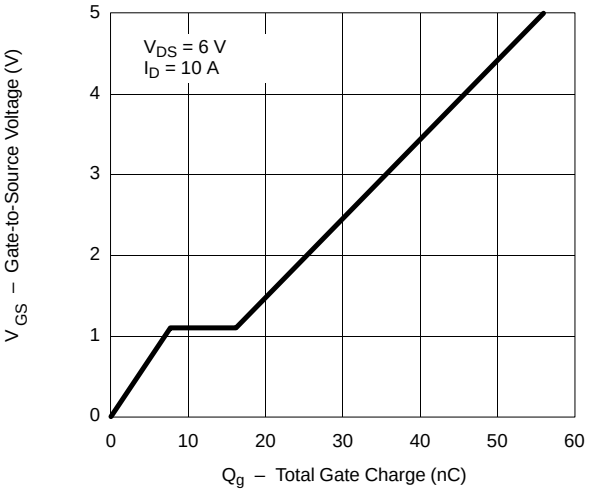
On-Resistance vs. Drain Current



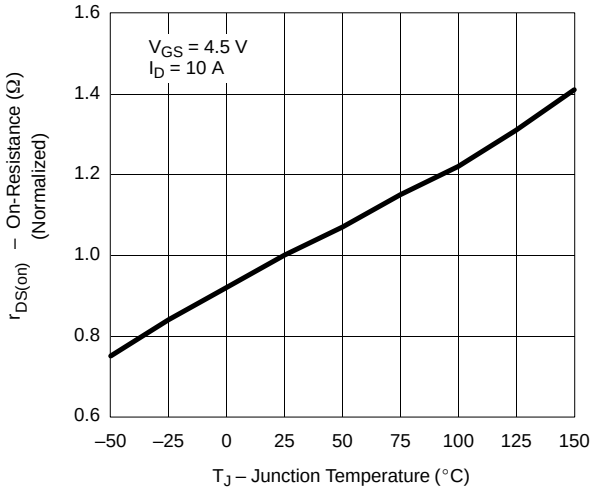
Capacitance



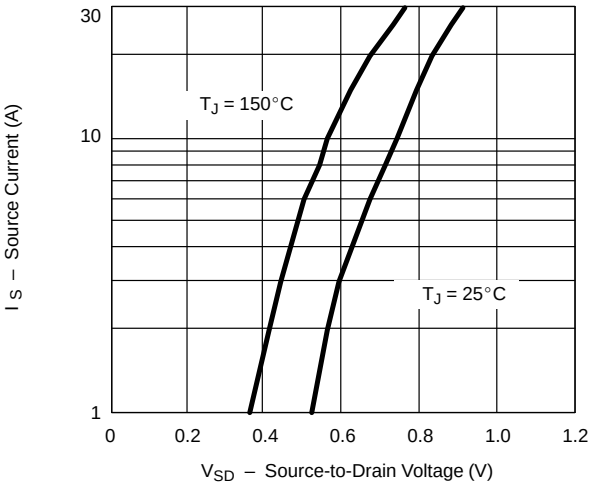
Gate Charge



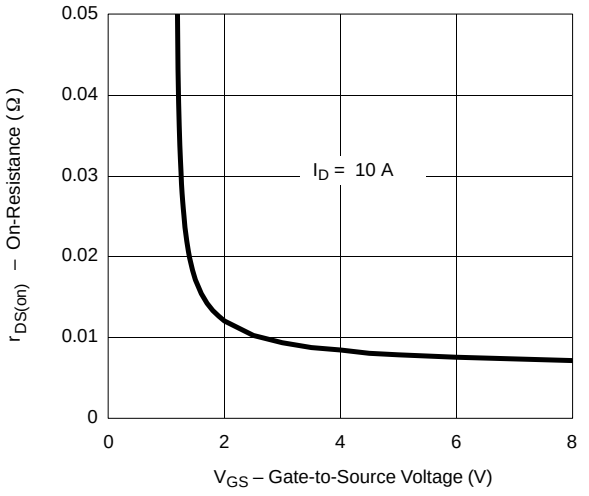
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

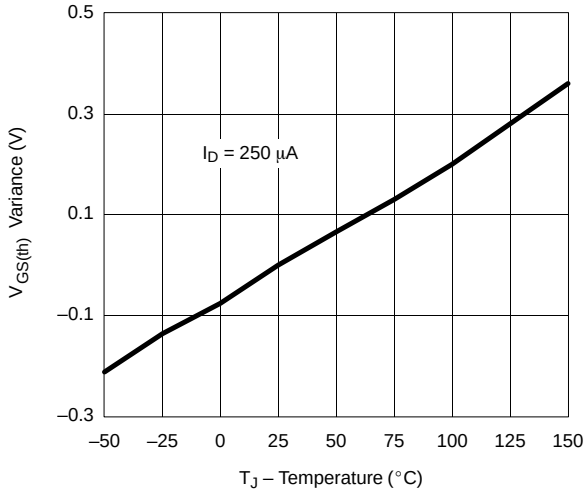


On-Resistance vs. Gate-to-Source Voltage

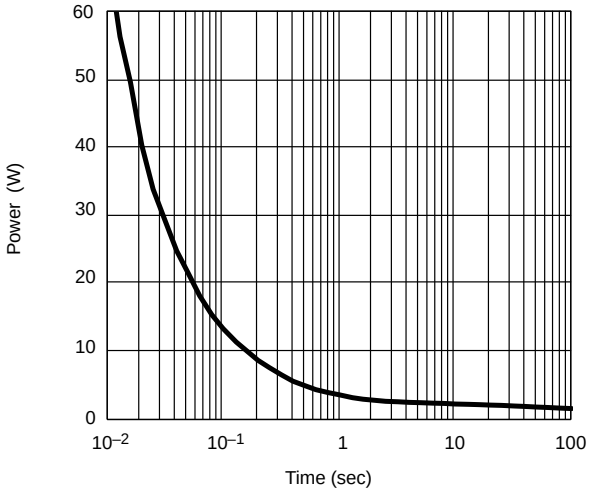


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

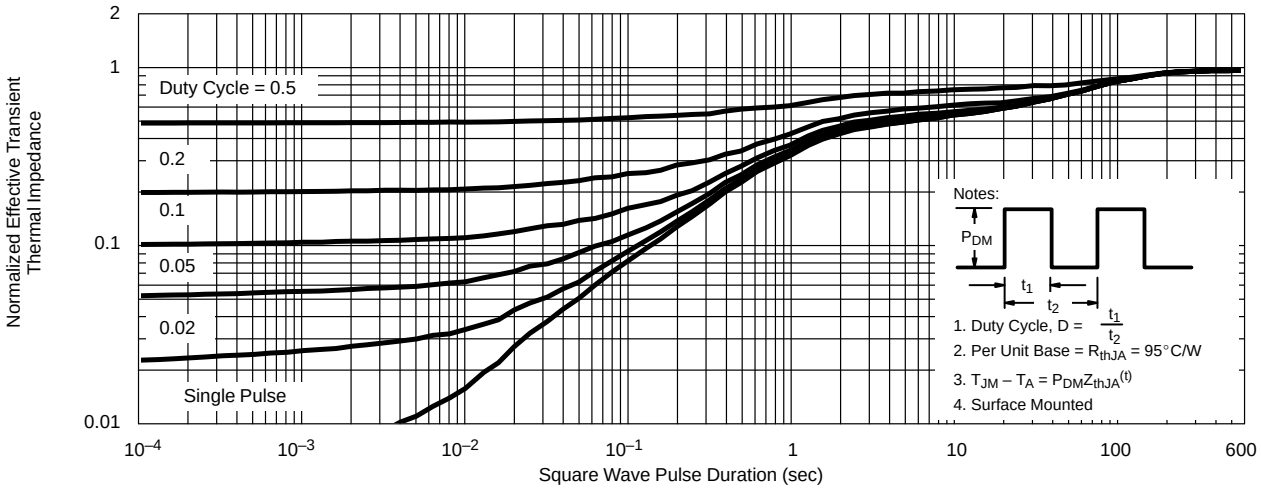
Threshold Voltage



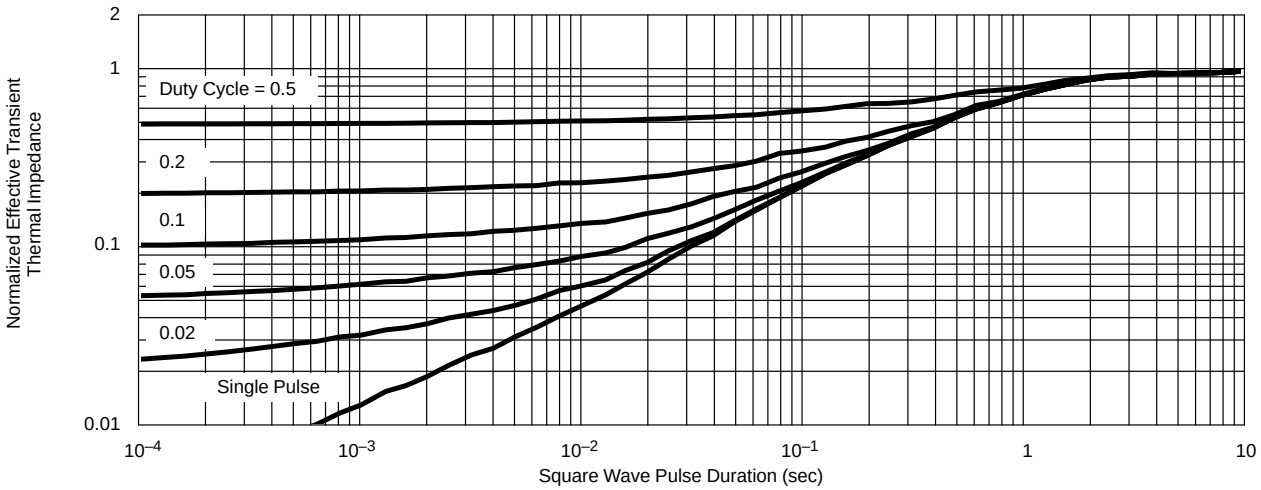
Single Pulse Power, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



Document Number: 71294
S-01889—Rev. A, 28-Aug-00