International
IOR Rectifier

PD - 93849C

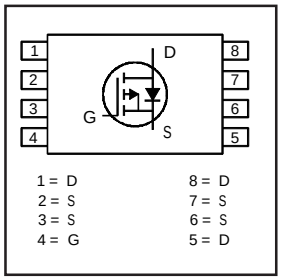
PROVISIONAL

IRF7702

HEXFET® Power MOSFET

- Ultra Low On-Resistance
- -1.8V Rated
- P-Channel MOSFET
- Very Small SOIC Package
- Low Profile (< 1.1mm)
- Available in Tape & Reel

V_{DSS}	$R_{DS(on)}$ max	I_D
-12V	0.014@V_{GS} = -4.5V	-8.0A
	0.019@V_{GS} = -2.5V	-7.0A
	0.027@V_{GS} = -1.8V	-5.8A



Description

HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the ruggedized device design, that International Rectifier is well known for, provides thedesigner with an extremely efficient and reliable device for battery and load management.

The TSSOP-8 package has 45% less footprint area than the standard SO-8. This makes the TSSOP-8 an ideal device for applications where printed circuit board space is at a premium. The low profile (<1.1mm) allows it to fit easily into extremely thin environments such as portable electronics and PCMCIA cards.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain- Source Voltage	-12	V
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -4.5V	±8.0	A
I_D @ T_C = 70°C	Continuous Drain Current, V_{GS} @ -4.5V	±7.0	
I_{DM}	Pulsed Drain Current ①	±70	
P_D @T_C = 25°C	Power Dissipation	1.5	W
P_D @T_C = 70°C	Power Dissipation	0.96	
	Linear Derating Factor	0.01	W/°C
V_{GS}	Gate-to-Source Voltage	± 8.0	V
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

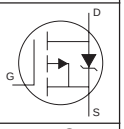
	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient③	83	°C/W

6/19/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-12	—	—	V	V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.007	—	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.014	Ω	V_{GS} = -4.5V, I_D = -8.0A ②
		—	—	0.019		V_{GS} = -2.5V, I_D = -7.0A ②
		—	—	0.027		V_{GS} = -1.8V, I_D = -5.8A ②
$V_{GS(th)}$	Gate Threshold Voltage	-0.45	—	-1.2	V	V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	26	—	—	S	V_{DS} = -10V, I_D = -8.0A
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	µA	V_{DS} = -12V, V_{GS} = 0V
		—	—	-25		V_{DS} = -9.6V, V_{GS} = 0V, T_J = 70°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V_{GS} = -8.0V
	Gate-to-Source Reverse Leakage	—	—	100		V_{GS} = 8.0V
Q_g	Total Gate Charge	—	54	81	nC	I_D = -8.0A
Q_{gs}	Gate-to-Source Charge	—	7.8	12		V_{DS} = -9.6V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	15	23		V_{GS} = -4.5V②
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	V_{DD} = -6.0V
t_r	Rise Time	—	21	—		I_D = -1.0A
$t_{d(off)}$	Turn-Off Delay Time	—	320	—		R_D = 6.0Ω
t_f	Fall Time	—	250	—		R_G = 6.0Ω ②
C_{iss}	Input Capacitance	—	3470	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1040	—		V_{DS} = -10V
C_{rss}	Reverse Transfer Capacitance	—	670	—		f = 1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-1.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-70		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	T_J = 25°C, I_S = -1.5A, V_{GS} = 0V ②
t_{rr}	Reverse Recovery Time	—	58	87	ns	T_J = 25°C, I_F = -1.5A
Q_{rr}	Reverse RecoveryCharge	—	41	62	nC	di/dt = 100A/µs ②

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width ≤ 300µs; duty cycle ≤ 2%.

③ When mounted on 1 inch square copper board, t<10 sec

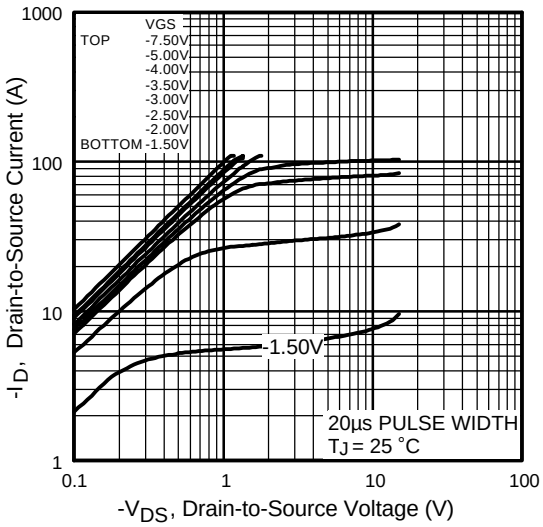


Fig 1. Typical Output Characteristics

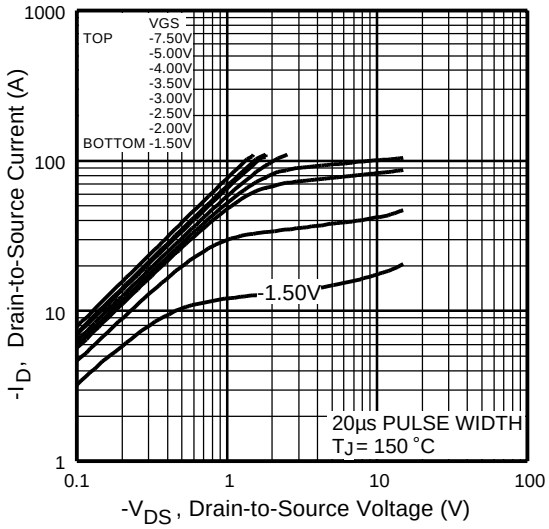


Fig 2. Typical Output Characteristics

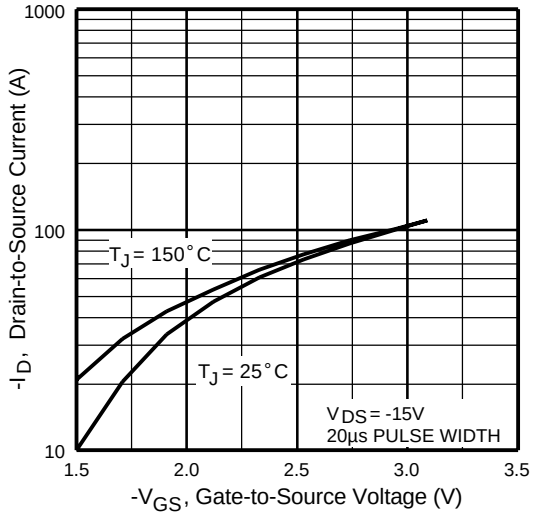


Fig 3. Typical Transfer Characteristics

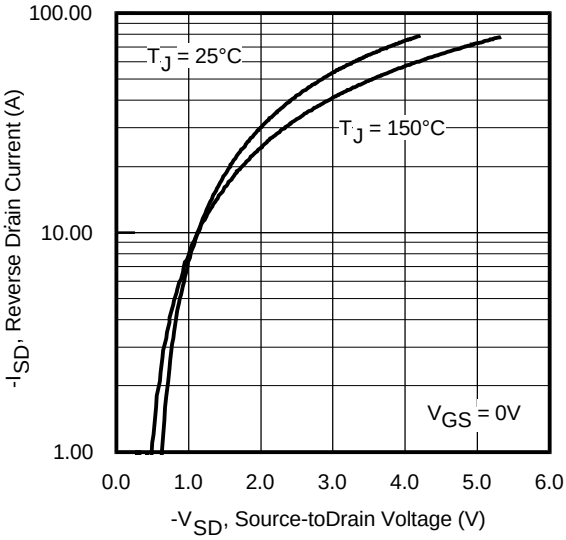


Fig 4. Typical Source-Drain Diode Forward Voltage

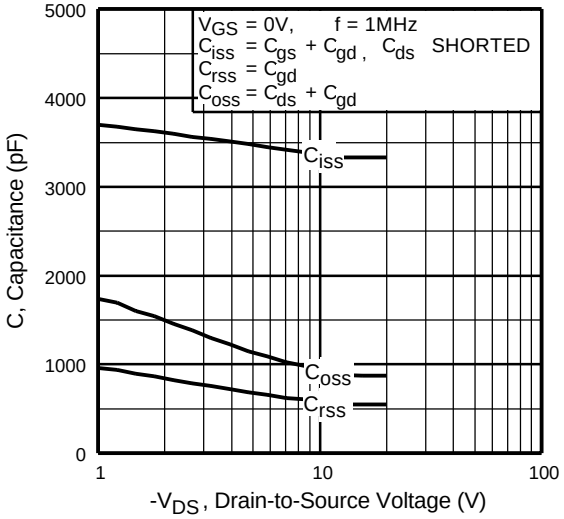


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

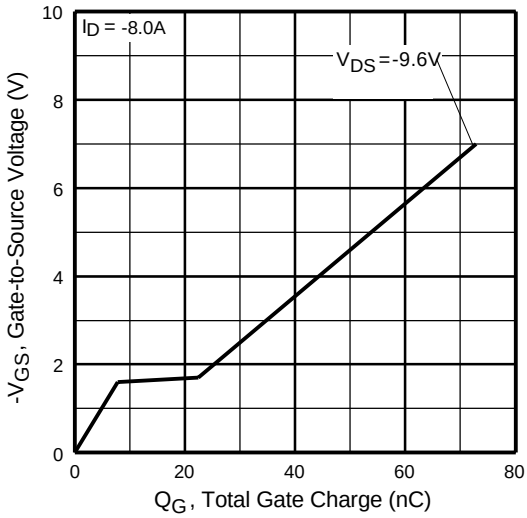


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

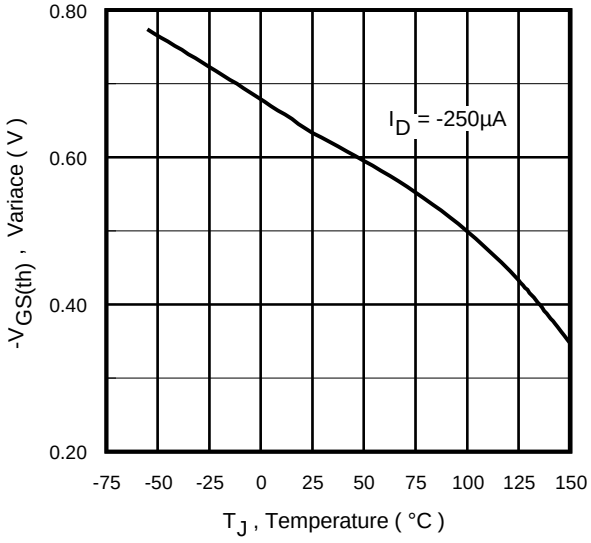


Fig 7. Threshold Voltage Vs. Temperature

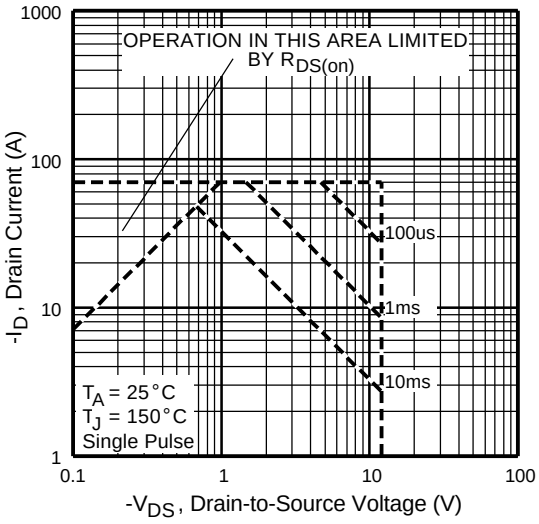


Fig 8. Maximum Safe Operating Area

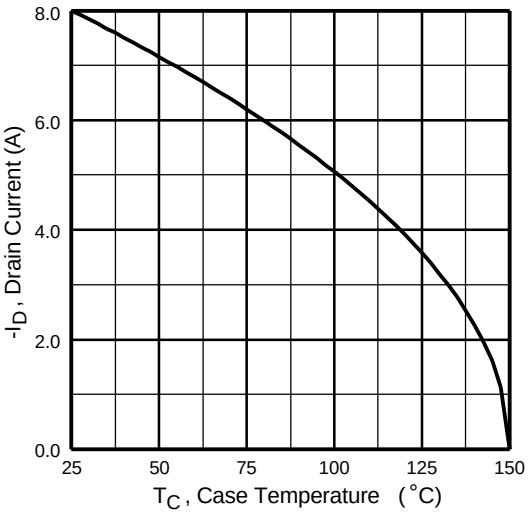


Fig 9. Maximum Drain Current Vs. Case Temperature

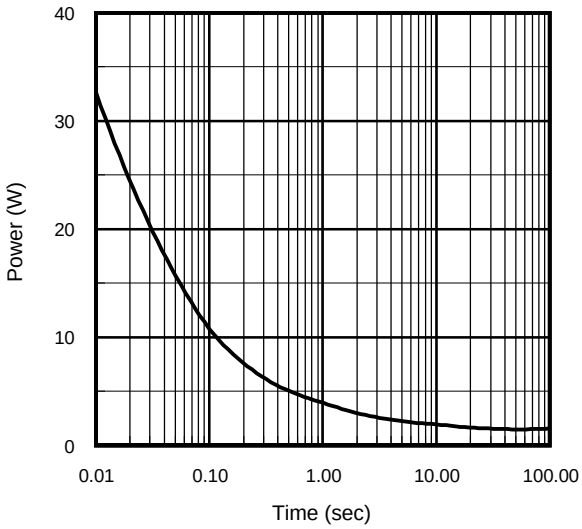


Fig 10. Typical Power Vs. Time

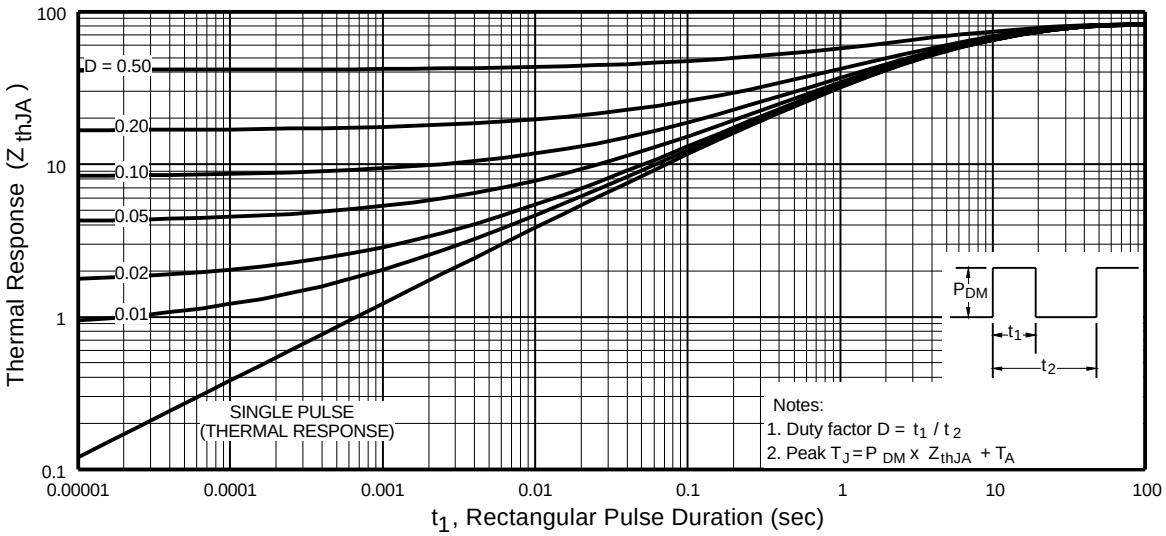


Fig 11. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

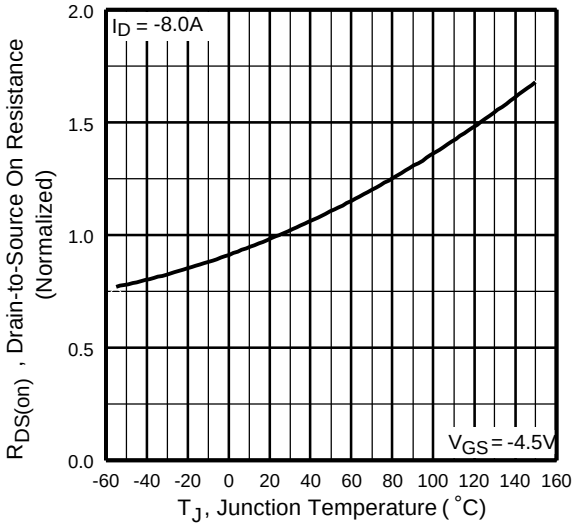


Fig 12. Normalized On-Resistance Vs. Temperature

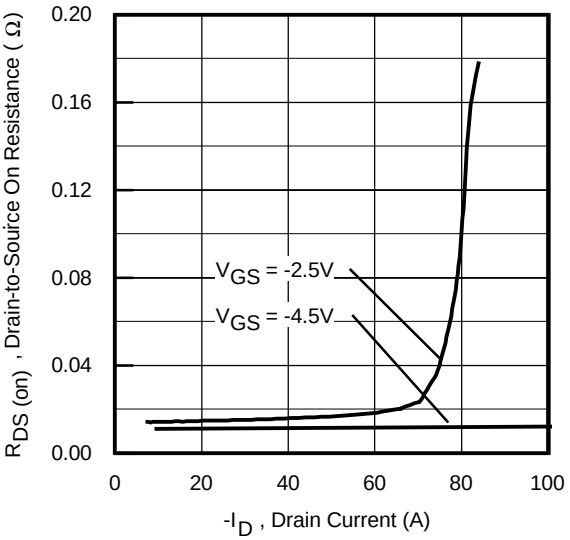


Fig 13. Typical On-Resistance Vs. Drain Current

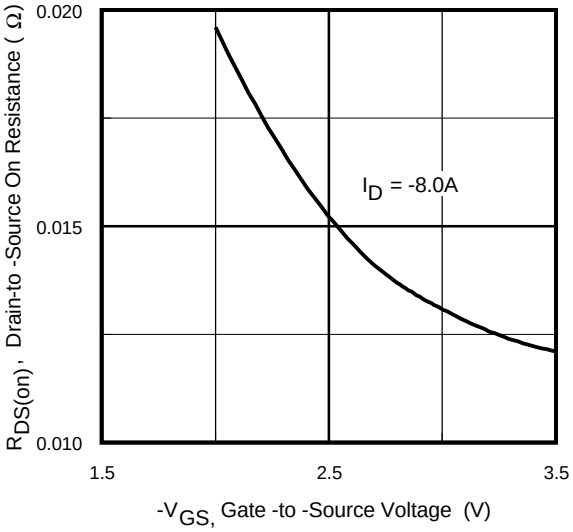
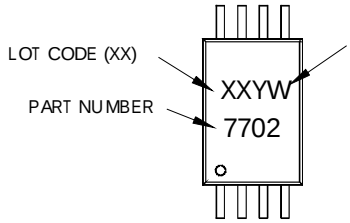


Fig 14. Typical On-Resistance Vs. Gate Voltage

TSSOP-8 Part Marking Information

EXAMPLE: THIS IS AN IRF7702



DATE CODE EXAMPLES:

9503 = 5C
9532 = EF

TABLE 1

WORK WEEK 1-26, NUMERIC YEAR CODE (1,2, ...ETC.)

YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
1994	4	04	D
1995	5		
1996	6		
1997	7		
1998	8		
1999	9		
2000	0	24	X
		25	Y
		26	Z

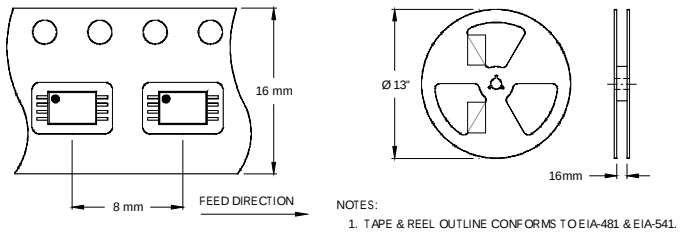
TABLE 2

WORK WEEK 27-52, ALPHANUMERIC YEAR CODE (A,B, ...ETC.)

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
1994	D	30	D
1995	E		
1996	F		
1997	G		
1998	H		
1999	J		
2000	K	50	X
		51	Y
		52	Z

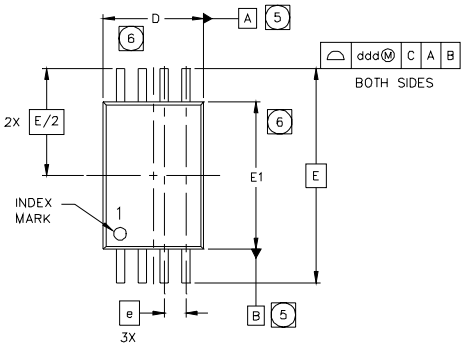
TSSOP-8 Tape and Reel

8LTSSOP (MO-153AA)

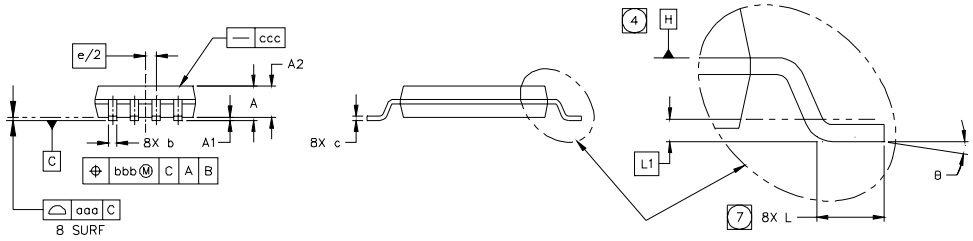


NOTES:
1. TAPE & REEL OUTLINE CONFORMS TO EIA-481 & EIA-541.

TSSOP-8 Package Outline



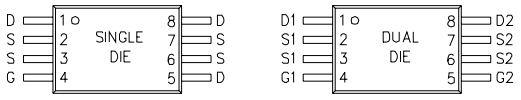
SYMBOL	MO-153AA DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	---	.0472
A1	0.05	---	0.15	.0020	---	.0059
A2	0.80	1.00	1.05	.032	.039	.041
b	0.19	---	0.30	.0075	---	.0118
c	0.09	---	0.20	.0036	---	.0078
D	2.90	3.00	3.10	.115	.118	.122
E	6.40 BSC			.251 BSC		
E1	4.30	4.40	4.50	.170	.173	.177
e	0.65 BSC			.0256		
L	0.45	0.60	0.75	.0178	.0236	.0290
L1	0.25 BSC			.010 BSC		
θ	0°	---	8°	0°	---	8°
aaa	0.10			.0039		
bbb	0.10			.0039		
ccc	0.05			.0019		
ddd	0.20			.0078		



NOTES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DATUM PLANE H IS LOCATED AS SHOWN.
5. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
6. DIMENSIONS D AND E1 ARE MEASURED AT DATUM PLANE H.
7. DIMENSION L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE.
8. OUTLINE CONFORMS TO JEDEC OUTLINE MO-153AA.

LEAD ASSIGNMENTS



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