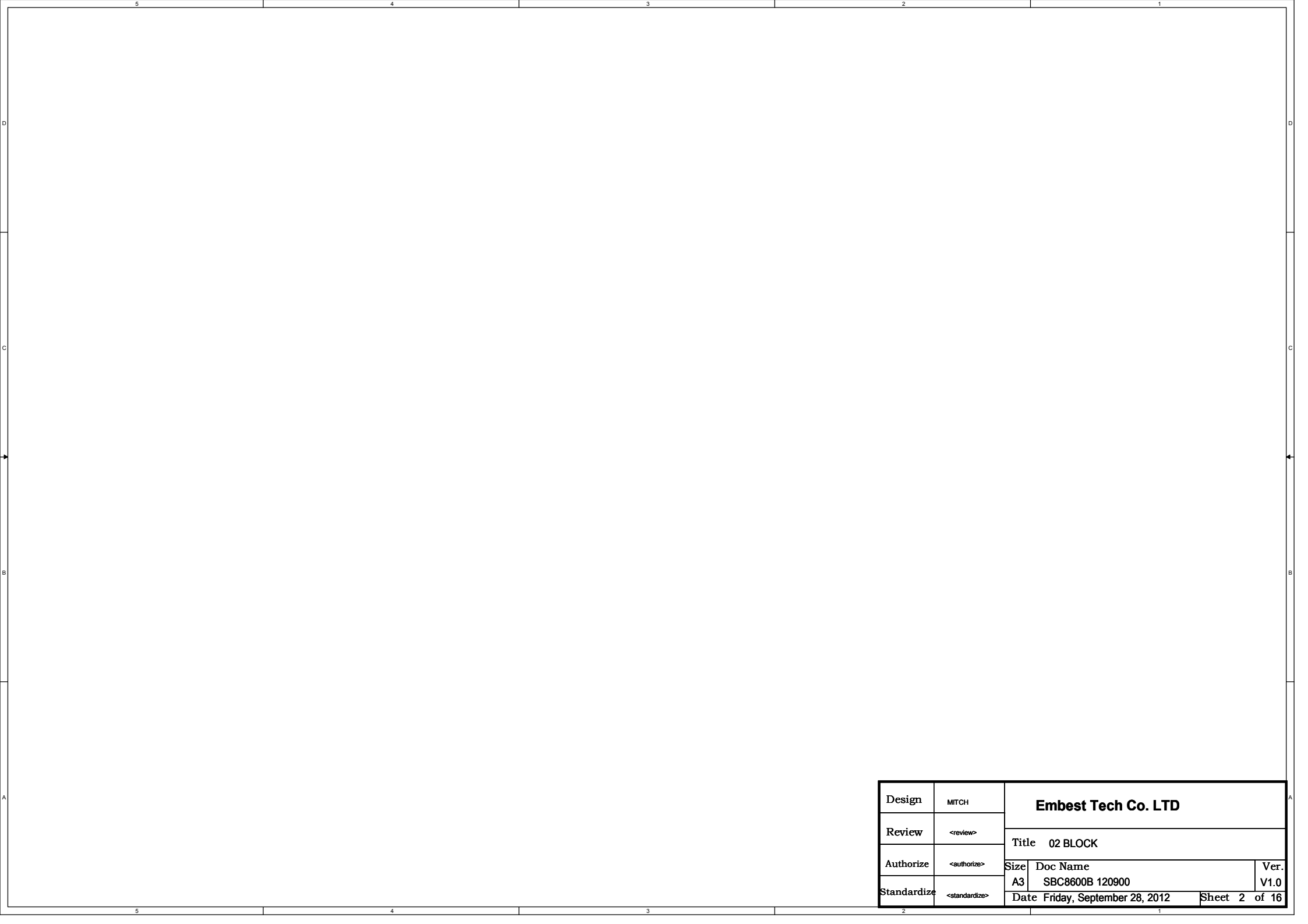


# SBC8600B 120900

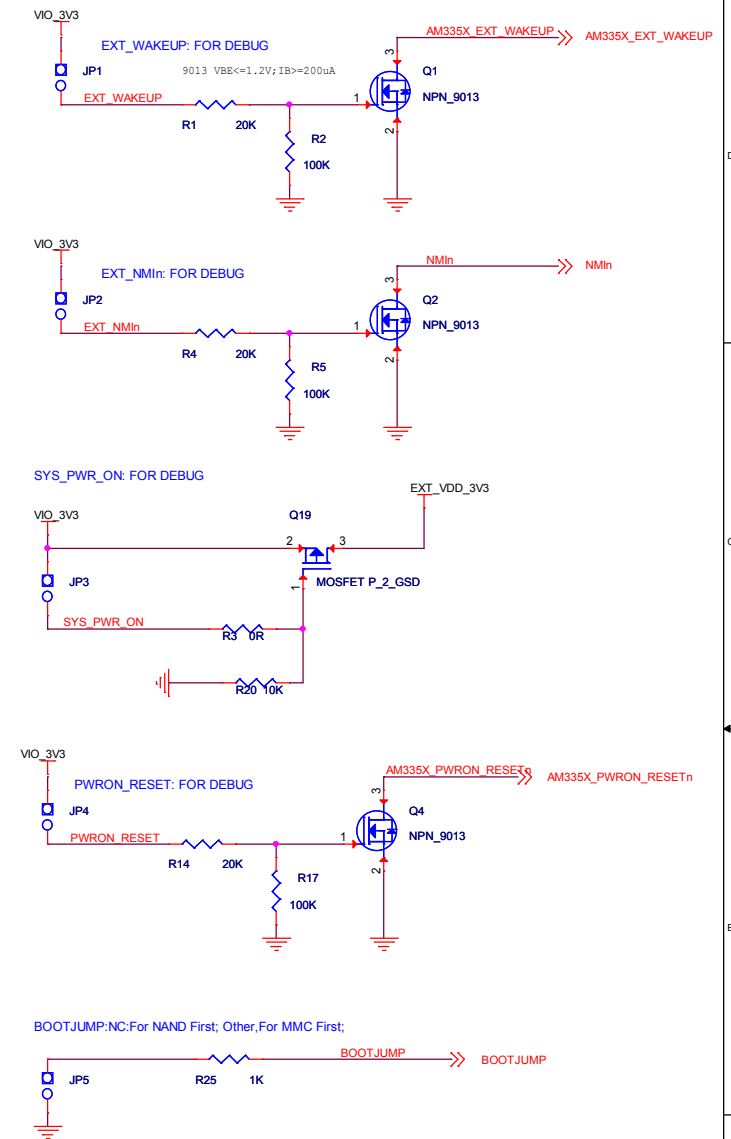
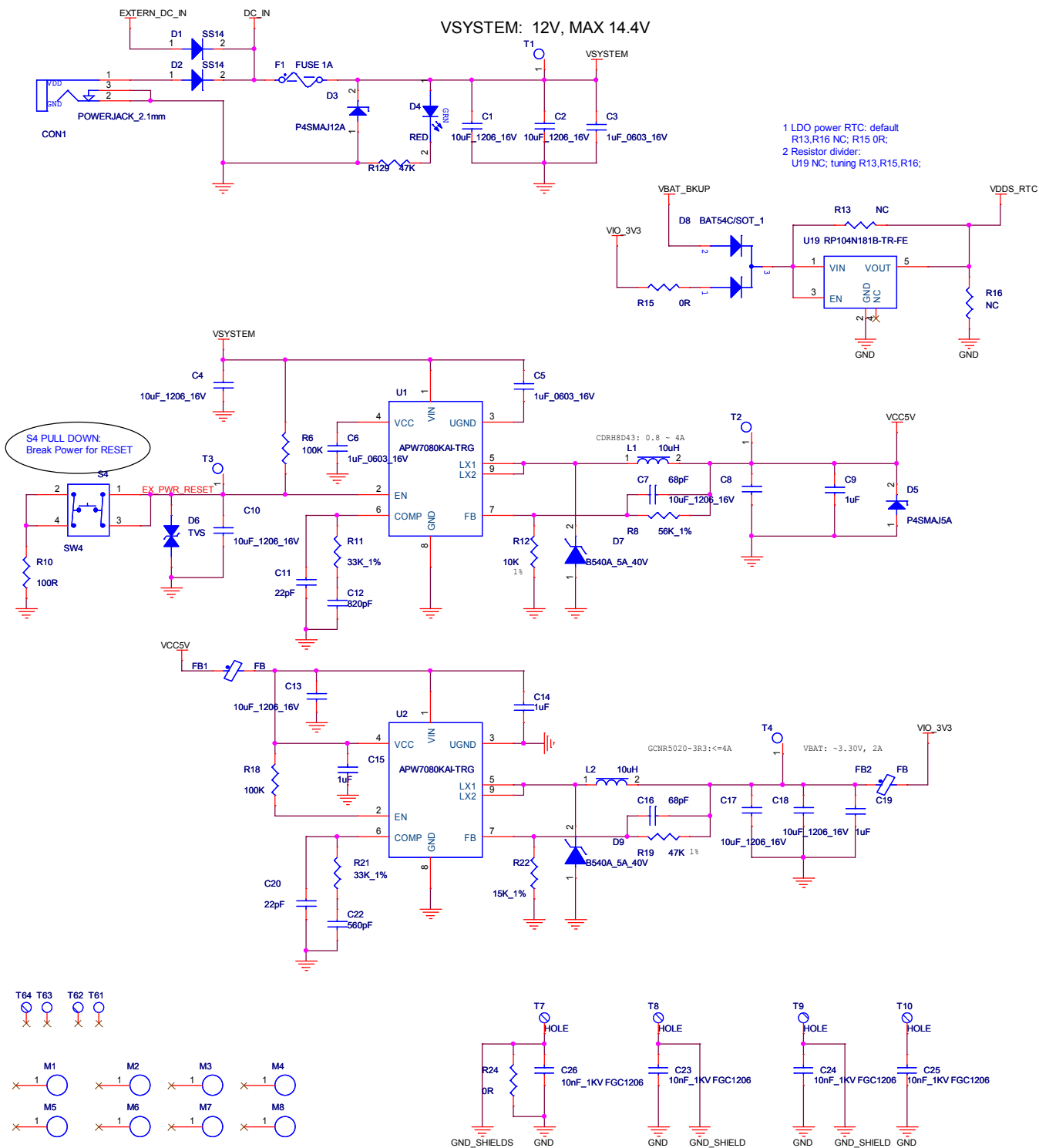
- 01 INDEX PAGE
- 02 BLOCK
- 03 INSTRUCTION
- 04 PWR
- 05 AM335XZCZ-CON
- 06 NAND
- 07 NETA
- 08 NETB
- 09 AUDIO
- 10 LCD
- 11 USB OTG & USB X 2
- 12 RS485 X 1 & CAN X 1
- 13 RS232 X 2
- 14 EXTERN
- 15 MISC
- 16 REVISION HISTORY

Design	MITCH	Embest Tech Co. LTD		
Review	<review>	Title00 INDEX PAGE		
Authorize	<authorize>	Size	Doc Name	Ver.
Standardize	<standardize>	A3	SBC8600B 120900	V1.0
		Date	Friday, September 28, 2012	Sheet 1 of 16



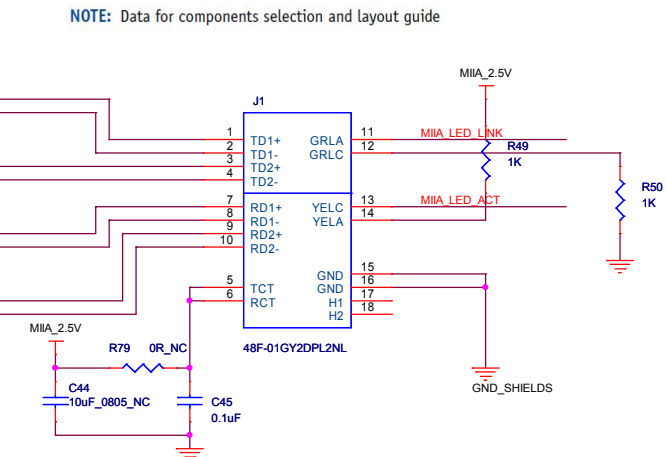
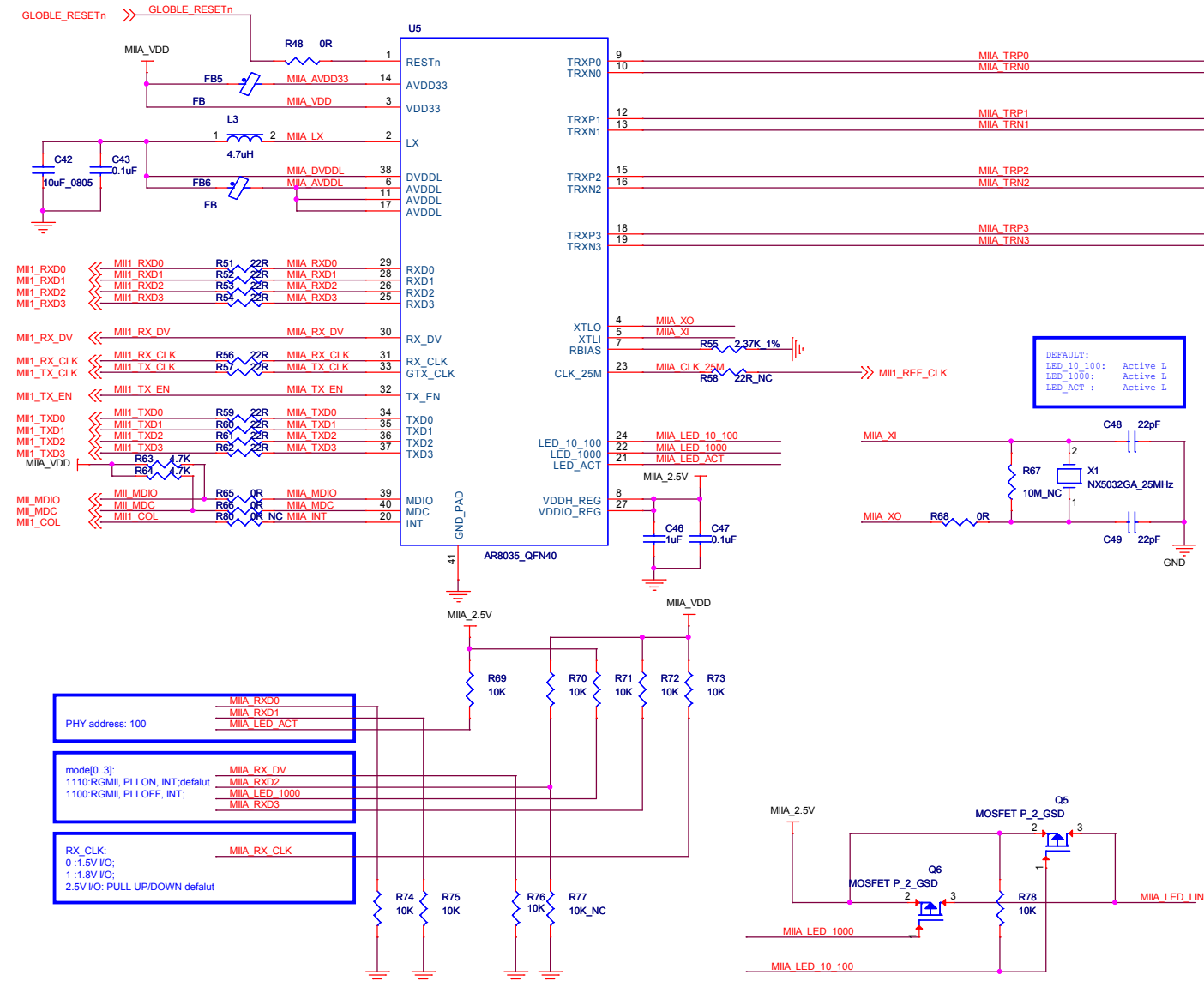
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Review	<review>	Title 02 BLOCK		
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Standardize	<standardize>	A3	SBC8600B 120900	V1.0
		Date	Friday, September 28, 2012	Sheet 2 of 16

Design	MITCH	Embest Tech Co. LTD		
Review	<review>			
Authorize	<authorize>	Title 03 INSTRUCTION		
Standardize	<standardize>	Size	Doc Name	Ver.
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		Date	Friday, September 28, 2012	Sheet 3 of 16



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Review	<review>	Title 04 PWR		
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Review	<review>			
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		Date	Friday, September 28, 2012	Sheet 6 of 16

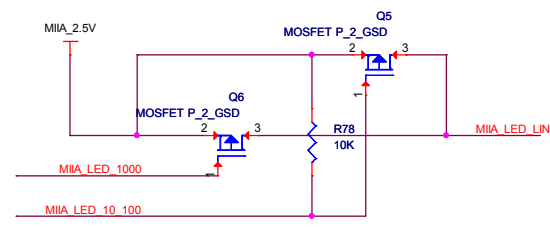


**NOTE:** 0=Pull-down, 1=Pull-up

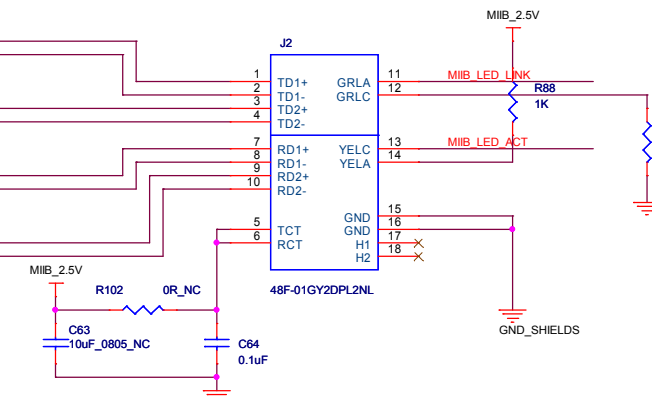
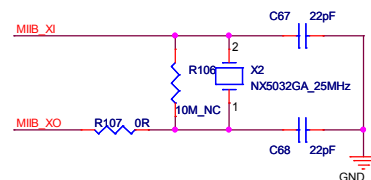
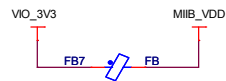
**NOTE:** Power on strapping pins are latched during power-up reset or warm hardware reset.

**NOTE:** Some MAC devices input pins may drive high/low during power-up or reset. So PHY power on transition status may be affected by the MAC.

MODE[3:0]	Description
1100	RGMII, PLOFF, INT;
1110	RGMII, PLLON, INT;
Others	Reserved



Design	MITCH	Embest Tech Co. LTD		
Review	<review>			
Authorize	<authorize>	Title 07 NETA		
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		Date	Friday, September 28, 2012	Sheet 7 of 16

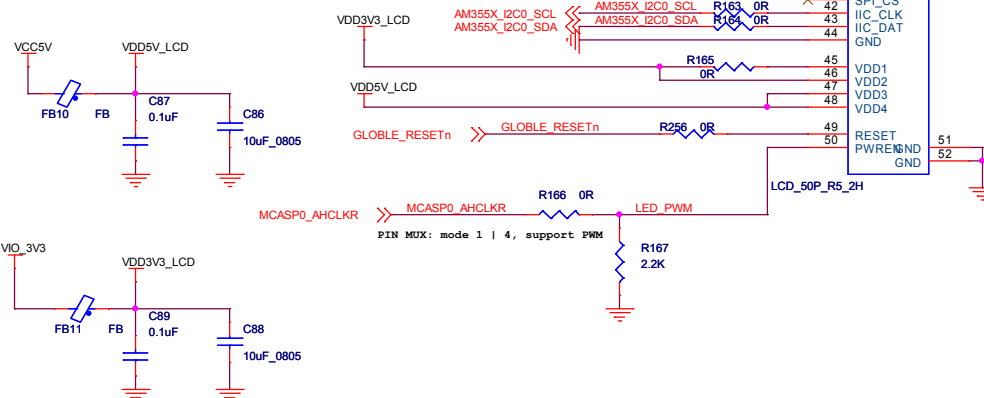
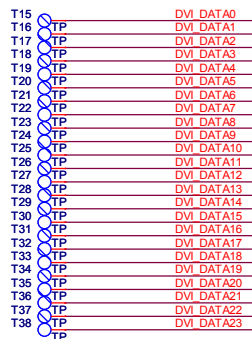
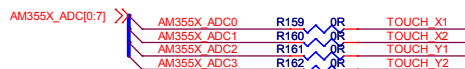
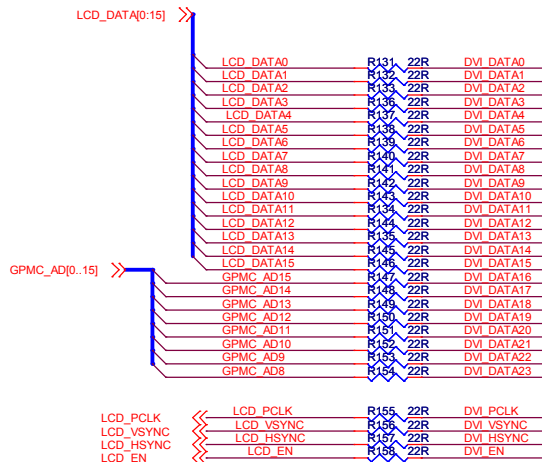


Symbol	Voltage Range	Current
AVDDL	1.1V $\pm$ 5%	50.8 mA
DVDDL	1.1V $\pm$ 5%	113.7 mA
AVDD33	3.3V $\pm$ 5%	63.8 mA
VDDIO_REG	Connect VDDH_REG 2.5V	20.9 mA

PHY Pin	PHY Core Config Signal	Description	Default Internal Weak Pull-up/Pull-down
RXD0	PHYADDRESS0	LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00"	0
RXD1	PHYADDRESS1		0
LED_ACT	PHYADDRESS2		1
RX_DV	MODE0	mode select bit 0	0
RXD2	MODE1	mode select bit 1	0
LED_1000	MODE2	mode select bit 2	1
RXD3	MODE3	mode select bit 3	0
RX_CLK	1.8V/1.5V	Select the RGMII/RMII I/O voltage level 1: 1.8V I/O 0: 1.5V I/O	0

MODE[3:0]	Description
1100	RGMII, PLL0FF, INT;
1110	RGMII, PLLON, INT;
Others	Reserved

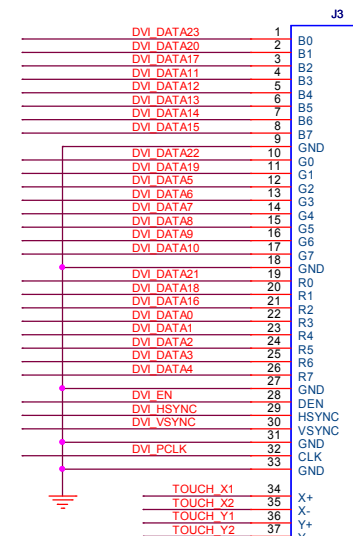
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		A3	SBC8600B 120900	V1.
		Date	Friday, September 28, 2012	Sheet 8 of 1



BLUE

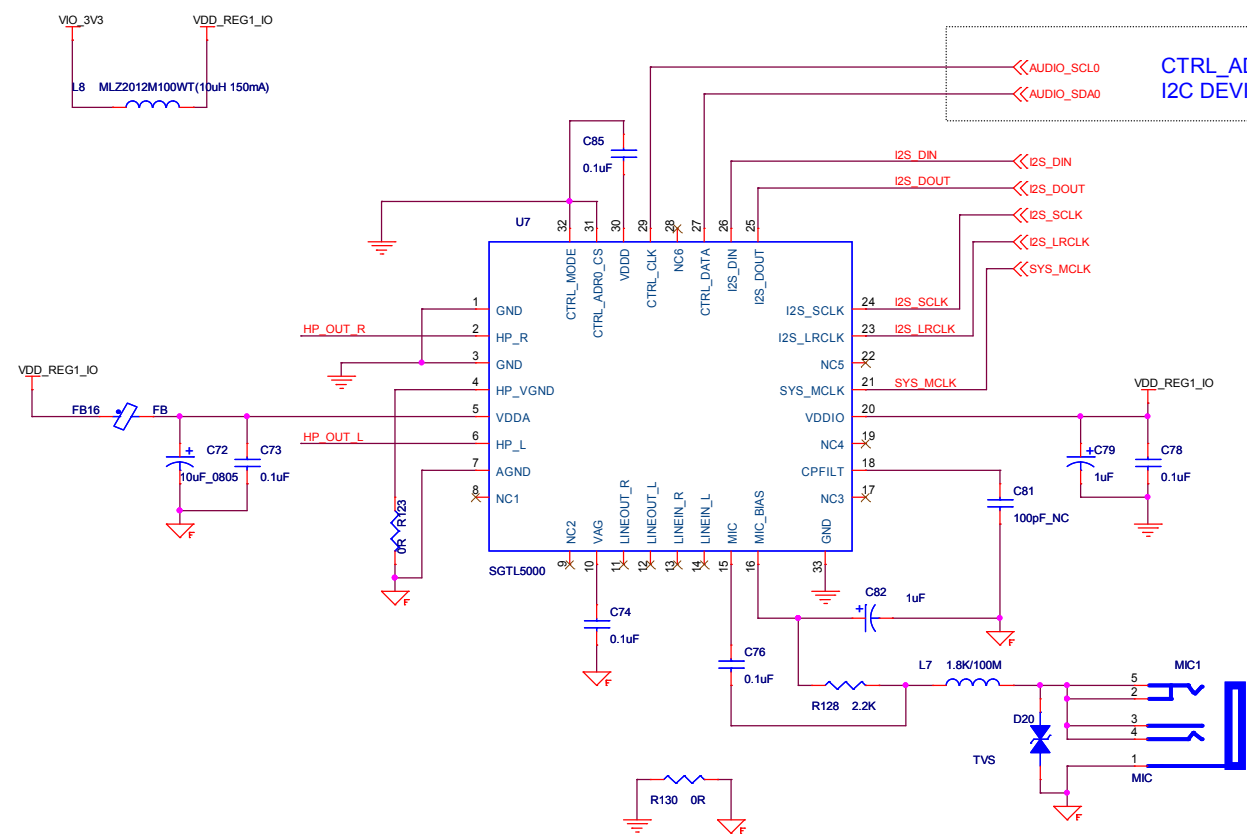
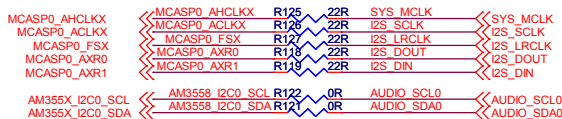
GREEN

RED



Design	MITCH	Embest Tech Co. LTD		
Review	<review>	Title 10 LCD		
Authorize	<authorize>	Size A3	Doc Name SBC8600B 120900	Ver. V1.0
Standardize	<standardize>	Date Friday, September 28, 2012	Sheet 10 of 16	





Attack (0.8dB/s to ~3200dB/s)  
DAP\_AVC\_ATTACK

### Figure 16. DAP AVC Block Diagram

threshold, the  
The  
2 dB. When  
is a limiter. In  
signal level

uated down  
of an attack  
is distorted.  
e output as  
kly enough.  
nge of

will adjust the

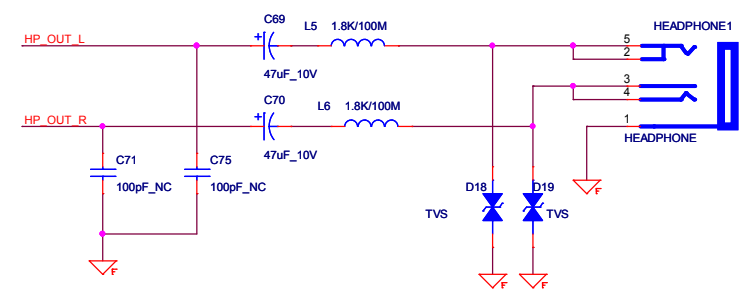
### I<sup>2</sup>C

The I<sup>2</sup>C port is implemented according to the I<sup>2</sup>C specification v2.0. The I<sup>2</sup>C interface is used to read and write all registers.

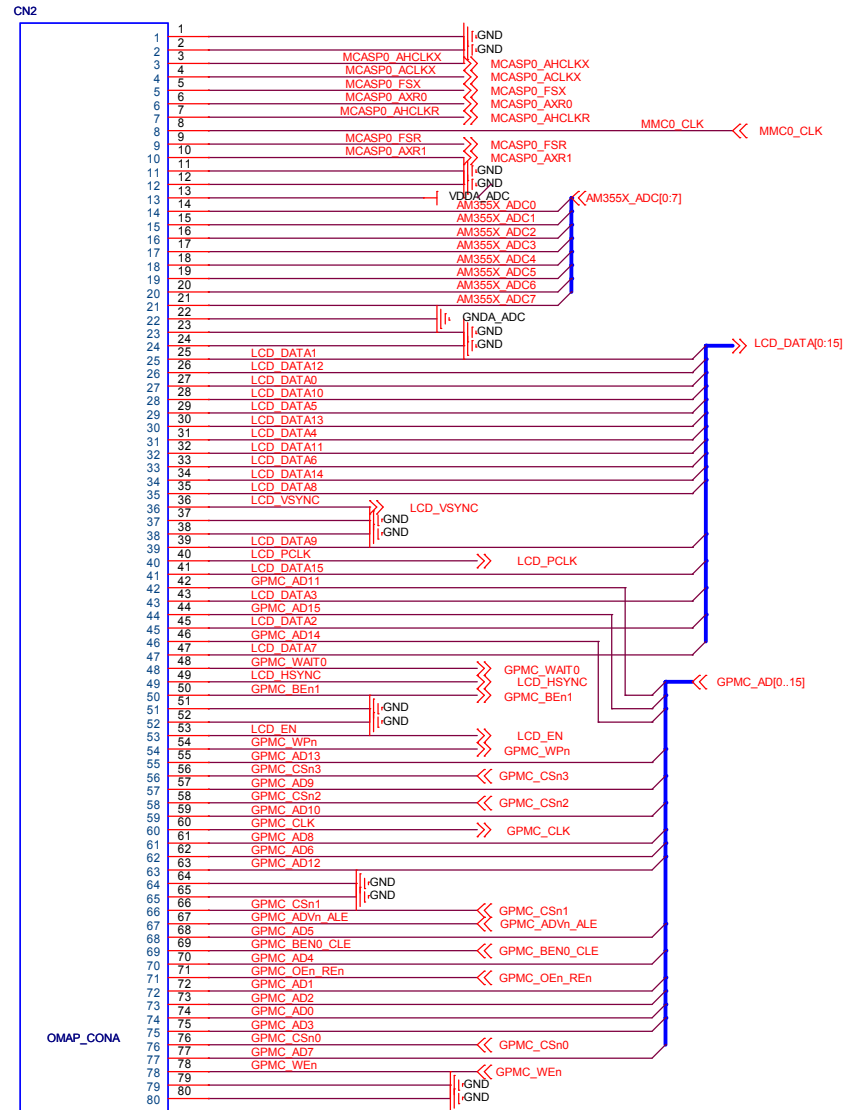
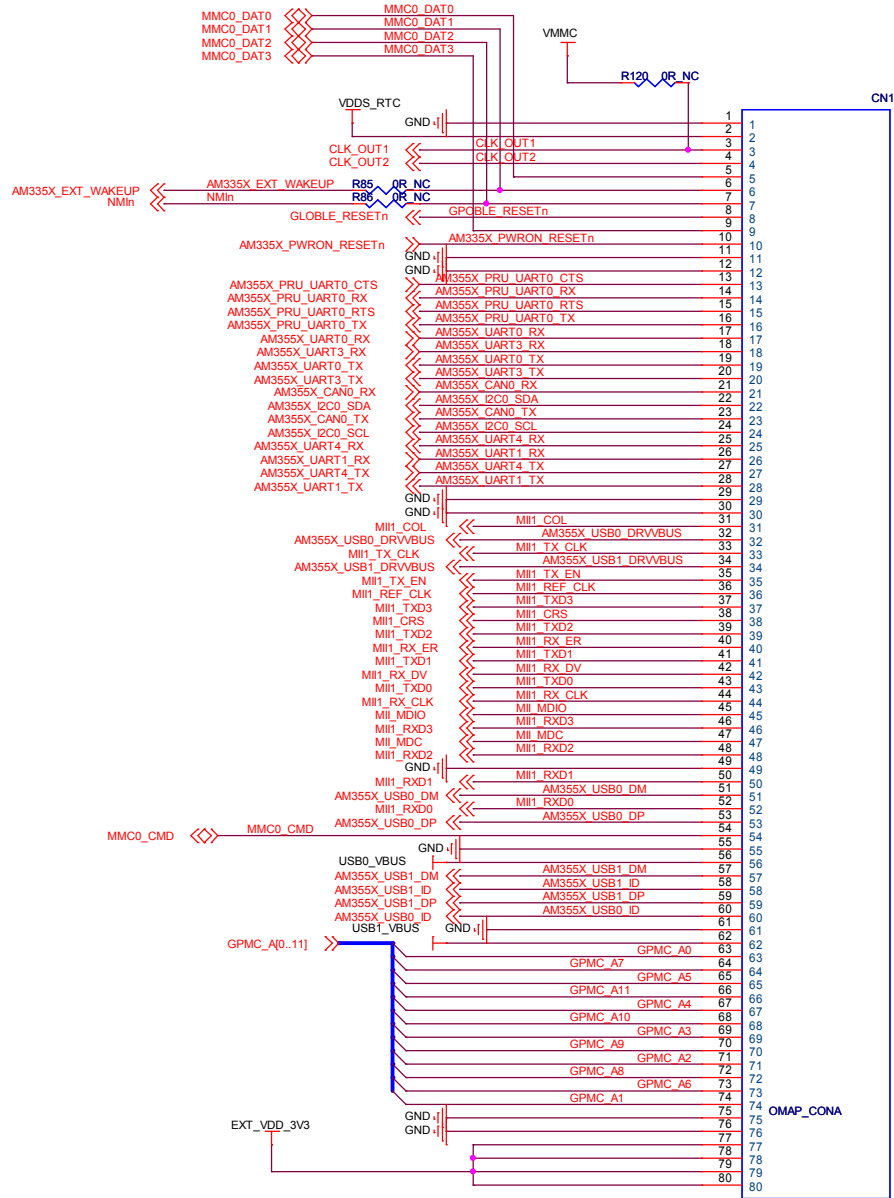
For the 32 QFN version of the SGTL5000, the I<sup>2</sup>C device address is 0n01010(R/W) where n is determined by I2C\_ADR0\_CS and R/W is the read/write bit from the I<sup>2</sup>C protocol.

For the 20 QFN version of the SGTL5000 the I<sup>2</sup>C address is always 0001010(R/W).

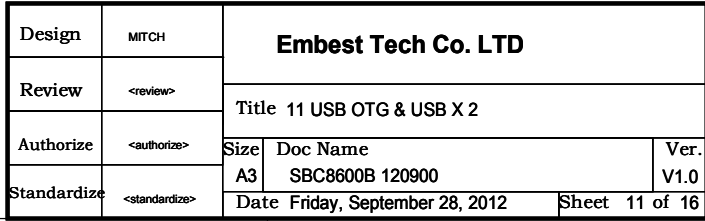
The SGTL5000 is always the slave on all transactions which means that an external master will always drive CTRL\_CLK.

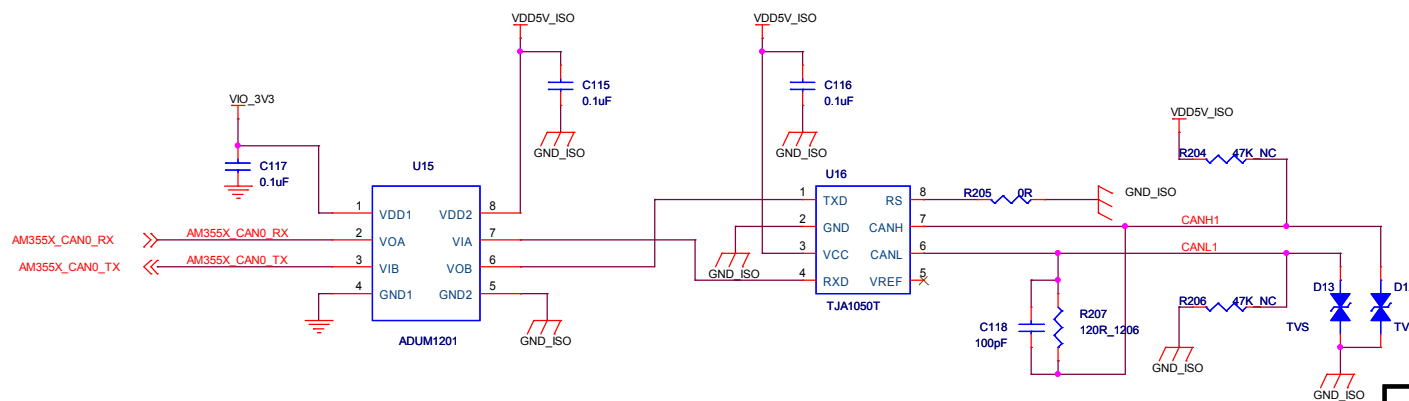
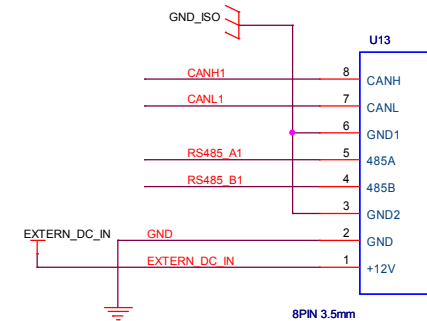
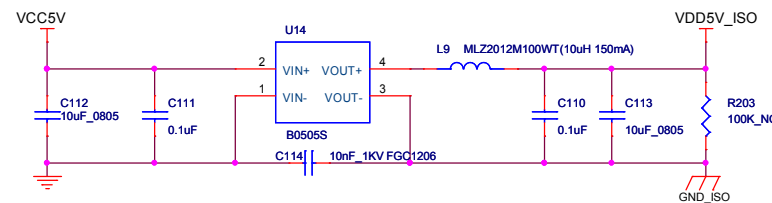
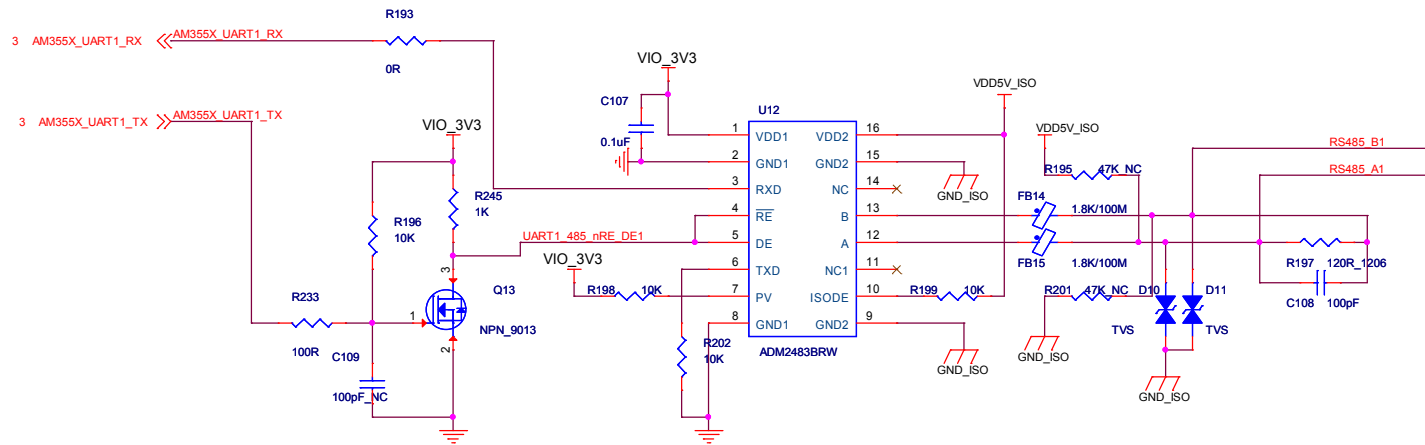


Design	MITCH	Embest Tech Co. LTD		
Review	<review>	Title 10 AUDIO		
Authorize	<authorize>	Size A3	Doc Name SBC8600B 120900	Ver. V1.0
Standardize	<standardize>	Date Friday, September 28, 2012	Sheet 10 of 18	

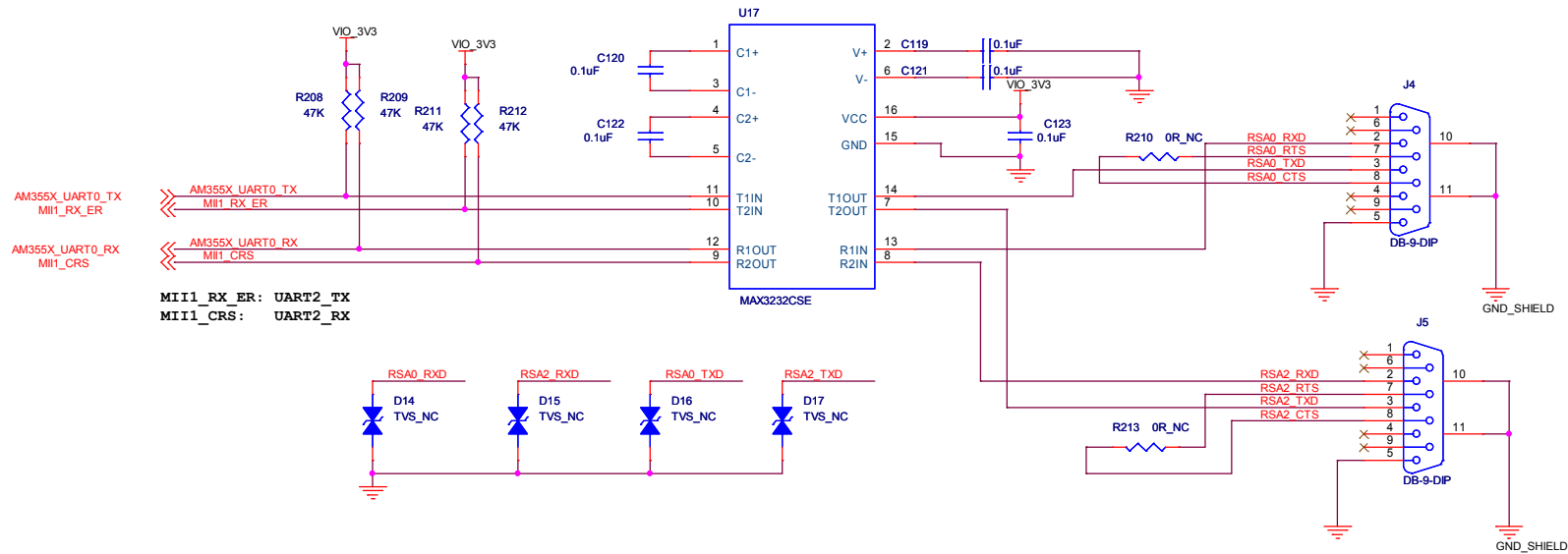
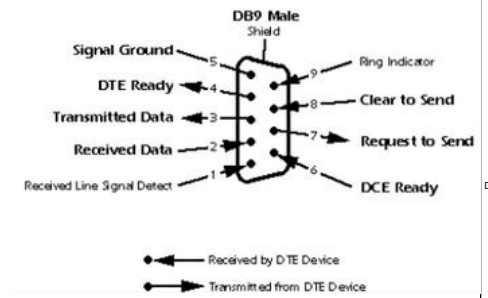


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Standardize	<standardize>	Date Friday, September 28, 2012	Sheet 10 of 11	



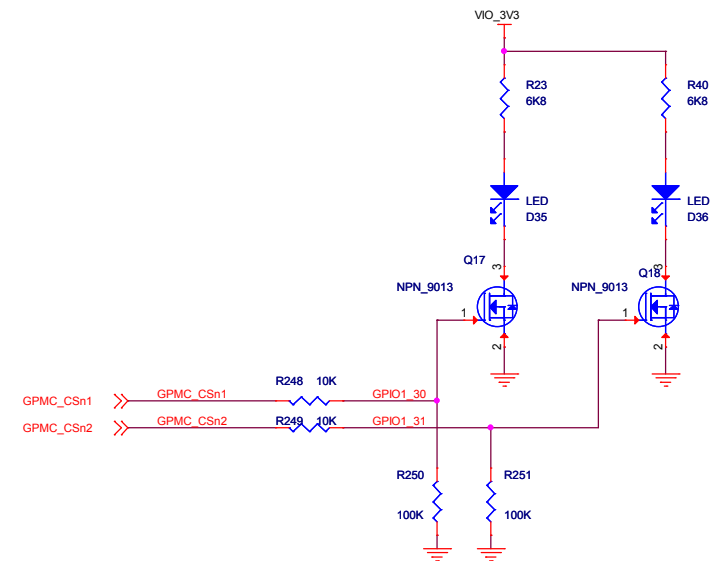
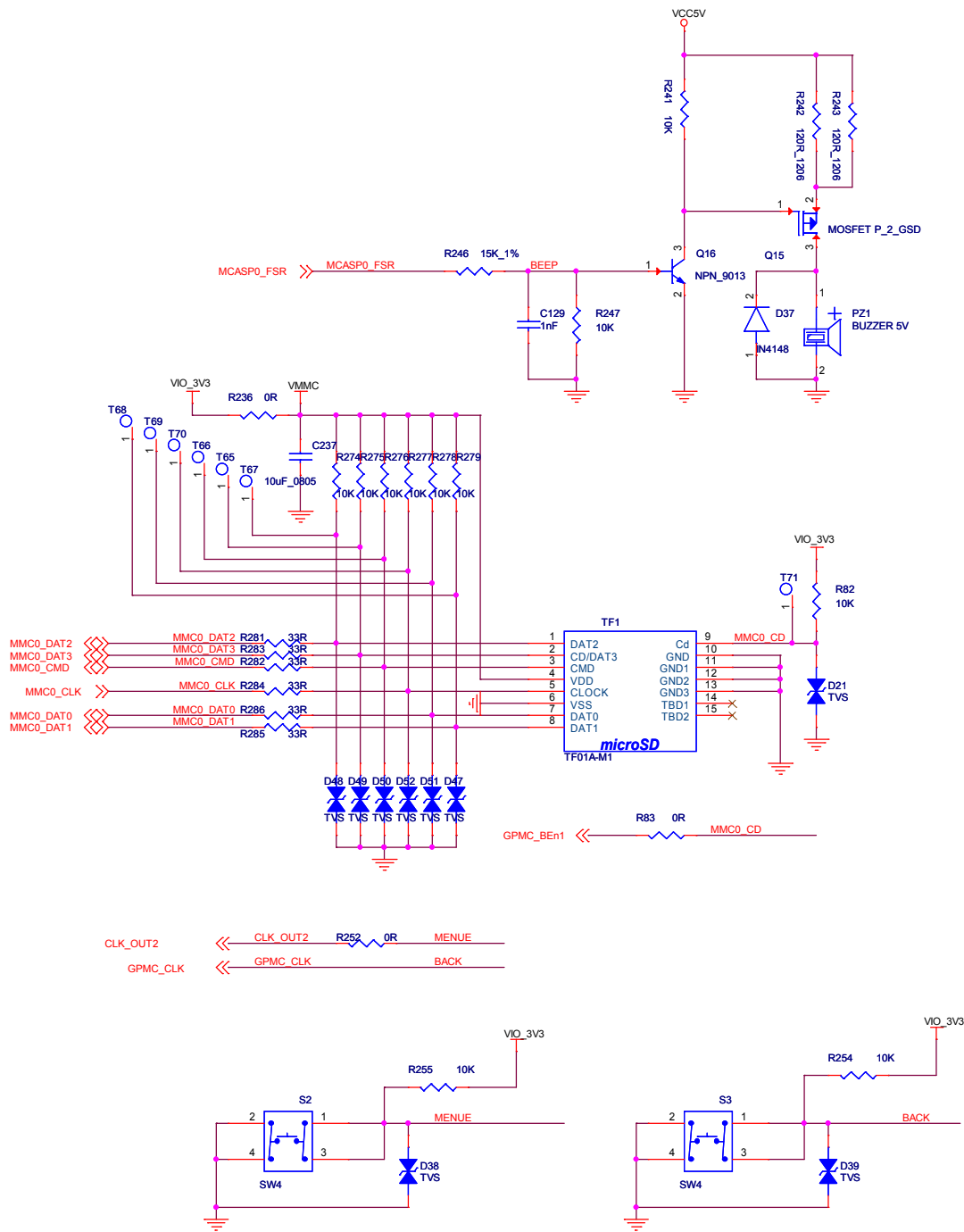


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Review	<review>	Title 12 RS485 X 1 & CAN X 1		
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Standardize	<standardize>	Date Friday, September 28, 2012	Sheet 12 of 16	

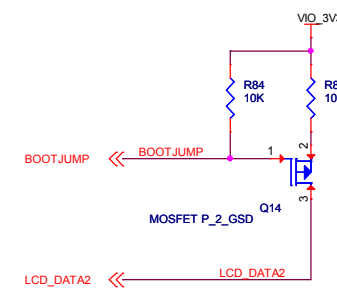


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Review	<review>	Title 13 RS232 X 2		
Authorize	<authorize>	Size A3	Doc Name SBC8600B 120900	Ver. V1.0
Standardize	<standardize>	Date Friday, September 28, 2012	Sheet 13 of 16	





FOR BATTERY:Need Power Management Optimized by Application



Design	MITCH	Embest Tech Co. LTD		
Review	<review>	Title 15 MISC		
Authorize	<authorize>	Size A3	Doc Name SBC8600B 120900	Ver. 1.0
Standardize	<standardize>	Date Friday, September 28, 2012	Sheet 15 of 16	

# SBC8600B Revision History

## SBC8600B 110900

1 Modify From SBC8600 120601: RM Nand; Add TF;

Design	MITCH	Embest Tech Co. LTD		
Review	<review>	Title 16 REVISION HISTORY		
Authorize	<authorize>	Size A3	Doc Name SBC8600B 120900	Ver. V1.0
Standardize	<standardize>	Date Friday, September 28, 2012	Sheet 16	of 16