4Gb NAND FLASH
H27U4G8_6F2D
H27S4G8_6F2D

Document Title

4 Gbit (512M x 8 bit) NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	Jan. 12. 2010	Preliminary
1.0	ICC2: Saparate Cache case and normal case tCBSYW value update (5us-Typ.)	Mar. 04. 2010	
1.1	tCEA -> tCR Typo correction ICC2 Typcal delete (because of same as max. value)	Mar. 31. 2010	
1.2	Adding Bad Block Marking Information	April 14. 2010	
1.3	Parameter page update Fig. 37 correction at least five times -> 3 times in 3.21	June 29. 2010	
1.4	Typo correction D1 -> D in Table. 29	OCT. 8. 2010	
1.5	Correction Table 29: 48-TSOP1 - 48-lead Plastic Thin Small Out-line, 12 x 20mm, Package Mechanical Data	Jul. 25. 2011	

FEATURES SUMMARY

DENSITY

- 4Gbit: 4096blocks

Nand FLASH INTERFACE

- NAND Interface
- ADDRESS / DATA Multiplexing

SUPPLY VOLTAGE

- Vcc = 3.0/1.8V Volt core supply voltage for Program, Erase and Read operations.

MEMORY CELL ARRAY

- X8: (2K + 64) bytes x 64 pages x 4096 blocks
- X16: (1k+32) words x 64 pages x 2048 blocks

PAGE SIZE

- X8: (2048 + 64 spare) bytes
- X16:(1024 + 32spare) Words

Block SIZE

- X8: (128K + 4K spare) bytes
- X16:(64K + 2K spare) Words

PAGE READ / PROGRAM

- Random access: 25us (Max)
- Sequentiall access: 25ns / 45ns (3.0V/1.8V, min.)
- Program time(3.0V/1.8V): 200us / 250us (Typ)
- Multi-page program time (2 pages):
  200us / 250us (3.0V/1.8V, Typ.)

BLOCK ERASE / MULTIPLE BLOCK ERASE

- Block erase time: 3.5 ms (Typ)
- Multi-block erase time (2 blocks):
  3.5ms/ 3.5ms (3.0V/1.8V, Typ.)

SEQURITY

- OTP area
- Sreial number (unique ID)
- Non-volatile protection option for OTP and Block0(Opt.)
- Hardware program/erase disabled during power transition

ADDTIONAL FEATURE

- Multiplane Architecture
  : Array is split into two independent planes. Parallel operations on both planes are available, having program and erase time.
- Single and multiplane copy back program with automatic EDC (error detection code)
- Single and multiplane page re-program
- Single and multiplane cache program
- Cache read
- Multiplane block erase

Reliability

- 100,000 Program / Erase cycles (with 1bit /528Byte ECC)
- 10 Year Data retention

ONFI 1.0 COMPLIANT COMMAND SET

ELECTRONICAL SIGNATURE

- Munufacture ID: ADh
- Device ID

PACKAGE

- Lead/Halogen Free
- TSOP48 12 x 20 mm

CONTENTS

1 Summary Description

H27(U_S)4G8_6F2D series is a 512Mx8bit with spare 16Mx8 bit capacity.
The device is offered in 3.0/1.8 Vcc Power Supply, and with x8 and x16 I/O interface
Its NAND cell provides the most cost-effective solution for the solid state mass storage market.
The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.
The device contains 4096 blocks, composed by 64 pages.
Memory array is split into 2 planes, each of them consisting of 2048 blocks.
Like all other 2KB - page NAND Flash devices, a program operation allows to write the 2112-byte page in typical 200us(3.3V) and an erase operation can be performed in typical 3.5ms on a 128K-byte block.
In addition to this, thanks to multi-plane architecture, it is possible to program 2 pages at a time (one per each plane) or to erase 2 blocks at a time (again, one per each plane). As a consequence, multi-plane architecture allows program time to be reduced by 40% and erase time to be reduction by 50%. In case of multi-plane operation, there is small degradation at 1.8V application in terms of program/erase time.

The multiplane operations are supported both with traditional and ONFI 1.0 protocols.
Data in the page can be read out at 25ns (3V version) and 45nsec (1.8V version) cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.
Commands, Data and Addresses are synchronously introduced using CE#, WE#, ALE and CLE input pin.
The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data.

A WP# pin is available to provide hardware protection against program and erase operations.
The output pin RB# (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the RB# pins can be connected all together to provide a global status signal.
Each block can be programmed and erased up to 100,000 cycles with ECC (error correction code) on. To extend the lifetime of Nand Flash devices, the implementation of an ECC is mandatory.
The chip supports CE# don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the CE# transitions do not stop the read operation.
In addition, device supports ONFI 1.0 specification.

The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. Copy back operation automatically executes embedded error detection operation: 1 bit error out of every 528-byte (x8) or 1 bit error out of every 264-word (x16) can be detected. With this feature it is no longer necessary to use an external to detect copy back operation errors.
Multiplane copy back is also supported, both with traditional and ONFI 1.0 protocols. Data read out after copy back read (both for single and multiplane cases) is allowed.
In addition, Cache program and multi cache program operations improve the programing throughput by programing data using the cache register.

The devices provide two innovative features: page re-program and multiplane page re-program. The page re-program allows to re-program one page. Normally, this operation is performed after a previously failed page program operation. Similarly, the multiplane page re-program allows to re-program two pages in parallel, one per each plane. The first page must be in the first plane while the second page must be in the second plane; the multiplane page re-program operation is performed after a previously failed multiplane page program operation. The page re-program and multiplane

page re-program guarantee imporve performance, since data insertion can be omitted during re-program operations, and save ram buffer at the host in the case of program failure.

The devices, available in the TSOP48 (12X20mm) package, support the ONFI1.0 specfication and come with four sequrity features:

- OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permantely.
- Serial number (unique identifier), which allows the devices to be nuniquely indentified.
- Read ID2 extention
- Non-volatile protection to lock sensible data permanently.

These security features are subject to an NDA (non-disclosure agreement) and are, therefore, no described in the datasheet. For more details about them, contact your nearest Hynix sales office.

1.1.Product List

PART NUMBER	ORGANIZATION	Operating RANGE	PACKAGE
H27U4G8F2D	x8	2.7 to 3.6V	-
H27U4G6F2D	x16	2.7 to 3.6V	-
H27S4G8F2D	x8	1.7 to 1.95V	-
H27S4G6F2D	x16	1.7 to 1.95V	-

Table 1: list of supported versions / packages

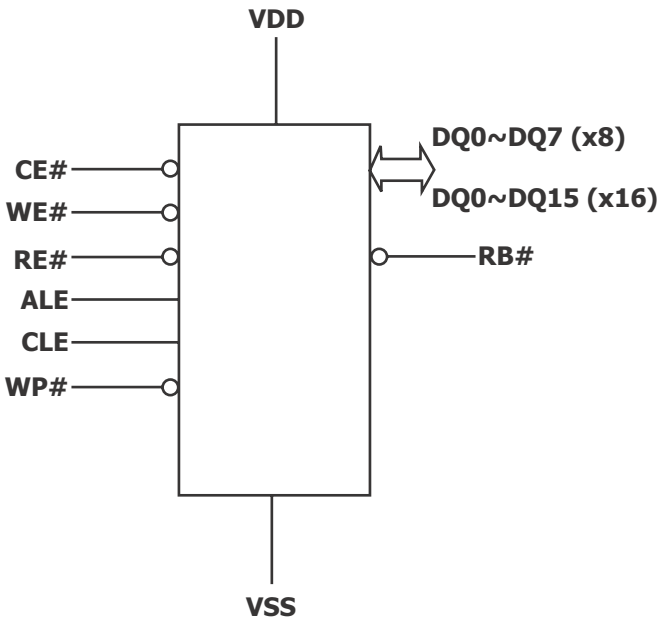


Figure 1: Logic Diagram

DQ7 - DQ0	Data Input / Outputs (x8/x16)
DQ15 - DQ8	Data Input / Outputs (x16)
CLE	Command latch enable
ALE	Address latch enable
CE#	Chip Enable
RE#	Read Enable
WE#	Write Enable
WP#	Write Protect
RB#	Ready/ Busy
V_{CC}	Power supply
V_{SS}	Ground
NC	No Connected internally

Table 2: Signal Names

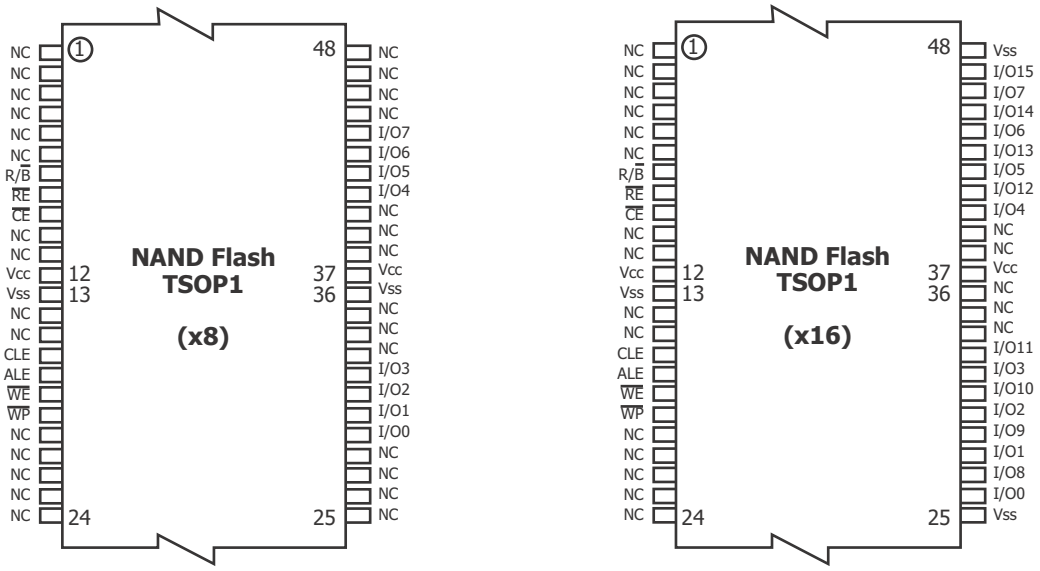


Figure 2. 48TSOP1 Contact, x8 and x16 Devic

1.2 PIN DESCRIPTION

Pin Name	Description
DQ0 - DQ15	**DATA INPUTS/OUTPUTS** The DQ pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable (WE#). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
CE#	**CHIP ENABLE** This input controls the selection of the device. When the device is busy CE# low does not deselect the memory.
WE#	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The DQ inputs are latched on the rise edge of WE#.
RE#	**READ ENABLE** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address counter by one.
WP#	**WRITE PROTECT** The WP# pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
RB#	**READY BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
V_{CC}	**SUPPLY VOLTAGE FOR IO BUFFER** The V_{CC} supplies the power for all the operations (Read, Write, Erase). An internal lock circuit prevent the insertion of Commands when V_{CC} is less than V_{LKO}
V_{SS}	**GROUND**
NC / DNU	**NO CONNECTED / DON'T USE**

Table 3: Pin Description

NOTE:

1. A 0.1uF capacitor should be connected between the V_{CC} Supply Voltage pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.
2. an internal voltage detector disables all functions whenever V_{CC} is below 1.8V (3V version) or 1.1V (1.8V) version to protect the device from any involuntary program/erase during power transitions.

1.3 Functional block diagram

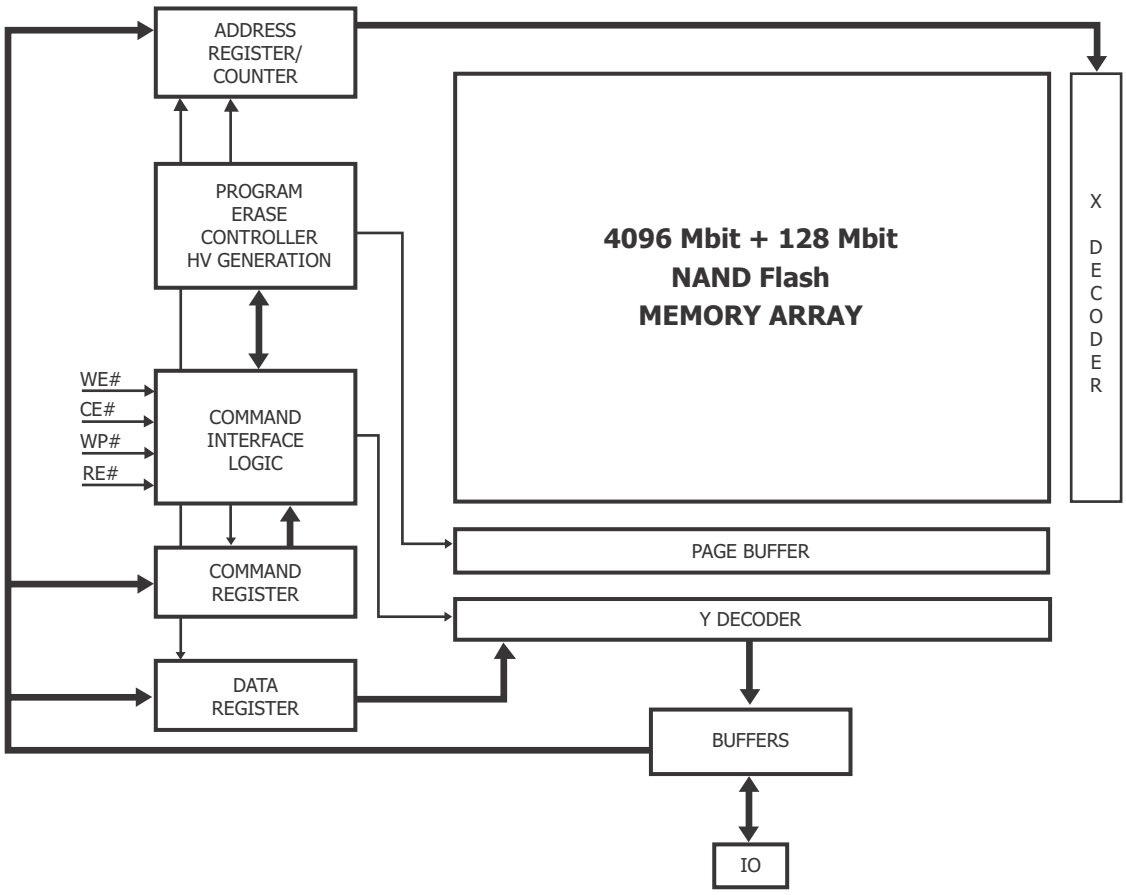


Figure 3: block description

1.4 Address role

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	0	0	0	0
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27
5th Cycle (*)	A28	A29	A30	A31	0	0	0	0

Table 4: Address Cycle Map (x8)

(*): A30 for 8Gbit DDP(1CE). A30:A31 for 16Gbit QDP(1CE).

As far as the address bits are concerned, the following rules apply:

A0 - A11 : column address in the page
A12 - A17 : page address in the block
A18 : plane address (for multi-plane operations) / block address (for normal operations)
A19 - A31 : block address

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	0	0	0	0	0
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18
4th Cycle	A19	A20	A21	A22	A23	A24	A25	A26
5th Cycle (*)	A27	A28	A29	A30	0	0	0	0

Table 5: Address Cycle Map (x16)

(*): A29 for 8Gbit DDP(1CE). A29:A30 for 16Gbit QDP(1CE)

As far as the address bits are concerned, the following rules apply:

A0 - A10 : column address in the page
A11 - A16 : page address in the block
A17 : plane address (for multi-plane operations) / block address (for normal operations)
A18 - A30 : block address

1.5 Command Set

Command(1)	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
READ	00h	30h			
READ FOR COPY-BACK	00h	35h			
SPECIAL READ FOR COPY BACK	00h	36h			
READ ID	90h				
READ ID2	30h-65h-00h	30h			
RESET	FFh				Yes(2)
PAGE PGM (start) / CACHE PGM (end)	80h	10h			
CACHE PGM (Start) / (continue)	80h	15h			
PAGE REPROGRAM / Nth PAGE CACHE REPROGRAM (end)	8Bh	10h			
Nth PAGE CACHE REPROGRAM (continue)	8Bh	15h			
N-1th PAGE CACHE REPROGRAM (continue)	8Ah	15h			
COPY BACK PGM (start)	85h	10h			
(Traditional) MULTI PLANE PROGRAM(3)	80h	11h	81h	10h	
ONFI MULTIPLANE PROGRAM	**80h**	**11h**	**80h**	**10h**	
MULTIPLANE PAGE RE-PROGRAM	8Bh	11h	8Bh	10h	
(Traditional) MULTIPLANE CACHE PGM (start/cont)	80h	11h	81h	15h	
ONFI MULTIPLANE CACHE PGM (start/cont)	**80h**	**11h**	**80h**	**15h**	
(Traditional) MULTIPLANE CACHE PGM (end)(3)	80h	11h	81h	10h	
ONFI MULTIPLANE CACHE PGM (end)	**80h**	**11h**	**80h**	**10h**	
Nth PAGES MULTIPLANE CACHE RE-PROGRAM (cont)	8Bh	11h	8Bh	15h	
Nth PAGES MULTIPLANE CACHE RE-PROGRAM (end)	8Bh	11h	8Bh	10h	
N-1th PAGES MULTIPLANE CACHE RE-PROGRAM (cont)	8Ah	11h	8Ah	15h	
(Traditional) MULTI PLANE COPY BACK PROGRAM(3)	85h	11h	81h	10h	
ONFI MULTIPLANE COPYBACK PGM	**85h**	**11h**	**85h**	**10h**	
BLOCK ERASE	60h	D0h			
(Traditional) MULTI PLANE BLOCK ERASE(3)	60h	60h	D0h		
ONFI MULTIPLANE BLOCK ERASE	**60h**	**D1h**	**60h**	**D0h**	
READ STATUS REGISTER	70h				Yes
READ STATUS ENHANCED	**78h**				**Yes**
RANDOM DATA INPUT	85h				
RANDOM DATA OUTPUT	05h	E0h			
CACHE READ(SEQUENTIAL)	**31h**				
CACHE READ ENHANCED (RANDOM)	**00h**	**31h**			
CACHE READ END	**3Fh**				
READ PARAMETER PAGE	**Ech**				
EDC STATUS READ	7Bh				
EXTENDED READ STATUS	F2h/F3h/F4h/F5h				Yes

Table 6: Public Command Set

NOTE:
1. Commands listed in BOLD are referring to ONFI 1.0 Specification.
2. Only during cache ready busy.
3.Command maintained for backward compatibility

CLE	ALE	CE#	WE#	RE#	WP#	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input
L	L	L	Rising	H	H	Data Input	
L	L	L(1)	H	Falling	X	Data Output (on going)	
X	X	L(1)	H	H	X	Data Output (suspended)(2)	
L	L	L	H	H	X	Busy time in Read	
X	X	X	X	X	H	Busy time in Program	
X	X	X	X	X	H	Busy time in Erase	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0 V / V_{CC}	Stand By	

Table7: Mode Selection

NOTES:
1. As 4Gbit SLC F41 is CE# don't care device, CE# high during latency time does not stop the read operation.

2. BUS OPERATION

There are six standard bus operationTable 28s that control the device. These are Command Input, Address Input, Data Input, Data Output, Write PrTable 28otect, and Standby. (see **Figure 1** and **Table 6**)
Typically glitches less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1. Command Input

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See **Figure 5** and **Table 28** for details of the timings requirements. Command codes are always applied on IO7:0 regardless of the bus configuration. (X8 or X16)

2.2. Address Input

Address Input bus operation allows the insertion of the memory address. 5 clock cycles are needed to input the addresses. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See **Figure 5** and **Table 28** for details of the timings requirements. Addresses are always applied on IO7:0 regardless of the bus configuration. (X8 or X16). Refer to **Table 4** and **Table 5** for more detailed information.

2.3. Data Input

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serial and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See **Figure 7** and **Table 28** for details of the timings requirements.

2.4. Data Output

Data Output bus operation allows to read data from the memory array and to check the status register content, the EDC register content and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See **Figure 8** to **Figure 11** and **Table 28** for details of the timings requirements.

2.5. Write Protect

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6. Standby

In Standby the device is deselected, outputs are disabled and Power Consumption is reduced.

3. DEVICE OPERATION

3.1. Page Read

This operation is initiated by writing 00h and 30h to the command register along with five address cycles. Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 2112 bytes (x8) or 1056 (x16) of data within the selected page are transferred to the data registers in less than 25us(tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns (3V version) and 45nsec (1.8V version) cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address.
The device may output random data in a page instead of the sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command.
Random data output can be operated multiple times regardless of how many times it is done in a page.
After power up device is in read mode, so 00h command cycle is not necessary to start a read operation. Any operation other than read or random data output causes device to exit read mode.
Check **Figure 12, Figure 13, Figure 14** as references.

3.2 Data handling restirctions during program sequences

Applications which use the error detection code in copy back must respect some restrictions related to data handling during program sequence.
The error dection code check is used during copy back program and multiplane copy back program operations to detect single bit errors pccurred in the source page (for details about EDC)

Note: The restrictions described below are not valid if the application uses the copy back program or multiplane copy back program without EDC check.

When data handling is performed, the page program, multiplane page program, page re-program, multiplane page re-program, cache ptrgram and multiplane cache program operations, must respect the following restrictions:
1. Program operations must be performed on the whole page, or on the whple EDC unit at a time.
2. For each program operation, random data input can be executed only once for each EDC unit.

Copy back program or multiplane copy back program opeations must respect the following restrictions:
1. If rando, data input is applied in a given EDC unit, the data of the whole EDC unit must be inserted. In ohter words, the EDC check is possible only if the whole EDC unit is modified during a copy back program sequence.
2. For each program operation, rando, data input can be executed only once for each EDC unit.

3.3 Page Program

A page program cycle consists of a serial data loading period in which up to 2112 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.
The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.
The Page Program confirm command (10h) initiates the programming process. The internal write state controller automat-

ically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) or Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 14 and Figure 15 detail the sequence.
The device is programmed basically by page, but it also allows multiple partial page programming of a word or consecutive bytes up to 2112 (x8) or 1056 (x16) in a single page program cycle.
The number of consecutive partial page programming operations (NOP) within the same page must not exceed the number indicated in **Table 27**. In addition, pages must be sequentially programmed within a block.
Users which use "EDC check" in copy back must comply with some limitations related to data handling during one page program sequence. Please refer to Section 3.10 for details.

3.4. Multiple plane program

Device supports multiple plane program: it is possible to program 2 pages in parallel, one per each plane.
A multiple plane program cycle consists of a double serial data loading period in which up to 4224bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins with inputting the Serial Data Input command (80h), followed by the five cycle address inputs and serial data for the 1^{st} page. Address for this page must be in the 1^{st} plane (A<18>=0). The device supports random data input exactly same as in the case of page program operation. The Dummy Page Program Confirm command (11h) stops 1^{st} page data input and devices becomes busy for a short time (t_{DBSY}). Once it has become ready again, either the traditional "81h" or the ONFI 1.0 "80h" command must be issued, followed by 2^{nd} page address (5 cycles) and its serial data input. Address for this page must be in the 2^{nd} plane (A<18>=1). Program Confirm command (10h) makes parallel programming of both pages to start. **Figure 20** and **Figure 21** describe the sequences.

User can check operation status by monitoring RB# pin or reading status register commands (70h or 78h), as if it were a normal page program: read status register command is also available during Dummy Busy time (t_{DBSY}).
In case of fail in any of 1^{st} and 2^{nd} page program, fail bit of status register will be set however, in order to know which page failed, ONFI 1.0 "read status enhanced" command must be issued Refer to **section 3.11** for further info.

The number of consecutive **partial page programming operations** (NOP) within the same page must not exceed the number indicated in **Table 27.** In addition, it is recommended to program pages sequentially within a block.

3.5. Block Erase

The Block Erase operation is done on a block basis. Block address loading is accomplished in 3 cycles initiated by an Erase Setup command (60h). Only addresses A18 to A29 are valid while A12 to A17 are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase-verify.
Once the erase process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of an erase by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.
Figure 19 details the sequence.

3.6. Multiple plane Block Erase

Multiple plane erase, allows parallel erase of two blocks in parallel, one per each memory plane.
Two different command sequences are allowed in these case, traditional and ONFI 1.0.

In traditional case, Block erase setup command (60h) must be repeated two times, followed by 1st and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation to start.

In this case, multiplane erase does not need any Dummy Busy Time between 1st and 2nd block insertion.
See **Figure 25** for details.

As an alternative, the ONFI 1.0 multiplane command protocol can be used, with 60h erase setup followed by 1st block address and D1h first confirm, 60h erase setup followed by 2nd block address and D0h (multiplane confirm). Between the two block-related sequences, a short busy time t_{IEBSY} will occur. See **Table 27** and **Figure 26** for details.

Address limitation required for multiple plane program applies also to multiple plane erase. Also operation progress can be checked like in the multiple plane program through Read Status Register, or ONFI 1.0 Read Status Enhanced.

As for multiplane page program, the address of the first second page must be within the first plane (A18=0 for x8 devices, A17=0 for x16 devices) and second plane (A18 = 1 for devices, A17=1 for x16 devices), respectively.

3.7. Copy-Back Program.

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is greatly improved. The benefit is especially obvious when a portion of a block needs to be updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read (without mandatory serial access) and copy back -program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112byte data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE# (see **Figure 17**), or Copy Back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation.

Source and Destination page in the copy back program sequence must belong to the same device plane (x8 : same A18, x16 : same A17)

Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in **Figure 18.**

This device includes automatic Error Detection Code check during copy back operation, to detect single bit errors in EDC units occurred in the source page.

More details on EDC operation, and limitation related to data input handling during one copy back program sequence are available in **section 3.10**

3.8. Multiple plane copy back Program

As for page program, device supports Multi-plane copy back program with exactly same sequence and limitations. Multi plane copy back program must be preceded by 2 single page read for copy back command sequences (1st page must be read from the 1st plane and 2nd page from the 2nd plane).
Multi-plane copy back cannot cross plane boundaries : the contents of the source page of one device plane can be copied only to a destination page of the same plane.
EDC check is available also for multi-plane copy back program.
Users which use "EDC check" in copy back must comply with some limitations related to data handling during one multi-plane copy back program sequence. Please refer to **Section 3.10** for details.

Also in this case, two different sequences are allowed : the traditional one (85h, first plane address 11h, 81h, second plane address, 10h) represented in **Figure 22**, and ONFI 1.0 sequence (85h, first plane address 11h, 85h, second plane address, 10h) represented in **Figure 23 and Figure 24**.

3.9. Special read for copy back

The device feature the "special read for copy back".
If copy back read (described in **sections 3.7** and **3.8**) is triggered with confirm command "36h" instead "35h", copy back read from target page(s) will be executed with an increased internal (Vpass) voltage.
This special feature is used in order to try to recover incorrigible ECC read errors due to over-program or read disturb: it shall be used ONLY if ECC read errors have occurred in the source page using "standard read" or "standard read for copy back" sequences..

Excluding the copy-back read confirm command, all other features described in **sections 3.7** and **3.8** for standard copy back remain valid (including the figures referred to in those sections).

3.10. EDC operation

Error Detection Code check is a feature which be used during copy back program operation (both single and multi-plane) to detect single bit errors occurred in the source page (s).

- In the x8 version EDC check allows detection of up to 1 single bit error every 528 bytes, where each 528 byte group is composed by 512 byte of main array and 16 bytes of spare area (see **Table 8** and **Table 9**). The described 528 byte area is called "EDC unit".

- In the x16 version EDC allows detection of up to 1 single bit error every 264 words, where each 264 word group is composed by 256 words of main array and 8 words of spare area (see **Table 10** and **Table 11**). The described 264 word area is called "EDC unit".

EDC result can be checked through specific Read EDC register command, available only during copy back program and only for the device version supporting ECC=1. EDC register can be queried during the copy back program busy time. (t_{PROG})

For "EDC check" feature to operate correctly specific conditions on data input handling apply for page program and copy back program (single, cached, multi-plane):

For the case of page program

1) In section 3.2 it was explained that a number of consecutive partial program operations (NOP) is allowed within the same page. In case this feature is used, the number of partial program operations occurring in the same EDC unit must not exceed "one" (1). In other words, page program operations must be performed on the whole page, or on whole EDC unit at a time.

2) "random data input" in a given EDC unit can be executed several times during one page program sequence, but data insertion in each column address of each EDC unit must not exceed "one" (1).

For the case of copy back program

1) If random data input is applied in a given EDC unit, the data of the whole EDC unit must be inserted. In other words, the EDC check is possible only if the whole EDC unit is modified during one copy back program sequence

2) "random data input" in a given EDC unit can be executed several times during one copy back sequence , but data insertion in each column address of the EDC unit must not exceed "one" (1)

For the user which use Copy Back without EDC check, all the limitations described above do not apply.

"A"area (1st sector)	"B"area (2nd sector)	"C"area (3rd sector)	"D"area (4th sector)	"E"area (1st sector)	"F"area (2nd sector)	"G"area (3rd sector)	"H"area (4th sector)
512 Byte	512 Byte	512 Byte	512 Byte	16 Byte	16 Byte	16 Byte	16 Byte

Table 8: page organization in EDC units (x8)

Sector	Main Field (Column 0~2047)		Spare Field (Column 2048~2111)	
	Area Name	Column Address	Area Name	Column Address
1st 528-Byte Sector	"A"	0~511	"E"	2048~2063
2nd 528-Byte Sector	"B"	512~1023	"F"	2064~2079
3rd 528-Byte Sector	"C"	1024~1535	"G"	2080~2095
4th 528-Byte Sector	"D"	1536~2047	"H"	2096~2111

Table 9: page organization in EDC units (x8)

"A"area (1st sector)	"B"area (2nd sector)	"C"area (3rd sector)	"D"area (4th sector)	"E"area (1st sector)	"F"area (2nd sector)	"G"area (3rd sector)	"H"area (4th sector)
256 words	256 words	256 words	256 words	8 words	8 words	8 words	8 words

Table 10: page organization in EDC units (x16)

Sector	Main Field (Column 0~1023)		Spare Field (Column 1024~1055)	
	Area Name	Column Address	Area Name	Column Address
1st 264-word Sector	"A"	0~255	"E"	1024~1031
2nd 264-word Sector	"B"	256~511	"F"	1032~1039
3rd 264-word Sector	"C"	512~767	"G"	1040~1047
4th 264-word Sector	"D"	768~1023	"H"	1048~1055

Table 11: page organization in EDC units (x16)

3.11 Read Status Register.

The device contains a Status Register to retrieve the status value for the last operation issued. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when RB# pins are common-wired. Refer to **Table 12** for specific Status Register definition, and to **Figure 10** and **Figure 38** for timings.

If Read Status register command is issued during multi-plane operations Read Status Register polling shall return the combined status value related to the outcome of the operation in the two planes according to this table:

Status Register bit	Composite status value
Bit 0, Pass/Fail	OR
Bit 1, Cache Pass/Fail	OR

Status register is dynamic in other words, user is not required to toggle RE# / CE# to update it.

The command register remains in Status Read mode until further commands are issued. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

Note:
Read Status Register command shall not be used for concurrent operations in of multi-dice stack configurations (single CE#). For this case, either "Read Status Enhanced" (**Section 3.12**) shall be used instead.

3.12 Read Status Enhanced

Read Status Enhanced is an additional feature used to retrieve the status value for a previous operation in the following cases:

- on a specific die of a multi-dice stack configurations (single CE#), in case of concurrent operations

When 4Gbit dice are stacked(*) to form 8Gbit DDP or 16Gbit QDP (single CE#), it is possible to run a first operation on the first 4Gbit, then activate a concurrent operation on the second (or third or fourth) device. (examples: Erase while Read, Read while Program, etc.)

- on a specific plane in case of multi-plane operations in the same die.

Figure 39 defines the Read Status Enhanced behavior and timings. The plane and die address must be specified in the command sequence in order to retrieve the status of the die and the plane of interest.

Refer to **Table 12** for specific Status Register definition. The command register remains in Status Read mode until further commands are issued.

Status register is dynamic in other words, user is not required to toggle RE# / CE# to update it.

3.13 Read Status Register field definition

Table 12 below lists the meaning of each bit of Read Status Register and Read Status Enhanced

IO	Page Program/ Page Reprogram	Block Erase	Read	Cache Read	Cache Program/ Cache reprogram	CODING
0	Pass / Fail	Pass / Fail	NA	NA	Pass / Fail	N Page Pass: '0' Fail: '1'
1	NA	NA	NA	NA	Pass / Fail	N - Page Pass: '0' Fail: '1'
2	NA	NA	NA	NA	NA	-
3	NA	NA	NA	NA	NA	-
4	NA	NA	NA	NA	NA	-
5	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Active: '0' Idle: '1'
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data cache Read/Busy Busy: '0' Ready: '1'
7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected: '0' Not Protected: '1'

Table 12: Status Register Coding

3.14 Read EDC status register

This operation is available only in copy back program and it allows the detection of errors occurred during read for copy back. In case of multiple plane copy back, it is not possible to know which of the two read operation caused the error. After writing Read EDC status register command (7Bh) to the command register, a read cycle outputs the content of the EDC Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last.
Operation is same as read status register command. Refer to **Table 13** for specific EDC Register definitions:

IO	Copy back program	CODING
0	Pass / Fail	Pass: '0' Fail: '1'
1	EDC status	No error: '0' Error: '1'
2	EDC validity	Invalid: '0' Valid: '1'
3	NA	-
4	NA	-
5	Ready / Busy	Busy: '0' Ready: '1'
6	Ready / Busy	Busy: '0' Ready: '1'
7	Write Protect	Protected: '0' Not Protected: '1'

Table 13: EDC register coding

3.15 Reset

The device offers a reset feature, executed by writing FFh to the command register. If the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high. Refer to **table 16** for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The RB# pin transitions to low for t_{RST} after the Reset command is written. Refer to **Figure 28** for further details.

3.16 Cache Read

Cache Read can be used to increase the read operation speed, as defined in **Section 3.1**, which is available only within a block. As soon as the user starts to read one page, the device automatically loads the next page into the cache register. Serial data output may be executed while data in the memory is read into cache register, Cache Read is initiated by the page read sequence (00-30h) on a page M.
After random access to the first page is complete (R/B# returned to high, or read status register IO<6> switches to high), two command sequences can be used to continue read cache:

- sequential read cache continue (command "31h" only): once the command is latched into the command register (see **Figure 30**), device does busy for a short time (t_{RCBSY}), during which data of the first page is transferred from the data register to the cache register. At the end of this phase cache register data can be output by toggling RE# while the "next "page (page address M+1) is read from the memory array into data register.

- random read cache continue (sequence "00h" <page N address> "31"): once the command is latched into the command register (see **Figure 31**), device does busy for a short time (t_{RCBSY}), during which data of the first page is transferred from the data register to the cache register. At the end of this phase cache register data can be output by toggling RE# while page N is read from the memory array into data register.

Subsequent pages are read by issuing additional "sequential" or "random" read cache continue command sequences.
If serial data output time of one page exceeds random access time (t_R), the random access time of the next page is hidden by data downloading of the previous page.
On the other hand, if 31h is issued prior to complete the random access to the next page, the device will stay busy as long as needed to complete random access to this page, transfer its contents into the cache register, and trigger the random access to the following page.
To terminate cache read, 3Fh command should be issued (see **Figure 32**). This command transfer data from data register to the cache register without issuing next page read.
During the Cache Read Operation, device doesn't allow any other command except for 31h, 3Fh, Read SR or reset (FFh).
To carry out other operations Cache read must be ended either by 3Fh command or device must be reset by issuing FFh.

Read Status command (70h) may be issued to check the status of the different registers, and the busy/ready status of the cached read operations. More in detail:
a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to output new data.
b) the status bit I/O<5> can be used to determine when the cell reading of the current data register contents is complete.

Note:
31h and 3Fh commands reset the column counter thus when RE# is toggled to output the data of a given page, the first output data is related to the first byte of the page (column address 00h). Random data output command can be used to switch column address.

3.17 Cache Program

Cache Program is used to improve the program throughput by programing data using the cache register. The cache program operation can only be used within one block. The cache register allows new data to be input while the previous data that was transffered to the page buffer is programmed into the memory array.
Cache program is available only within a block

After the serial data input command (80h) is loaded to the command register, followed by 5 cycles of address, a full or partial page of data is latched into the cache register.
Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state For a short time (tCBSYW). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence (80h-15h).
The Busy time following the first sequence 80h - 15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is conse quently processed through a pipeline model.
In case of any subsequent sequence 80h - 15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete: till this moment the device will stay in a busy state (tCBSYW).
Read Status commands (70h or 78h) may be issued to check the status of the different registers, and the pass/fail status of the cached program operations. More in detail:
a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data.
b) the status bit I/O<5> can be used to determine when the cell programming of the current data register contents is complete.
c) the cache program error bit I/O<1> can be used to identify if the previous page (page N-1) has been successfully programmed or not in cache program operation. The latter can be polled upon I/O<6> status bit changing to "1" .
d) the error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while program ming page N. The latter can be polled upon I/O<5> status bit changing to "1".

I/O<1> may be read together with I/O<0>.
If the system monitors the progress of the operation only with R/B#, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation.

See **Table 12** and **Figure 40** for more details.

3.18 Multi-plane Cache Program

The device supports multi-plane cache program, which enables high program throughput by programming two pages in parallel while exploiting the data and cache registers of both planes to implement cache.
The device supports both the traditional and ONFI 1.0 command sets.

The command sequence can be summarized as follows:
a) Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1^{st} page. Ad dress for this page must be within 1^{st} plane (A<20>=0). The data of 1^{st} page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation.
b) The Dummy Page Program Confirm command (11h) stops 1^{st} page data input and the device becomes busy for a short time (t_{DBSY}).
c) Once device returns to ready again, 81h (or 80h) command must be issued, followed by 2^{nd} page address (5 cycles) and its serial data input. Address for this page must be within 2^{nd} plane (A<20>=1). The data of 2^{nd} page other than those to be programmed do not need to be loaded.
d) Cache Program confirm command (15h) Once the cache write command (15h) is loaded to the command register, the

data in the cache registers is transferred into the data registers for cell programming. At this time the device remains in Busy state for a short time (tCBSYW). After all data of the cache registers are transferred into the data registers, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command se quence.

The sequence 80h-...- 11h...-...81h...-...15h (or the corresponding ONFI 80h-...- 11h...-...80h...-...15h) can be iterated, and any new time the device will be busy for a for the tCBSYW time needed to complete cell programming of current data registers contents, and transfer from cache registers can be allowed.

The sequence to end multi-plane cache program is 80h-...- 11h...-...81h...-...10h (or 80h-...- 11h...-...80h...-...10h for the ONFI 1.0 case).
Figure 50 and Figure 51 show the command sequence for the multi plane cache program operation for the two protocols.
Multi-plane Cache program is available only within two paired blocks belonging to the two planes..

User can check operation status by R/B# pin or read status register commands (70h or 78h)
If user opts for 70h, Status register read will provide a "global" information about the operation in the two planes. More in detail:

a) I/O<6> indicates when both cache registers are ready to accept new data.
b) I/O<5> indicates when the cell programming of the current data registers is complete
c) I/O<1> identifies if the previous pages in both planes (pages N-1) have been successfully programmed or not. The latter can be polled upon I/O<6> status bit changing to "1".
d) I/O<0> identifies if any error has been detected by the program / erase controller while programming the two pages N. The latter can be polled upon I/O<5> status bit changing to "1".

See **Table 12** for more details

If the system monitor rs the progress of the operation only with R/B#, the last pages of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the sta tus bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation.
Refer to **section 3.11** for further information.

3.19 Read ID.

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.

The 5-byte Read ID configuration are supported: The device operating mode (5-byte) is selected through cam setting.

3.19.1 Legacy Read ID

Five read cycles sequentially output the manufacturer code (20h), and the device code and 3rd, 4th, and 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. **Figure 27** shows the operation sequence, while **Table 14** to **Table 18** explain the byte meaning. Complete read id code table is as follows.

DENSITY	ORG	VCC	1st	2nd	3rd	4th (1)	5th
4 Gbit	X8	3.0V	ADh	DCh	90h	95h	54h
	X16	3.0V	ADh	CCh	90h	D5h	54h
	X8	1.8V	ADh	ACh	90h	15h	54h
	X16	1.8V	ADh	BCh	90h	55h	54h
8 Gbit DDP	X8	3.0V	ADh	D3h	D1h	95h	58h
	X16	3.0V	ADh	C3h	D1h	D5h	58h
	X8	1.8V	ADh	A3h	D1h	15h	58h
	X16	1.8V	ADh	B3h	D1h	55h	58h
16 Gbit QDP	X8	3.0V	ADh	D5h	D2h	95h	5Ch
	X16	3.0V	ADh	C5h	D2h	D5h	5Ch
	X8	1.8V	ADh	A5h	D2h	15h	5Ch
	X16	1.8V	ADh	B5h	D2h	55h	5Ch

Table 14: Legacy " Read ID for supported configurations

NOTE: for 1.8V version, IO<7,3>=00 would mean "50nsec", while device serial cycle time is 45nsec

DEVICE IDENTIFIER BYTE	DESCRIPTION
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell type, etc.
4th	Page Size, Block Size, Spare Size, Organization
5th	Multiplane information

Table 15: "Legacy" Read ID bytes meaning

3rd ID Data

	Description	I/O7	I/O6	I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleave Program Between multiple chips	Not Support Support		0 1			
Cache Program	Not Support Support	0 1				

Table 16: Legacy Read ID 3rd byte description

4th ID Data

	Description	I/O7	I/O6	I/O5 I/O4	I/O3	I/O2	I/O1 I/O0
Page Size (w/o redundant area)	1KB 2KB 4KB 8KB						0 0 0 1 1 0 1 1
Block Size (w/o redundant area)	64KB 128KB 256KB 512KB			0 0 0 1 1 0 1 1			
Redundant Area Size (byte/512byte)	8 16					0 1	
Organization	X8 X16		0 1				
Serial Access Minimum	50ns/30ns 25ns Reserved Reserved	0 1 0 1			0 0 1 1		

Table 17: Legacy Read ID 4th byte description

5th ID Data

	Description	I/O7	I/O6 I/O5 I/O4	I/O3 I/O2	I/O1	I/O0
Plane Number	1 2 4 8			0 0 0 1 1 0 1 1		
Plane Size (w/o redundant Area)	64Mb 128Mb 256Mb 512Mb 1Gb 2Gb 4Gb 8Gb		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1			
Reserved		0			0	0

Table 18: Legacy Read ID 5th byte description

3.20 Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. **Figure 28** shows the operation sequence

3.21 Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timings and other behavioral parameters. **Figure 37** defines the Read Parameter Page behavior.
This data structure enables the host processor to automatically recognize the Nand Flash configuration of a device. The whole data structure is repeated at leat three times.

The Random Data Read command can be issued during execution of the read parameter page to read specific portions of the parameter page.

The Read Status command may be used to check the status of read parameter page during execution. After completion of the Read Status command, 00h is issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.

Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

3.22 Parameter Page Data Structure Definition

Table21 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.
Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the chip will return how many data bytes are in a page. For a device that supports 16-bit data access, the host is required to convert byte values to word values for its use. Unused fields should be cleared to 0h.
For more detailed information about Parameter Page Data bits, refer to ONFI Specification 1.0 **section 5.4.1**

Byte	O/M	Description	Values
	Revision information and features block		
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	4Fh, 4Eh, 46h, 49h
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)	02h, 00h
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width	**H27U4G8F2DKA-BM**:1Ch, 00h **H27S4G8F2DKA-BM**:1Ch, 00h **H27S4G6F2DKA-BM**:1Dh, 00h **H27U4G8F2DTR-BC**:1Ch, 00h **H27U4G8F2DTR-BI**:1Ch, 00h **H27U8G8G5DTR-BC**:1Ch, 00h **H27U8G8G5DTR-BI**:1Ch, 00h
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache ntegrit 0 1 = supports Page Cache Program command	1Bh, 00h
10-31		Reserved (0)	00h
	Manufacturer information block		
32-43	M	Device manufacturer (12 ASCII characters)	48h, 59h, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
44-63	M	Device model (20 ASCII characters)	**H27U4G8F2DKA-BM** 48h, 32h, 37h, 55h, 34h, 47h, 38h, 46h, 32h, 44h, 4Bh, 41h, 2Dh, 42h, 4Dh, 20h, 20h, 20h, 20h, 20h **H27S4G8F2DKA-BM** 48h, 32h, 37h, 53h, 34h, 47h, 38h, 46h, 32h, 44h, 4Bh, 41h, 2Dh, 42h, 4Dh, 20h, 20h, 20h, 20h, 20h **H27S4G6F2DKA-BM** 48h, 32h, 37h, 53h, 34h, 47h, 36h, 46h, 32h, 44h, 4Bh, 41h, 2Dh, 42h, 4Dh, 20h, 20h, 20h, 20h, 20h **H27U4G8F2DTR-BC** 48h, 32h, 37h, 55h, 34h, 47h, 38h, 46h, 32h, 44h, 54h, 52h, 2Dh, 42h, 43h, 20h, 20h, 20h, 20h, 20h **H27U4G8F2DTR-BI** 48h, 32h, 37h, 55h, 34h, 47h, 38h, 46h, 32h, 44h, 54h, 52h, 2Dh, 42h, 49h, 20h, 20h, 20h, 20h, 20h **H27U8G8G5DTR-BC** 48h, 32h, 37h, 55h, 38h, 47h, 38h, 47h, 35h, 44h, 54h, 52h, 2Dh, 42h, 43h, 20h, 20h, 20h, 20h, 20h **H27U8G8G5DTR-BI** 48h, 32h, 37h, 55h, 38h, 47h, 38h, 47h, 35h, 44h, 54h, 52h, 2Dh, 42h, 49h, 20h, 20h, 20h, 20h, 20h
64	M	JEDEC manufacturer ID	ADh
65-66	O	Date code	00h
67-79		Reserved (0)	00h

	Memory organization block		
80-83	M	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	M	Number of spare bytes per page	40h, 00h
86-89	M	Number of data bytes per partial page	00h, 02h, 00h, 00h
90-91	M	Number of spare bytes per partial page	10h, 00h
92-95	M	Number of pages per block	40h, 00h, 00h, 00h
96-99	M	Number of blocks per logical unit (LUN)	00h, 10h, 00h, 00h
100	M	Number of logical units (LUNs)	01h
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles	23h
102	M	Number of bits per cell	01h
103-104	M	Bad blocks maximum per LUN	50h, 00h
105-106	M	Block endurance	01h, 05h
107	M	Guaranteed valid blocks at beginning of target	01h
108-109	M	Block endurance for guaranteed valid blocks	00h, 00h
110	M	Number of programs per page	04h
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00h
112	M	Number of bits ECC correctability	01h
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	01h
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	04h
115-127		Reserved (0)	00h
	Electrical parameters block		
128	M	I/O pin capacitance	0Ah
129-130	M	Timing mode support 6-1 5Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1	**H27U4G8F2DKA-BM**:1Fh, 00h **H27S4G8F2DKA-BM**:03h, 00h **H27S4G6F2DKA-BM**:03h, 00h **H27U4G8F2DTR-BC**:1Fh, 00h **H27U4G8F2DTR-BI**:1Fh, 00h **H27U8G8G5DTR-BC**:1Fh, 00h **H27U8G8G5DTR-BI**:1Fh, 00h

131-132	O	Program cache timing mode support 6-1 5Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0,	**H27U4G8F2DKA-BM**:1Fh, 00h **H27S4G8F2DKA-BM**:03h, 00h **H27S4G6F2DKA-BM**:03h, 00h **H27U4G8F2DTR-BC**:1Fh, 00h **H27U4G8F2DTR-BI**:1Fh, 00h **H27U8G8G5DTR-BC**:1Fh, 00h **H27U8G8G5DTR-BI**:1Fh, 00h
133-134	M	t_{PROG} Maximum page program time (µs)	BCh, 02h
135-136	M	t_{BERS} Maximum block erase time (µs)	0Ah, 00h
137-138	M	t_R Maximum page read time (µs)	19h, 00h
139-140	M	t_{ccs} Minimum Change Column setup time (ns)	64h, 00h
141-163		Reserved (0)	00h
	Vendor block		
164-165	M	Vendor specific Revision number	00h
166-253		Vendor specific	00h
254-255	M	Integrita CRC	**H27U4G8F2DKA-BM**:48h, F6h **H27S4G8F2DKA-BM**:9Bh, CEh **H27S4G6F2DKA-BM**:54h, 61h **H27U4G8F2DTR-BC**:1Fh, EDh **H27U4G8F2DTR-BI**:5Bh, 14h **H27U8G8G5DTR-BC**:FCh, C1h **H27U8G8G5DTR-BI**:B8h, 38h
	Redundant Parameter Pages		
256-511	M	Value of bytes 0-255	Repeat Value of bytes 0-255
512-767	M	Value of bytes 0-255	Repeat Value of bytes 0-255
768+	O	Additional redundant parameter pages	FFh

Table 21: Parameter Page Description

NOTE: “O” Stands for Optional, “M” for Mandatory

4. OTHER FEATURES

4.1 Data Protection and Power on / off sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.8V (3V version), or 1.1V (1.8V version).

The power-up and power-down sequence is shown in **Figure 32** in this case V_{CC} and V_{CCQ} on the one hand (and VSS and V_{SSQ} on the other hand) are shorted together at all times

The Ready/Busy signal shall be valid within 100us since the power supplies have reached the minimum values (as specified on), and shall return to one within 5msec (max).
During this busy time, the device executes the initialization process (cam reading), and dissipates a current ICC0 (30mA max) in addition, it disregards all command excluding Read Status Register (70h).
At the end of this busy time, the device deaults into "read setup", thus if user decides to issue page read command, the 00h command may be skipped.

WP# pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 100usec is required before internal circuit gets ready for any command sequences as shown in **Figure 33**. The two-step command sequence for program/erase provides additional software protection.

4.2 Ready/Busy.

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copyback, random read completion. The RB# pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more RB# outputs to be Or-tied. Because pull-up resistor value is related to tr(RB#) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (**refer to Figure 34**). Its value can be determined by the following guidance.

4.3 Write protect (#WP) handling

Erase and program operations are aborted if WP# is driven low during busy time, and kept low for about 100nsec.
Switching WP# low during this time is equivalent to issuing a Reset command (FFh)
The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased.
The R/B# pin will stay low for t_{RST} (similarly to **Figure 29**). At the end of this time, the command register is ready to process the next command, and the Status Register bit IO<6> will be cleared to "1", while IO<7> value will be related to the WP# value.
Refer to **Table 12** for more information on device status.

Erase and program operations are enabled or disabled by setting WP# to high or low respectively prior to issuing the set-up commands (80h or 60h).

The level of WP# shall be set tWW nsec prior to raising the WE# pin for the set up command, as explained in F**igure 35** and **Figure 36**.

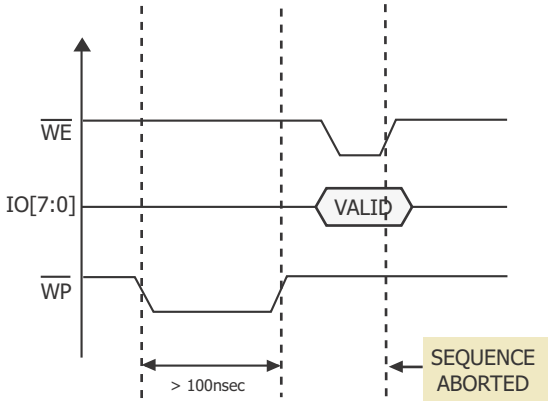


Figure 5: WP# low timing requirements during program/erase command sequence

5. Device Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Numbe, 4Gb	N_{VB}	4016	-	4096	Blocks
Valid Block Numbe, 8Gb	N_{VB}	8032(*)	-	8192	Blocks
Valid Block Numbe, 16Gb	N_{VB}	16064(*)	-	16284	Blocks

Table 22: Valid Blocks Number

(*) Each 4Gb has maximum 80 bad blocks
NOTE: The 1st block is quranteed to be a valid blick at the time of shipment.

Symbol	Parameter	Value	Unit
		3.0	
T_A	Ambient Operating Temperature (Commercial Temperature Range)	0 to 70	°C
	Ambient Operating Temperature (Industrial Temperature Range)	-40 to 85	°C
T_{BIAS}	Temperature Under Bias	-50 to 125	°C
T_{STG}	Storage Temperature	-60 to 150	°C
V_{IO}(2)	Input or Output Voltage	-0.6 to 4.6	V
V_{CC}	Supply Voltage	-0.6 to 4.6	V

Table 23: Absolute maximum ratings

NOTES:
1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Expo sure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMi croelectronics SURE Program and other relevant quality documents.

2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

Parameter		Symbol	Test Conditions	1.8Volt			3.0Volt			Unit
				Min	Typ	Max	Min	Typ	Max	
Power on current		I_{CC0}	Power up Current (Refer to 4.41)	-	15	30	-	15	30	mA
Operating Current	Sequential Read	I_{CC1}	t_{RC} = see **Table 28** CE#=v_{IL}, I_{out}=0MA	-	10	20	-	15	30	mA
	Program	I_{CC2}	Normal	-	-	20	-	-	30	mA
			Cache	-	-	30	-	-	40	mA
	Erase	I_{CC3}	-	-	10	20	-	15	30	mA
Stand-by Current (TTL)		I_{CC4}	CE#=V_{IH}, WP#=0V/Vcc	-	-	1	-	-	1	mA
Stand-By Current (CMOS)		I_{CC5}	CE#=Vcc-0.2, WP#=0/Vcc	-	10	50	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to 3.6V	-	-	±10	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to 3.6V	-	-	±10	-	-	±10	uA
Input High Voltage		V_{IH}	-	Vcc *0.8	-	Vcc +0.3	Vcc *0.8	-	Vcc +0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	Vcc-*0.2	-0.3	-	Vcc *0.2	V
Output High Voltage Level		V_{OH}	I_{OH}= -100uA	Vcc-0.1	-	-	-	-	-	V
			I_{OH}= -400uA	-	-	-	2.4	--	-	V
Output Low Voltage Level		V_{OL}	I_{OH}= -100uA	-	-	0.1	-		-	V
			I_{OL}= 2.1mA	-	-	-	-	-	0.4	V
Output Low Current (RB#)		I_{OL}(RB#)	V_{OL}= 0.1V	3	-	4	-	-	-	mA
			V_{OL}= 0.4V	-	-	-	8	-	10	mA

Table 24: DC and Operating Characteristics

NOTES:

1) all V_{CCQ} and VCC pins, and VSS and VSSQ pins respectively are shorted together
2) Values listed in this table refer to the complete voltage range for V_{CC} and V_{CCQ} and to a single device in case of device stacking refer to **Section 7.3**
3) All current measurement are performed with a 0.1uF capacitor connected between the Vcc Supply Voltage pin and the Vss Ground pin.
4) Standby current measurement can be performed after the device has completed the initialization process at power up. Refer to **Section 4.1**for more details

Parameter	Value	
	1.8Volt	3.0Volt
Input Pulse Levels	0V to Vcc	0V to Vcc
Input Rise and Fall Times	5ns	5ns
Input and Output Timing Levels	Vcc / 2	Vcc / 2
Output Load (1.7V - 1.95Volt & 2.7V-3.6V)	1 TTL GATE and CL=30(1.8V), 50pF(3.3V)	1 TTL GATE and CL=30(1.8V), 50pF(3.3V)

Table 25: AC Test Conditions

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance (1)	$C_{I/O}$	V_{IL}= 0V	-	10	pF
Input Capacitance (1)	C_{IN}	V_{IN}= 0V	-	10	pF

Table 26: Pin Capacitance (TA = 25C, f=1.0MHz)

NOTE: For the stacked devices version the Input Capacitance is **10pF x (number of stacked chips)** and the I/O ca pacitance is **10pF x (number of stacked chips)**

Parameter		Symbol	Min	Typ	Max	Unit
Program Time / Multi-plane program Time (3.0V)		t_{PROG}	-	200	700	us
Program Time/ Multi-plane program Time (1.8V)			-	250	700	us
Dummy Busy Time for Two Plane Program		t_{DBSY}	-	0.5	1	us
Cache program short busy time		t_{CBSYW}	-	5	t_{PROG}	us
Number of partial Program Cycles in the same page	Main + Spare Array	NOP	-	-	4	Cycle
Block Erase Time / Multi-plane Erase Time (3.0V)		t_{BERS}	-	3.5	10	ms
Block Erase Time/ Multi-plane Block Erase Time (1.8V)		t_{BERS}	-	3.5	10	ms
Read Cache busy time		tCBSYR	-	3	tR	us
Multi-plane erase short busy time (ONFI protocol only)		t_{IEBSY}	-	0.5	1	us

Table 27: Program / Erase Characteristics

NOTE: Typical program time is defined as the time within which more than 50% of the whole pages are programmed (Vcc=3.3V and 1.8V, 25*C)

Parameter	Symbol	1.8 Volt		3.0 Volt		Unit
		Min	Max	Min	Max	
CLE Setup time	t_{CLS}	25		12		ns
CLE Hold time	t_{CLH}	10		5		ns
CE# Setup time	t_{CS}	35		20		ns
CE# Hold time	t_{CH}	10		5		ns
WE# Pulse width	t_{WP}	25		12		ns
ALE Setup time	t_{ALS}	25		12		ns
ALE Hold time	t_{ALH}	10		5		ns
Data Setup time	t_{DS}	20		12		ns
Data Hold time	t_{DH}	10		5		ns
Write Cycle time	t_{WC}	45		25		ns
WE# High Hold time	t_{WH}	15		10		ns
Address to Data Loading time	t_{ADL}	100		70		ns
Data Transfer from Cell to Register	t_{R}		25		25	us
ALE to RE# Delay	t_{AR}	10		10		ns
CLE to RE# Delay	t_{CLR}	10		10		ns
Ready to RE# Low	t_{RR}	20		20		ns
RE# Pulse Width	t_{RP}	25		12		ns
WE# High to Busy	t_{WB}		100		100	ns
Read Cycle Time	t_{RC}	45		25		ns
RE# Access Time	t_{REA}		30		20	ns
CE# Low to RE# Low	t_{CR}	10		10		ns
RE# High to Output Hi-Z	t_{RHZ}		100		100	ns
CE# High to Output Hi-Z	t_{CHZ}		30		30	ns
CE# High to ALE or CLE Don't care	t_{CSD}	10		10		ns
RE# High to Output Hold	t_{RHOH}	15		15		ns
RE# Low to Output Hold	t_{RLOH}	-		5		ns
CE# High to Output Hold	t_{COH}	15		15		ns
RE# High Hold Time	t_{REH}	15		10		ns
Output Hi-Z to RE# Low	t_{IR}	0		0		ns
RE# High to WE# Low	t_{RHW}	100		100		ns
WE# High to RE# Low	t_{WHR}	60		60		ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	5/10/500(2)		5/10/500(2)	ns
Write protection time	t_{WW}	100		100		ns

Table 28: AC Timing Characteristics

NOTES: 1. The time to Ready depends on the value of the pull-up resistor tied to RB# pin
2. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us

6. Timing Diagrams

Command Latch Cycle

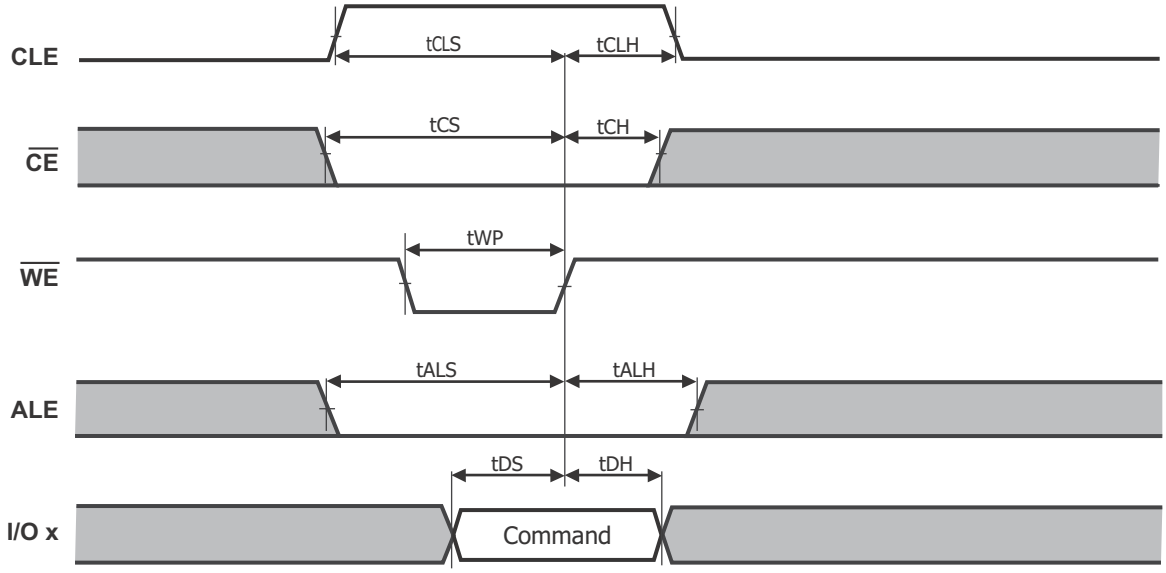


Figure 5: Command Latch Cycle

Address Latch Cycle

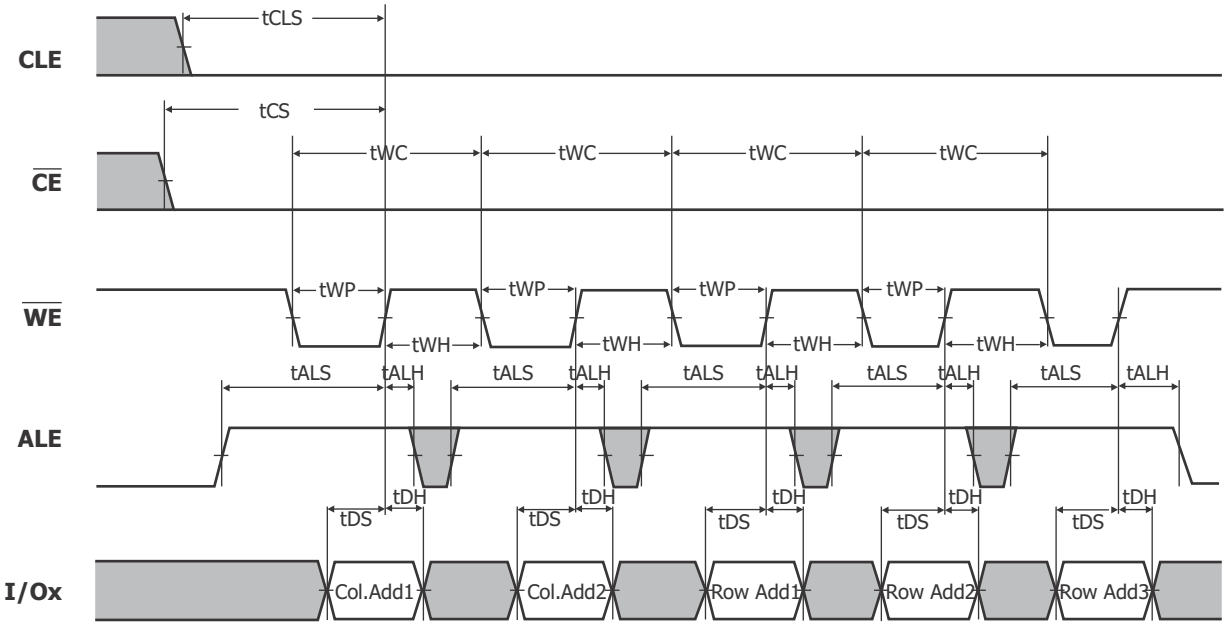


Figure 6: Address Latch Cycle

Input Data Latch Cycle

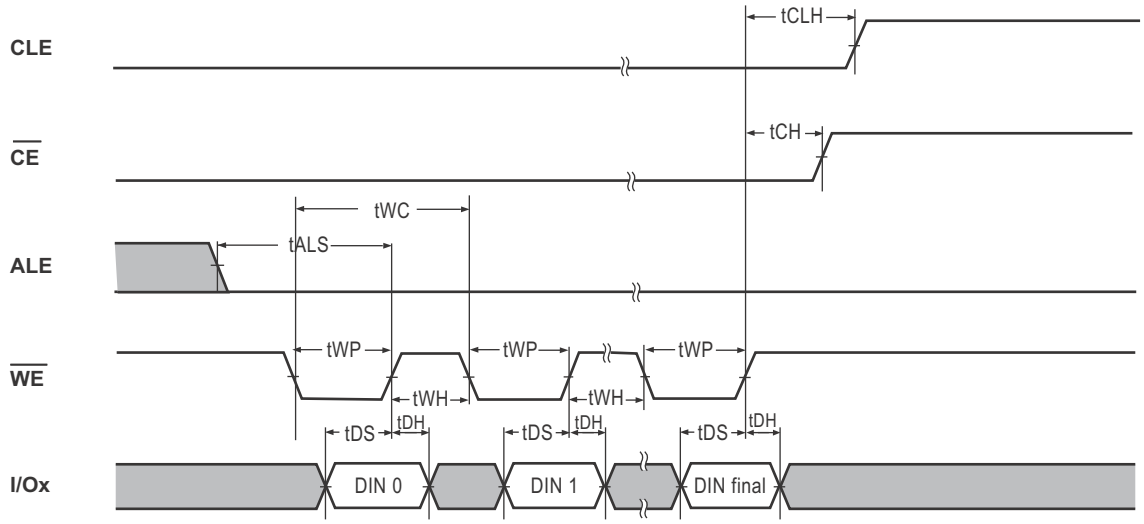
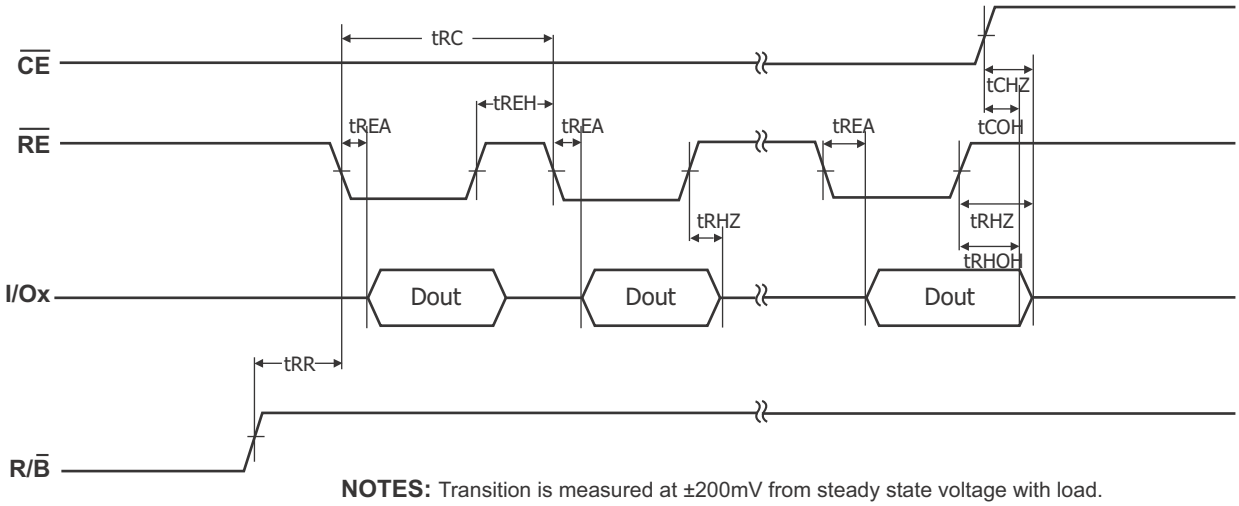


Figure 7: Input Data Latch Cycle

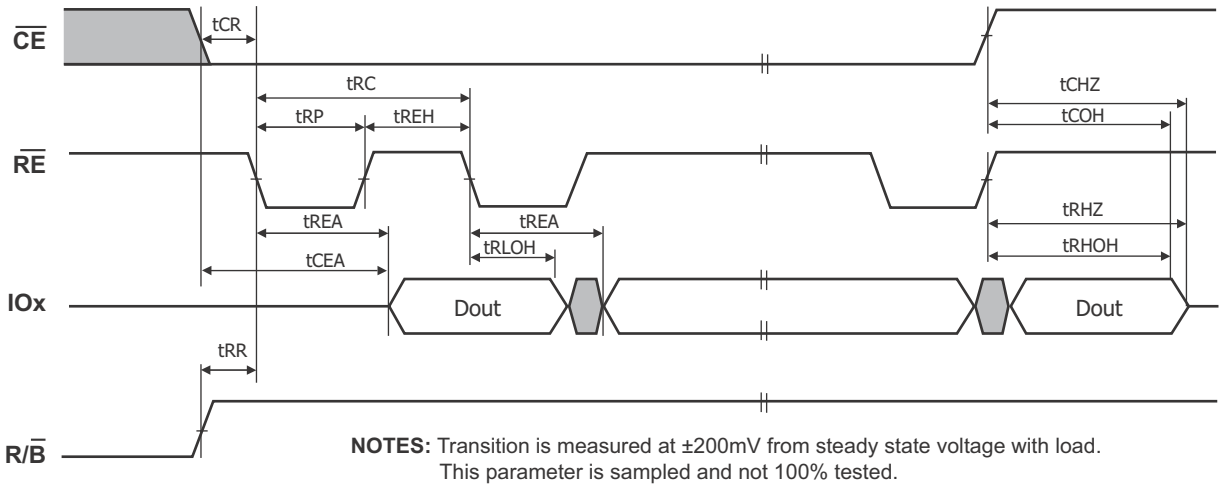
* Serial Access Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)



NOTES: Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 8: Sequential Out Cycle after Read

Serial Access Cycle after Read (EDO Type, CLE=L, $\overline{WE}$=H, ALE=L)



NOTES: Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to valid when frequency is lower than 33MHz.

Figure 9: Sequential Out Cycle after Read

Status Read Cycle & EDC Status Read Cycle

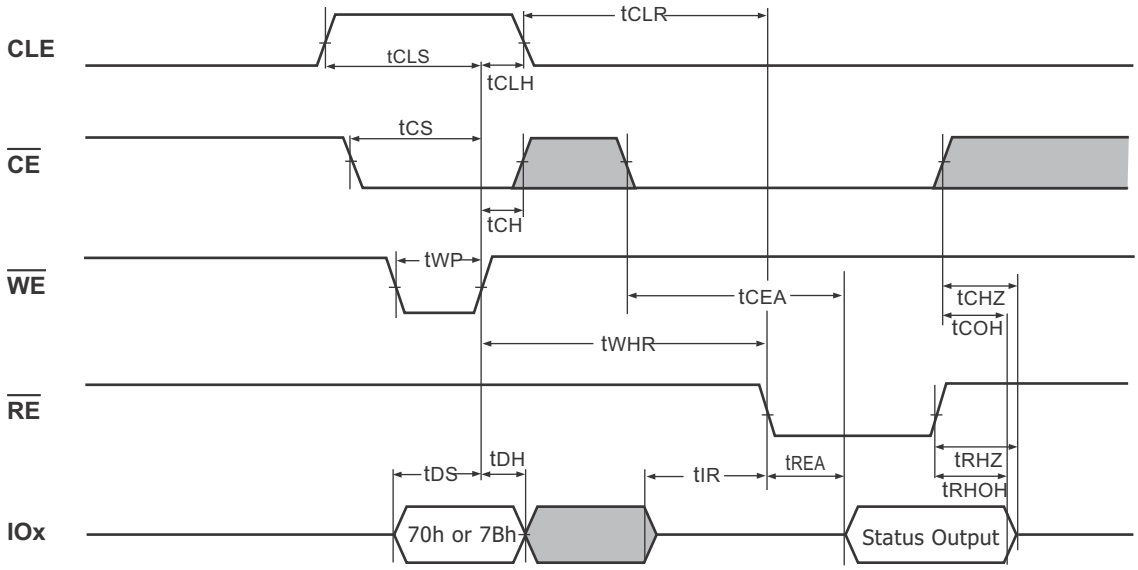


Figure 10: Status / EDC Read Cycle

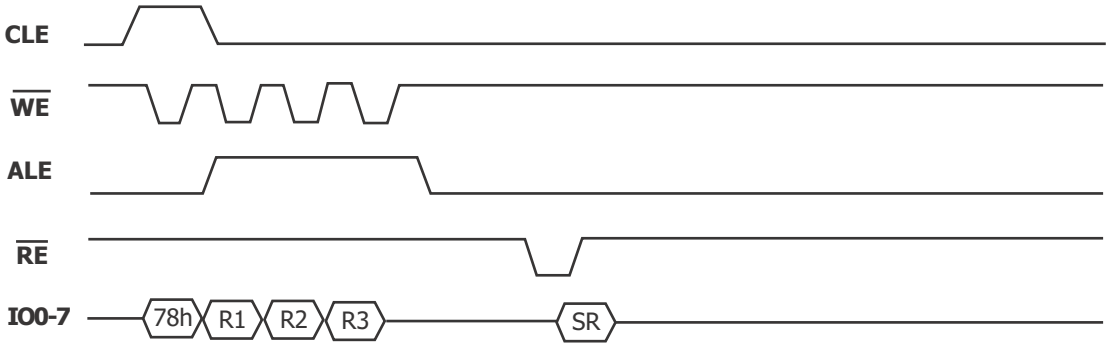


Figure 11: Read Status Enhanced cycle

Read Operation

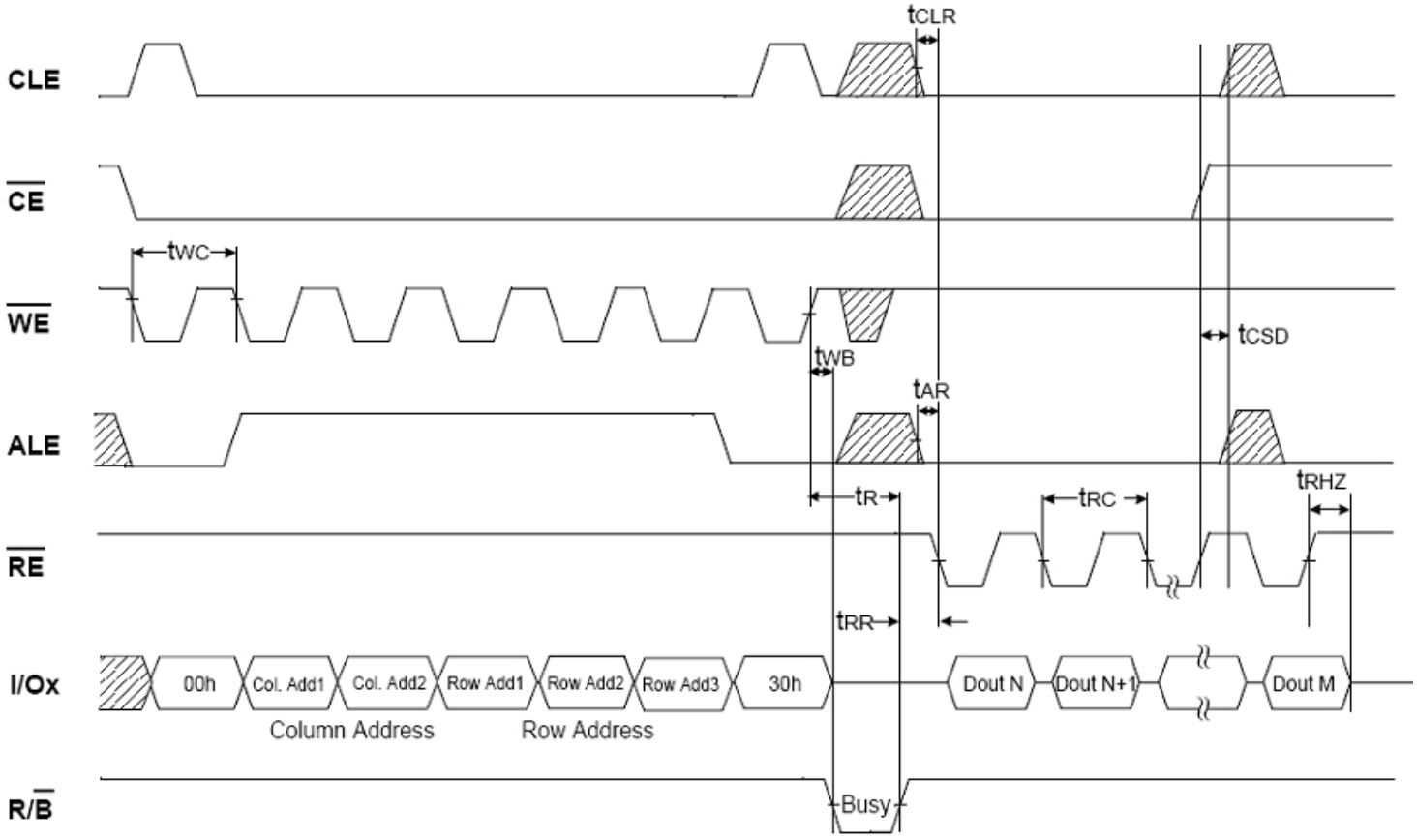


Figure 12: Read Operation (Read One Page)

Read Operation (Intercepted by $\overline{CE}$)

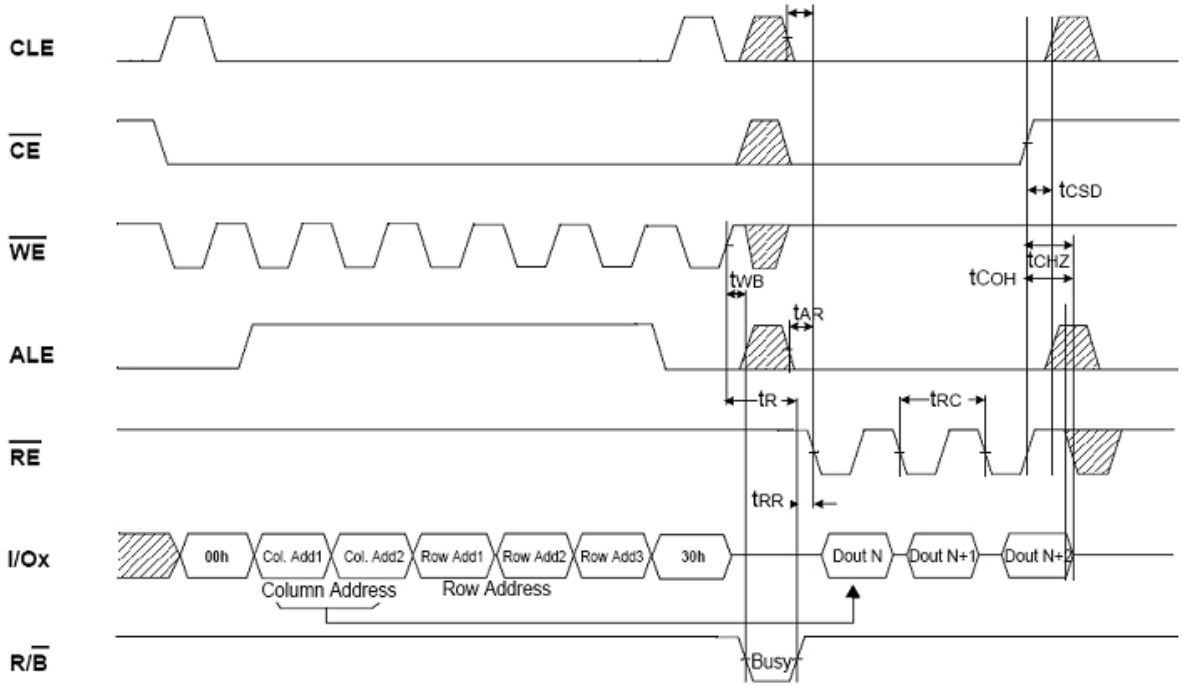


Figure 13: Read Operation intercepted by CE#

Random Data Output In a Page

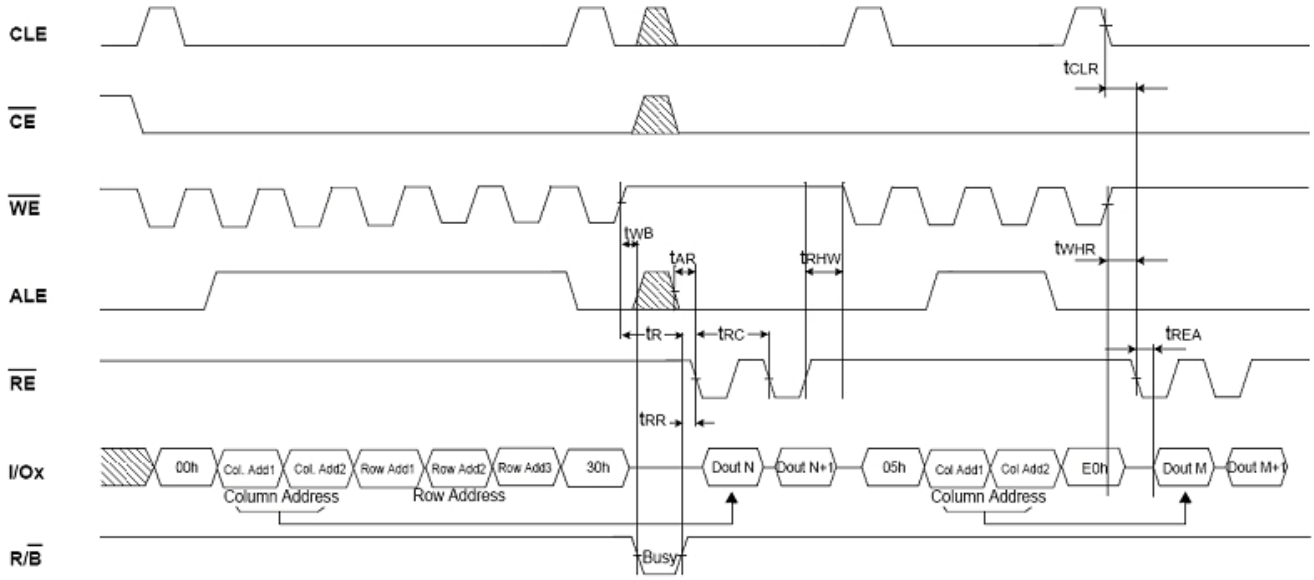
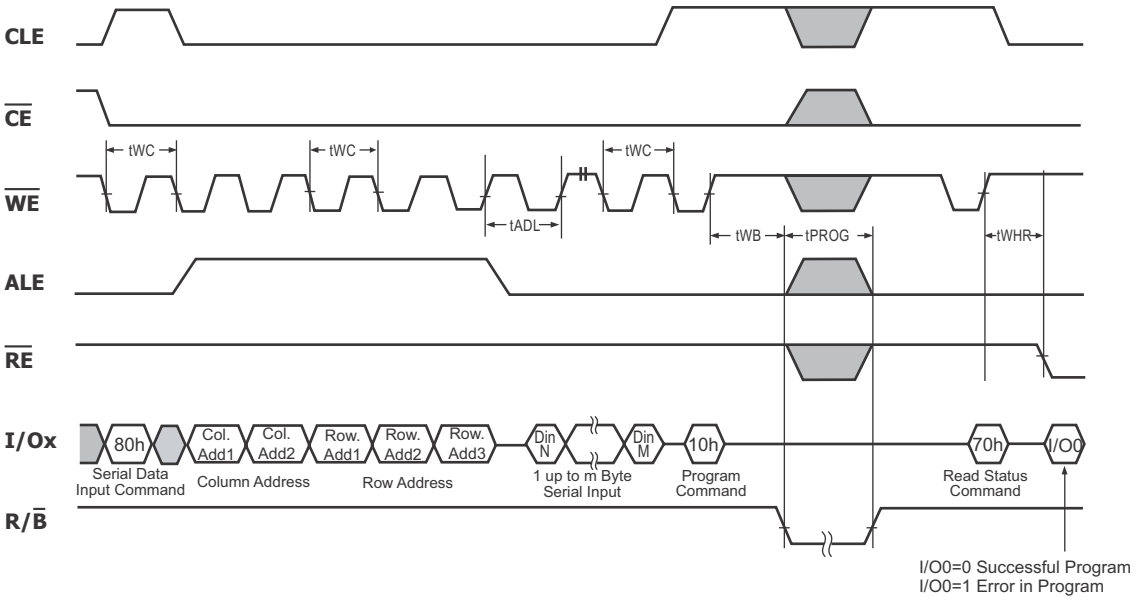


Figure 14: Random Data Output

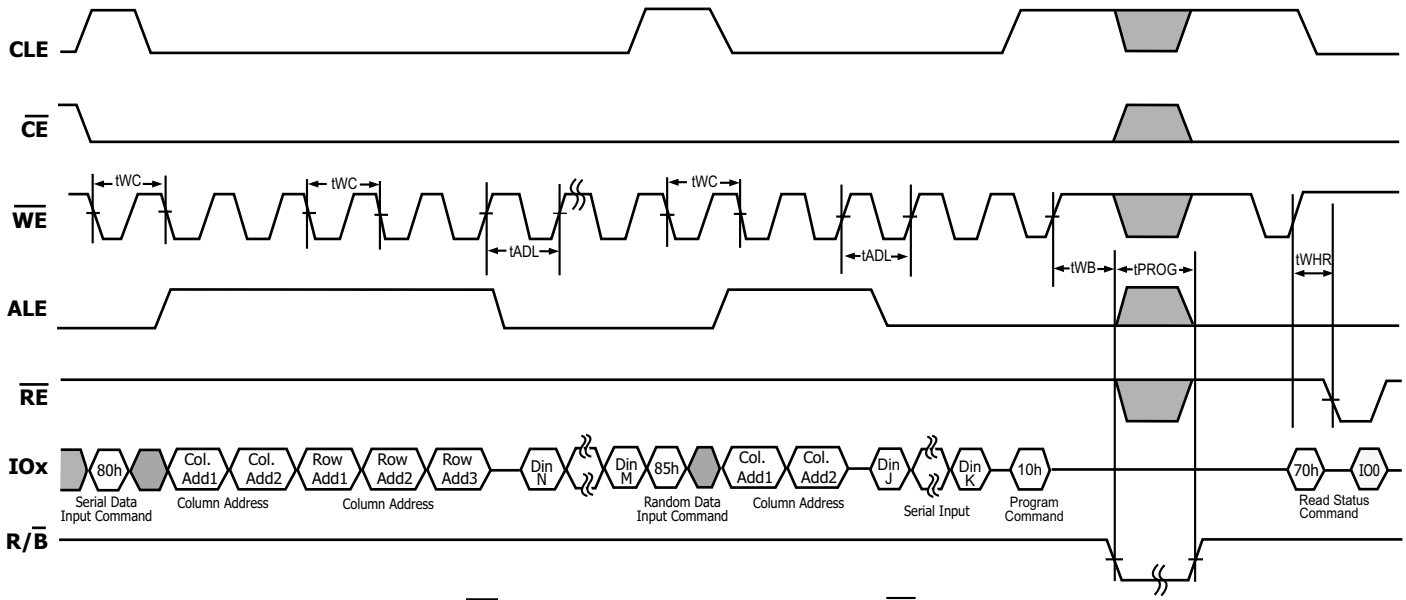
Page Program Operation



NOTES: tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

Figure 15: Page Program Operation

Page Program Operation with Random Data Input



NOTES : 1. tADL is the time from the $\overline{WE}$ risinig edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.
2. For EDC operation. only one time random data input is possible at same address.

Figure 16: Random Data In

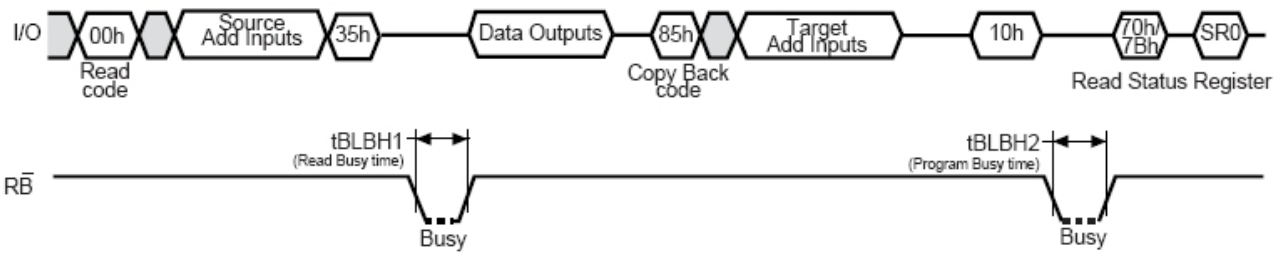


Figure 17: Copy back read with optional data readout

Copy- Back Program Operation With Random Data Input

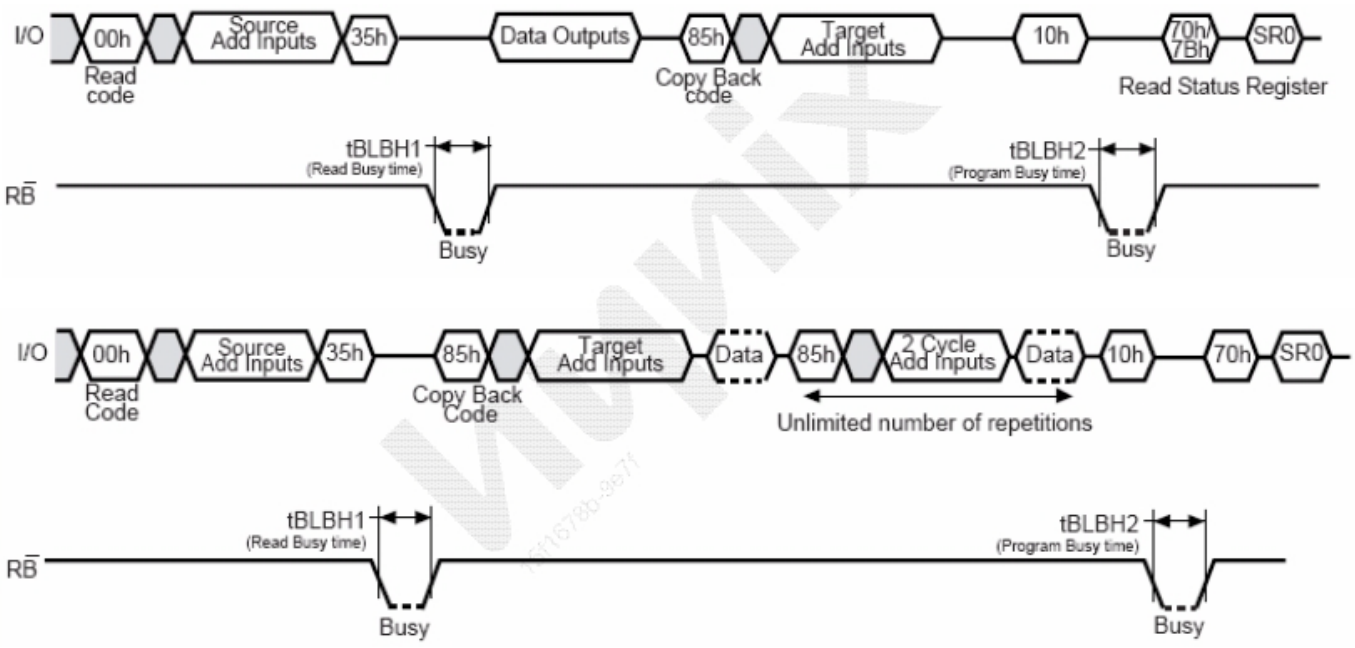


Figure 18: Copy Back Program with Random Data Input

Block Erase Operation

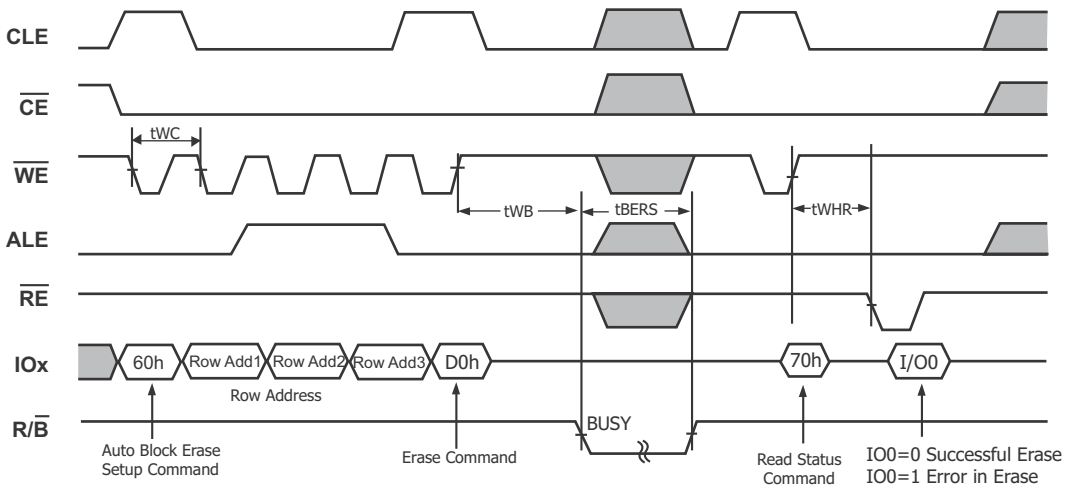
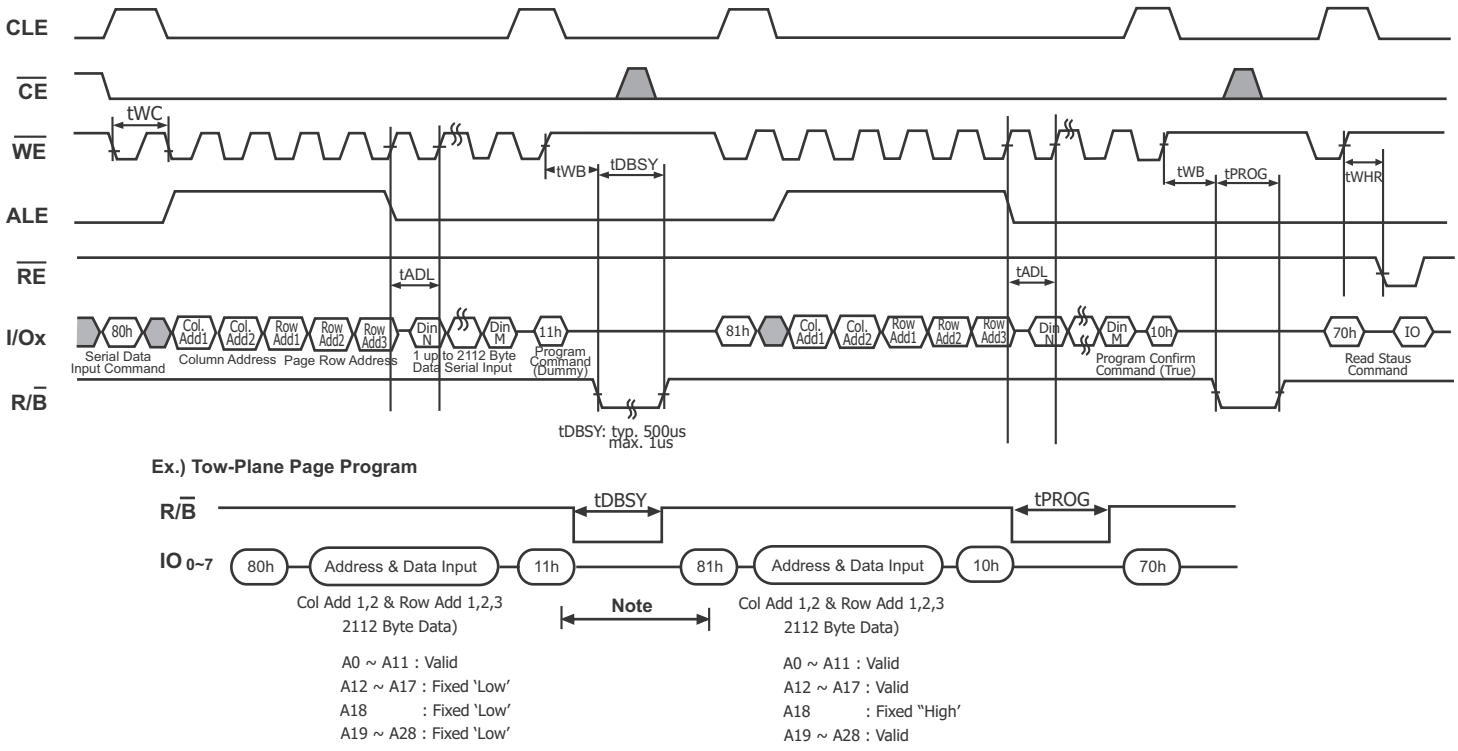


Figure 19: Block Erase Operation (Erase One Block)

Two-Plane Page Program Operation



Ex.) Tow-Plane Page Program

Col Add 1,2 & Row Add 1,2,3
2112 Byte Data)

A0 ~ A11 : Valid
A12 ~ A17 : Fixed 'Low'
A18 : Fixed 'Low'
A19 ~ A28 : Fixed 'Low'

Col Add 1,2 & Row Add 1,2,3
2112 Byte Data)

A0 ~ A11 : Valid
A12 ~ A17 : Valid
A18 : Fixed "High'
A19 ~ A28 : Valid

Note : Any command between 11h and 81h is prohibited except 70h and FFh

NOTES:

1) the figure refers to x8 case. Please refer to **Section 1.4** for address remapping rules for the x16 case
2) **any command between 11h and 81h is prohibited except 70h, 78h and FFh**

Figure 20: Multiple plane page program (traditional protocol)

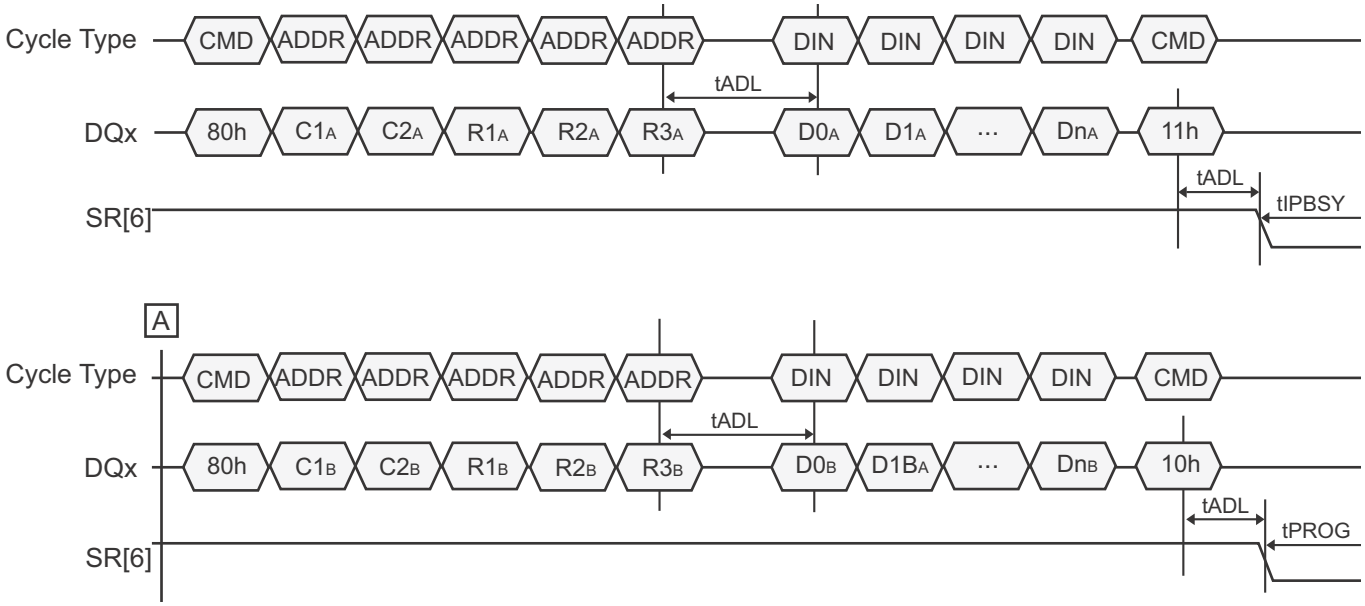
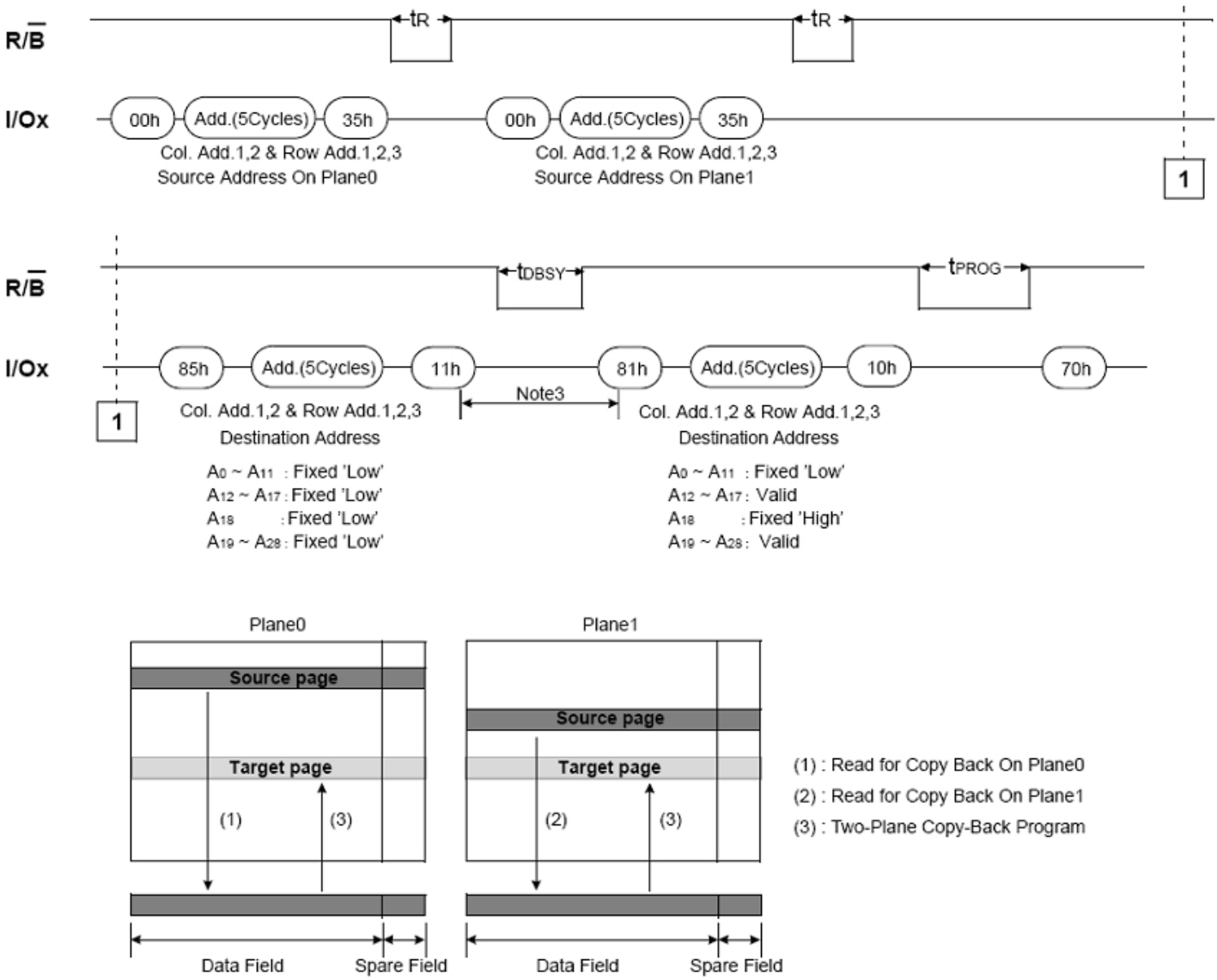


Figure 21 : Multiple plane page program (ONFI 1.0 protocol)

NOTES :
$C1_A$-$C2_A$ Column address for page A. $C1_A$ is the least significant byte.
$R1_A$-$R3_A$ Row address for page A. $R1_A$ is the least significant byte.
$D0_A$-Dn_A Data to program for page A.
$C1_B$-$C2_B$ Column address for page B. $C1_B$ is the least significant byte.
$R1_B$-$R3_B$ Row address for page B. $R1_B$ is the least significant byte.
$D0_B$-Dn_B Data to program for page B.

Same restrictions on address of pages A and B, and allowed commands as **Figure 20** apply



Note: 1. Copy-Back Program operation is allowed only within the same memory plane.
2. On the same plane, It's prohibited to operate copy-back program from an odd address page(source page) to an even address page(target page) or from an even address page(source page) to an odd address page(target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.
3. Any command between 11h and 81h is prohibited except 70h and FFh.

Figure 22: Multiple plane copy back program (traditional protocol)

NOTE: the figure refers to x8 case. Please refer to **Section 1.4** for address remapping rules for the x16 case

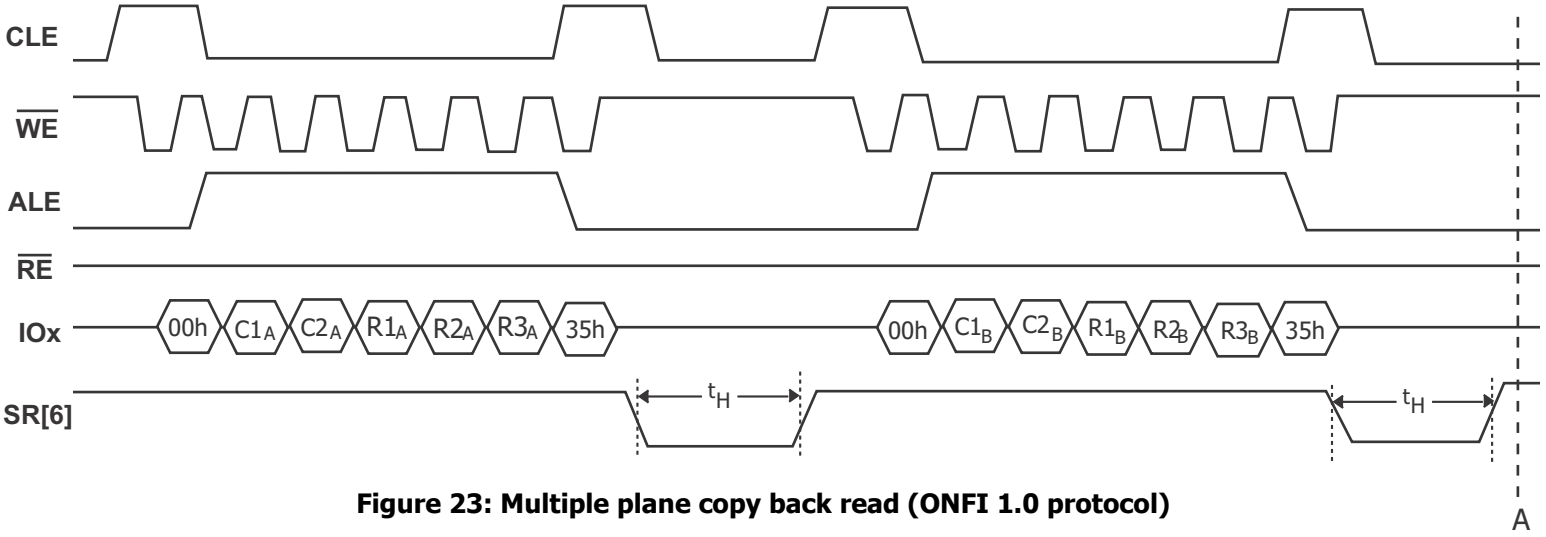


Figure 23: Multiple plane copy back read (ONFI 1.0 protocol)

NOTES:
$C1_A$-$C2_A$ Column address for page A. $C1_A$ is the least significant byte.
$R1_A$-$R3_A$ Row address for page A. $R1_A$ is the least significant byte.
$C1_B$-$C2_B$ Column address for page B. $C1_B$ is the least significant byte.
$R1_B$-$R3_B$ Row address for page B. $R1_B$ is the least significant byte.

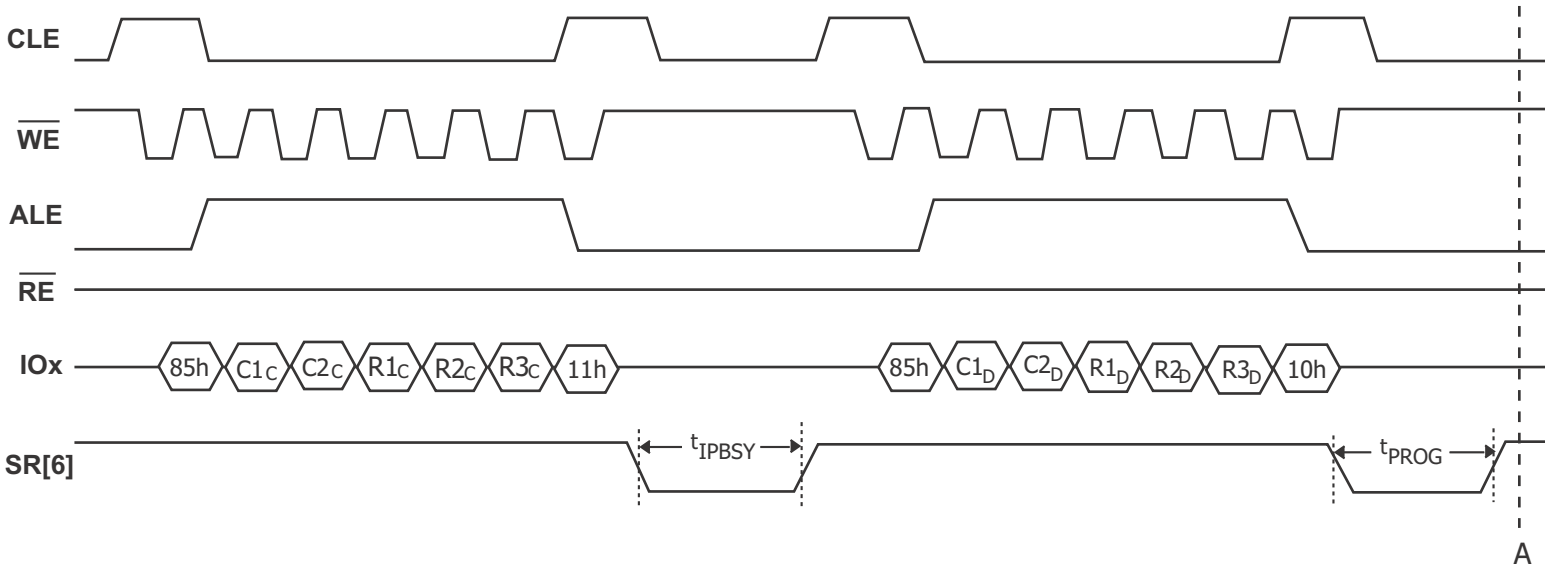
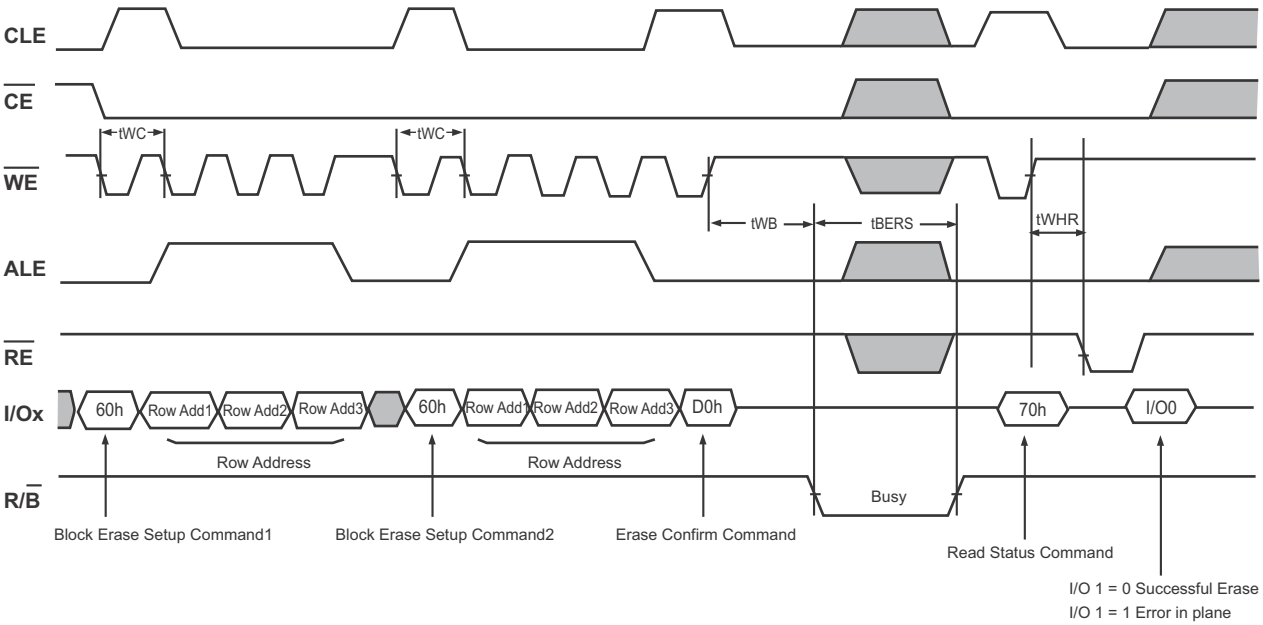


Figure 24: Multiple plane copy back program (ONFI 1.0 protocol)

NOTES:
$C1_C$-$C2_C$ Column address for page C. $C1_A$ is the least significant byte.
$R1_C$-$R3_C$ Row address for page C. $R1_A$ is the least significant byte.
$D0_C$-Dn_C Data to program for page C.
$C1_D$-$C2_D$ Column address for page D. $C1_B$ is the least significant byte.
$R1_D$-$R3_D$ Row address for page D. $R1_B$ is the least significant byte.
$D0_D$-Dn_D Data to program for page D.

Same restrictions on address of pages C and D, and allowed commands as **Figure 21** apply

Two-Plane Block Erase Operation



Ex.) Address Restriction for Two-Plane Block Erase Operation

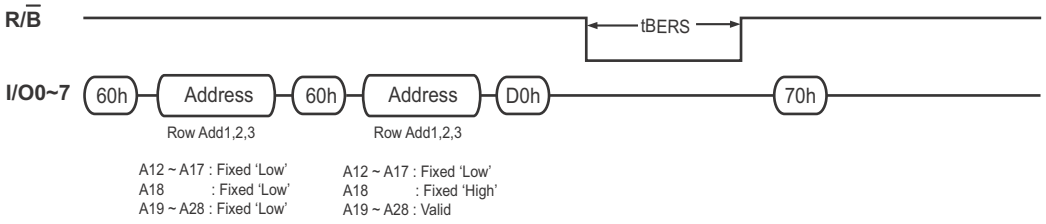


Figure 25: Multiple plane block erase (traditional protocol)

NOTE: the figure refers to x8 case. Please refer to **Section 1.4** for address remapping rules for the x16 case

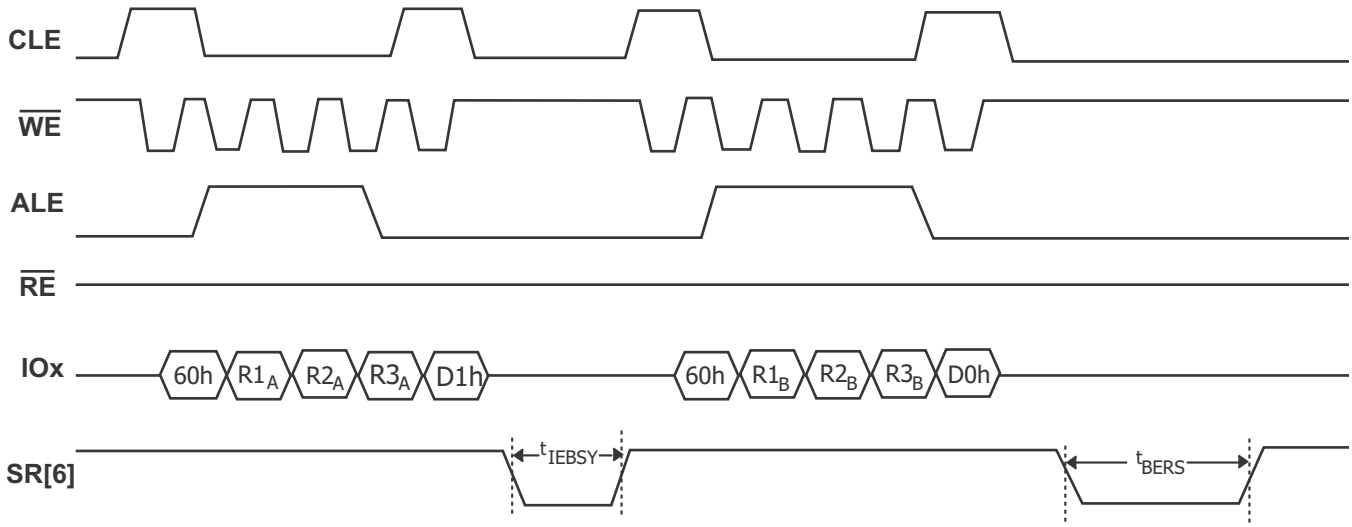


Figure 26: Multiple plane block erase (ONFI 1.0 protocol)

NOTES:
$R1_A$-$R3_A$ Row address for block on plane 0. $R1_A$ is the least significant byte.
$R1_B$-$R3_B$ Row address for block on plane 1. $R1_B$ is the least significant byte.

Same restrictions on address of blocks on plane 0(A) and 1(B) and allowed commands as **Figure 24** apply

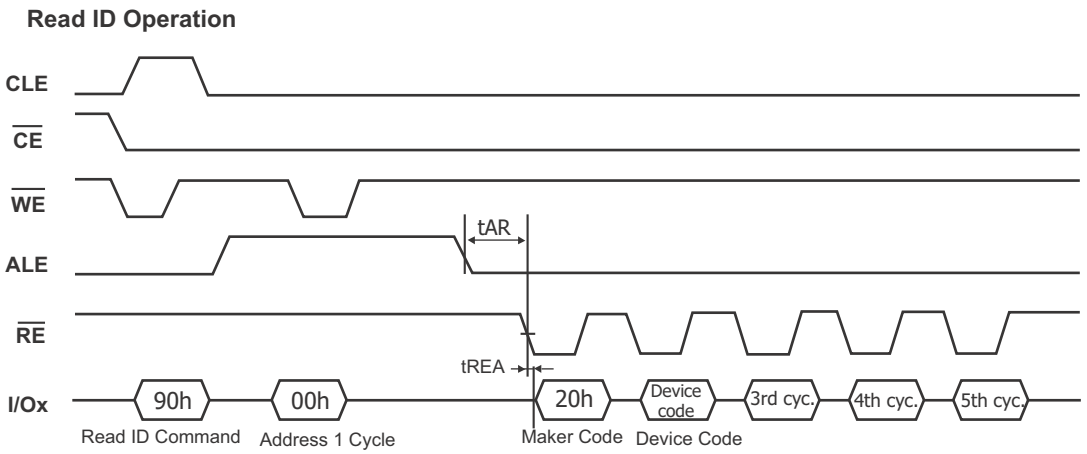


Figure 27: ID Read

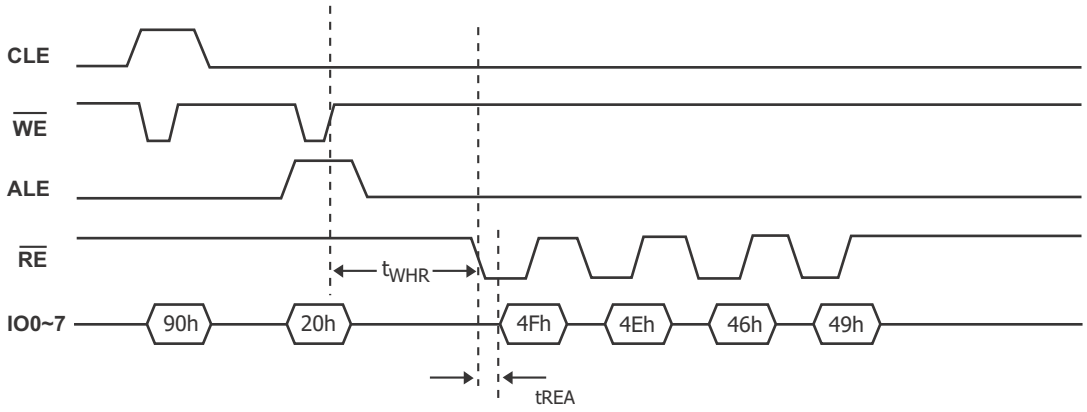


Figure 28: ONFI signature timing diagram

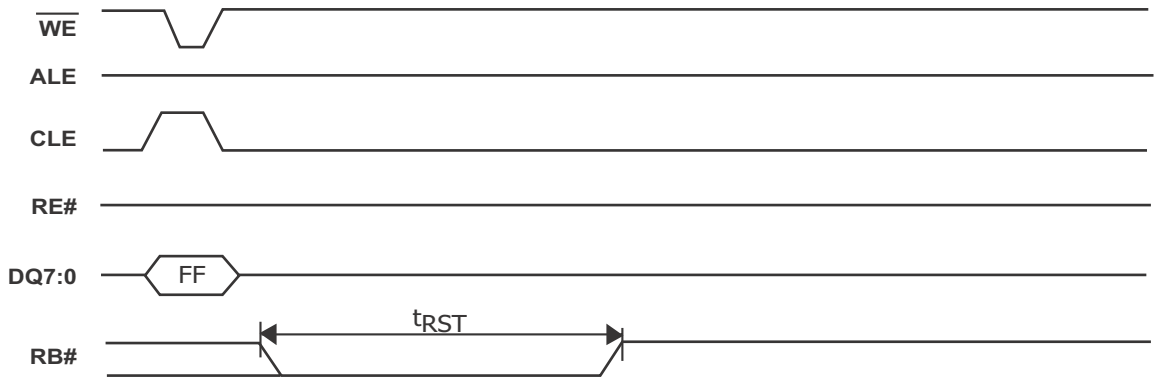


Figure 29: Reset operation timing

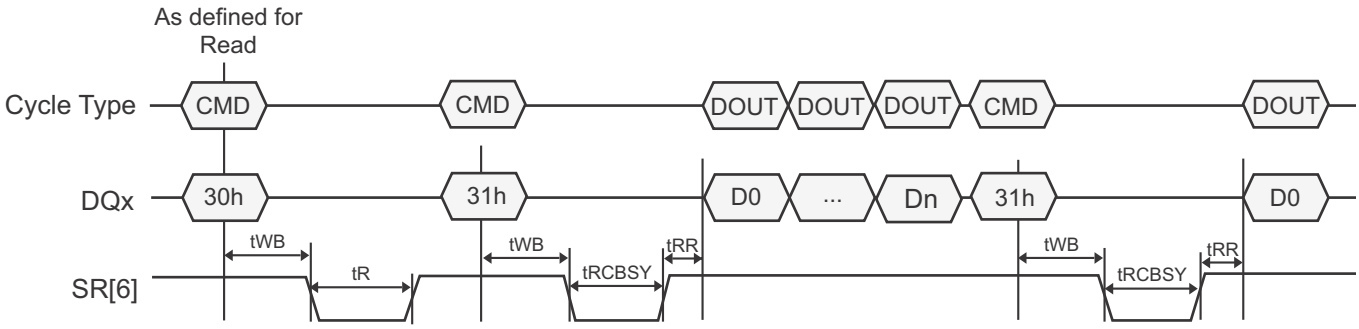


Figure 30: "sequential" read cache timings, start (and continuation) of cache operation

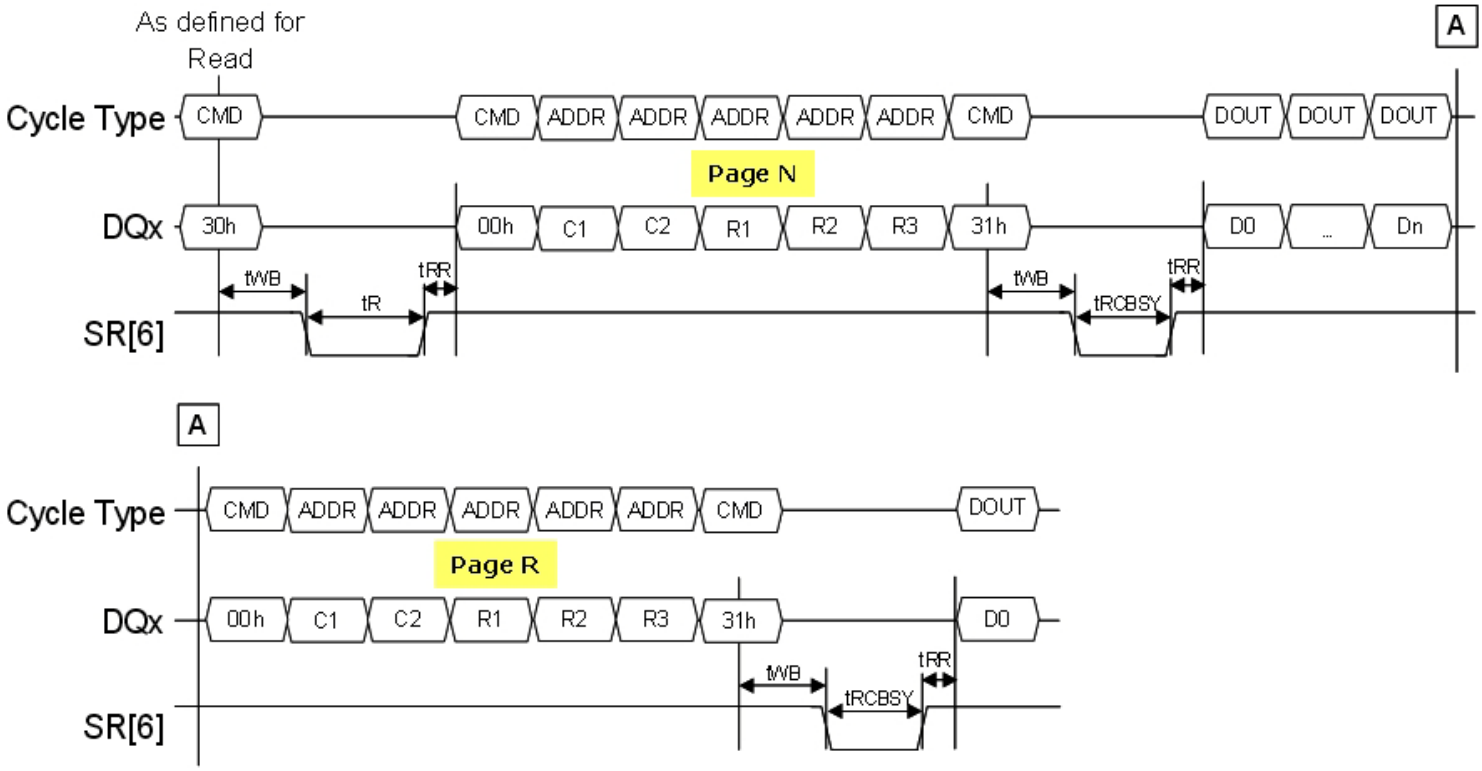


Figure 31: "random" read cache timings, start (and continuation) of cache operation

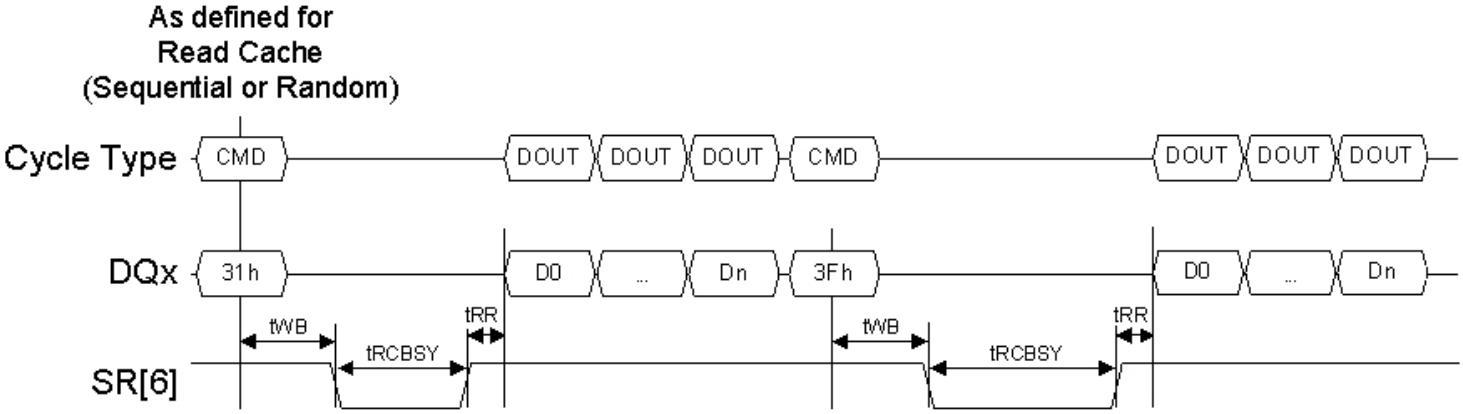


Figure 32 : read cache timings, end of cache operation

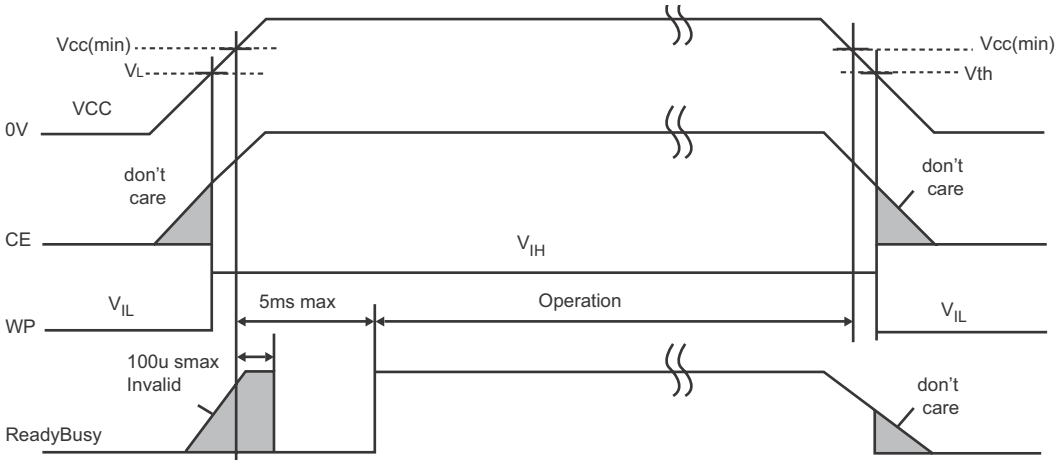
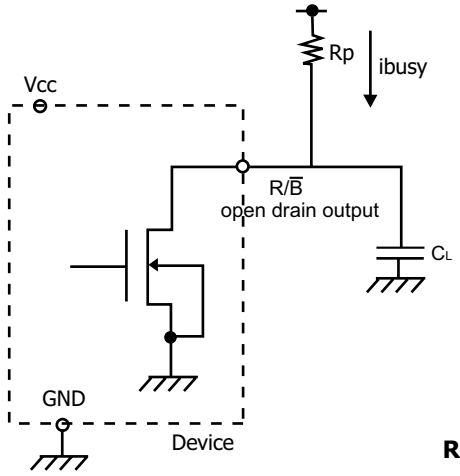
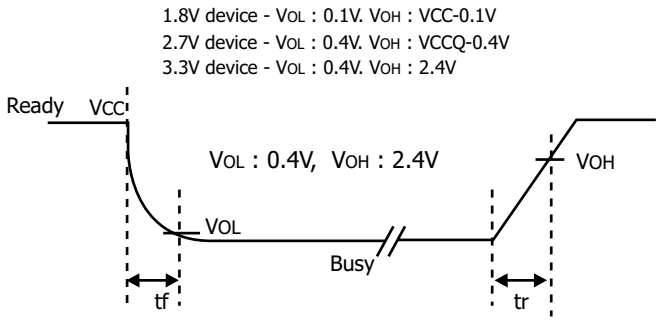


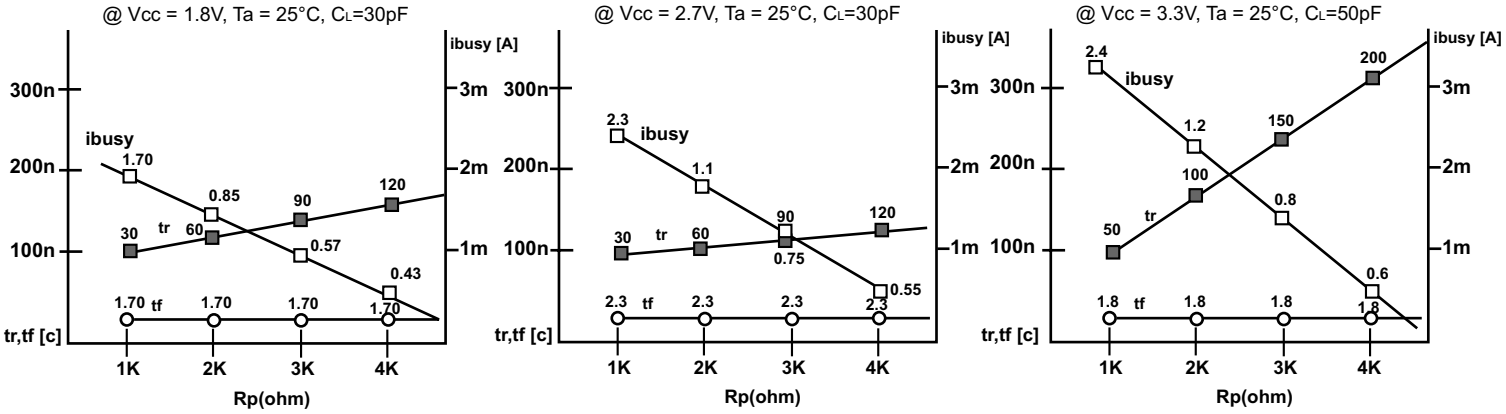
Figure 33: Power on and Data Protection timings

NOTE: V_{TH} = 1.2 Volt for 1.8 Volt Supply devices: 1.8 Volt for 3.0 Volt Supply devices.





Rp vs tr, tf & Rp vs ibusy



Rp value guidence

$$Rp\ (min.\ 1.8V\ part) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{1.85V}{3mA + \sum I_L}$$ 1.8V version

$$Rp\ (min.\ 2.7V\ part) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{2.5V}{3mA + \sum I_L}$$

$$Rp\ (min.\ 3.3V\ part) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$ 3.0V version

where IL is the sum of the input currnts of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 34: Ready/Busy Pin electrical application

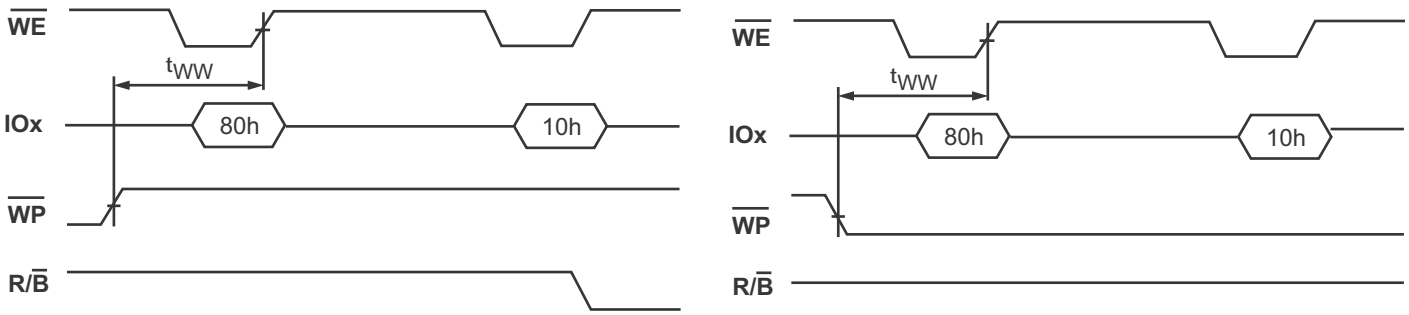


Figure 35: program Enabling / Disabling through WP# handling

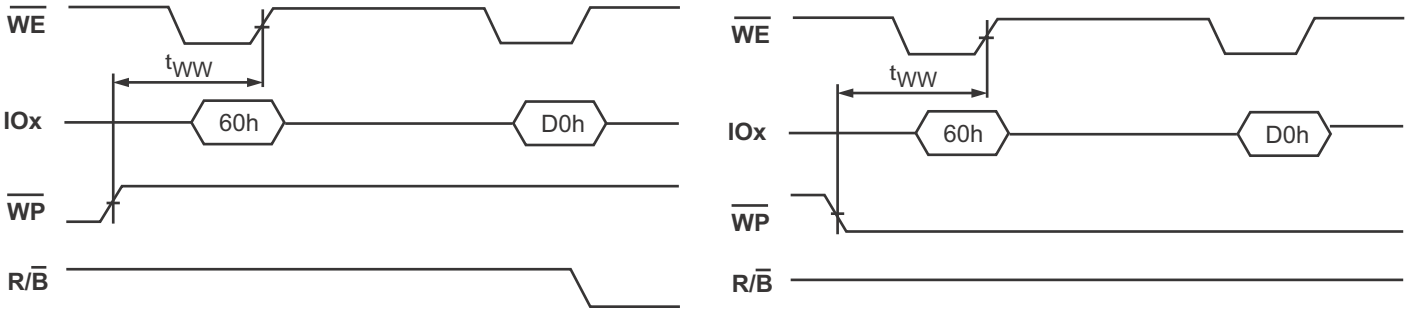


Figure 36: Erase Enabling / Disabling through WP# handling

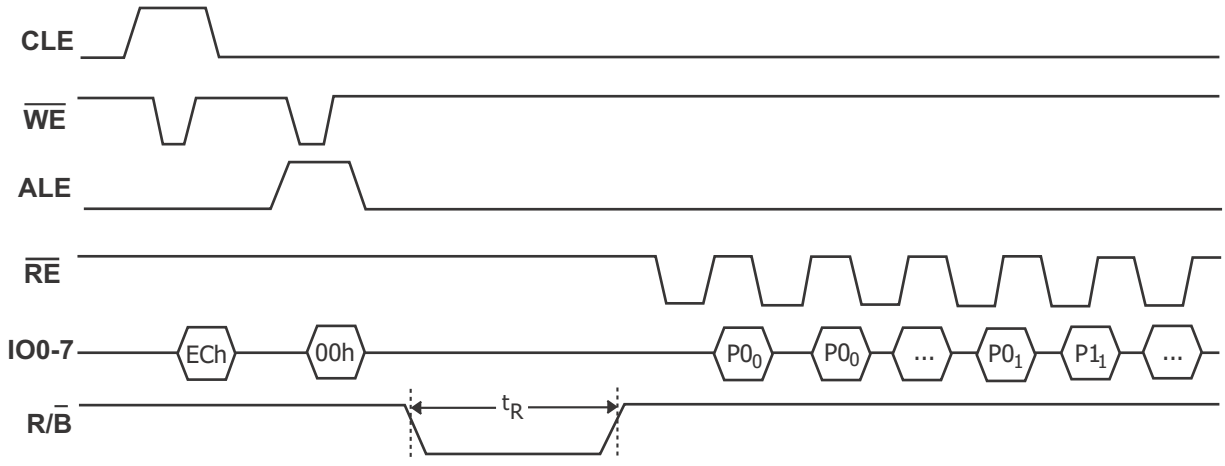


Figure 37: Read Parameter Page timings

Figure 38: Read Status Timings

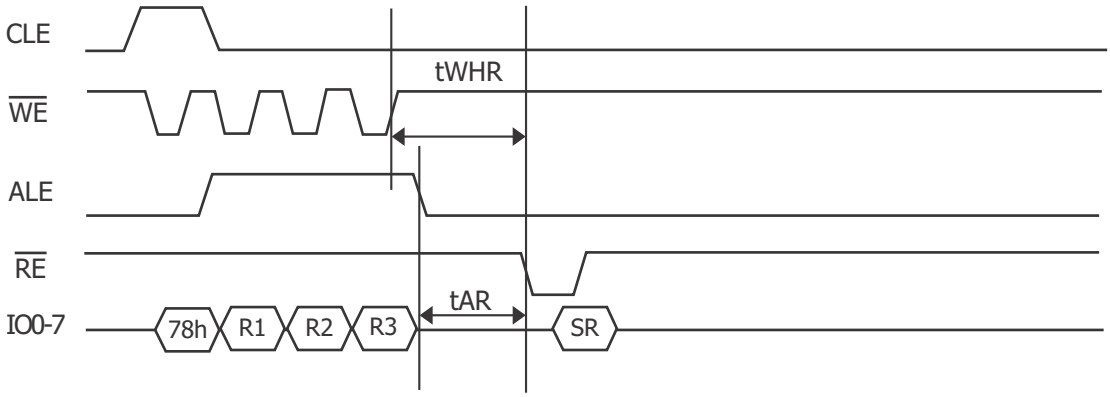


Figure 39: Read Status Enhanced timings

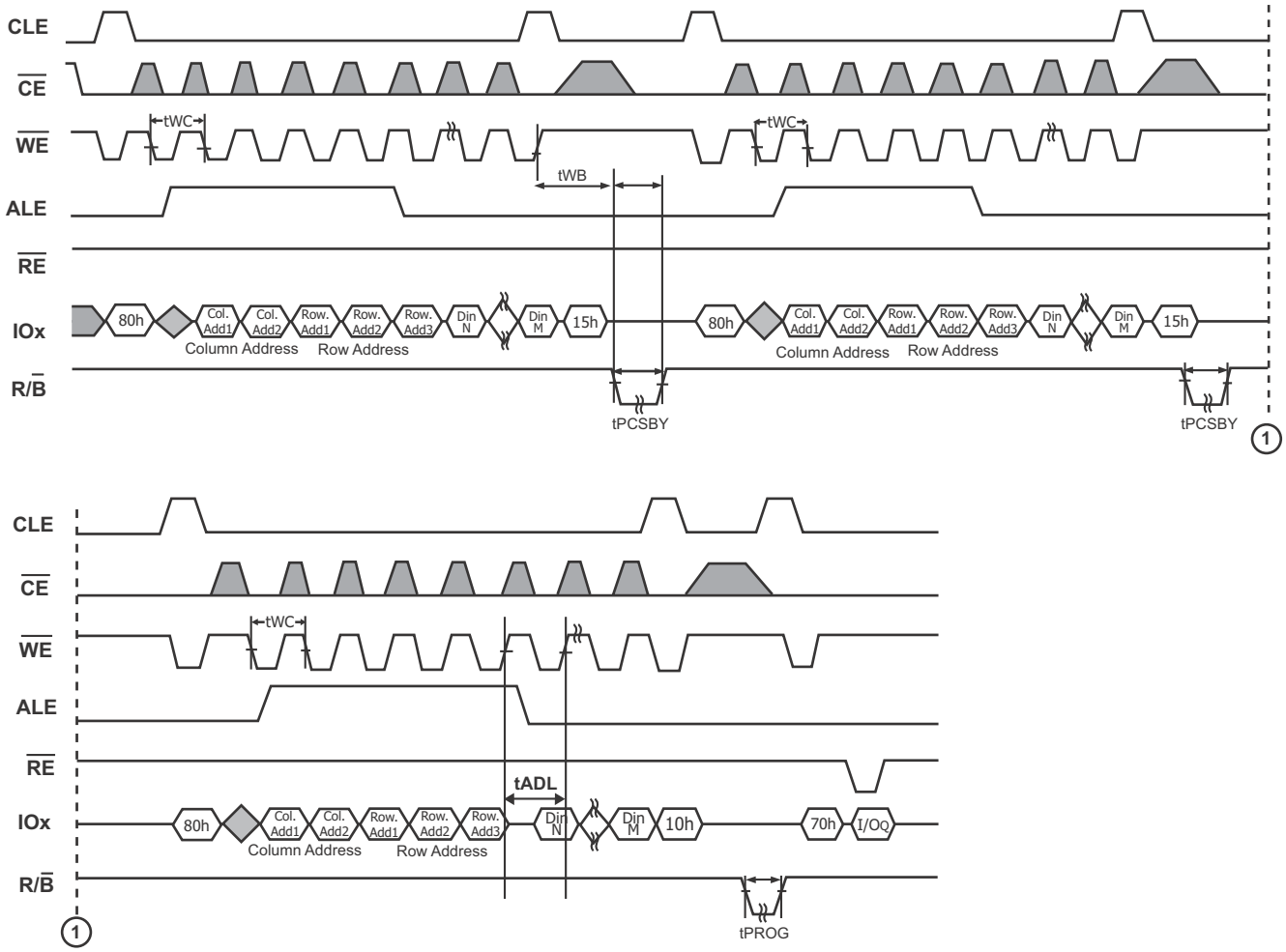


Figure 40: Cache program

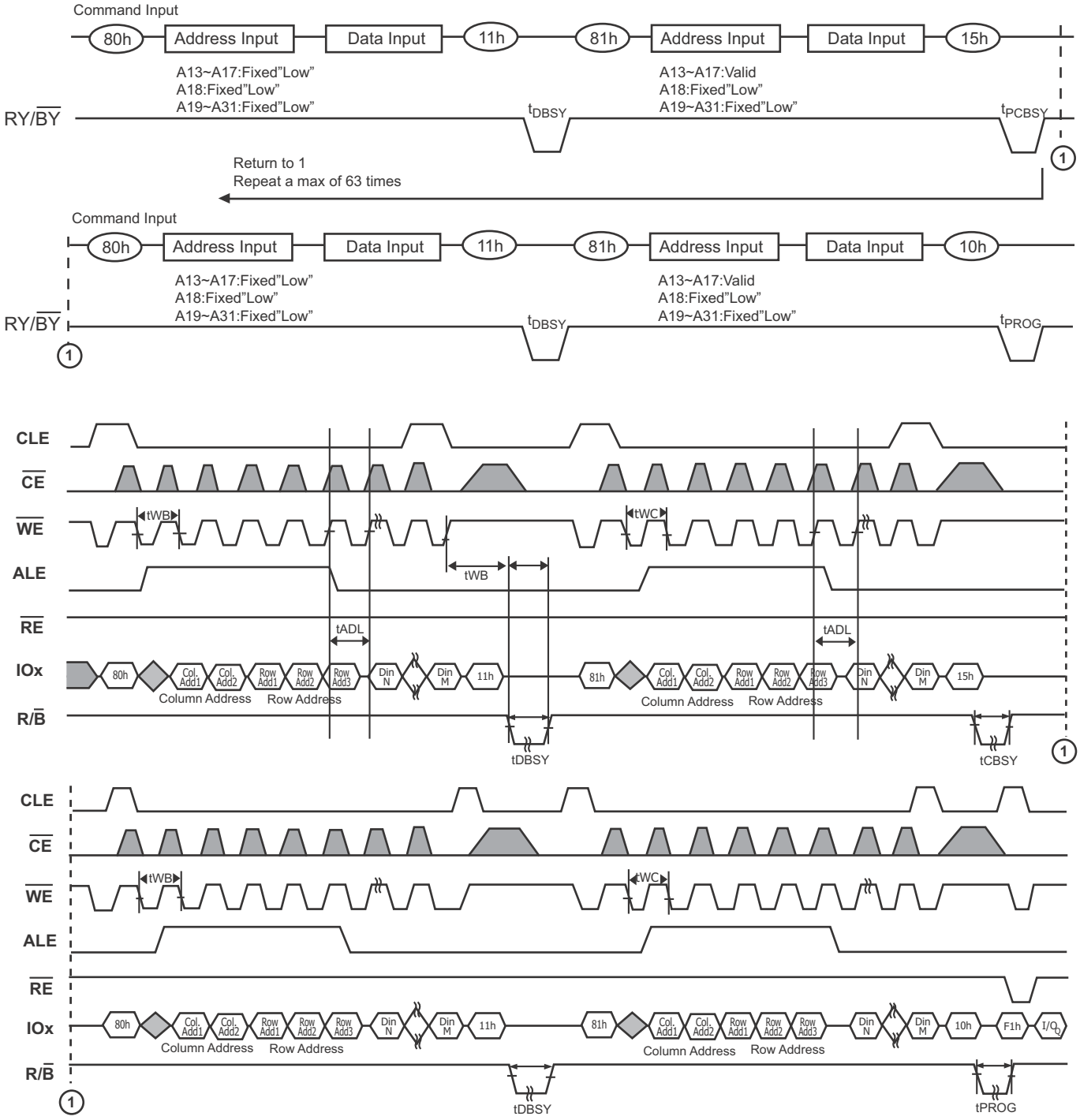


Figure 41: multi-plane cache program (traditional protocol)

NOTE:
1) the figure refers to x8 case. Please refer to **Section 1.4** for address remapping rules for the x16 case
2) Read Status register (70h) is used in the figure. Read Status Enhanced (78h) can be also used

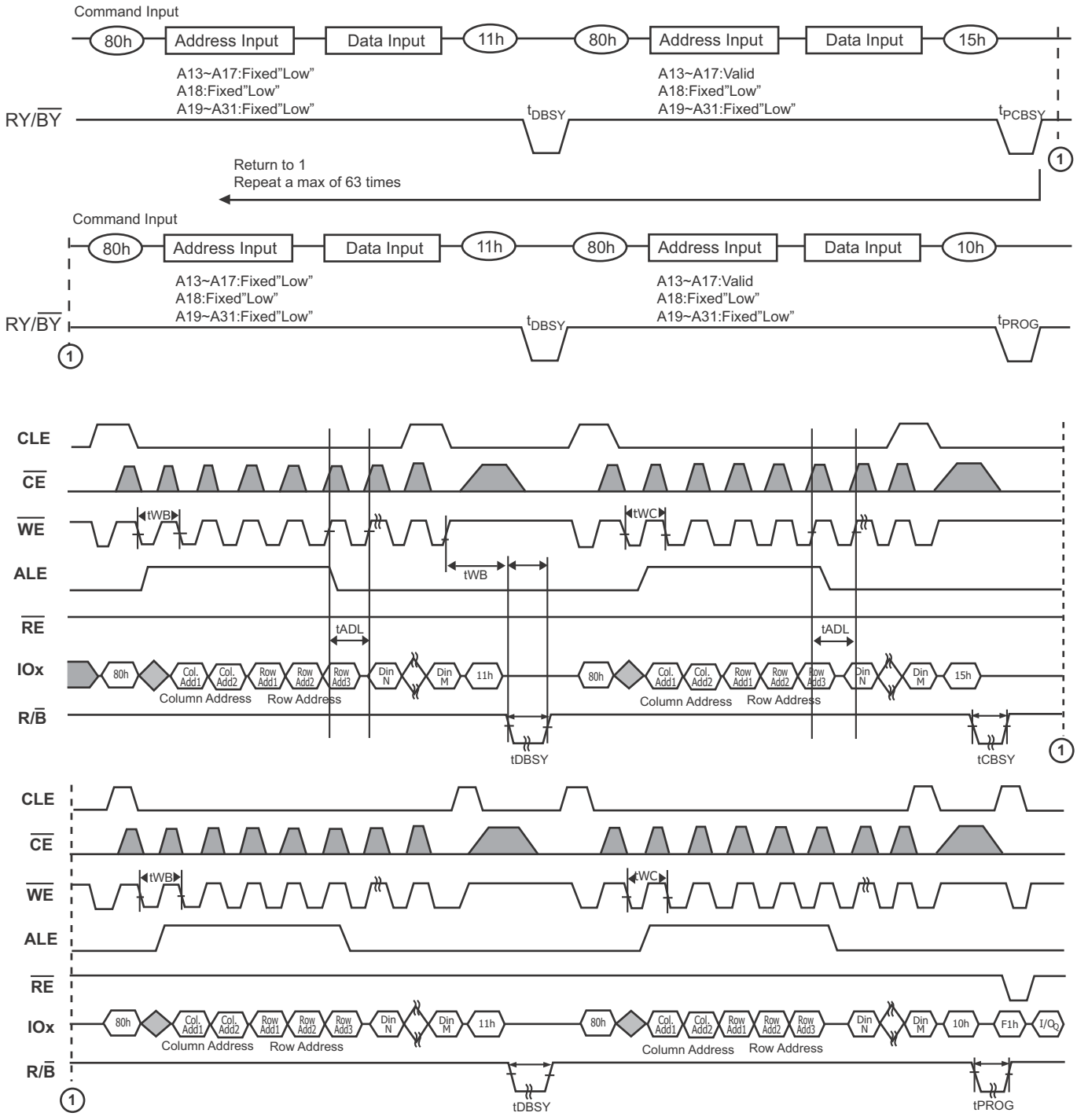


Figure 42: multi-plane cache program (ONFI protocol)

NOTE:

3) the figure refers to x8 case. Please refer to **Section 1.4** for address remapping rules for the x16 case

4) Read Status register (70h) is used in the figure. Read Status Enhanced (78h) can be also used

7. Package Mechanical

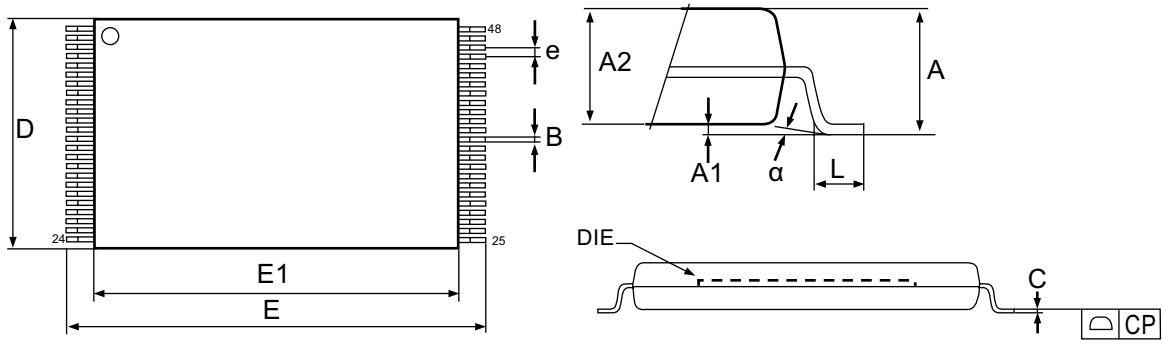


Figure 43. 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Outline

Symbol	Millimeters		
	Typ	Min	Max
A			1.200
A1		0.050	0.150
A2		0.950	1.050
B		0.170	0.250
C		0.100	0.200
CP			0.080
D	12.000	11.910	12.120
E	20.000	19.900	20.100
E1	18.400	18.300	18.500
e	0.500	-	-
L		0.500	0.680
alpha		0	5

Table 29: 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Mechanical Data

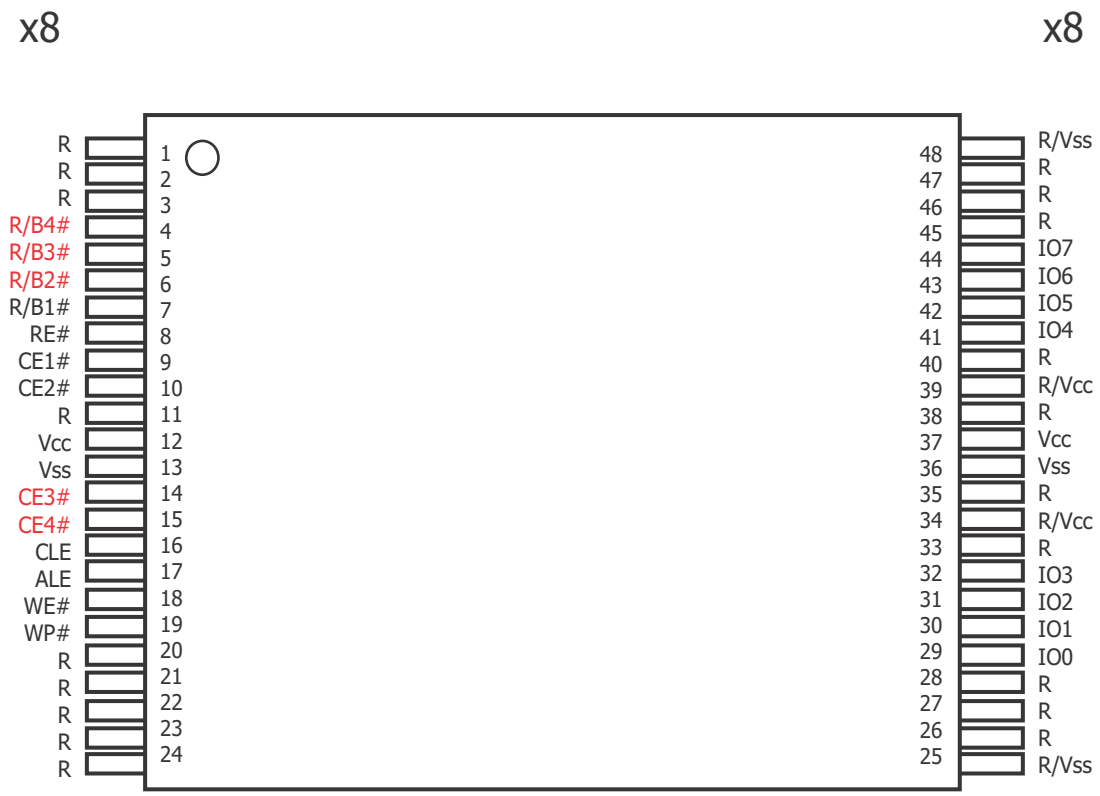


Figure 44: ONFI 1.0 TSOP and WSOP connection (x8 multi CE# / multi RyBYconfiguration) (*)

NOTES:
1) TSOP48 "ONFI" is supported only for x8 I/O configuration
2) Pins marked in **Red** are used in case a quad stack die is implemented with separated RyBy and CE# pins. If this is not the case, CE# for the stack is pin 9, and RyBy# for the stack is pin 7, and pins marked in Red Bold are Reserved ("R")
3) **this package is supported only if die is mounted OVER package frame**

7.1 Power consumptions and pin capacitance for allowed stacking configurations

Table 28 reports the power consumptions related to the single chip case. When multiple dice are stacked in the same package the power consumption of the stack will increase according to the nr of chips of it. As an example, the standby current is the sum of the standby currents of all the chips, while the active power consumption depends on the nr of chips concurrently executing different operations.

Similarly, **Table 26** reports the pin capacitance for the single chip case. When multiple dice are stacked in the same package the pin/ball capacitance for the single input and the single input/output of the combo package must be calculated based on the number of chips sharing that input or that pin/ball.

8 Application notes and comments

8.1 System Interface using CE# don't care

To simplify system interface, CE# may be un-asserted during data loading or sequential data-reading as shown below. By operating in this way, it is possible to connect NAND Flash to a microprocessor.
Contrary to standard Nand, CE# don't care devices do not allow sequential read function.

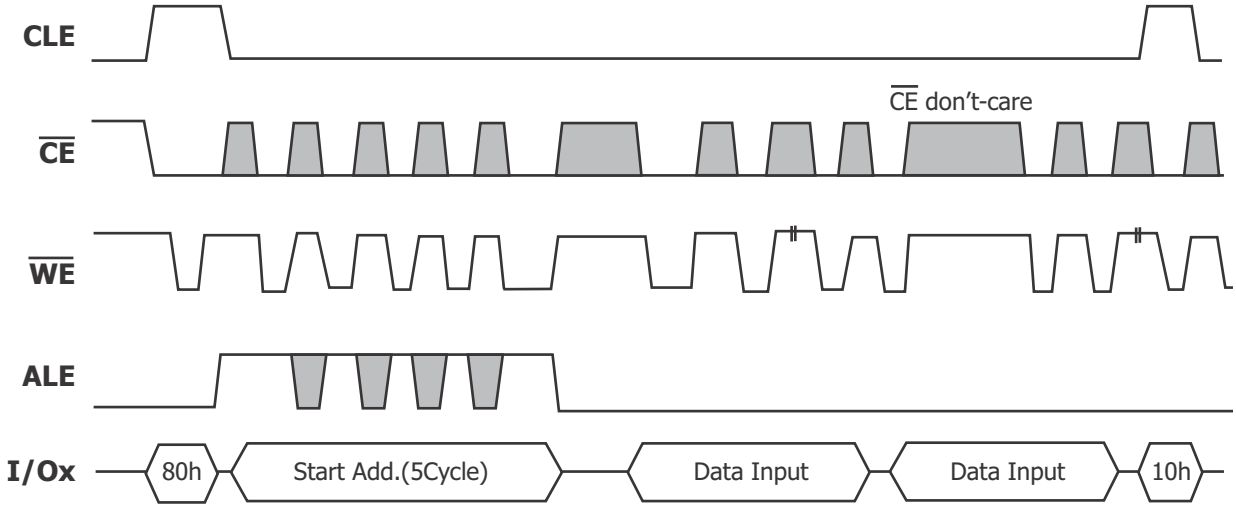


Figure 45: Program Operation with CE# don't-care.

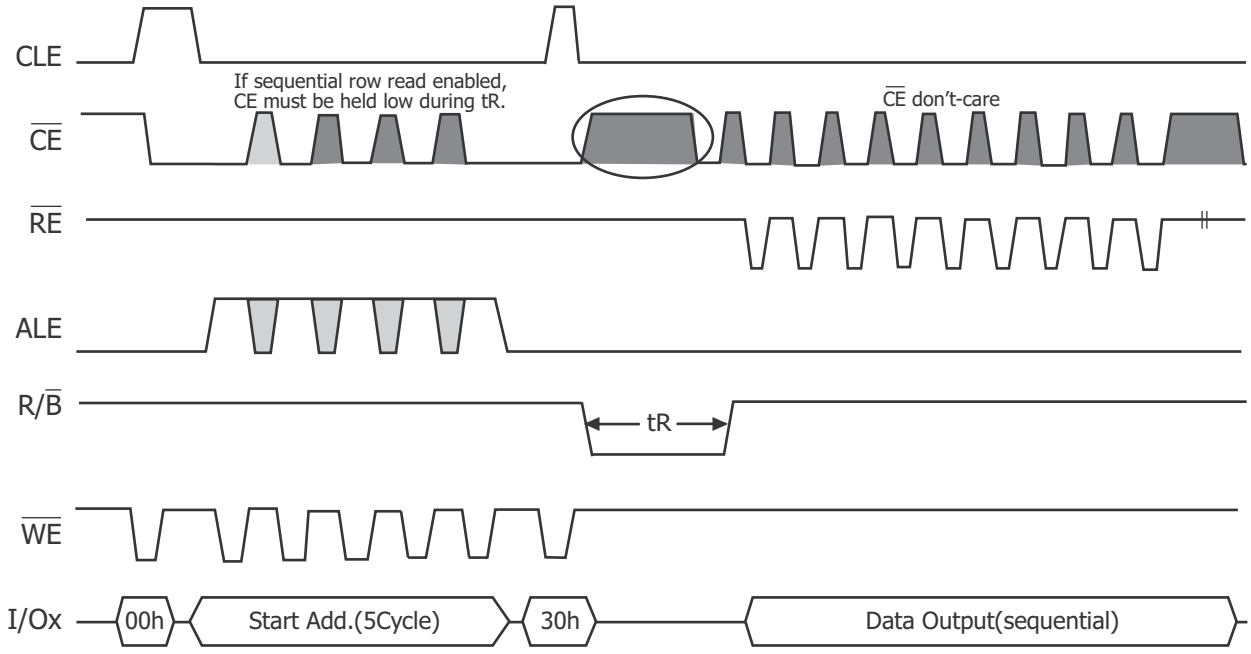


Figure 46: Read Operation with CE# don't-care.

8.2 System Bad Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case each bad block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will return "fail" after Read Status Register.
The failure of a page program operation does not affect the data in other pages in the same block, thus the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.
Refer to **Table 30** and **Figure 47** for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC

Table 30: Block Failure

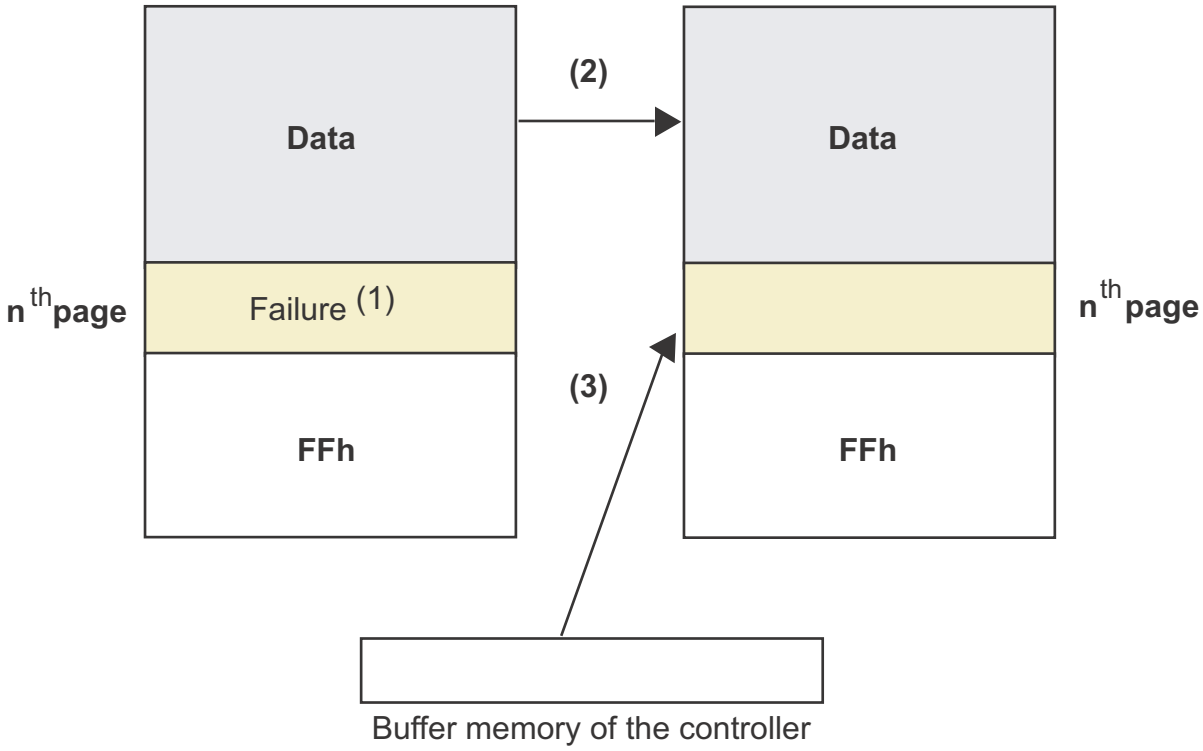


Figure 47 : Bad Block Replacement

NOTE:
1. An error occurs on N^{th} page of the Block A during program or erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. N^{th} page of block A which is in controller buffer memory is copied into N^{th} page of Block B
4. Bad block table should be updated to prevent from erasing or programming Block A

8.3 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the 1st or 2nd th page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 48. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

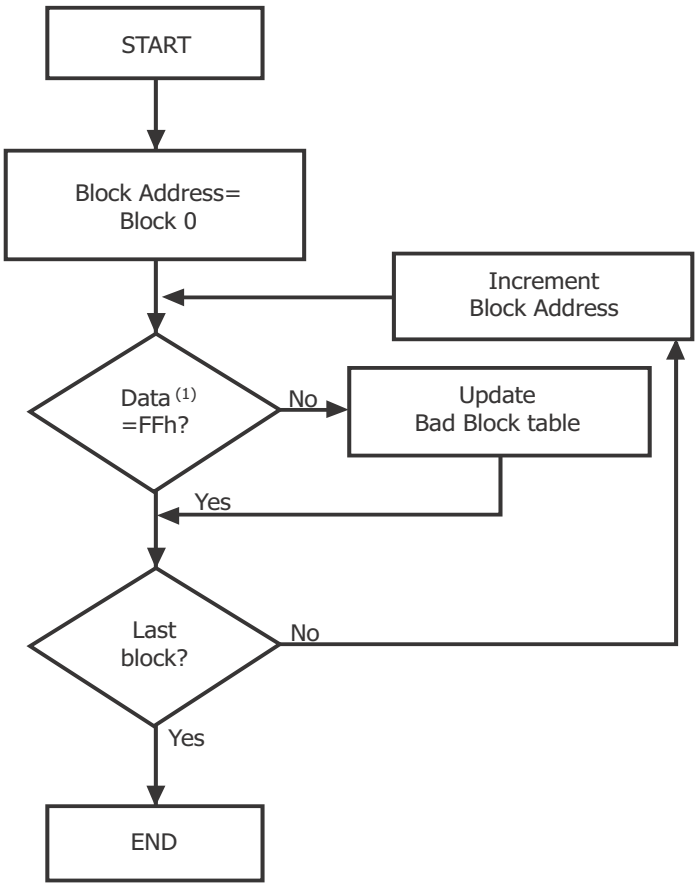


Figure 48: Bad Block Management Flowchart

NOTE :
1. Check FFh at 1st Byte in the spare area of the 1st or 2nd th page (if the 1st page is Bad).