SBC8600B 120901

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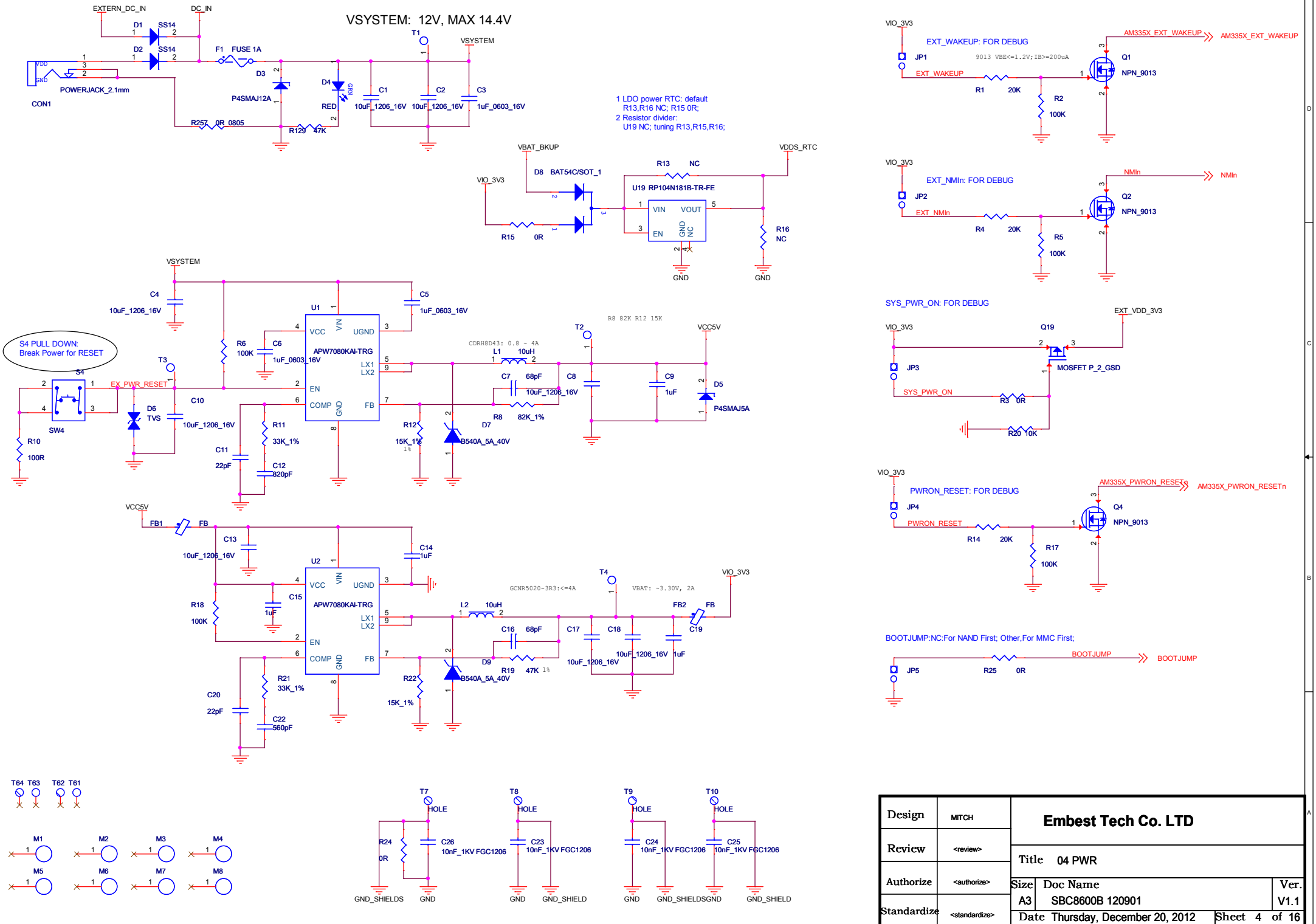

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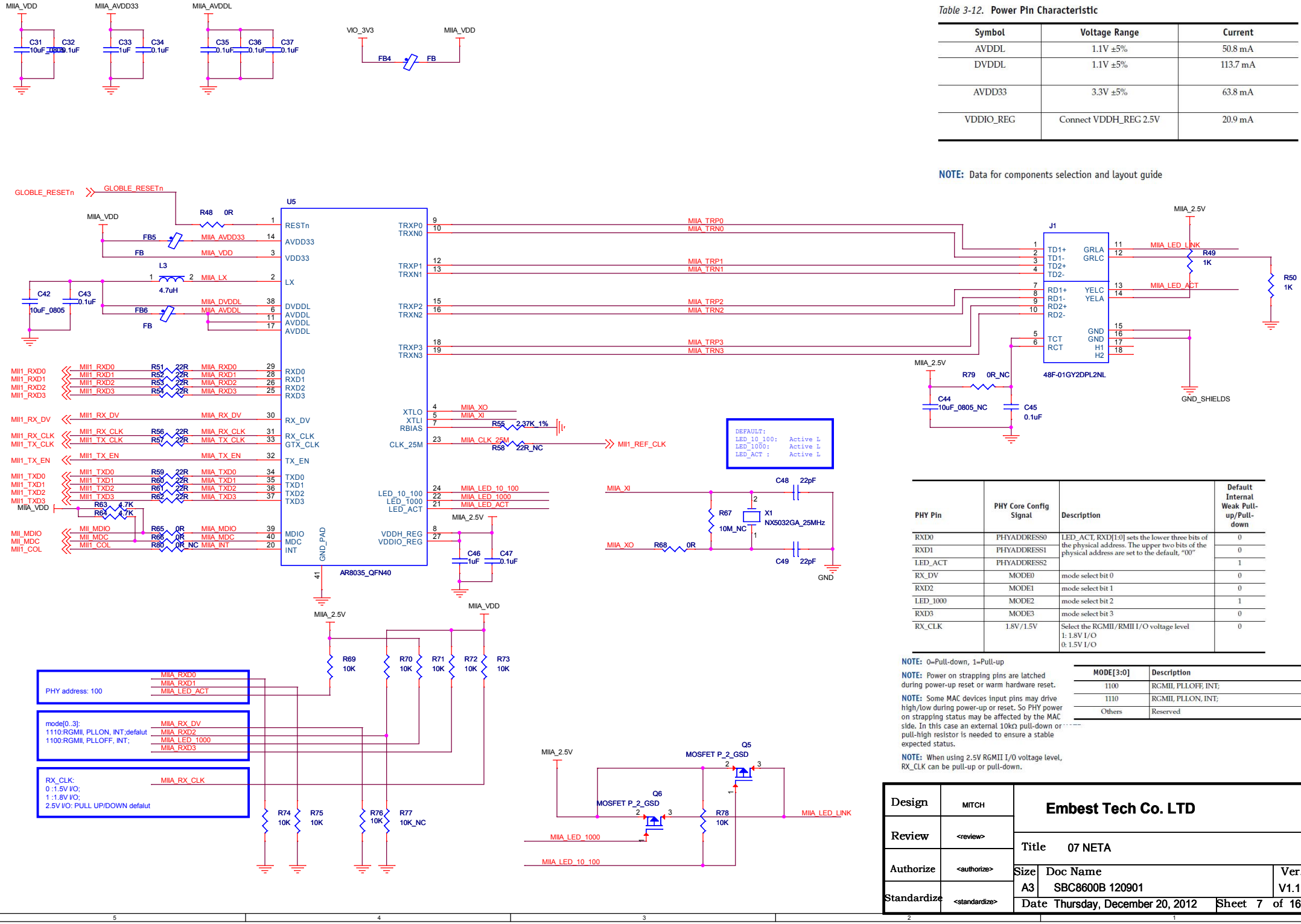
Standardize	<standardize>	Date Thursday, December 20, 2012	Sheet 4 of 16



3.6 Power Pin Consumption

Table 3-12. **Power Pin Characteristic**

Symbol	Voltage Range	Current
AVDDL	1.1V ±5%	50.8 mA
DVDDL	1.1V ±5%	113.7 mA
AVDD33	3.3V ±5%	63.8 mA
VDDIO_REG	Connect VDDH_REG 2.5V	20.9 mA

NOTE: Data for components selection and layout guide

PHY Pin	PHY Core Config Signal	Description	Default Internal Weak Pull-up/Pull-down
RXD0	PHYADDRESS0	LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00"	0
RXD1	PHYADDRESS1		0
LED_ACT	PHYADDRESS2		1
RX_DV	MODE0	mode select bit 0	0
RXD2	MODE1	mode select bit 1	0
LED_1000	MODE2	mode select bit 2	1
RXD3	MODE3	mode select bit 3	0
RX_CLK	1.8V/1.5V	Select the RGMII/RMII I/O voltage level 1: 1.8V I/O 0: 1.5V I/O	0

NOTE: 0=Pull-down, 1=Pull-up

NOTE: Power on strapping pins are latched during power-up reset or warm hardware reset.

NOTE: Some MAC devices input pins may drive high/low during power-up or reset. So PHY power on strapping status may be affected by the MAC side. In this case an external 10kΩ pull-down or pull-high resistor is needed to ensure a stable expected status.

NOTE: When using 2.5V RGMII I/O voltage level, RX_CLK can be pull-up or pull-down.

MODE[3:0]	Description
1100	RGMII, PLLOFF, INT;
1110	RGMII, PLLON, INT;
Others	Reserved

Design	MITCH	**Embest Tech Co. LTD**	
Review	<review>	Title 07 NETA	
Authorize	<authorize>	Size A3	Doc Name SBC8600B 120901 Ver. V1.1
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3.6 Power Pin Consumption

Table 3-12. **Power Pin Characteristic**

Symbol	Voltage Range	Current
AVDDL	1.1V ±5%	50.8 mA
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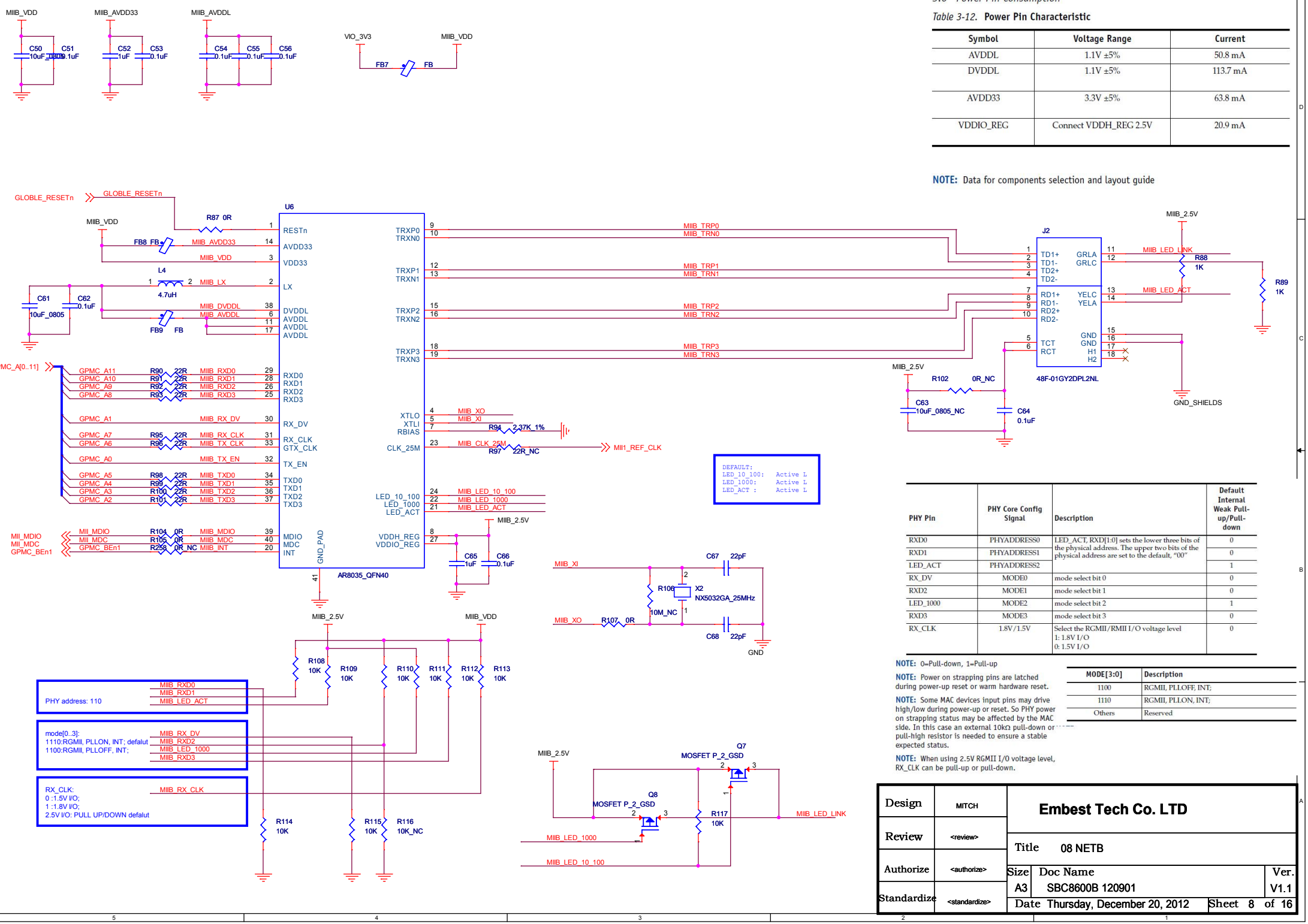
AVDD33	3.3V ±5%	63.8 mA
VDDIO_REG	Connect VDDH_REG 2.5V	20.9 mA

NOTE: Data for components selection and layout guide



PHY Pin	PHY Core Config Signal	Description	Default Internal Weak Pull-up/Pull-down
RXD0	PHYADDRESS0	LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00"	0
RXD1	PHYADDRESS1		0
LED_ACT	PHYADDRESS2		1
RX_DV	MODE0	mode select bit 0	0
RXD2	MODE1	mode select bit 1	0
LED_1000	MODE2	mode select bit 2	1
RXD3	MODE3	mode select bit 3	0
RX_CLK	1.8V/1.5V	Select the RGMII/RMII I/O voltage level 1: 1.8V I/O 0: 1.5V I/O	0

NOTE: 0=Pull-down, 1=Pull-up

NOTE: Power on strapping pins are latched during power-up reset or warm hardware reset.

NOTE: Some MAC devices input pins may drive high/low during power-up or reset. So PHY power on strapping status may be affected by the MAC side. In this case an external 10kΩ pull-down or pull-high resistor is needed to ensure a stable expected status.

NOTE: When using 2.5V RGMII I/O voltage level, RX_CLK can be pull-up or pull-down.

MODE[3:0]	Description
1100	RGMII, PLLOFF, INT;
1110	RGMII, PLLON, INT;
Others	Reserved

Design	MITCH	**Embest Tech Co. LTD**	
Review	<review>	Title 08 NETB	
Authorize	<authorize>	Size A3	Doc Name SBC8600B 120901 Ver. V1.1
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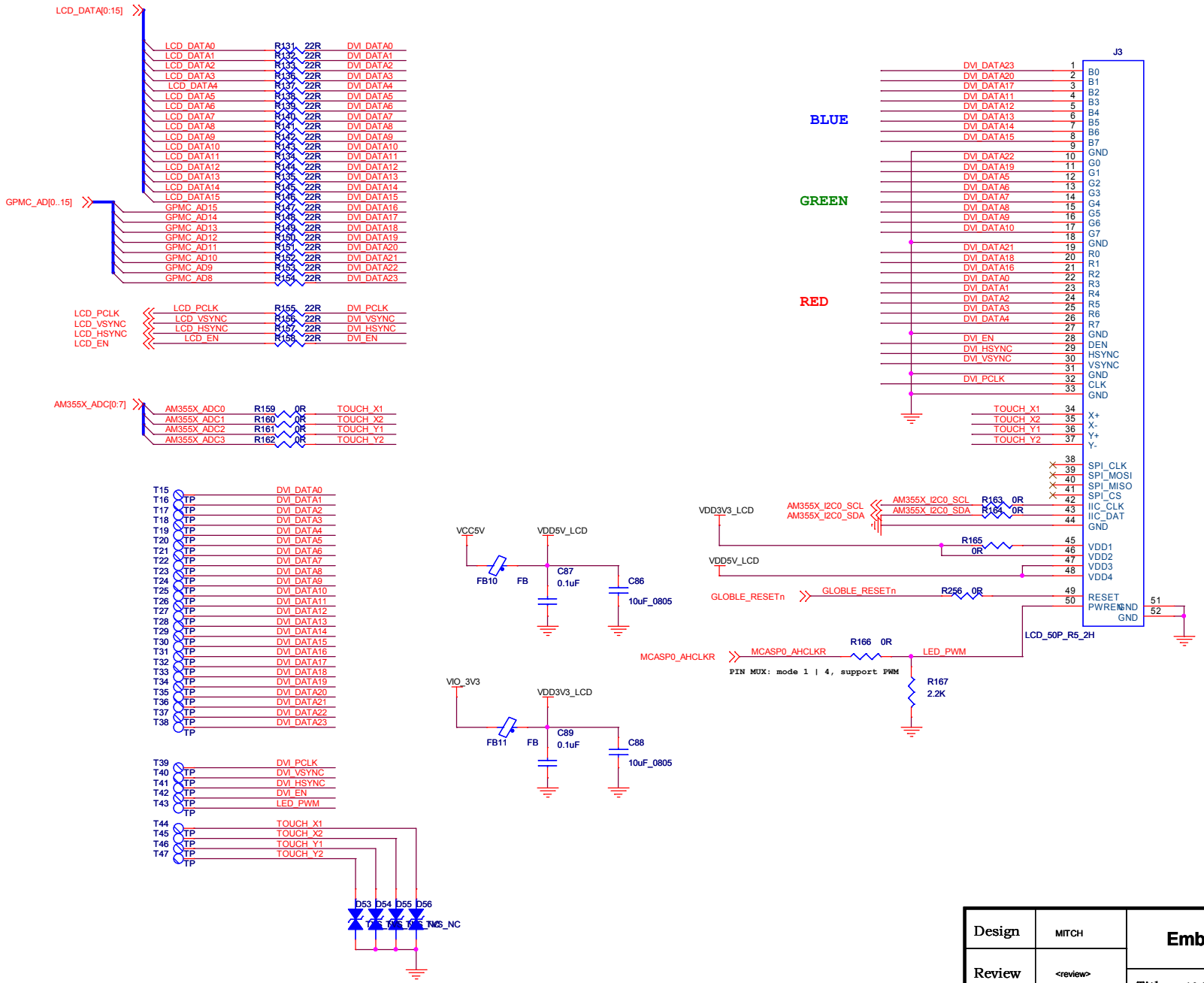

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Review	<review>	Title 10 LCD	
Authorize	<authorize>	Size A3	Doc Name SBC8600B 120901 / Ver. V1.1
Standardize	<standardize>	Date Thursday, December 20, 2012	Sheet 10 of 16

Attack (0.8dB/s to ~3200dB/s)
DAP_AVC_ATTACK

ure 16. DAP AVC Block Diagram

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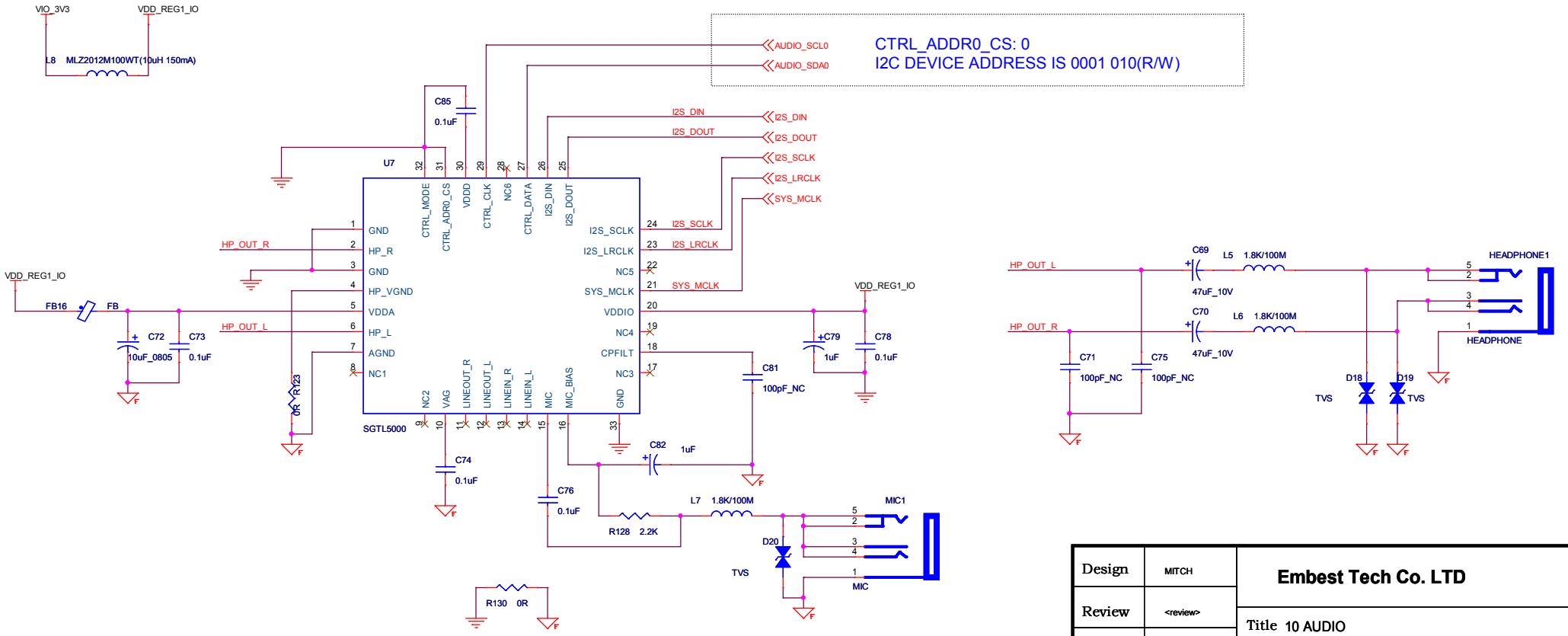
I²C

The I²C port is implemented according to the I²C specification v2.0. The I²C interface is used to read and write all registers.

For the 32 QFN version of the SGTL5000, the I²C device address is 0n01010(R/W) where n is determined by I2C_ADR0_CS and R/W is the read/write bit from the I²C protocol.

For the 20 QFN version of the SGTL5000 the I²C address is always 0001010(R/W).

The SGTL5000 is always the slave on all transactions which means that an external master will always drive CTRL_CLK.



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Review	<review>	Title 10 AUDIO		
Authorize	<authorize>	Size A3	Doc Name SBC8600B 120901	Ver. V1.1
Standardize	<standardize>	Date Thursday, December 20, 2012	Sheet 10 of 18	

Design	MITCH	**Embest Tech Co. LTD**		
Review	<review>	Title 10 AM335XZCZ-CON		
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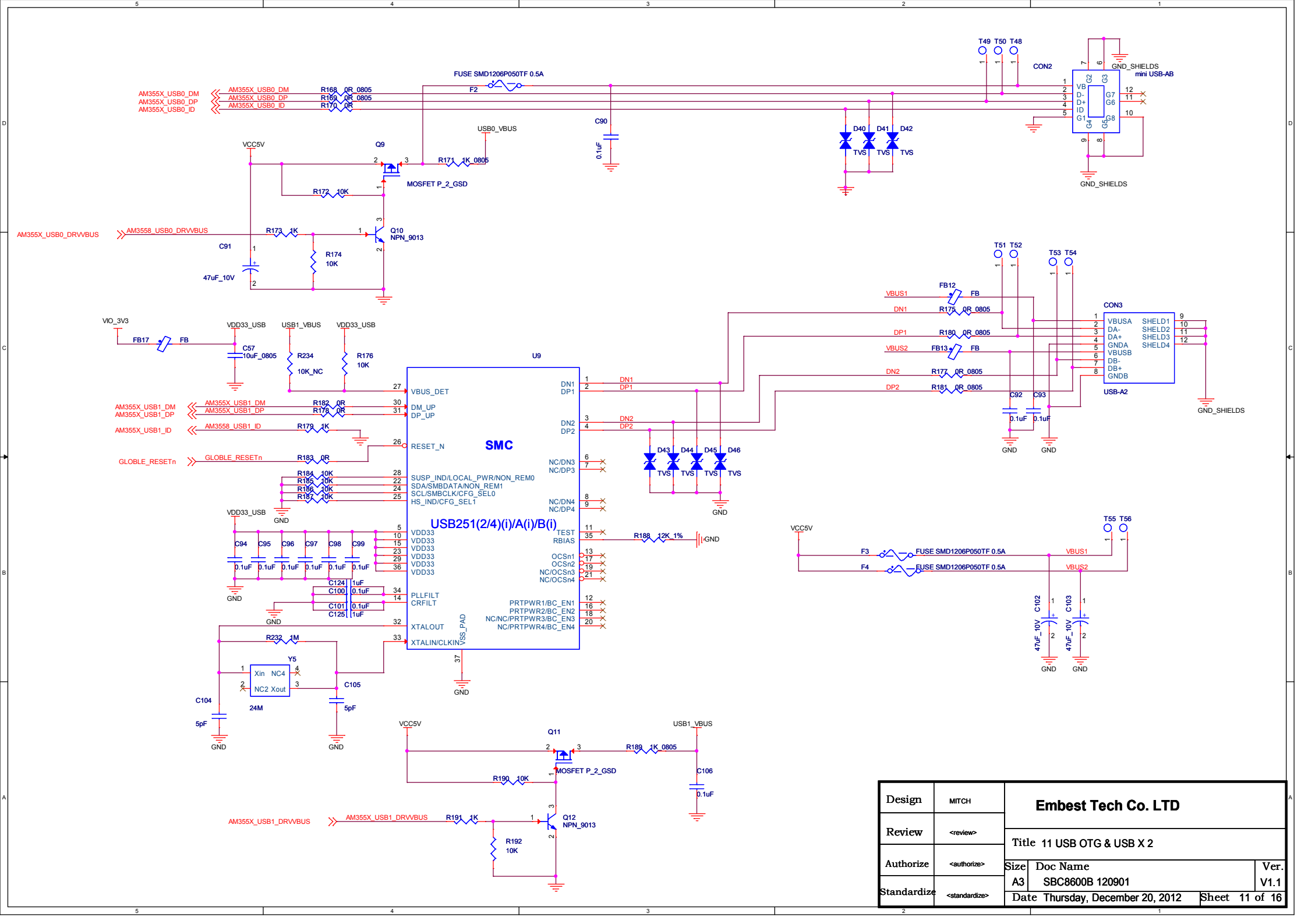

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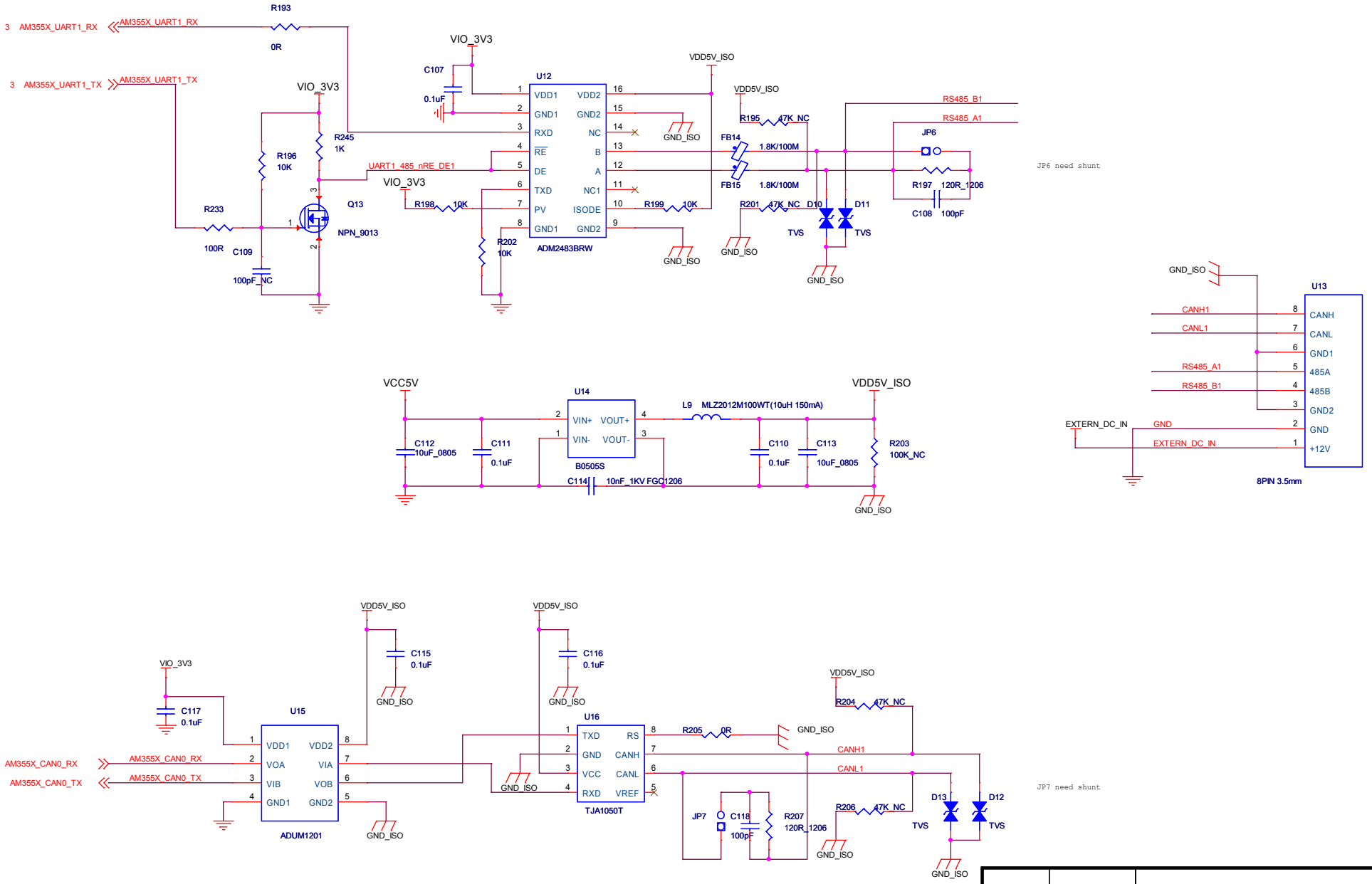
Standardize	<standardize>	Date Thursday, December 20, 2012	Sheet 11 of 16



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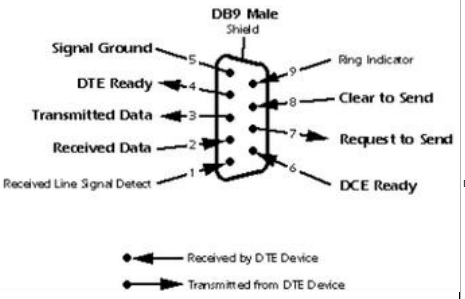
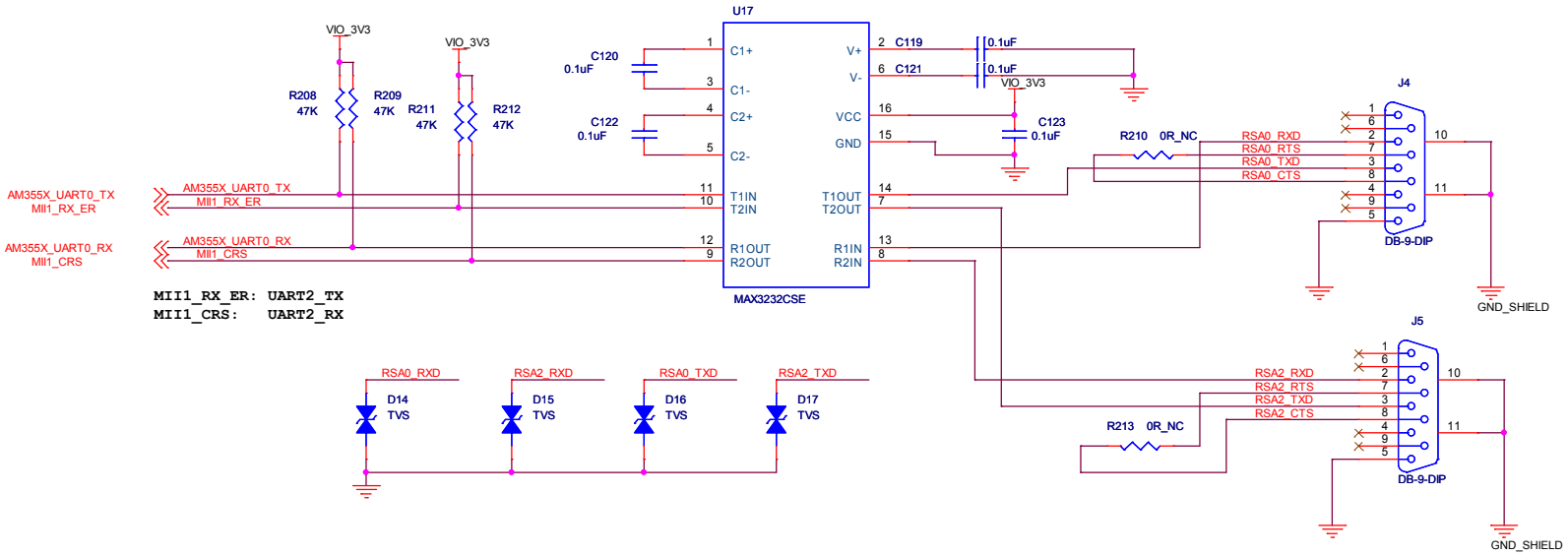
Standardize	<standardize>	Date Thursday, December 20, 2012	Sheet 12 of 16





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Review	<review>	Title 13 RS232 X 2	
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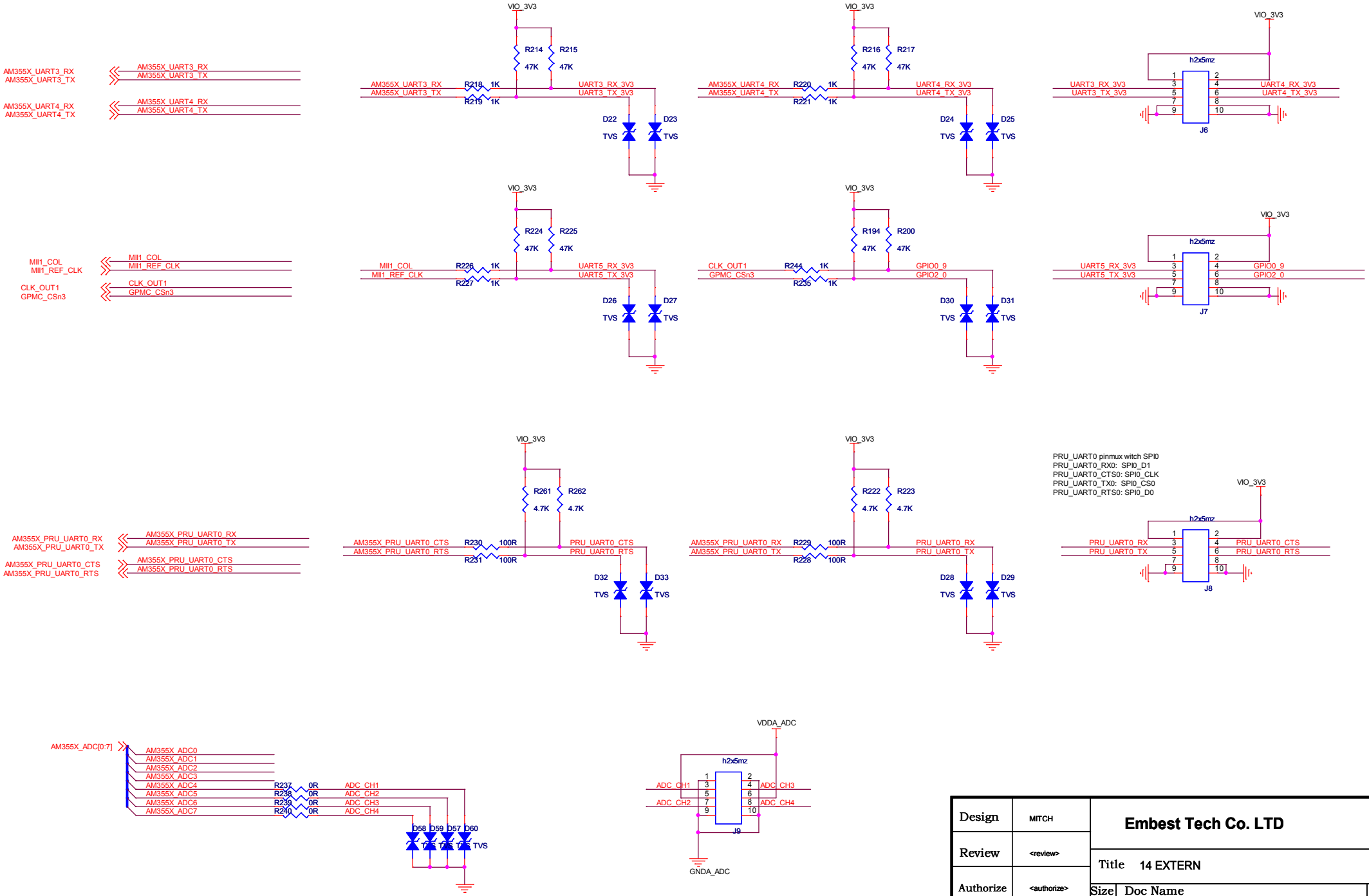
Standardize	<standardize>	Date Thursday, December 20, 2012	Sheet 13 of 16



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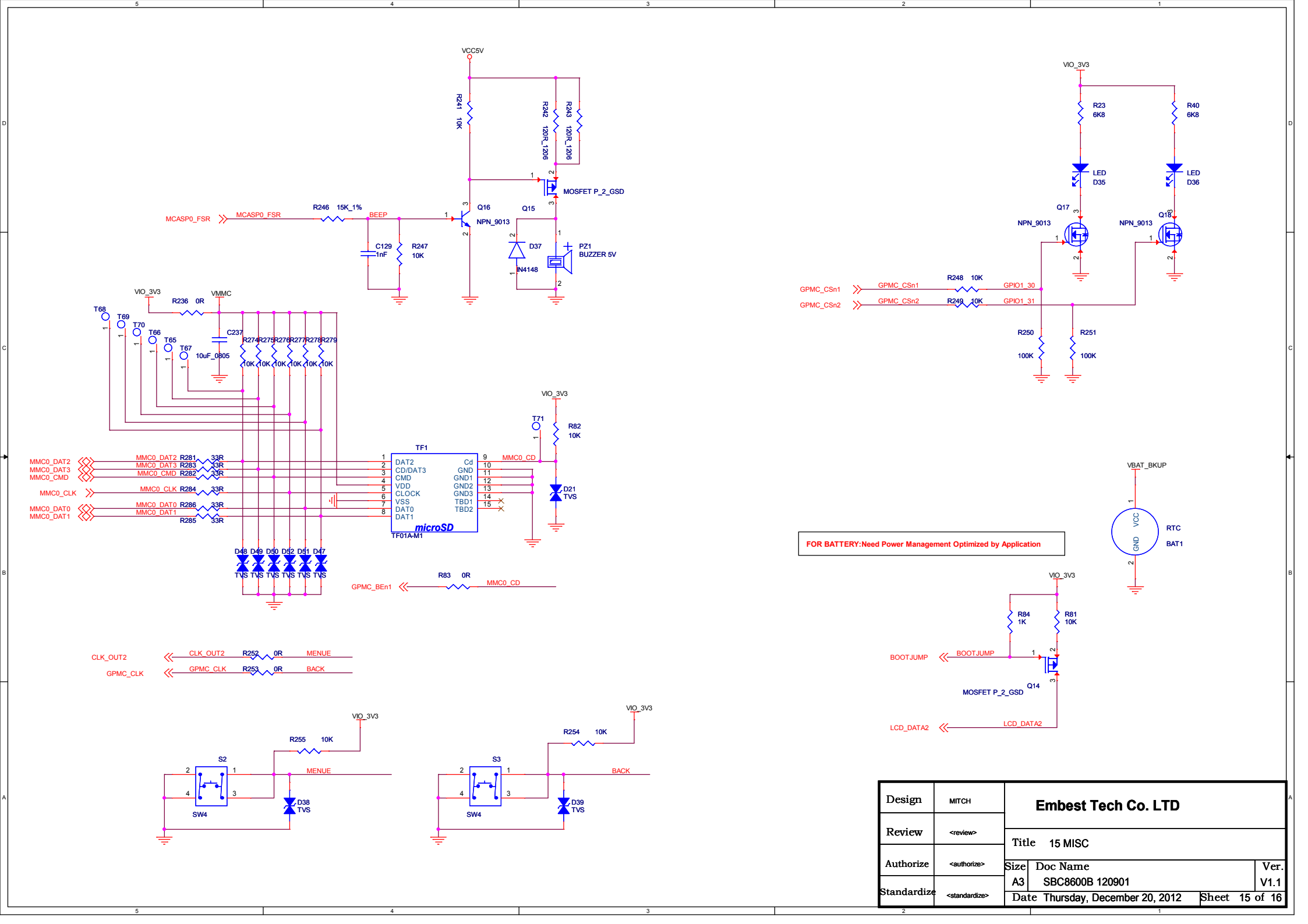

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Standardize	<standardize>	Date Thursday, December 20, 2012	Sheet 15 of 16

SBC8600B Revision History

SBC8600B 120900

1 Modify From SBC8600 120601: RM Nand; Add TF;

SBC8600B 120901

1 Add I2c0 pull up 10K
2 Add r232 1m5, modify C104&C105 5pf
3 modify R84 1K&R25 0R
4 Add D53~D60(ADC)
5 Add C124&C125 1uF
6 Modify R178&R182 0R
7Add jp6,jp7
7 Add R253 0R

Design	MITCH	Embest Tech Co. LTD	
Review	<review>	Title 16 REVISION HISTORY	
Authorize	<authorize>	Size A3	Doc Name SBC8600B 120901 Ver. V1.1
Standardize	<standardize>	Date Saturday, December 29, 2012	Sheet 16 of 16