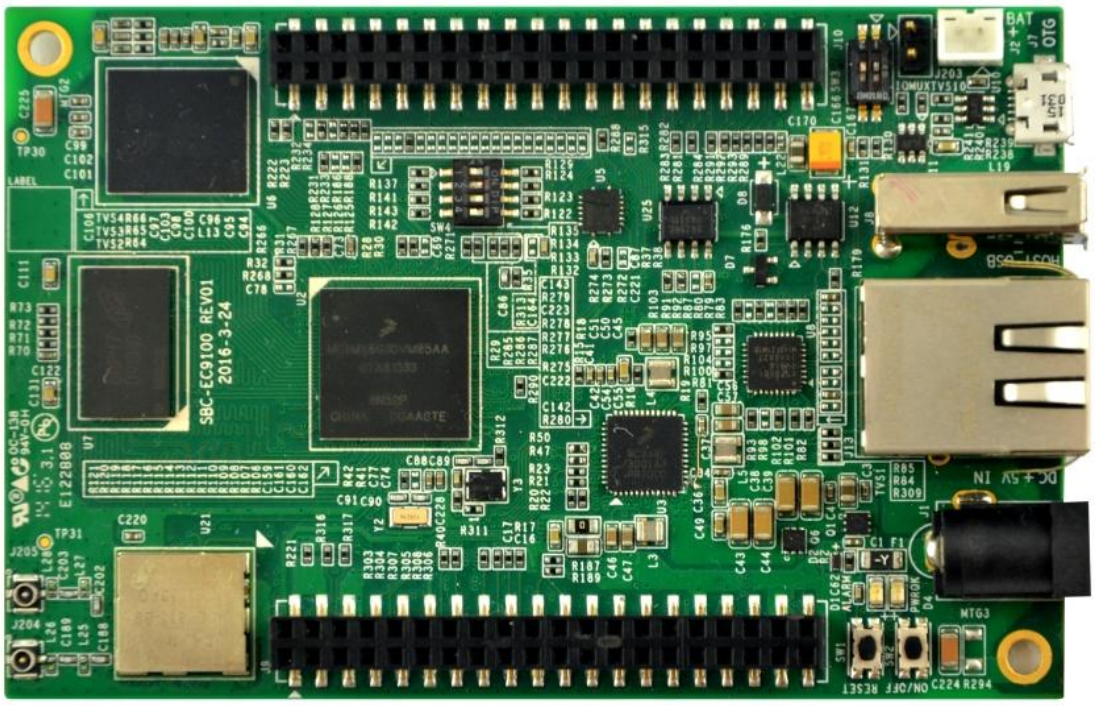
SBC-EC9100 Evaluation Board



User Manual

Rev00

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- Revision History:

Version	Updata Date	Describe
1.0	2016-6-20	Original Version

Table of Contents

Chapter 1 Product Overview

1.1 Brief Introduction

SBC-EC9100 is low cost evaluation board that using i.MX6UL processor by Embest design. The system is oriented to the industrial embedded control field, such as medical instrument, video monitor, communication and so on. Which is industrial embedded products without too much UE for human-computer interaction.SBC-EC9100 provides a rich resource of peripheral interfaces, with one USB2.0 host high-speed interface, storage, 12 bit camera interface, one gigabit network interface one OTG interface, high capacity of TF card expansion, 24bit LCD, WIFI&BT interface (optional and default version does not provide), UART, CAN and RS485 interface.at the same time,in order to extend for consumer conveniently,there are some UART,I2C,SPI,ADC,PWM,RMIIc resources connect to two biserial40PIN socket.BTW, one of the 40 pin socket signal definition compatible with raspberry pi 40 pin definition.

1.1.1 Packing List

- SBC-EC9100 evaluation board X1
- 5V DC power adapter X1（optional）
- 8GB TF card X1（optional）
- 4.3 inches LCD or 7 inches LCD display screen X1（optional）
- UART line X1（optional）
- USB OTG line X1（optional）
- Network line (direct links) X1（optional）

1.1.2 Product Features

- **Electrical Features:**
  - Operating temperature：0~70℃ （commercial grade）
  - Operating temperature：-40~85℃ （industrial grade）
  - Input voltage：5V
  - Operating humidity：20% ~ 80% no condensation
  - Mainboard size：100 mm×65 mm
  - PCB specifications：thickness:1.6mm，6 layer design
- **Communication Interface：**
  - One 8-bit digital camera interface
  - One 100MB Ethernet network interface(RJ45)
  - One RS485 interface
  - Two CAN interface
  - One USB2.0 Host high speed transmission interface
  - One USB OTG interface
  - One TF card interface
  - Two WIFI/BT module ant interface（2.4G/5G, optional）
  - Two 2*20 Pin expansion interface（extend I2C，UART，SPI、PWM、ADC singnal and so on）
- **Debugging Interface:**
  - Debugging Uart use the Uart3 of CPU，the singnal from pin6 and pin8 J10，TTLvoltage .
- **Others Interface:**
  - Power interface(DC-Jack power interface,2.1mm)
  - RTC battery interface（SIP2，2mm）
  - Power ON/OFFbutton， Reset button
  - LED indicator light（Power indicator light 、operating indicator light、overvolatage warning indicator light）

1.2 Detailed Breakdown Diagram

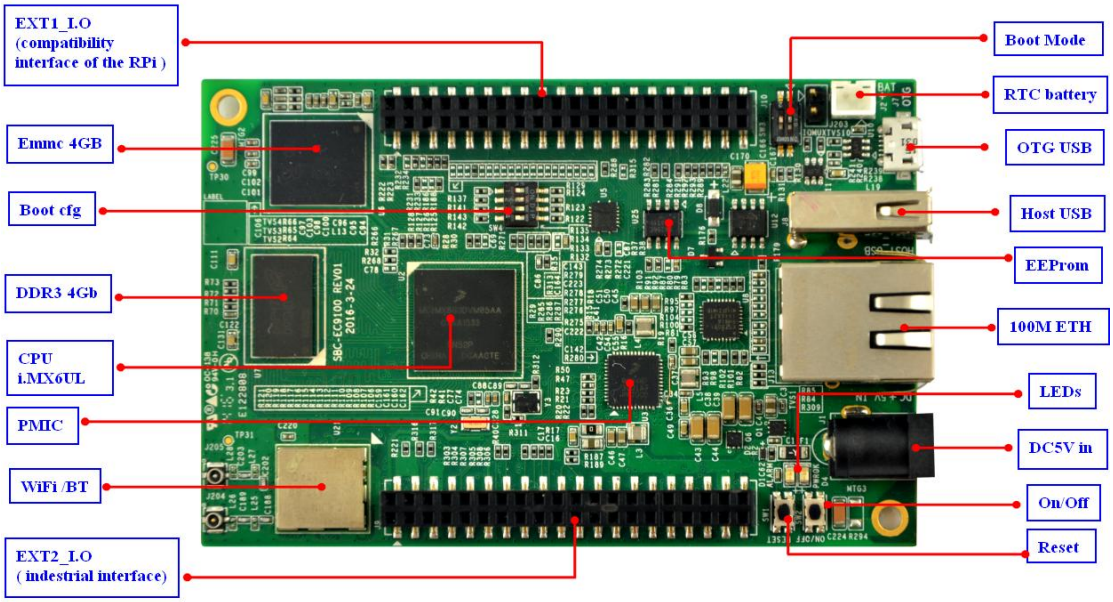


Figure 1-2.1， TOP

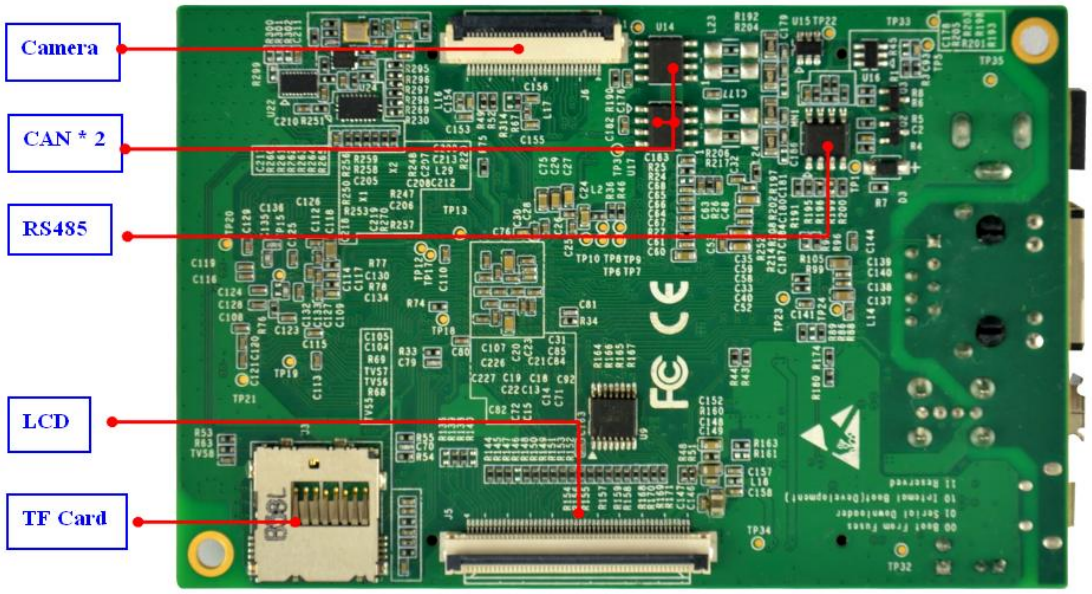


Figure 1-2.2 ， Bottom

1.3 System Block Diagram

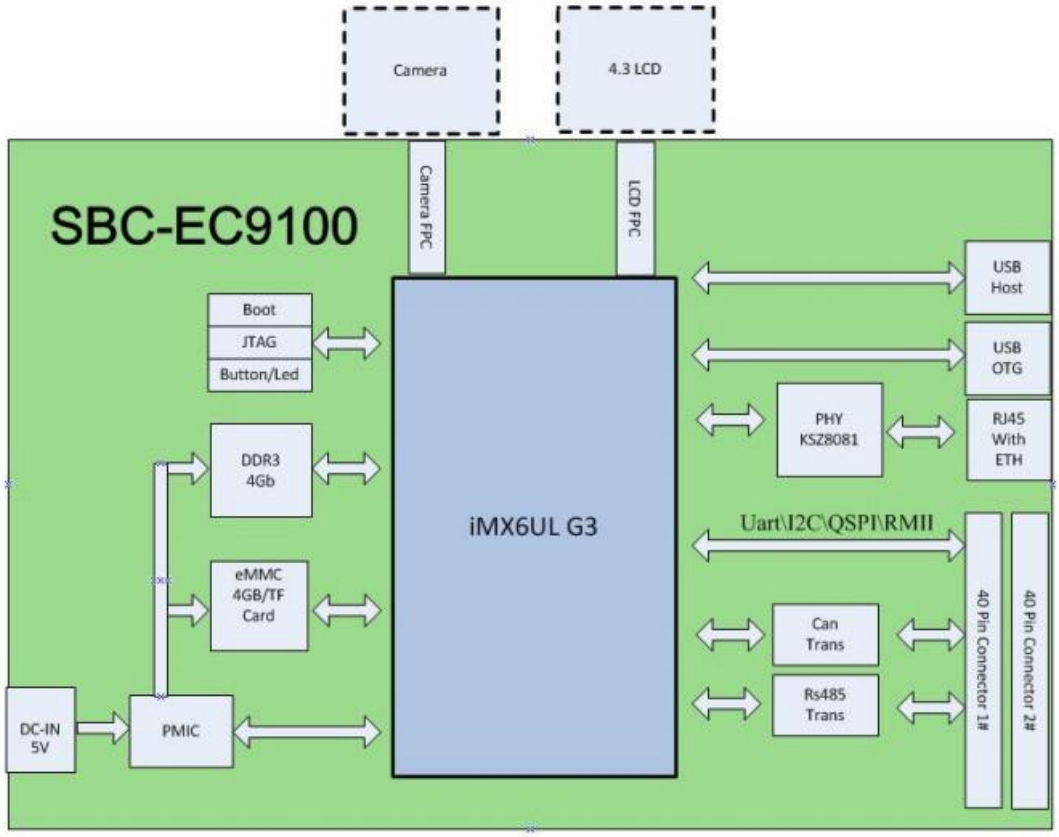


Figure **1-3** SBC-EC9100 System Block

1.4 Product Dimensions (unit：mm)

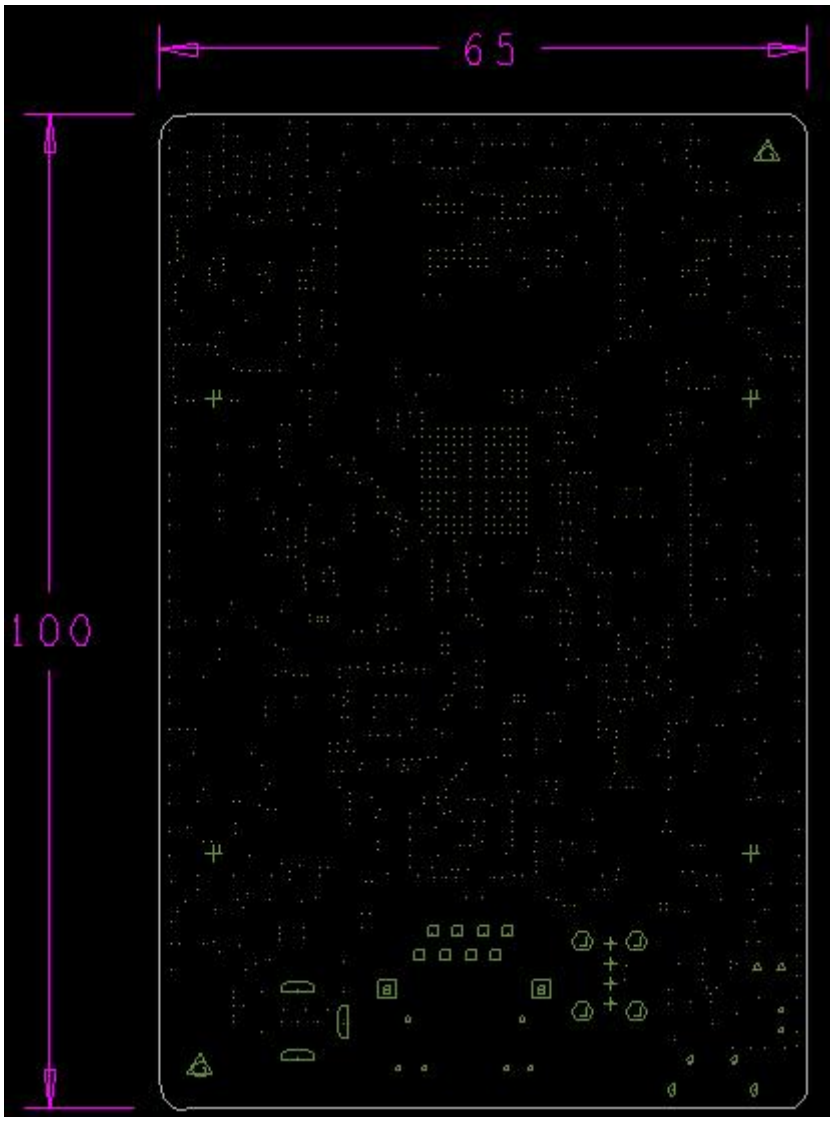


Figure **1-4** Product Dimensions

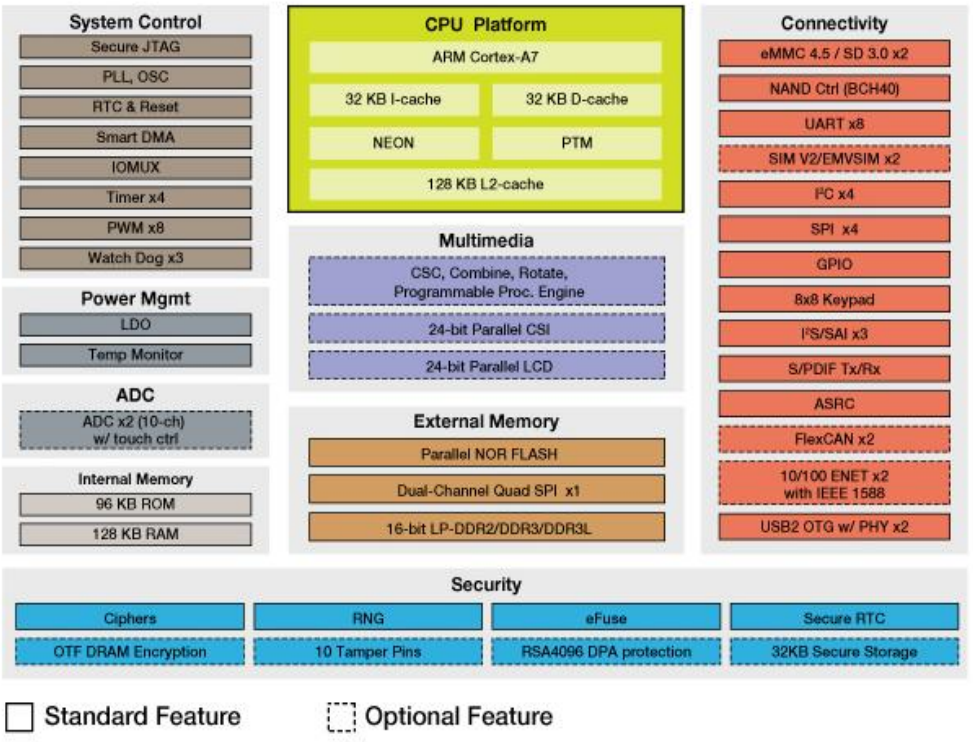
Chapter 2 Introduction to Hardware System

This chapter will do some detailed description about SBC-EC9100 hardware system structure、extend and peripheral interface,if there are some difference description between chip datasheet and this chapter chip description,please refere to official chip datasheet.

1.1 SBC-EC9100 Minimum System

1.1.1 CPU

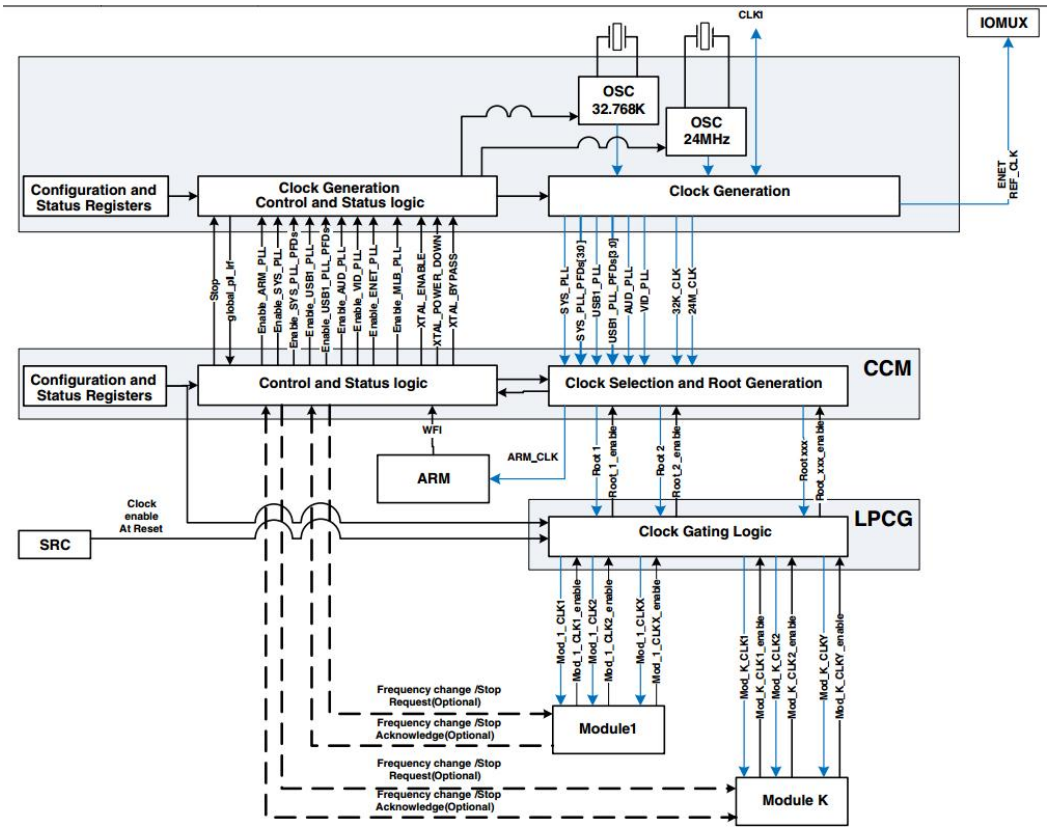
CPU adopt NXP i.MX66UltraLite series MCIMX6G3CVM05AA,adopt single and advanced ARM Cortex®-A7 core,14 x 14 mm, 0.8 pitch, BGA footprint,running speed up to 528MHz,and there are large of interfaces,including LPDDR2、DDR3、DDR3L、NAND flash、NOR flash、eMMC 、Quad SPI storage interfaces,and also there are some wide range peripheral equitment interface, such as WLAN、Bluetooth、GPS、Display and Camera.



CPU Internal Resources

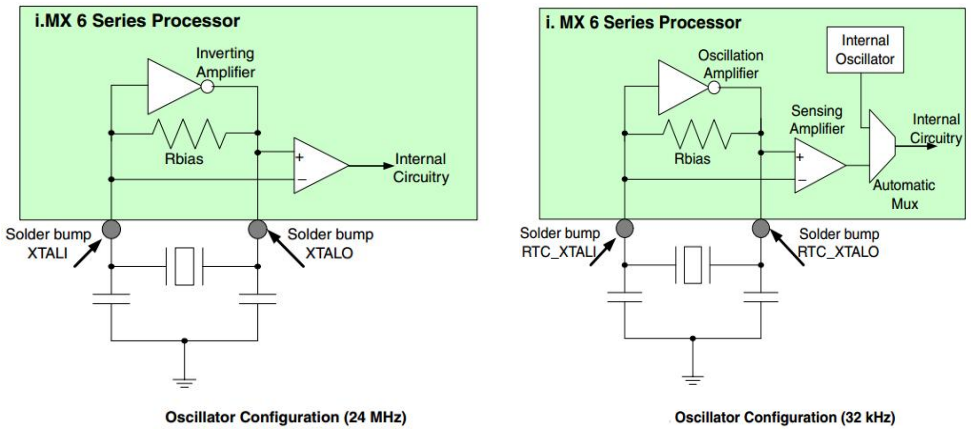
◆**Clock Cricuit**

CCM（Clock Control Module）control the generate 、partition、assign、synchronization of master clock and starting clock,the picture below is clock management system diagram:



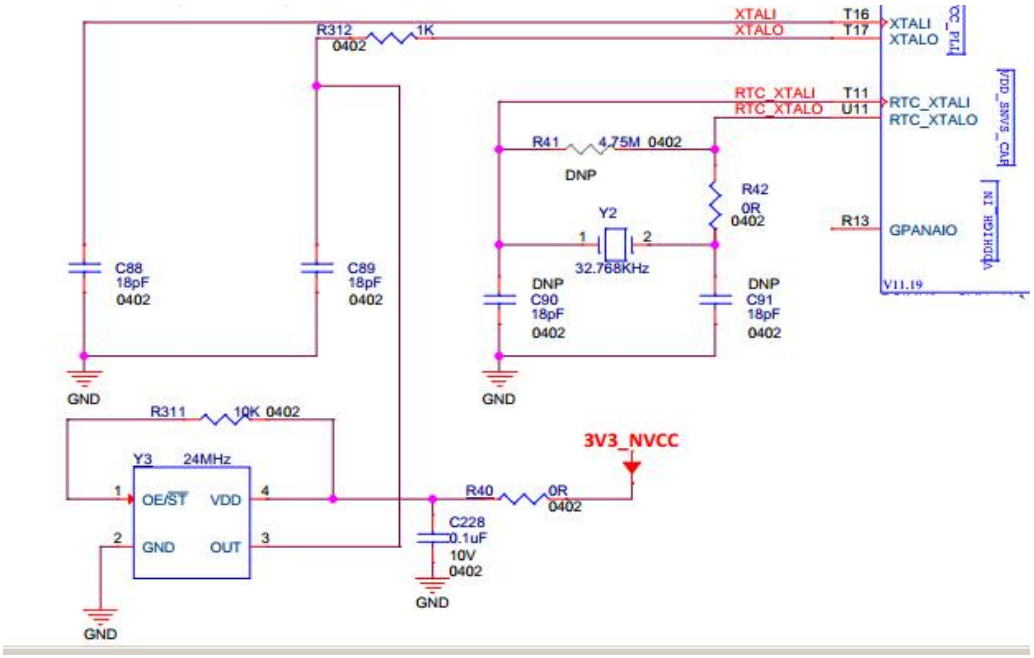
Clock Management System

CPU chip internal clock circuit



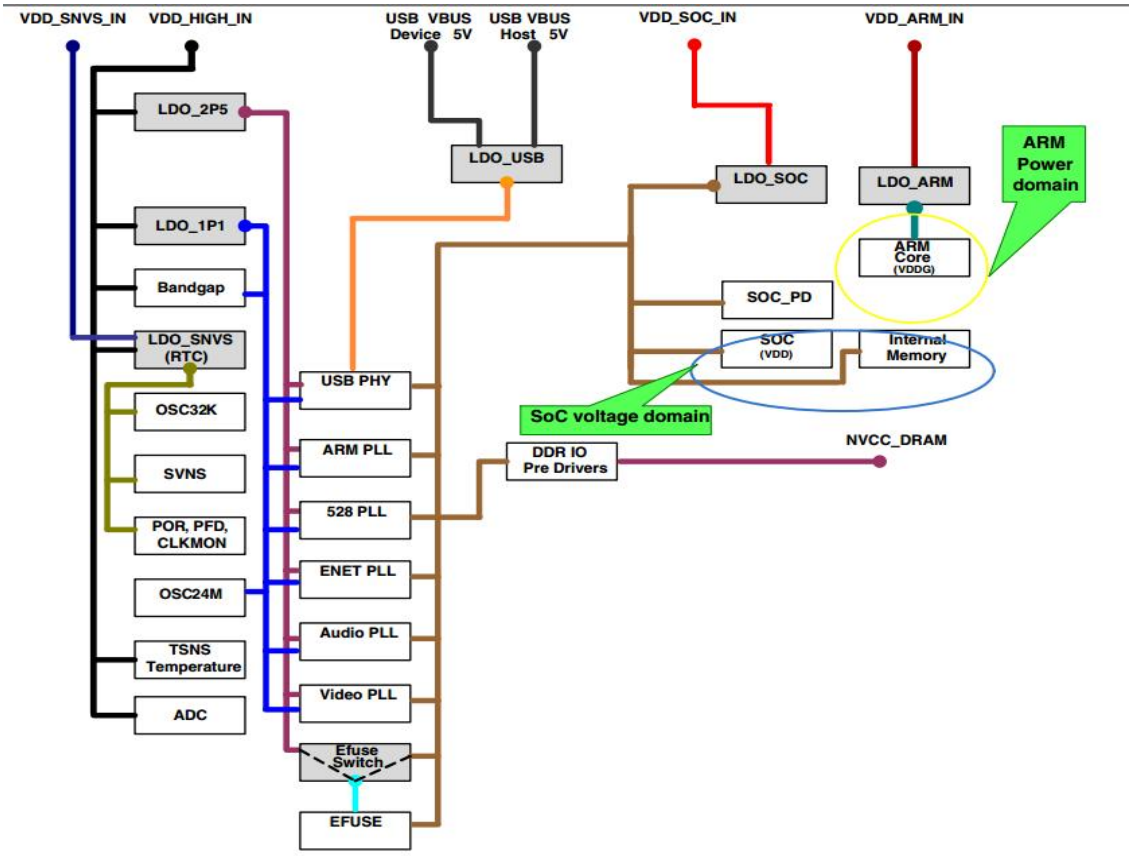
CPU chip external clock circuit

System main clock are provided by external 24M Oscillator, RTC clock are provided by crystal,peripheral design circuit as bellow：



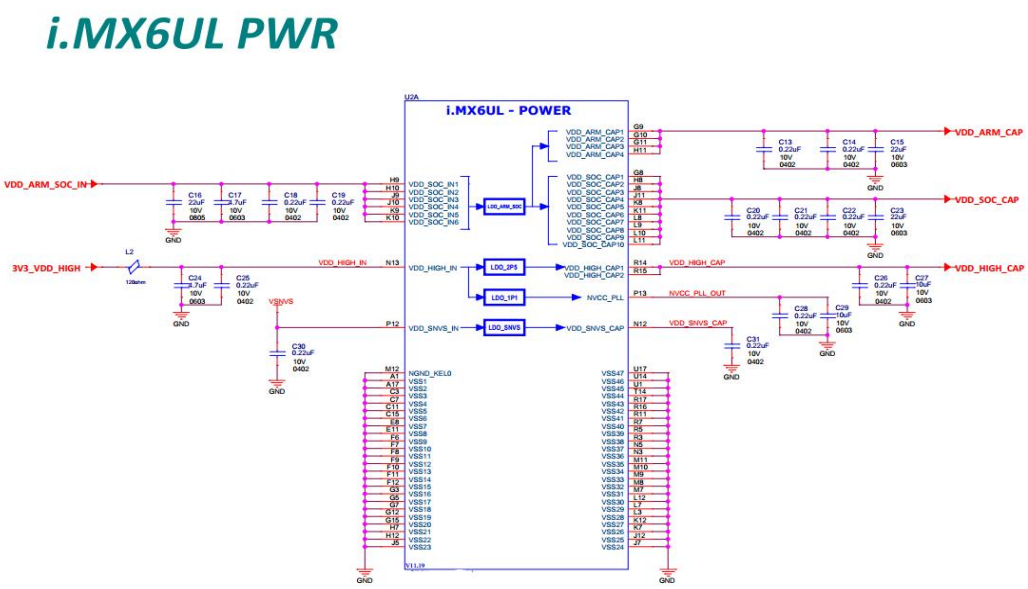
◆Power Circuit

There are some power management modules in CPU chip,simplifying the module power on timing sequence with it, power tree structure as bellow:



i.MX 6UltraLite Power Tree

The chip peripheral power hardware design as bellow:



The VDD_ARM_SOC_IN is 1.1 V input, provided by the PMIC SW1. 3V3_VDD_HIGH voltage of 3.3 V, which is provided by the PMIC and can provide 350ma current

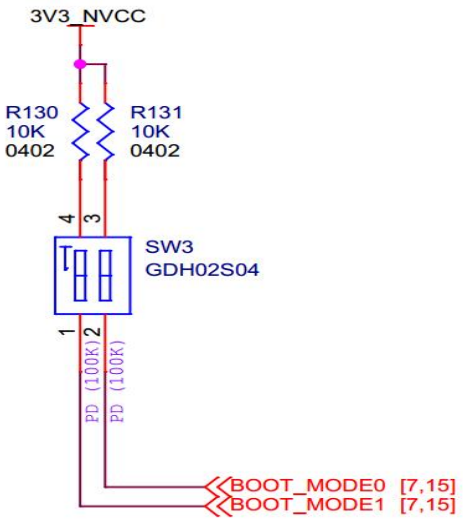
◆Starting Circuit

i.MX 6UltraLite processor supports a variety of startup mode, after the power on reset, ROM code boot will work based on the internal register BOOT_MODE[1:0] , Boot_MODE[1:0] defined as follows:

Boot MODE Pin Settings

BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

SBC-EC9100 use 2 bits for encoding the switch SW3 as boot mode choice, the switch to off position, using the chip internal pull-down, logic is set to 0, the switch to on, use external 10K, logic is set to 1, as shown in the figure on the right：.



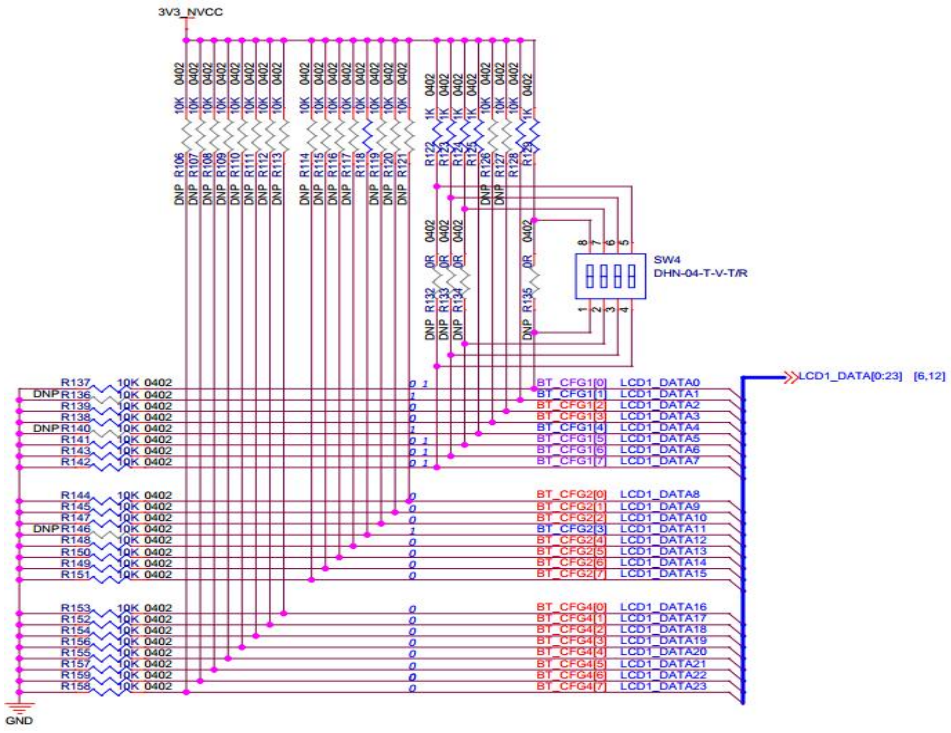
i.MX 6UltraLite processor through the BOOT_CFGx[7:0] to configure the GPIO register, its configuration is described as shown in the following table:

	0/1	0/1	0/1	1	0	0	1	0
TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
QSPI	0	0	0	1	Reserved	DDRSMP: "000" : Default "001-111"		
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST_pad (uSDHC3 & 4 only)	SD Loopback Clock Source Selfor SDR50 and SDR104 only) '0' - through SD pad '1' - direct
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - Highl 1- Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST_pad (uSDHC3 & 4 only)	SD Loopback Clock Source Selfor SDR50 and SDR104 only) '0' - through SD pad '1' - direct
NAND	1	BT_TOGGLEMODE	Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	

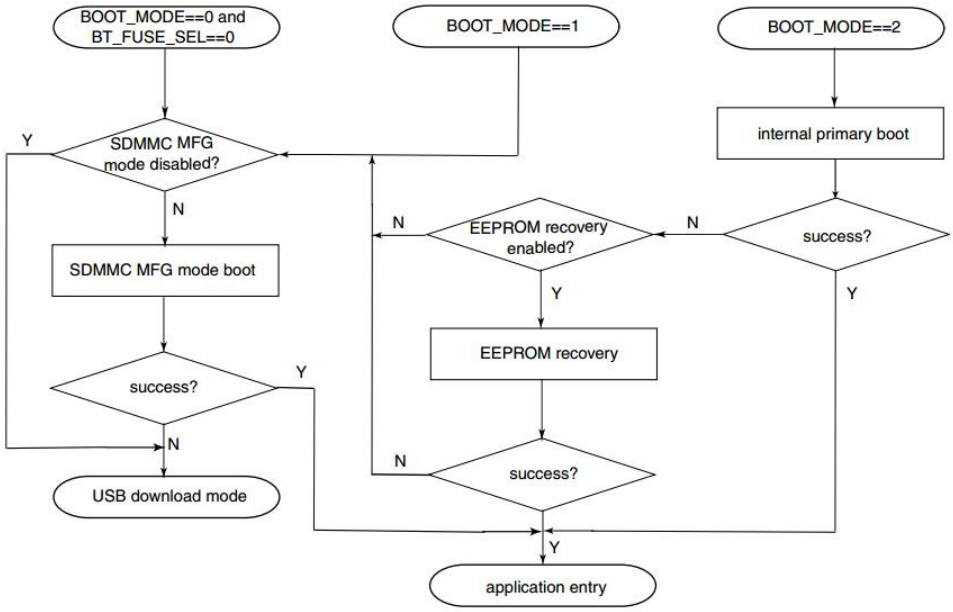
	0	0	0	0	1	0	0	0
TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved	HSPHS: Half Speed Phase Select i on 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	HSDLY: Half Speed Delay select i on 0 : one clock delay 1: two clock delay	FSPHS: Full Speed Phase Select i on 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	FSDLY: Full Speed Delay select i on 0 : one clock delay 1: two clock delay	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Muxing Scheme: 00 - A/D16 01 - A+DH 10 - A+DL 11- Reserved		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibrat i on Step '00' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit	Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
NAND	Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles.			BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reset_Time '0' - 12ms '1' - 22ms (LBA Nand)	Reserved

Note: the 0/1 is optional, and the 0 or 1 of the individual is indicated by means of welding resistance

The schematic design is as follows, SW4 code switch dial to OFF is 0, ON is 1, the corresponding way to see figure.



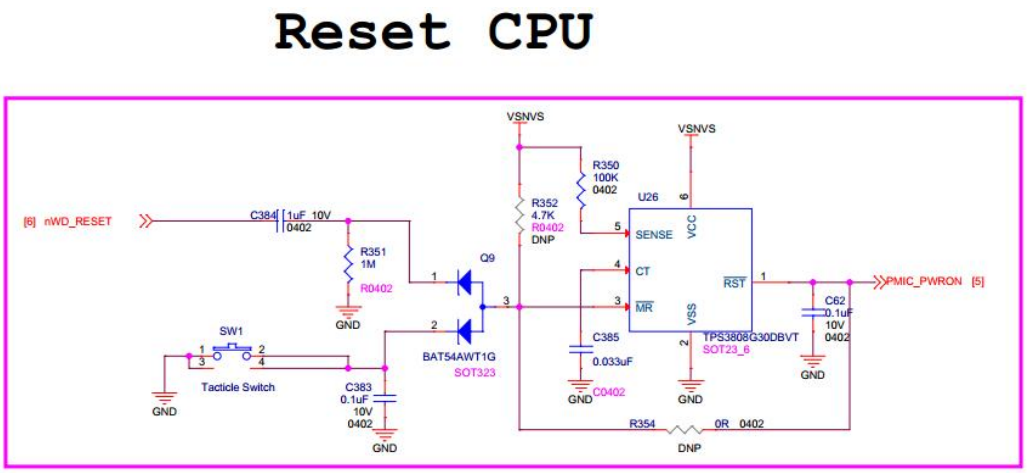
Special note, SBC-EC9100 has a factory mode, when the set of internal start and restore the start (if already open) are failure, SBC-EC9100 can enter the SD/MMC start before downloaded mode, and the process is as follows:



SD/MMC Manufacture boot flow

◆Reset Circuit

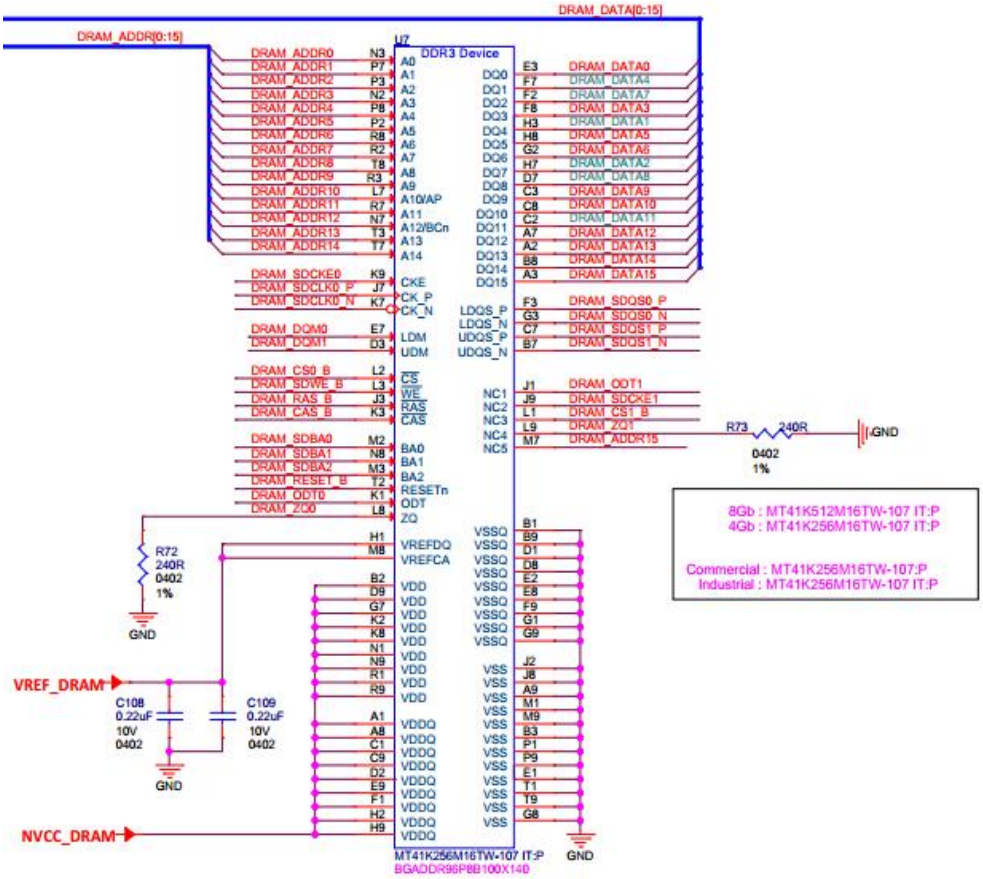
SBC-EC9100 with the Reset button, if you need to reset the system, you can press the reset button, you can enter the Linux and enter restet command, design schemetic as bellows:



1.1.2 Memory – DDR3L、 EMMC and EEPROM

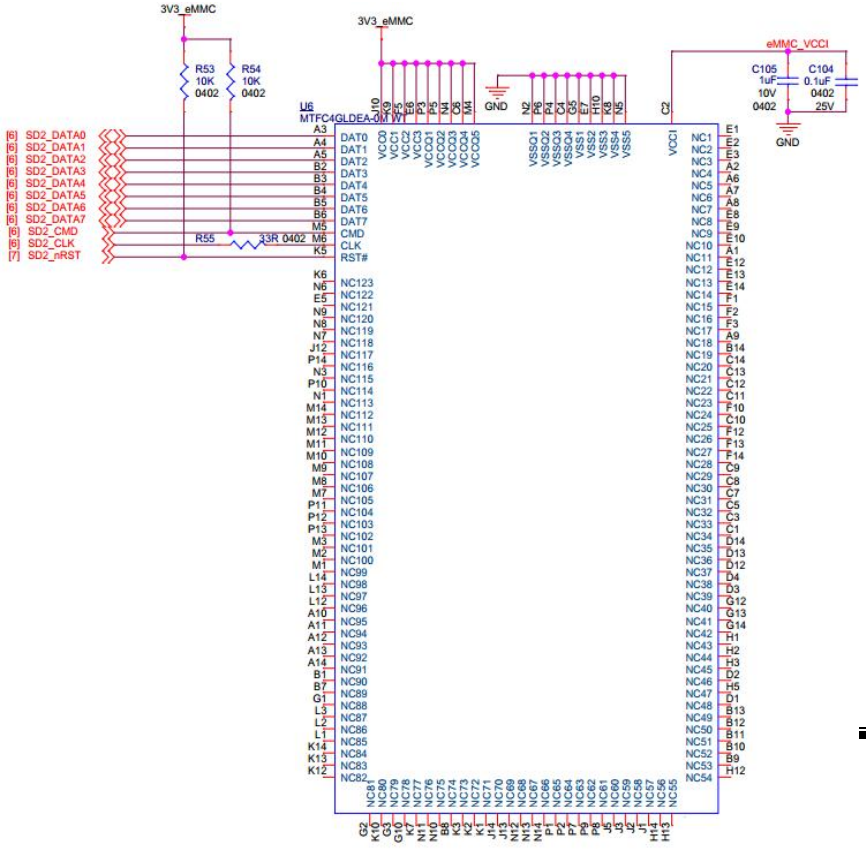
◆**DDR3L**

SBC-EC9100 using Kingston company's 4G bits DDR3L SDRAM and 4GB EMMC. DDR3 using FBGA96-ball package, schematic diagram, such as the right figure, 4Gb and 8Gb using in PCB, Commercial and industrial grade design compatible design.



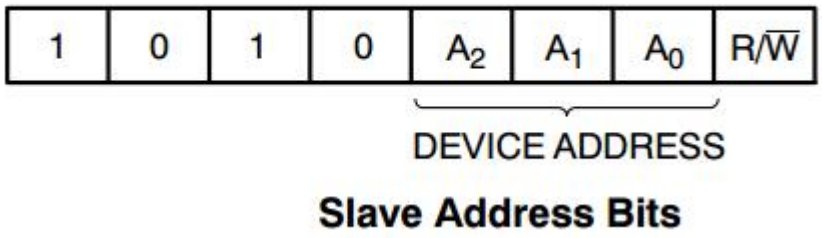
◆**EMMC**

Emmc using BGA153ball package,the same commercial and industrial grade design, circuit, such as the right



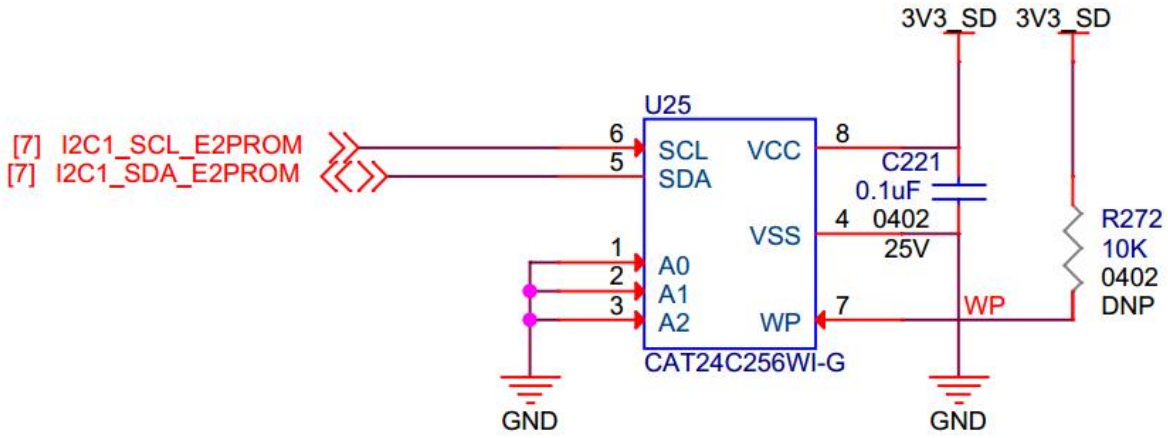
◆**EEPROM**

SBC-EC9100 to provide EEPROM 256Kb, to facilitate the user to store some important information, EEPROM using CAT24C256 company's ONSEMI, chip address A0, A1, A2 set to 0, as the bellows:



Slave Address Bits

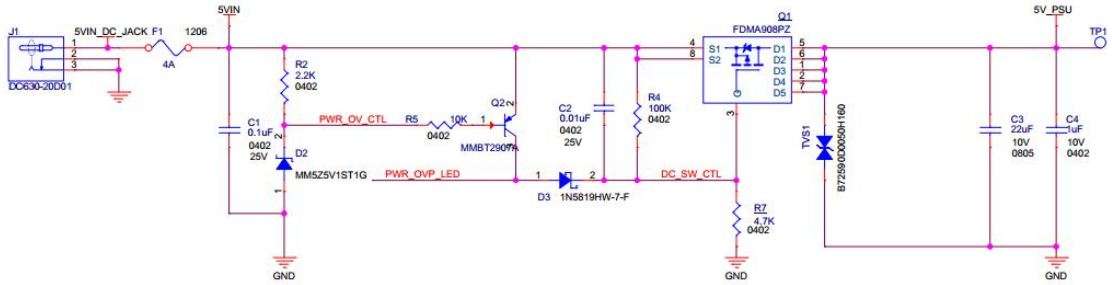
The schemetic as bellows:



1.1.3 Power Management

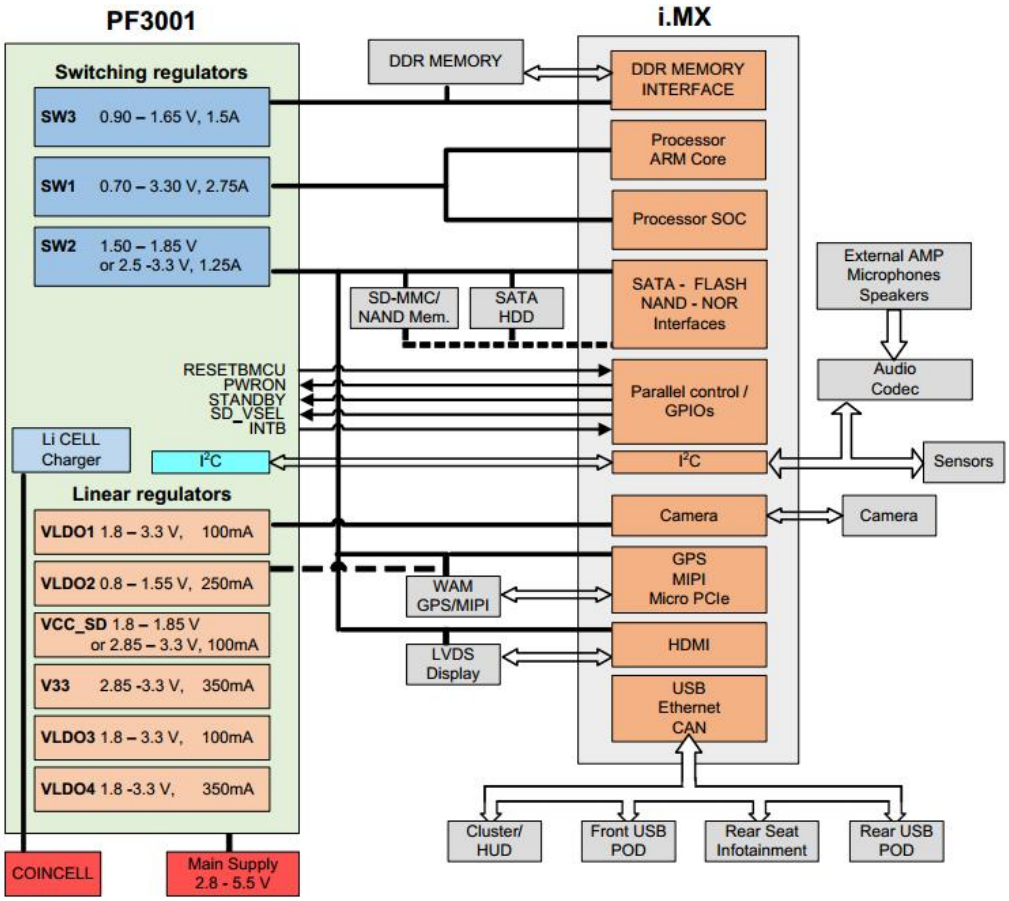
◆Power Supply

The SBC-EC9100 connected power input DC5V, with 5.5V overvoltage protection, 4a over current protection, power supply reverse connection protection function, input supply system directly start and normal green power indicator light, start running the green lights flashing, for close to press the on / off button for more than 5 seconds, boot again long press on / off button 3 seconds to open, the schematic diagram as follows:



◆PMIC

SBC-EC9100 using NXP power management chip PF3001, support for multi-channel programmable power output.



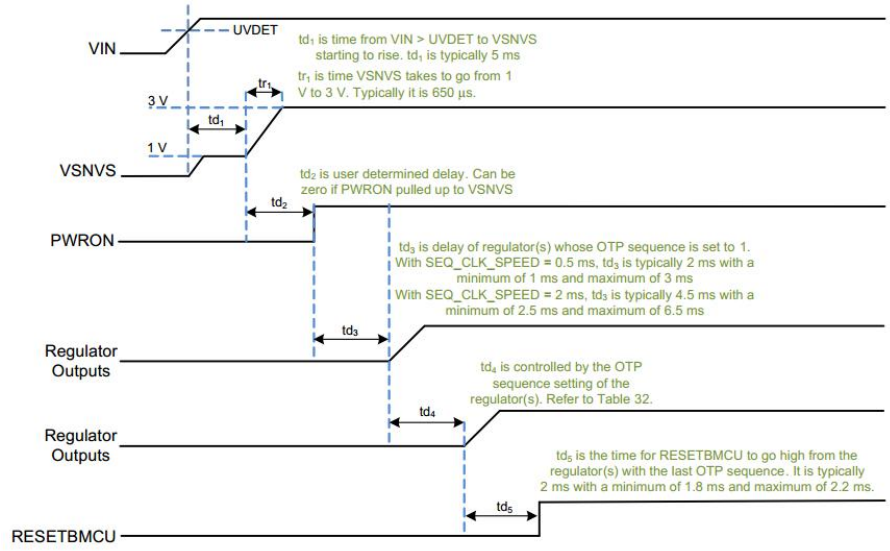
PF3001 Simplified Application Diagram

PF3001 the output power parameters are as follows:

PF3001 Power Tree

Supply	Output Voltage (V)	Programming Step Size (mV)	Maximum Load Current (mA)
SW1	0.7 to 1.425 1.8 and 3.3	25 (N/A)	2750
SW2	1.5 to 1.85 2.5 to 3.3	50 variable	1250
SW3	0.9 to 1.65	50	1500
VLDO1	1.8 to 3.3	50	100
VLDO2	0.8 to 1.55	50	250
VCC_SD	2.85 to 3.3 1.8 to 1.85	150 50	100
V33	2.85 to 3.3	150	350
VLDO3	1.8 to 3.3	100	100
VLDO4	1.8 to 3.3	100	350
VSNVS	3.0	NA	1.0

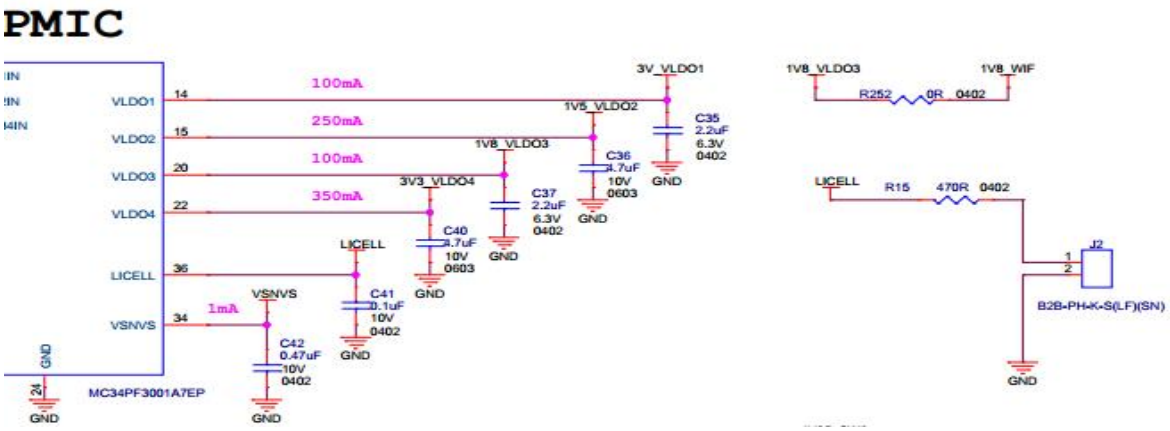
PF3001 startup sequence is as follows:



Start-up Timing Diagram

◆RTC Power

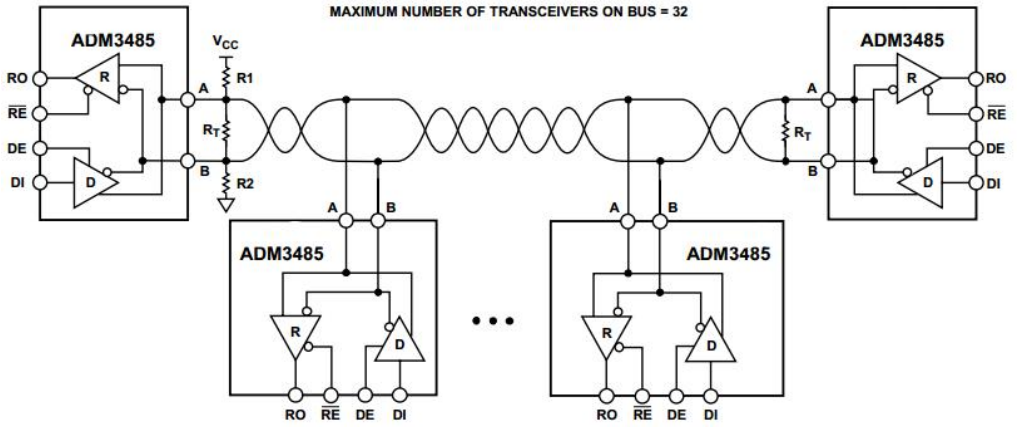
PF3001 has RTC power management function, but need to provide external power supply, SBC-EC9100 no design board RTC battery, the use of external RTC power design, as follows:



1.2 External Interface Detail

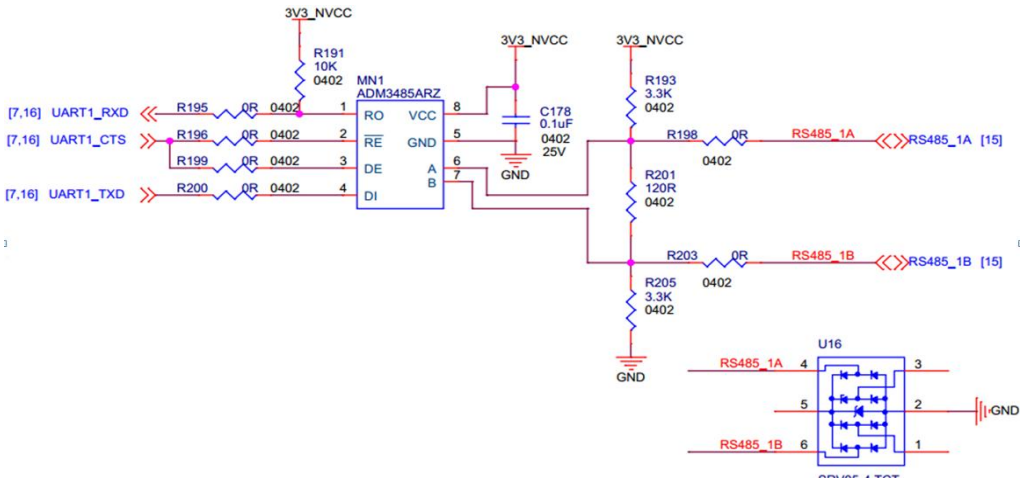
1.2.1 RS485 Interface

SBC-EC9100 provides one RS485 interface, the transceiver chip using Devices ADM3485 Analog, networking applications as fosllows:

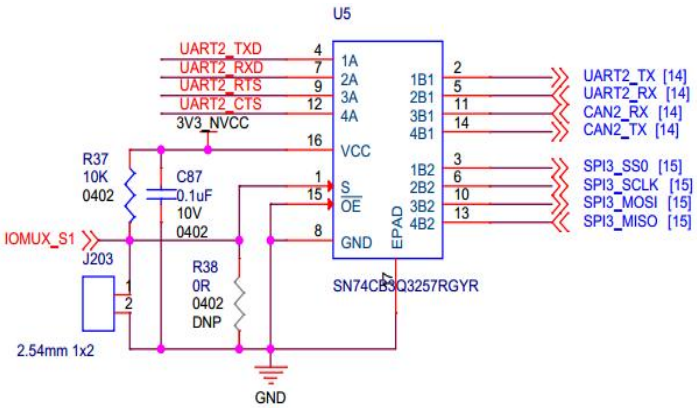


ADM3485 Typical Half-Duplex RS-485 Network

The processor using Uart1 to achieve RS485 communication, while increasing the ESD protection circuit, RS485 signal through the industrial interface J9 to connect exterior, the corresponding schematic design is as follows:

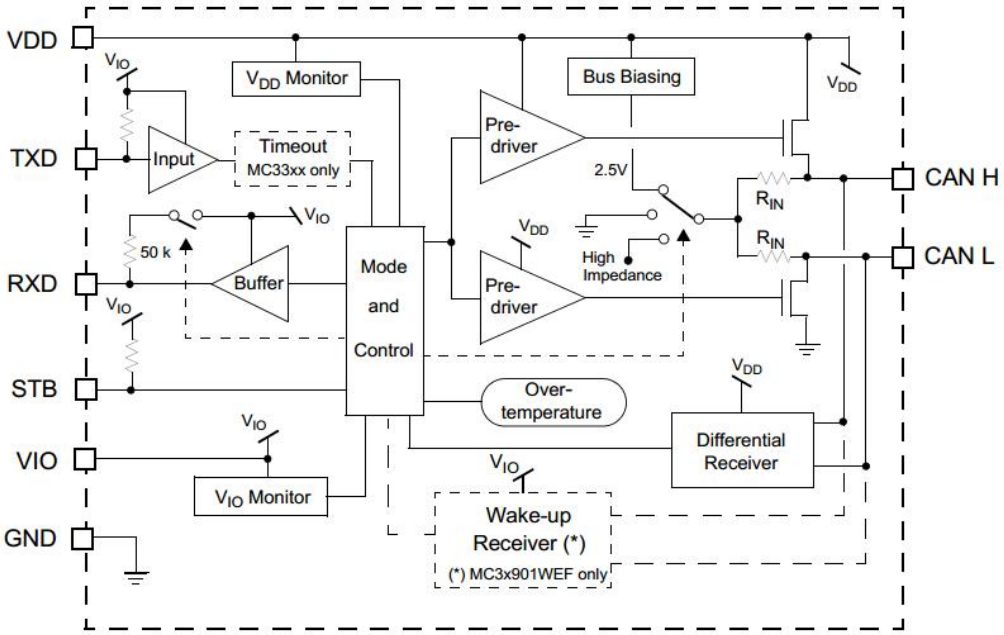


1.2.2 CAN Interface



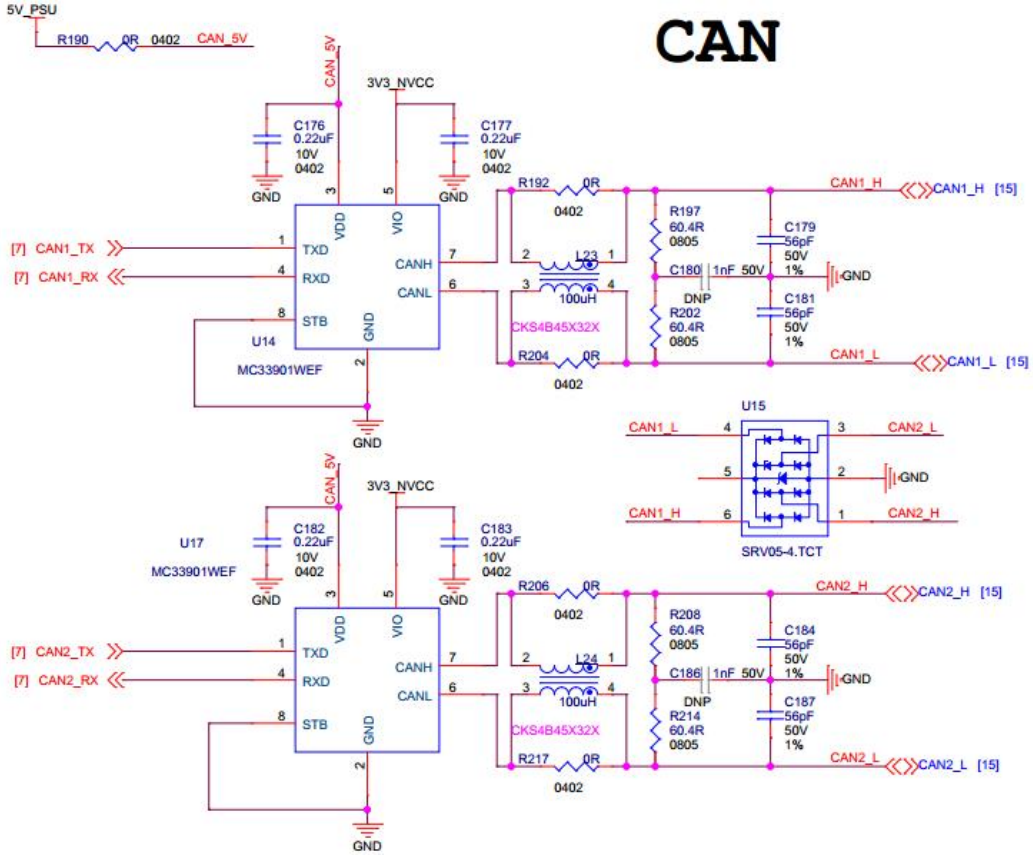
SBC-EC9100 can provide two CAN interfaces, which one requires to connect to external SPI signal multiplexing, select J203 by manual selection, the default state for the use of SPI signals. Short connected to J203, the system select the external CAN2 and external Uart2, disconnect the J203, the system select the external SPI interface.

CAN transceiver using NXP MC33901, the internal function as follows.



Internal Block Diagram for MC3x901xEF

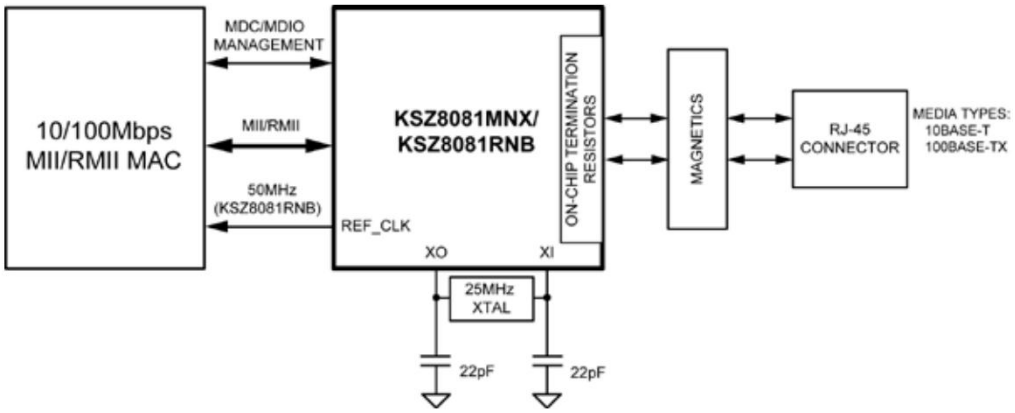
CAN signal and external connection by the industrial interface J9 , increasing the ESD protection design, application design as follows:



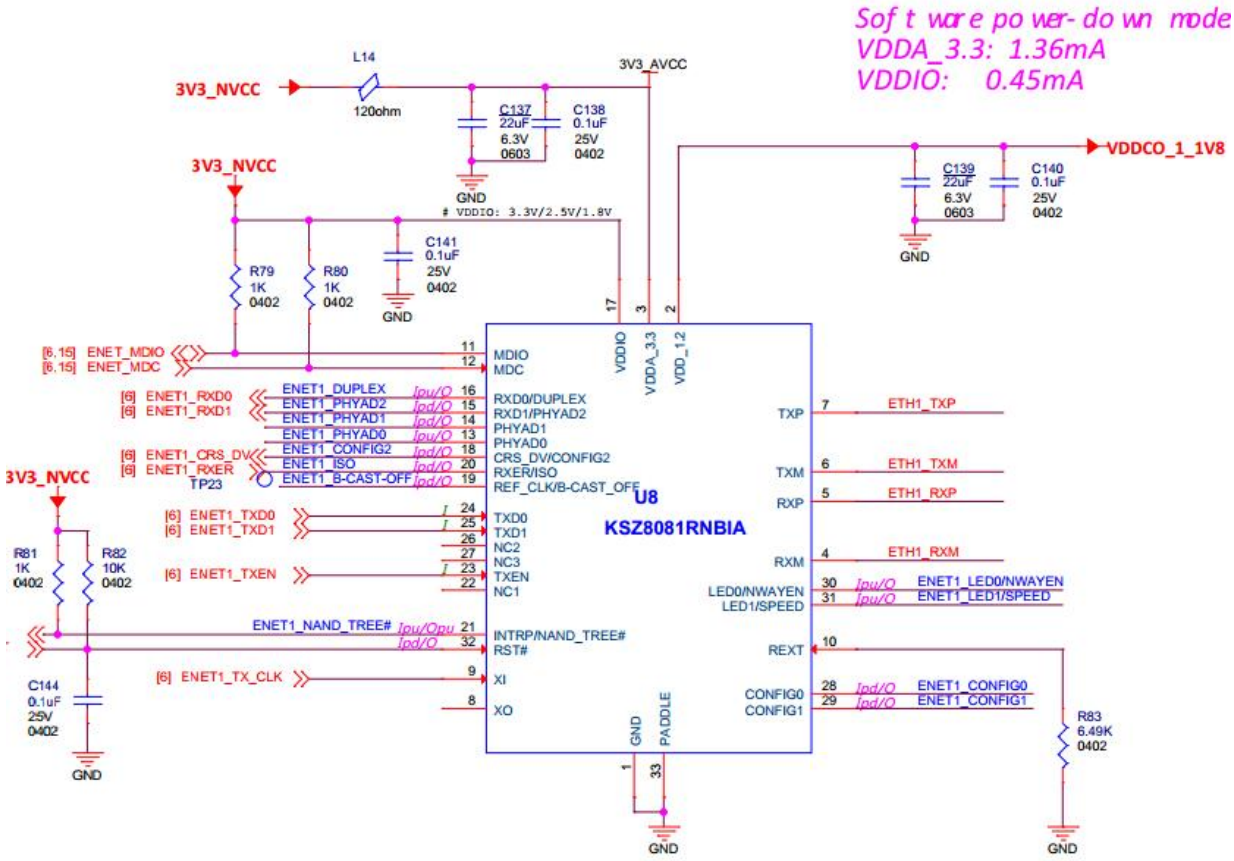
1.2.3 Ethernet Interface

SBC-EC9100 provides a complete 100M Ethernet interface, while also providing one way with the GPIO function of the RMII interface. 100M Ethernet interface using the PHY transceiver for KSZ8081 MICREL, the functional block diagram as follows:

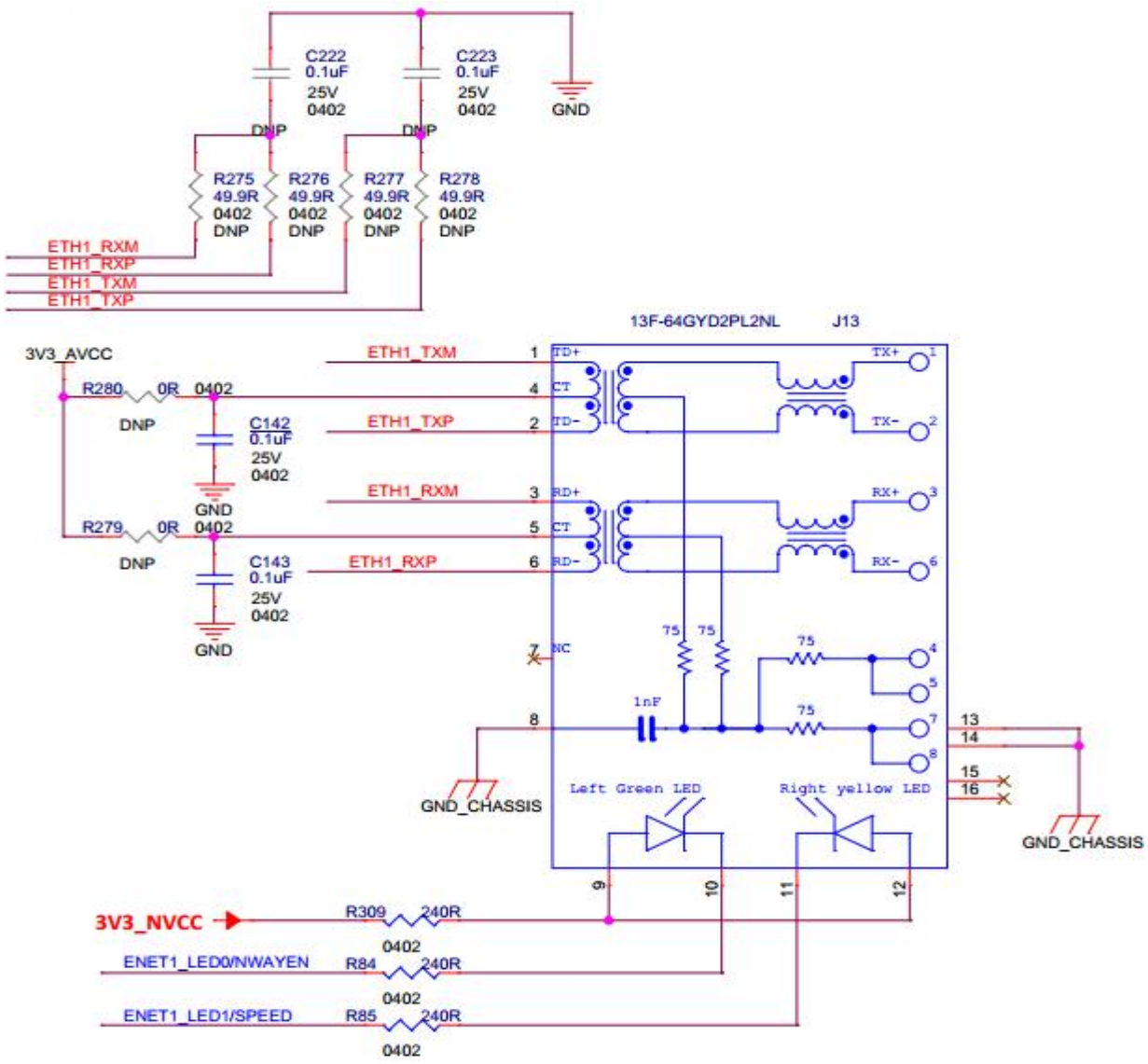
Diagram



The schemetic as follows:

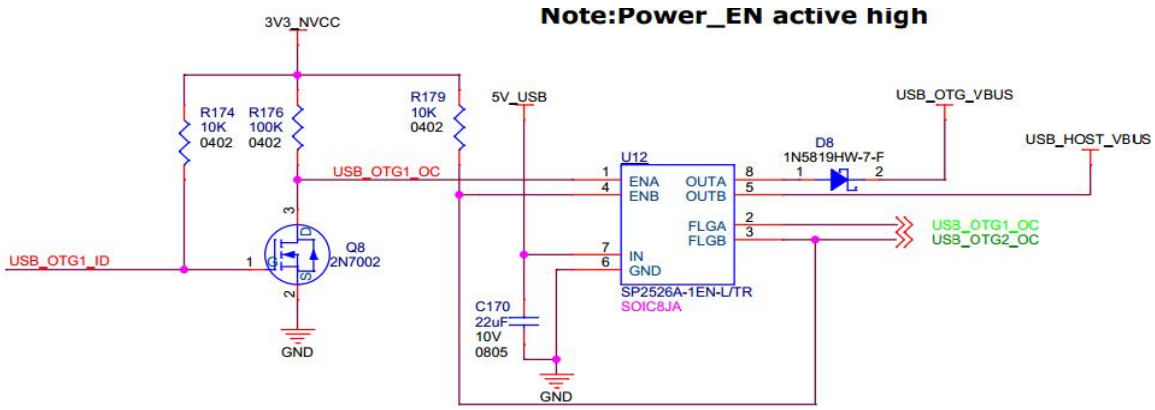


The Ethernet interface section as follows:



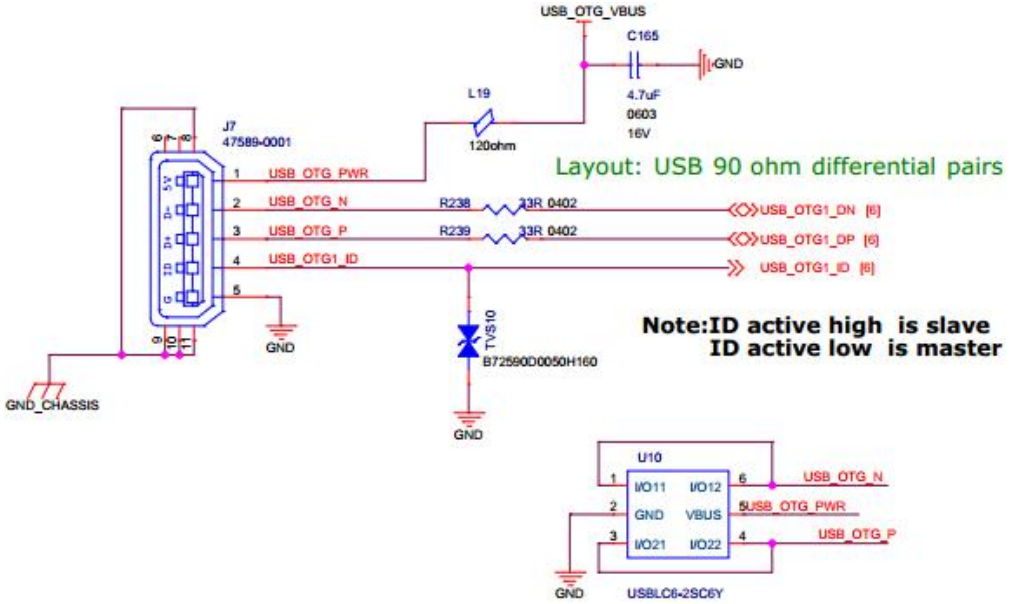
1.2.4 USB Interface

SBC-EC9100 provides one way 2.0 standard USB OTG and one way 2.0 standard USB Host, and using a SP2526 management USB power.



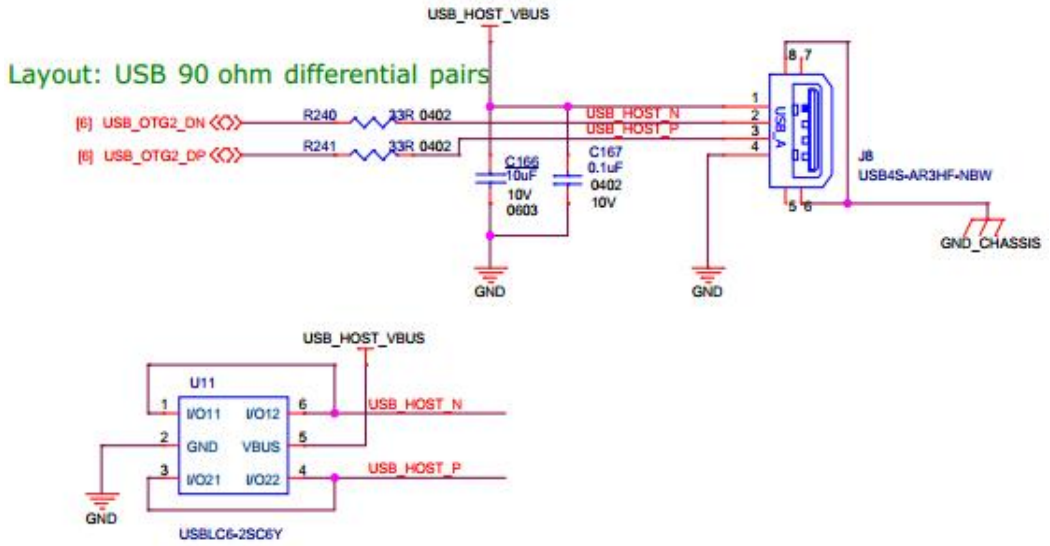
◆OTG USB

USB OTG interface using the standard USB AB Micro interface (receptacle Miro-AB), the principle as follows:



◆Host USB

USB Host interface using the standard A USB interface (receptacle USB-A), the principle as follows:



1.2.5 LCD &Touch Screen Controller

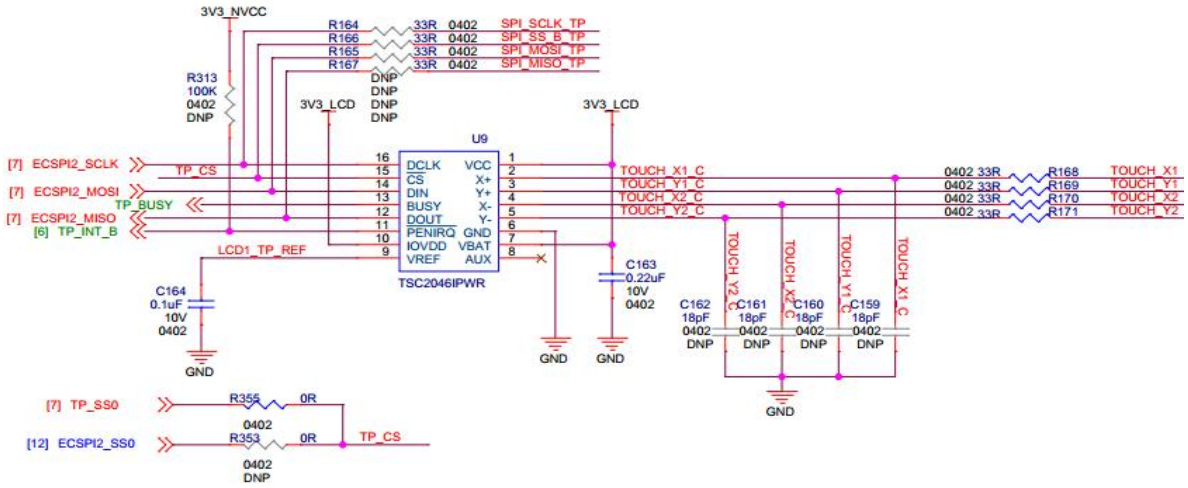
Based on the positioning of design, SBC-EC9100 does not provide a powerful video display function, only to provide a 24bit LCD HDMI display interface, for the basic LVDS. Output interface using the 50pin FPC flat cable seat, IO level for 3.3V and support the company's LCD8000-43T (4.3 inch screen) and LCD8000-70T (7 inch screen). LCD interface pin signal is defined as follows (a fixed pin of the connector in the table):

Table1-1 LCD display

LCD Display: J5			
Pin	Signal Description	Device	Signal Type
1	DSS_D0		
2	DSS_D1		
3	DSS_D2		
4	DSS_D3		Data
5	DSS_D4		Blue
6	DSS_D5		
7	DSS_D6		
8	DSS_D7		
9	GND		Ground
10	DSS_D8		
11	DSS_D9		
12	DSS_D10		Data
13	DSS_D11		Green
14	DSS_D12		
15	DSS_D13		

LCD Display: J5			
16	DSS_D14		
17	DSS_D15		
18	GND		Ground
19	DSS_D16		Data Red
20	DSS_D17		
21	DSS_D18		
22	DSS_D19		
23	DSS_D20		
24	DSS_D21		
25	DSS_D22		
26	DSS_D23		
27	GND		Ground
28	DSS_DEN		Data Sync
29	DSS_HSYNC		
30	DSS_VSYNC		
31	GND		Ground
32	DSS_PCLK		Clock
33	GND		Ground
34	TOUCH_X+		Touch Panel
35	TOUCH_X-		
36	TOUCH_Y+		
37	TOUCH_Y-		
38	SPI0_CLK		SPI
39	SPI0_MOSI		
40	SPI0_MISO		
41	SPI0_CSn		
42	LCD_I2C_SCL		I2C
43	LCD_I2C_SDA		
44	GND		Ground
45	3.3V_LCD_VDD		Power 3.3V
46	3.3V_LCD_VDD		
47	5V_LCD_VDD		Power 5V
48	5V_LCD_VDD		
49	LCD_RESETn		Reset
50	LCD_PWM		Control
51	GND		Ground
52	GND		

About Touch functions of SBC-EC9100, subject to resource constraints, using SPI interface to complete the touch screen function instead of CPU comes with TSC functional module, using TI's TSC2016 connection resistance touch screen by default as bellows:.



If using external LCD screen, will be need to select the right singnal from R164~R167,and it be connected to FPC connector(J5).

1.2.6 CAMERA

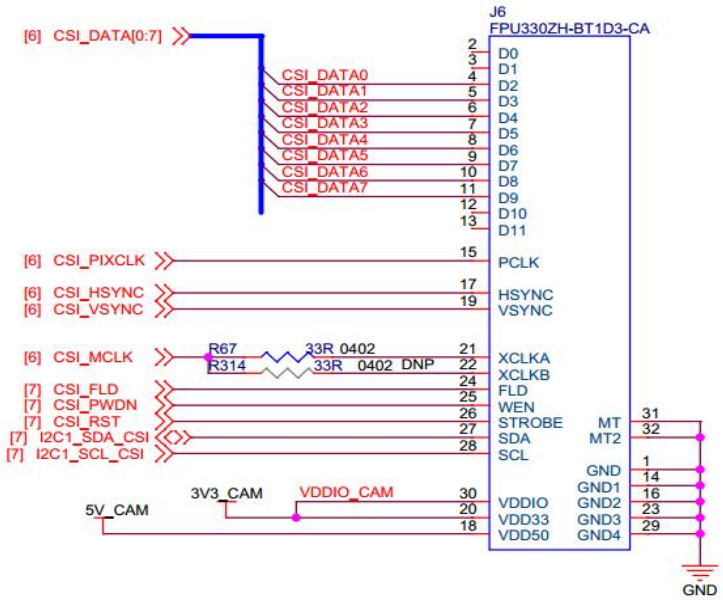
The J6 of SBC-EC9100 is the FPC connector to be used to support the highest 12 digit digital camera input. The voltage level is 3.3V. The following table is the FPC connector J6 signal pin definition table:

Table1-1 Camera

Camera(J6)			
Pin	Signal Description	Device	Signal Type
1	GND		Ground
2	CAM_D0		Data
3	CAM_D1		
4	CAM_D2		
5	CAM_D3		
6	CAM_D4		
7	CAM_D5		
8	CAM_D6		
9	CAM_D7		
10	CAM_D8		
11	CAM_D9		
12	CAM_D10		
13	CAM_D11		
14	GND		Ground
15	PCLK		Clock
16	GND		Ground
17	CAM_HS		SYNC
18	VDD_5V		Power 5V

Camera(J6)			
19	CAM_VS		SYNC
20	3.3V_CAMERA		Power 3.3V
21	CAM_CLK		Clock
22	CAM_CLK1		
23	GND		Ground
24	CAM_FLD		Status
25	CAM_WEN		
26	CAM_STROBE		
27	CAM_SDA		I2C
28	CAM_SCL		
29	GND		Ground
30	VDDIO		Power for IO
31	GND		Power
32	GND		

I.MX 6UltraLite processor only supports 8bit camera input, low starting from D2, the IO level for 3.3V, such as the right:



1.2.7 TF Card

SBC-EC9100 can be used for curing TF card interface, storage startup code and program system, using MMC interface.Its interface is defined as shown below:

Table 1-1 TF card interface

TF card connector: J2			
Pin	Signal Description	Device	Signal Type
1	MMC_DAT2		Data
2	MMC_DAT3		
3	MMC_CMD		Command
4	3.3V_VDD		Power 3.3V
5	MMC_CLK		Clock
6	GND		Ground
7	MMC_DAT0		Data
8	MMC_DAT1		
9	GND		Ground
10	MMC_CD		Command
11	GND		
12	GND		
13	GND		
14	NC		Fixed
15	NC		

1.2.8 Expand Interface

◆GPIO/PWM/ADC

In order to facilitate customer expansion, i.MX 6UltraLite GPIO SBC-EC9100 processor has not yet been used to lead to the 2 2*20PIN socket J9 and J10, which contains the ADC and PWM functions with GPIO. Extension socket spacing of 100 Mil, J10 socket signals definition of compatible RPI 2x20 expansion socket, and J9 signals defined mostly function for industrial use, in addition to CPU leads to the GPIO and part of other interface signal, such as RS-485 and can. Specific signal definition see table below

NOTE：1、Note the position of the extension socket on the PCB first fee

2、J10 signal definition is compatible with the basic RPI expansion socket, for RPI expansion in the same tube feet more functions and meet and compatible interface with I2C, SPI, UART, I2S and GPIO, while increasing the signal RMII interface.

3、The special function signals in the table are distinguished according to color, and

the signal with no fixed name is expressed by GPIO

4、The signal in the J9 interface has the potential to be multiplexed, does not guarantee that the same time can provide the defined signal, use, please check the schematic.

*5. Table with * characters of CLK_P and CLK_N for CCM_CLK LVDS signal。*

6. The signal in the table with a character in the configuration of the GPIO, please refer to the CPU manual on the introduction of the SNVS_TAMPER signal.

Extend interface (J9)									
CPU pad	Signal Name	Signal Description		Pin no.	Pin no.	Signal Description		Signal Name	CPU pad
		ALT 2	ALT 1			ALT 1	ALT 2		
	5V_PSU		5V	1	2	3.3V		3V3_NVCC	
	5V_PSU		5V	3	4	3.3V		3V3_NVCC	
	GND		GND	5	6	GND		GND	
M17	GPIO/ADC2	GPIO	ADC	7	8	ADC	GPIO	GPIO/ADC1	M16
		NC		9	10		NC		
	GND		GND	11	12	GND		GND	
D5	NAND_WP	GPIO	QSPI_CLK	13	14	QSPI_CS	GPIO	NAND_DQS	E5
A3	NAND_READY	GPIO	QSPI_D0	15	16	QSPI_D2	GPIO	NAND_CE1	B5
C5	NAND_CE0	GPIO	QSPI_D1	17	18	QSPI_D3	GPIO	NAND_CLE	A4
P8	POR_B		RST_B	19	20	TXD2	GPIO	UART2_TXD	J17
N17	GPIO/PWM1	GPIO	PWM	21	22	RXD2	GPIO	UART2_RXD	J16
M15	GPIO/PWM2	GPIO	PWM	23	24		NC		
		NC		25	26		NC		
U10	BOOT_MODE1		BOOT_M1	27	28		NC		
K17	ENET_MDIO	GPIO	ETH_MDIO	29	30	ETH_MDC	GPIO	ENET_MDC	L16
	GND		GND	31	32	GND		GND	
H15	CAN1_TX		CAN1_H	33	34	CAN2_H		UART2_RTS	H14
G14	CAN1_RX		CAN1_L	35	36	CAN2_L		UART2_CTS	J15
	GND		GND	37	38	GND		GND	
K16	UART1_RXD		RS485_A	39	40	RS485_B		UART1_TXD	K14

Extend interface (J10)									
CPU pad	Signal Name	Signal Description		Pin no.	Pin no.	Signal Description		Signal Name	CPU pad
		ALT 2	ALT 1			ALT 1	ALT 2		
	3V3_NVCC		3.3V	1	2	5V		5V_PSU	
L17	I2C1_SDA	GPIO	SDA1	3	4	5V		5V_PSU	
L14	I2C1_SCL	GPIO	SCL1	5	6	GND		GND	
P9	SNVS_TAMPER4	GPIO	GPCLK0①	7	8	TXD	GPIO	UART3_TXD	H17
	GND		GND	9	10	RXD	GPIO	UART3_RXD	H16
A15	ENET2_TXD0	GPIO	RMII_TXD0	11	12	PCMCLK	GPIO	JTAG_TDI	N16
A16	ENET2_TXD1	GPIO	RMII_TXD1	13	14	GND		GND	
P10	SNVS_TAMPER3		GPIO①	15	16	GPIO		BOOT_MODE0	T10

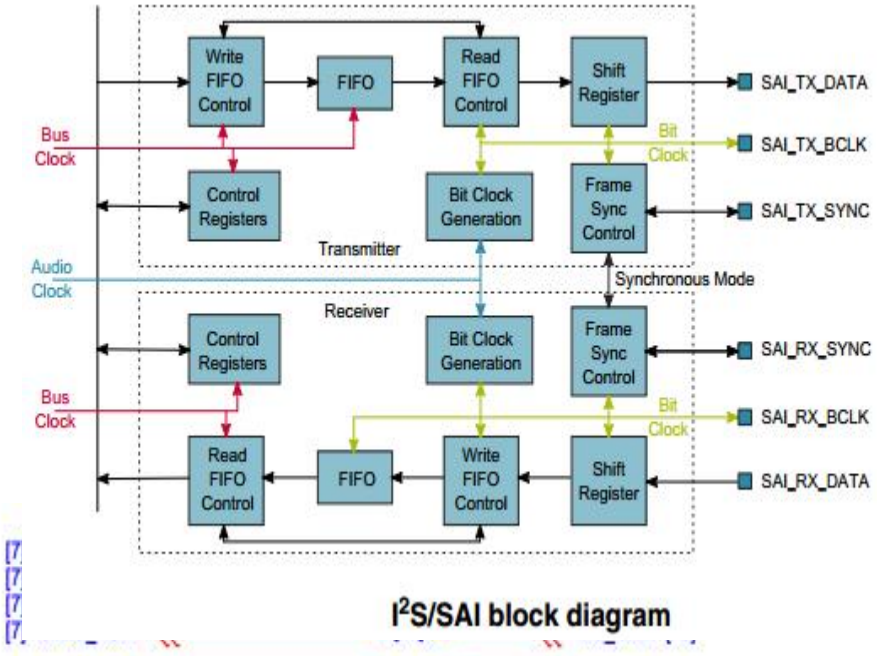
Extend interface (J10)									
	3V3_NVCC		3.3V	17	18	RMII_TXEN	GPIO	ENET2_TXEN	B15
H14	UART2_RTS	GPIO	MOSI	19	20	GND		GND	
J15	UART2_CTS	GPIO	MISO	21	22	RMII_TCLK	GPIO	ENET2_TX_CLK	D17
J16	UART2_RXD	GPIO	SCLK	23	24	SS0	GPIO	UART2_TXD	J17
	GND		GND	25	26	GPIO		JTAG_MOD	P15
P16	CLK1_N		CLK1_N*	27	28	GPIO	GPIO	JTAG_TMS	N16
C17	ENET2_RXD0	GPIO	RMII_RXD0	29	30	GND		GND	
C17	ENET2_RXD1	GPIO	RMII_RXD1	31	32	GPIO		NAND_ALE	
P17	CLK1_P		CLK1_P*	33	34	GND		GND	
N15	JTAG_TDO	GPIO	PCMFS	35	36	RMII_RXDV	GPIO	ENET2_CRS_DV	B17
D16	ENET2_RXER	GPIO	RMII_RXER	37	38	PCMDIN	GPIO	JTAG_nTRST	N14
	GND		GND	39	40	PCMDOUT	GPIO	JTAG_TCK	M14

The following is a description of the function signal of the expansion seat

◆I2S

i.MX 6UltraLite processor synchronous audio interface (SAI) to support the full duplex serial interface, such as I2S, AC97, TDM, etc..

The extend interface of SBC-EC9100 provide a I2S interface, easy to connect the audio function, I2S signal connect wth others by J10 interface, compatible with the extension of the Rpi definition the socket



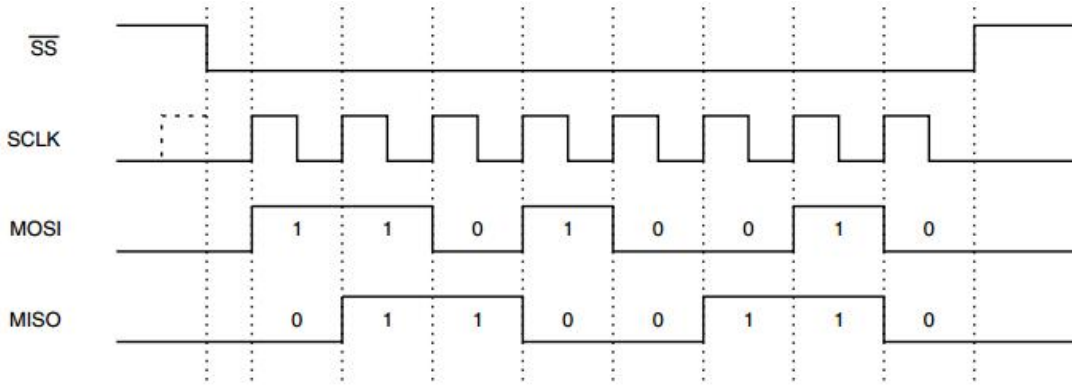
I²S/SAI block diagram

◆SPI & QSPI

i.MX 6UltraLite processor provide multiple SPI & QSPI interface, in addition to the internal use of some resources, but also to provide a 1 way SPI & QSPI to the extended interface. SPI signal connection socket on the J10 extensions compatible RPI signal, but need to pay attention to, due to resource constraints, the SPI signals is J9 socket Uart2 & can2 multiplexing, that if you

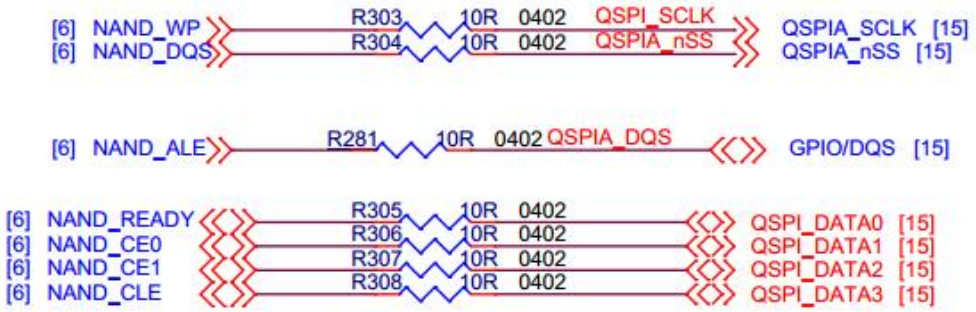
choose to use the SPI functions, J9 socket UART and can2 can not be used. Similarly, if you choose to use CAN2&Uart2 J9 socket, J10 socket SPI cannot use too. The selection method and schematic diagram are introduced in the 2.2.2 chapter.

SPI timing diagram as follows:



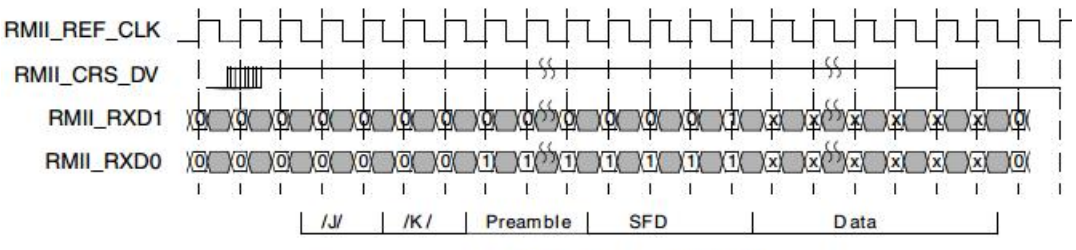
Typical SPI Burst (8-bit Transfer)

QSPI signal is connected to the J9 socket, QSPI signal and FLASH NAND signal multiplexing, the schematic as follows:

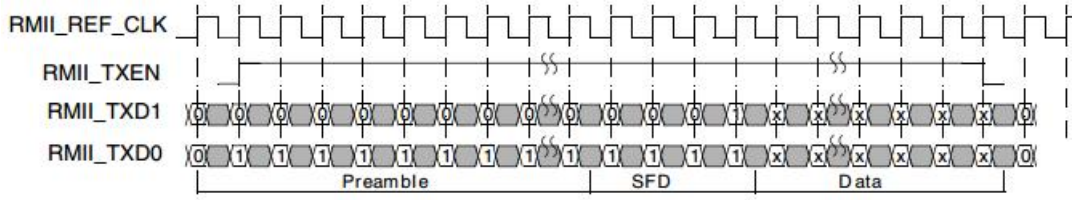


◆RMII

SBC-EC9100 not only boardload one 10M/100M Ethernet, but also can be extended to the J10 socket and to get a complete function of the RMII signal

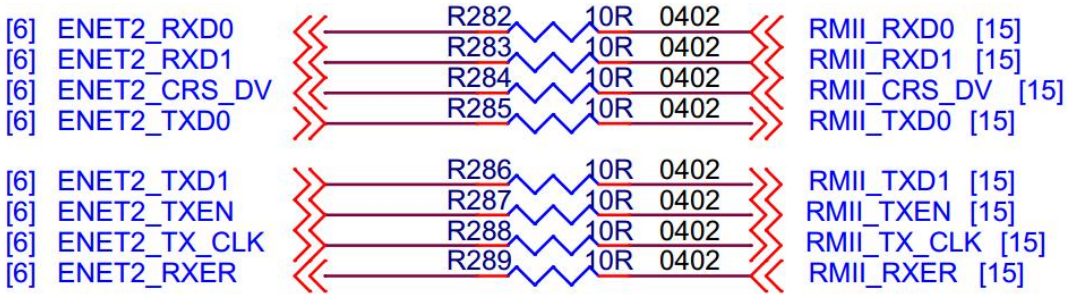


RMII receive operation



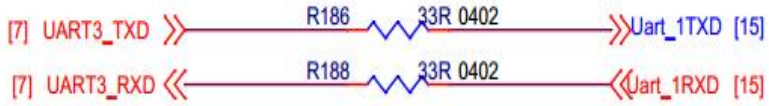
RMII transmit operation

The schemetic design as bellows:

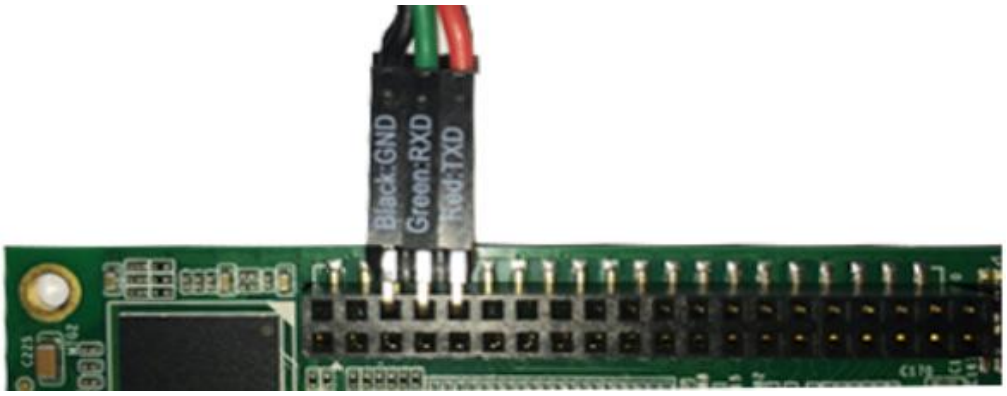


◆Uart

SBC-EC9100 expansion J9 and J10 socket have Uart signal output, both TTL level. One of the Uart J10 default for the debug serial port, and Rpi socket compatible with the debug information obtained from here. Connect the cable to recommend the use of our company's USB to the serial port line Uart8000-U, debug serial connection as shown below:



Debug



Extended socket J9 also provides a TTL level of the serial port, as shown below:

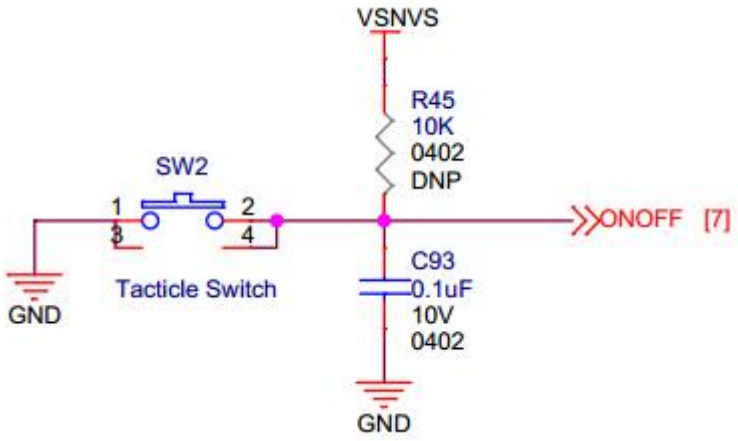
1.2.9 Button

◆Reset Button

SBC-EC9100 board hardware reset button SW1, you can manually press SW1 to reset the system, the circuit diagram in the reset circuit section is introduced.

◆ON/OFF Buttom

SBC-EC9100 besides the reset button, but also there is the design of a power ON/OFF SW2 button, when the system is connected to the external power supply, the default state is ON, that is, when the power is not pressed the ON/OFF button to boot. When you need to turn off the power, press the ON/OFF button 5 seconds or more, the system power off, the extension socket on the 3.3V output is also closed, +5V power is not affected, if you need to disconnect the +5V output need to unplug the DC-Jack plug. Need to re open the power, press the ON/OFF button for more than 2 seconds, the power will be open again. The key schematic is as follows:



1.2.10 LED

The SBC-EC9100 board provided 3 LED indicator lights: the power indicator, the overvoltage indicator, and the system operation indicator. When the external input DC 5V power is normal, the green power indicator D4 lights; when the external power supply more than 5.6v. SBC-EC9100 into overvoltage protection state, then close any power output, overvoltage red indicator light D1; when the input power supply is normal, system successfully started, run green indicating D9 flicker. Green running light is controlled by the CPU output, so it can also be provided to the user to use programming.

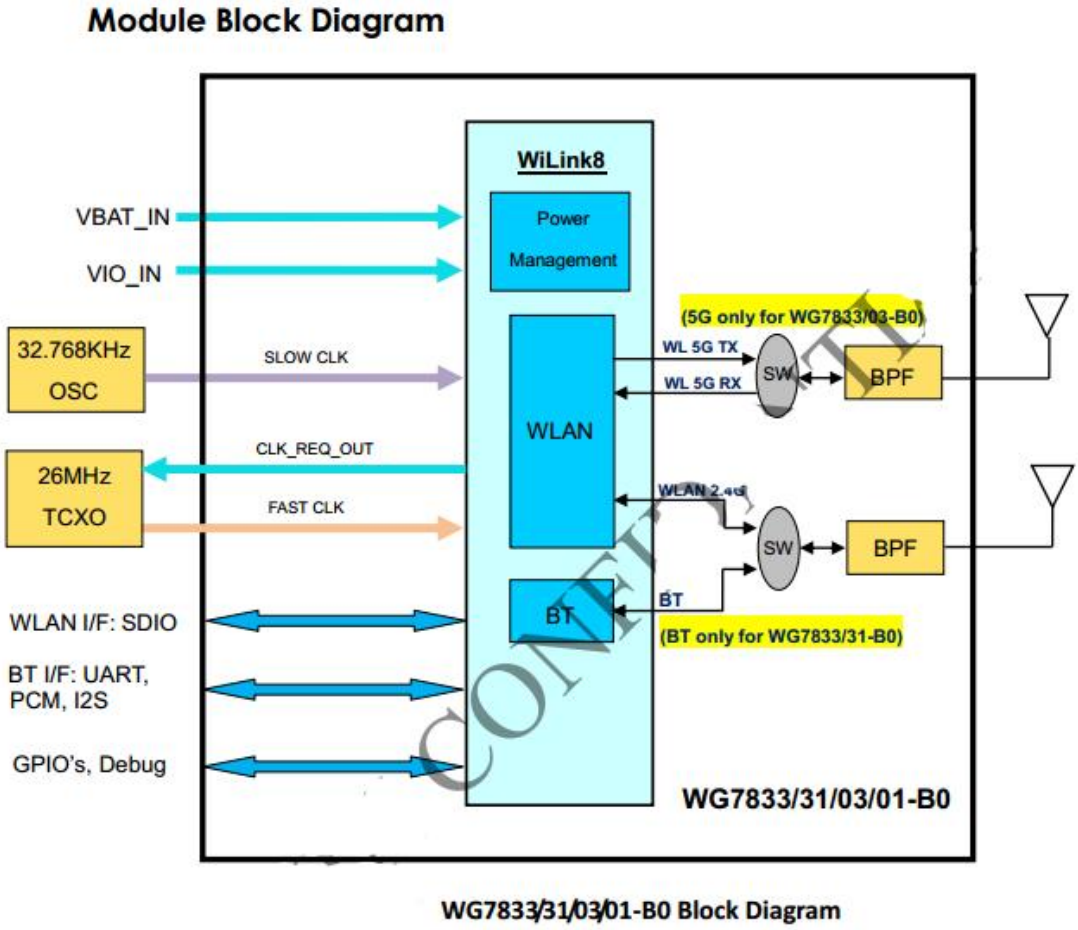
The following table indicates the status of the LED of the running indicator:

Table 1-1 LED status

LED Ref	LED Function	Signal Name	CPU Pad（BGA 14 x 14 mm）
D9	System RUN	UART_RTS	J14

1.2.11 Wifi

SBC-EC9100 board set aside an industrial grade BLE & Wifi module, the function block diagram as follows:



WG7833/31/03/01-B0 Block Diagram

◆WIFI Parameter

- Integrated 2.4 & 5G GHz Power Amplifier (PA) for WLAN solution
- WLAN Baseband Processor and RF transceiver Supporting IEEE Std 802.11b/g/n
- WLAN 2.4GHz SISO (20/40 MHz channels)
- 2.4-GHz MRC Support for Extended Range

- Baseband Processor
  - ► IEEE Std 802.11a/b/g/n data rates and IEEE Std 802.11n data rates with 20 or 40 MHz SISO.
- Fully calibrated system. Production calibration not required.
- Medium Access Controller (MAC)
  - ► Embedded ARM™ Central Processing Unit (CPU)
  - ► Hardware-Based Encryption/Decryption using 64-, 128-, and 256-Bit WEP, TKIP or AES Keys,
  - ►Supports requirements for Wi-Fi Protected Access (WPA and WPA2.0) and IEEE Std 802.11i [includes hardware-accelerated Advanced Encryption Standard (AES)]
  - ►Designed to work with IEEE Std 802.1x
- IEEE Std 802.11d,e,h,i,k,r PICS compliant.
- New advanced co-existence scheme with BT/BLE/ANT.
- 2.4 GHz Radio
  - ► Internal LNA and PA
  - ►Supports: IEEE Std 802.11a, 802.11b, 802.11g and 802.11n
- Supports 4 bit SDIO host interface, including high speed (HS) and V3 modes.

◆Bluetooth Parameter

- Supports Bluetooth 4.0 as well as CSA2
- Includes concurrent operation and built -in coexisting and prioritization handling of Bluetooth, BLE, ANT, audio processing and WLAN
- Dedicated Audio processor supporting on chip SBC encoding + A2DP:
  - ► Assisted A2DP (A3DP) support - SBC encoding implemented internally
  - ►Assisted WB-Speech (AWBS) support - modified SBC codec implemented internally

Technical Support and Warranty

Technical Support

Embest Technology provides its product with one-year free technical support including:

- Providing software and hardware resources related to the embedded products of Embest Technology;
- Helping customers properly compile and run the source code provided by Embest Technology;
- Providing technical support service if the embedded hardware products do not function properly under the circumstances that customers operate according to the instructions in the documents provided by Embest Technology;
- Helping customers troubleshoot the products.

The following conditions will not be covered by our technical support service. We will take appropriate measures accordingly:

- Customers encounter issues related to software or hardware during their development process;
- Customers encounter issues caused by any unauthorized alter to the embedded operating system;
- Customers encounter issues related to their own applications
- Customers encounter issues caused by any unauthorized alter to the source code provided by Embest Technology.

Warranty Conditions

1） 12-month free warranty on the PCB under normal conditions of use since the sales of the product;

2） The following conditions are not covered by free services; Embest Technology will charge accordingly:

- Customers fail to provide valid purchase vouchers or the product identification tag is damaged, unreadable, altered or inconsistent with the products;
- Not according to the user's manual operation causes damage to the product;
- Products are damaged in appearance or function caused by natural disasters (flood, fire, earthquake, lightning strike or typhoon) or natural aging of components or other force majeure;

- Products are damaged in appearance or function caused by power failure, external forces, water, animals or foreign materials;
- Products malfunction caused by disassembly or alter of components by customers or, products disassembled or repaired by persons or organizations unauthorized by Embest Technology, or altered in factory specifications, or configured or expanded with the components that are not provided or recognized by Embest Technology and the resulted damage in appearance or function;
- Product failures caused by the software or system installed by customers or inappropriate settings of software or computer viruses;;
- Products purchased from unauthorized sales;
- Warranty (including verbal and written) that is not made by Embest Technology and not included in the scope of our warranty should be fulfilled by the party who committed. Embest Technology has no any responsibility;

3） Within the period of warranty, the freight for sending products from customers to Embest Technology should be paid by customers; the freight from Embest to customers should be paid by us. The freight in any direction occurs after warranty period should be paid by customers;

4） Please contact technical support if there is any repair request.

Note：

🕮 Embest Technology will not take any responsibility on the products sent back without the permission of the company.

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