

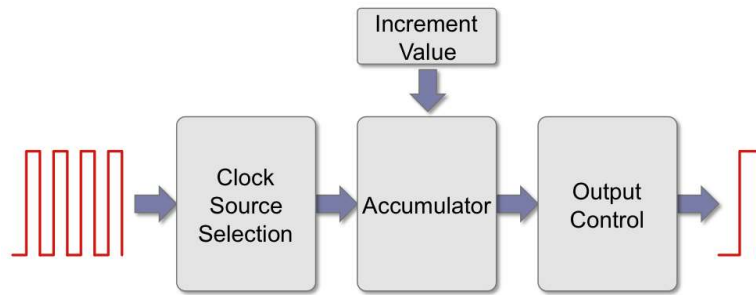
Oscilador controlado numéricamente

El módulo **Oscilador controlado numéricamente (NCOx)** es un temporizador que utiliza el desbordamiento de un acumulador para crear una señal de salida. El desbordamiento del acumulador se controla mediante un valor de incremento ajustable en lugar de un solo pulso de reloj o un incremento posterior al escalador. Esto ofrece una ventaja sobre un simple contador accionado por temporizador en el sentido de que la resolución de la división no varía con el valor del divisor del preescalador/postescalador algo limitado. El NCOx es más útil para aplicaciones que requieren precisión de frecuencia y resolución fina en un ciclo de trabajo fijo.

Las características del NCOx incluyen:

- función de incremento de 16 bits
- Modo de ciclo de trabajo fijo (FDC)
- Modo de frecuencia de pulso (PF)
- Control de ancho de pulso de salida
- Múltiples fuentes de entrada de reloj
- Control de polaridad de salida
- capacidad de interrupción

El NCOx opera agregando repetidamente un valor fijo a un acumulador. Las adiciones ocurren a la velocidad del reloj de entrada. El acumulador se desbordará con un acarreo periódicamente, que es la salida de NCOx sin procesar. Esto reduce efectivamente el reloj de entrada en la proporción del valor agregado al valor máximo del acumulador.



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La salida NCOx se puede modificar aún más estirando el pulso o alternando un flip-flop. La salida NCOx modificada se distribuye internamente a otros periféricos y, opcionalmente, se envía a un pin de E/S. El desbordamiento del acumulador también puede generar una interrupción. El período NCOx cambia en pasos discretos para crear una frecuencia promedio. Esta salida depende de la capacidad del circuito receptor (es decir, CWG o circuito convertidor resonante externo) para promediar la salida NCOx para reducir la incertidumbre.

The overflow of the NCO module is based on the formula below:

The NCO output is based on the formula below

$$\text{Accumulator Overflow Rate} = \frac{\text{Accumulator Overflow Value}}{\text{Input Clock Frequency} \times \text{Increment Value}}$$

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NCO Video Tutorial

This video introduces the Numerically Controlled Oscillator (NCO) for Microchip 8-bit MCU devices and shows how to use it.



Microchip Self-Paced Training – Numerically Controlled Oscillat...



NCO Modes

The NCO module can output a signal in one of the two modes.

NCO has Two modes of operation:

- Fixed 50% duty cycle (FDC) 
- Pulse Frequency Modulation (PFM) 

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The NCOCON register controls the mode setting for the NCO.

NCOxCON Register

NxEN	NxOE	NxOUT	NxPOL	-	-	-	NxPFM
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NxPFM NCOx Pulse Frequency Mode Bit

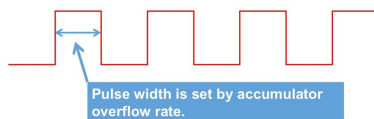
- 1 – NCOx operates in Pulse Frequency Mode
- 0 – NCOx operates in Fixed Duty Cycle Mode

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Fixed Duty Cycle

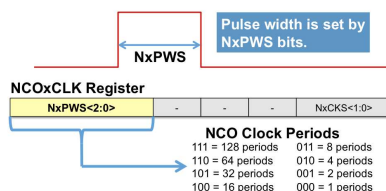
The Fixed Duty Cycle mode toggles the output on every accumulator overflow. As long as the adder value and clock don't change, this will result in a 50% duty cycle output.



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Pulse Frequency Modulation

The Pulse Frequency Modulation mode will trigger a pulse on every accumulator overflow for a period set by three bits in the NCOCON register.

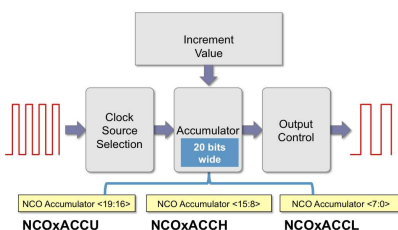


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Accumulator

The accumulator is a 20-bit register with a maximum value of 1,048,575. Read and write access to the accumulator is available through three registers:

- NCOxACCL
- NCOxACCH
- NCOxACCU



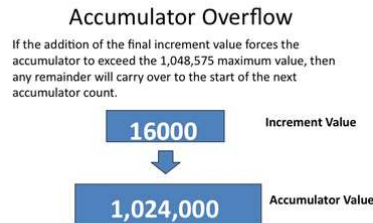
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When the accumulator overflows, the output of the NCO module will change state.

Adder

The NCOx adder is a full adder, which operates independently from the system clock. It adds the value of the increment value to the accumulator on each NCO clock pulse. The adder takes the value in the accumulator and then adds the increment value. The result is placed back in the accumulator. The accumulator value will roll over and any value beyond the 1,048,575 will get placed as the starting value in the accumulator.

This can be reset if desired by writing a zero to the accumulator. This is typically done within the interrupt service routine if that is enabled on the NCO module.

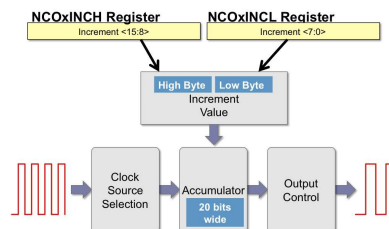


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Increment Registers

The increment value is stored in two 8-bit registers making up a 16-bit increment value. The lower 8-bits are in the NCOxINCL register and the upper 8-bits are in the NCOxINCH register.

- NCOxINCL
- NCOxINCH



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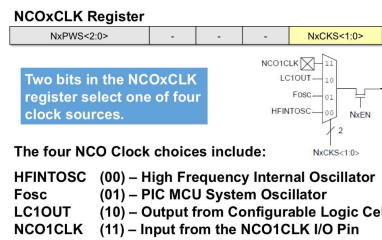
Both of the registers are readable and writeable. The increment registers are double-buffered to allow for value changes to be made without first disabling the NCOx module. The buffer loads are immediate when the module is disabled. Writing to the NCOxINCH register first is necessary because then the buffer is loaded synchronously with the NCOx operation after the write is executed on the NCOxINCL register.

Clock Sources

Clock sources available to the NCOx include:

- HFINTOSC
- F_{osc}
- LCxOUT
- CLKIN pin

The NCOx clock source is selected by configuring the NxCKS<2:0> bits in the NCOxCLK register.



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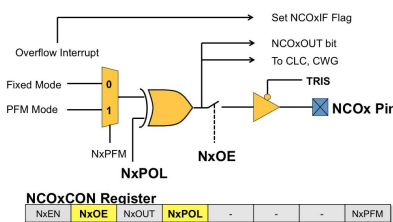
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The HFINTOSC selection will continue to run even if the device is put into sleep mode.

Output

The output of the NCO has several options that can be set in the NCOCON register.

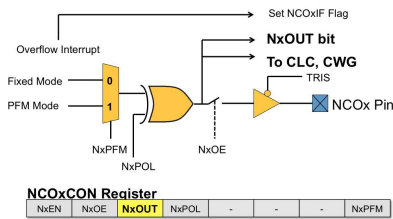
The output can be enabled or disabled (NxOE bit) and also inverted (NxPOL bit) by setting or clearing bits in the NCOCON register.



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The output can also be monitored in software by reading the state of the NxOUT bit in the NCOCON register.



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The NxEN bit can disable the whole NCO module. A '1' setting enables the module and a '0' setting disables it.

Interrupt

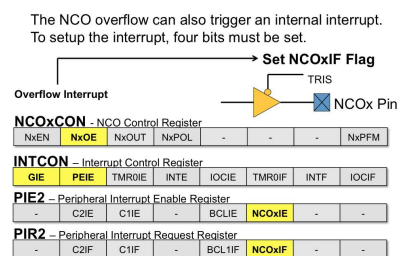
The NCO output can trigger an internal interrupt when the accumulator overflows. This is handled by three bits (GIE, PEIE, NCOxIE) in the set of registers shown below. This will allow the NCO to control software actions through the interrupt service routine in the application code while also outputting a signal to an I/O pin.

GIE is the Global Interrupt Enable bit.

PEIE is the Peripheral Interrupt Enable bit.

NCOxIE is the NCO Interrupt Enable bit. There can be multiple NCO modules. The "x" represents the NCO number.

The NCOxIF bit is the interrupt indicator flag. This can be monitored in the software to see if an interrupt has occurred. This needs to be cleared in the interrupt service routine or in the software routine that read the bit.



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