Generador de forma de onda complementaria (CWG)

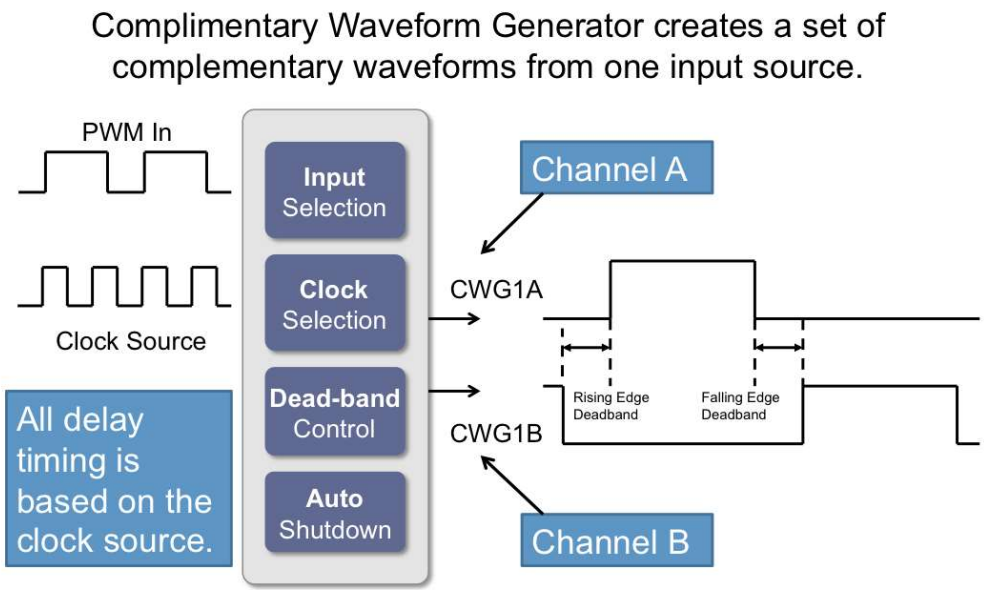
El generador de forma de onda complementaria (CWG) produce una forma de onda complementaria con el retardo de banda muerta a partir de una selección de fuentes de entrada.

El módulo CWG tiene las siguientes características:

- Control de fuente de reloj de banda muerta seleccionable
- Fuentes de entrada seleccionables
- Control de habilitación de salida
- Control de polaridad de salida
- Control de banda muerta con contadores independientes de banda muerta de flanco ascendente y descendente de 6 bits
- Control de apagado automático con:
    - Fuentes de apagado seleccionables
    - Habilitar reinicio automático
    - Control de anulación de pin de apagado automático

El CWG genera una forma de onda complementaria de dos salidas a partir de una de varias fuentes de entrada seleccionables. La transición de apagado a encendido de cada salida se puede retrasar con respecto a la transición de encendido a apagado de la otra salida, creando así un retraso de tiempo inmediato en el que no se activa ninguna salida. Esto se conoce como tiempo muerto o banda muerta y se trata en la sección a continuación titulada "Control de banda muerta".

Puede ser necesario protegerse contra la posibilidad de fallas en el circuito. En este caso, el variador activo puede terminarse antes de que la condición de falla cause daño. Esto se conoce como apagado automático y se cubre en la sección a continuación titulada "Control de apagado automático".



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El CWG requiere que se establezcan cinco secciones:

- Aporte
- Reloj
- banda muerta
- Cerrar
- Control de salida

Videotutorial de CWG

This video introduces the Complementary Waveform Generator (CWG) for Microchip 8-bit MCU devices and shows how to use it.

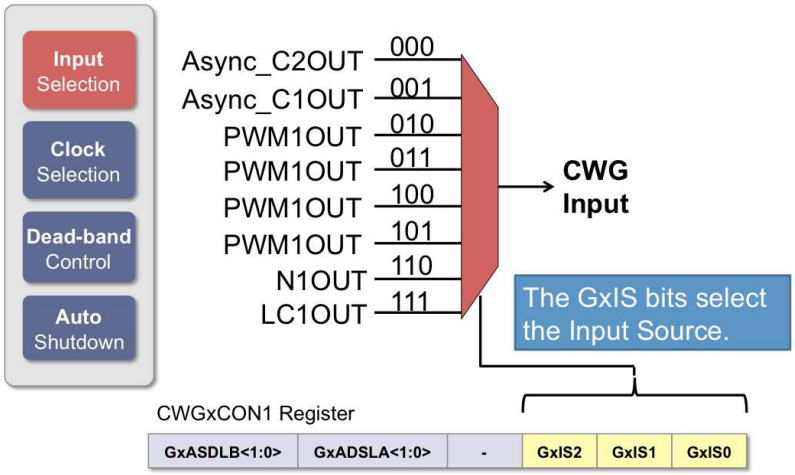
Input Source

The CWG offers several input sources to generate the complementary waveform. This may vary from device to device. The list below is from the PIC16F1507 device. The list includes:

• PWM1 (Pulse Width Modulated Output 1)
• PWM2 (Pulse Width Modulated Output 2)
• PWM3 (Pulse Width Modulated Output 3)
• PWM4 (Pulse Width Modulated Output 4)
• N1OUT (Numerically Controlled Oscillator Output)
• LC1OUT (Configurable Logic Cell Output)

The input source is selected using the GxIS<2:0> bits in the CWGxCON1 register.

Some devices also include the output from a comparator module as input to the CWG. It's best to refer to the data sheet for the device you are using for the updated list of selected input choices.



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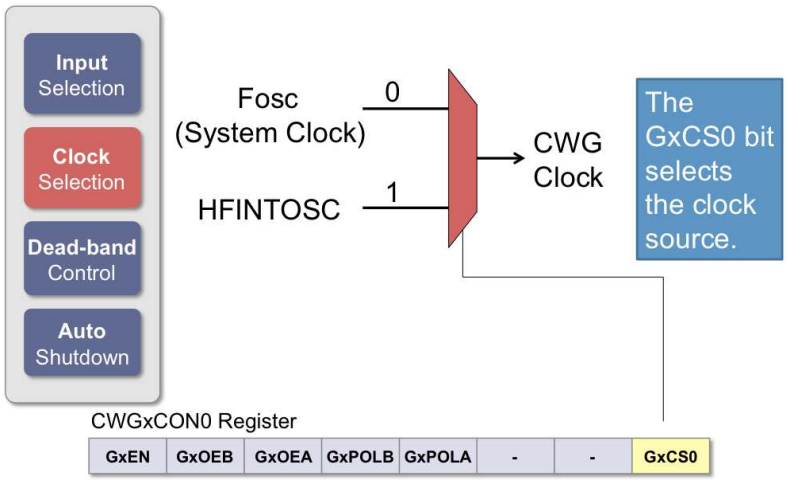
Clock Source

The CWG module allows for one of two clock sources to be selected:

- F_{OSC} (system clock)
- HFINTOSC (16 MHz only)

The clock sources are selected using the G1CS0 bit of the CWGxCON0 register.



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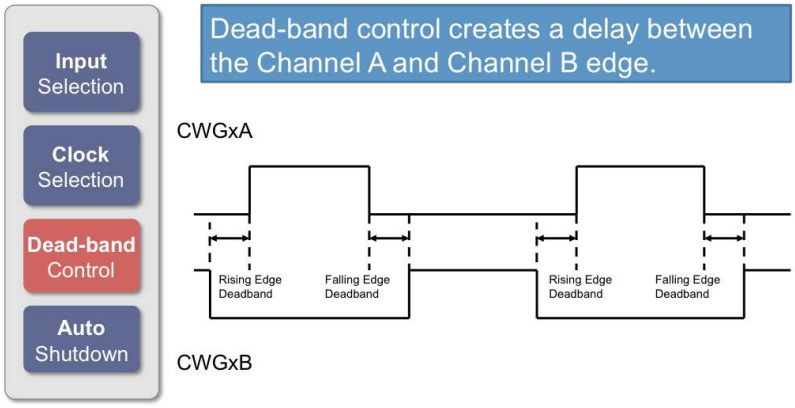
Dead-band Control

Dead-band control provides for non-overlapping output signals, to prevent shoot-through current in power switches. The CWG contains two 6-bit dead-band counters (CWGxDBR and CWGxDBF registers). One dead-band counter is used for the rising edge of the input source control while the other is used for the falling edge of the input source control.

Dead-band is timed by counting CWG clock periods from zero up to the value in the rising or falling dead-band counter registers.



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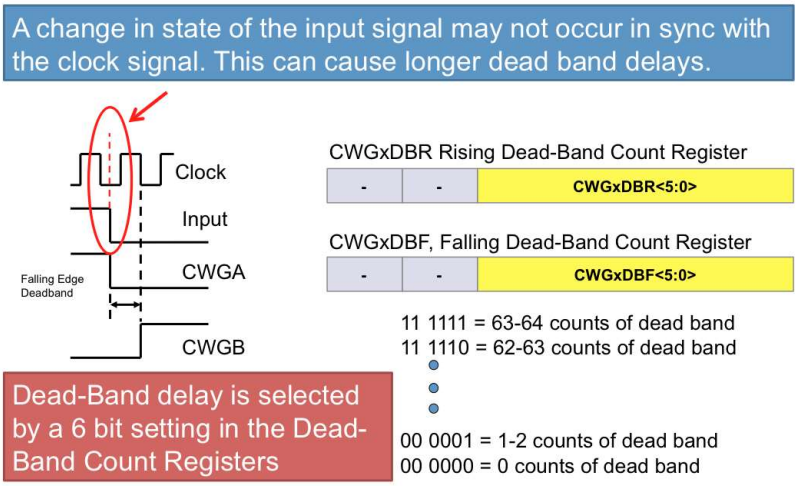
Rising Edge Control

The rising edge dead-band delays the turn-on of the CWGxA output from when the CWGxB output is turned off. The rising edge dead-band time starts when the rising edge of the input source signal goes true. When this happens, the CWGxB output is immediately turned off and the rising edge dead-band delay time starts. When the rising edge dead-band delay time is reached, the CWGxA output is turned on.

The CWGxDBR register sets the duration of the dead-band interval on the rising edge of the input source signal. This duration is from 0 to 64 counts of dead-band. Dead-band is always counted off the edge on the input source signal. A count of zero (0), indicates that no dead-band is present. If the input source signal is not present for enough time for the count to be completed, no output will be seen on the respective output.



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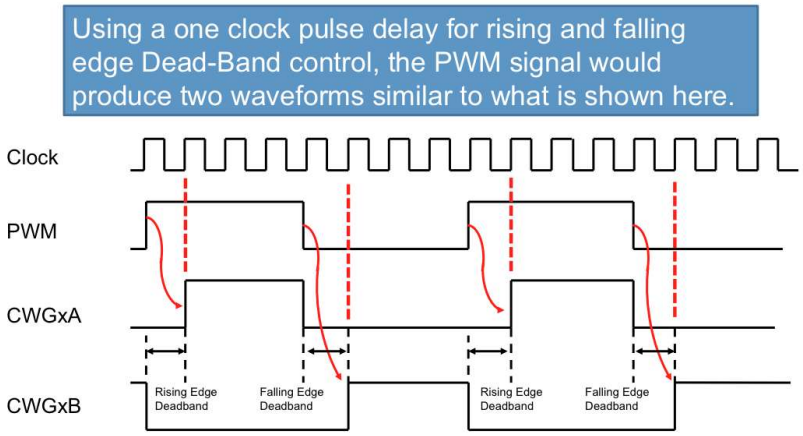
Falling Edge Control

The falling edge dead-band delays the turn-on of the CWGxB output from when the CWGxA output is turned off. The falling edge dead-band time starts when the falling edge of the input source goes true. When this happens, the CWGxA output is immediately turned off and the falling edge dead-band delay time starts. When the falling edge dead-band delay time is reached, the CWGxB output is turned on.

The CWGxDBF register sets the duration of the dead-band interval on the falling edge of the input source signal. This duration is from 0 to 64 counts of dead-band. Dead-band is always counted off the edge on the input source signal. A count of zero (0), indicates that no dead-band is present. If the input source signal is not present for enough time for the count to be completed, no output will be seen on the respective output.



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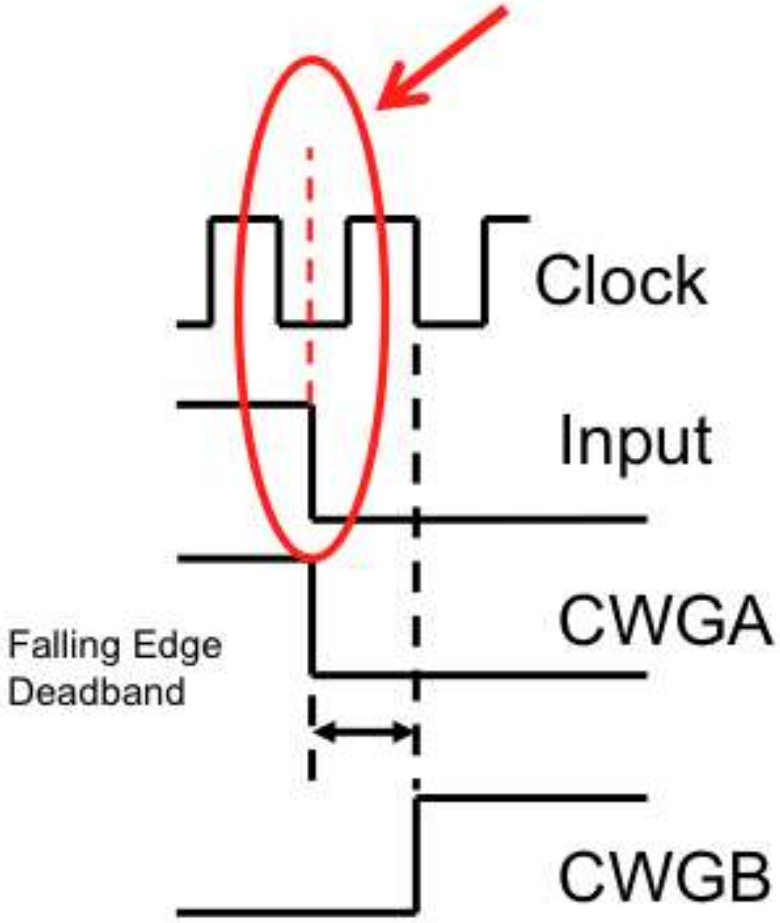
Dead-band Uncertainty

When the rising and falling edges of the input source trigger the dead-band counters, the input may be asynchronous to the clock input. This will create some uncertainty in the dead-band time delay. The maximum uncertainty is equal to one CWG clock period.



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Auto-shutdown Control

Auto-shutdown is a method to immediately override the CWG output levels with specific settings that allow for safe shutdown of the circuit. The shutdown state can be either cleared automatically or held until cleared by software.

The shutdown state can be entered by either of the following two methods:

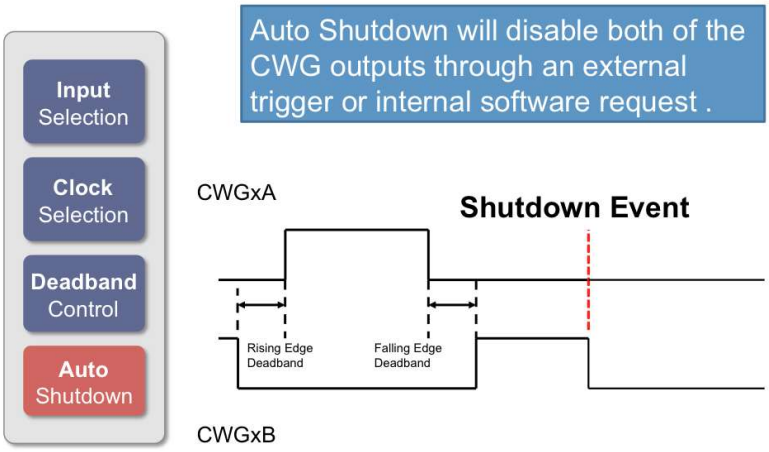
- Software generated
- External input

Software Generated

Setting the GxASE bit of the CWGxCON2 register will force the CWG into the shutdown state. When auto-restart is disabled, the shutdown state will persist as long as the GxASE bit is set. When auto-restart is enabled, the GxASE bit will clear automatically and resume operation on the next rising edge event.

External Input

External shutdown signals provide the fastest way to safely suspend CWG operation in the event of a fault condition. When any of the selected shutdown signals go active, the CWG outputs will immediately go to the selected override levels without software delay. Any combination of two shutdown signals can be selected to cause a shutdown condition. The shutdown signals offered may vary with the device being used but those shutdown sources are selected by the GxASDS0 and GxASDS1 bits of the CWGxCON2 register.



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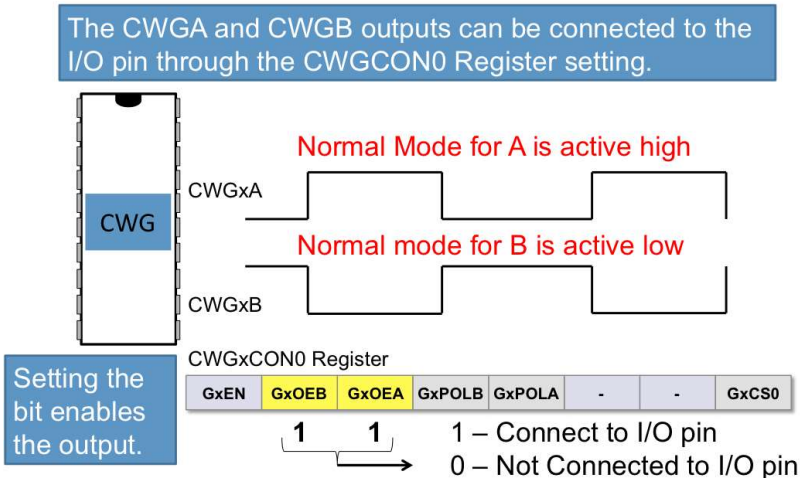
Output Control

Output Pin Enable

Each CWG output pin has an individual output pin enable control. The output enables are selected with the GxOEA and GxOEB bits of the CWGxCON0 register. When an output pin enable is cleared, the CWG has no connection to the output pin. When the output enable is set, the override value or active PWM waveform is applied to the pin per the internal port priority selection.

The CWG function can be completely disabled by clearing the GxEN pin in the CWGxCON0 register.



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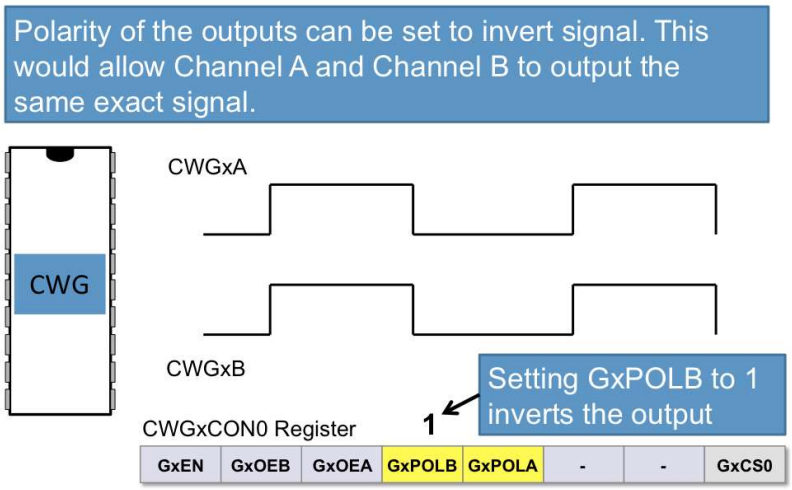
Polarity Control

The polarity of each CWG output can be selected independently. When the output polarity bit is set, the corresponding output is active high. Clearing the output polarity bit configures the corresponding output as active low. However, polarity does not affect override levels. Output polarity is selected with the GxPOLA and GxPOLB bits of the CWGxCON0 register.



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Operation During Sleep Mode

The CWG module operates independently from the system clock and will continue to run during Sleep, provided that the clock and input sources selected remain active. The High-Frequency Internal Oscillator (HFINTOSC) remains active during Sleep, provided that the CWG module is enabled, the input source is active, and the HFINTOSC is selected as the clock source, regardless of the system clock source selected.

In other words: if the HFINTOSC is simultaneously selected as the system clock and the CWG clock source, then when the CWG is enabled and the input source is active, the CPU will go idle during Sleep, but the CWG will continue to operate and the HFINTOSC will remain active. This will have a direct effect on the Sleep mode current.

CWG Example

Sometimes it is helpful to step through an example. Visit this CWG example (/8bit:cwgexample) to see step-by-step instructions for the CWG Module.