Celda lógica configurable

La celda lógica configurable (CLC) proporciona una lógica programable que opera fuera de las limitaciones de velocidad de ejecución del software. La celda lógica acepta hasta 16 señales de entrada y, mediante el uso de puertas configurables, reduce las 16 entradas en cuatro líneas lógicas que controlan una de las ocho funciones lógicas seleccionables de salida única.

Las fuentes de entrada son una combinación de lo siguiente:

- pines de E/S
- relojes internos
- Periféricos
- Bits de registro

La salida se puede dirigir internamente a los periféricos ya un pin de salida.

Las posibles configuraciones incluyen:

- Lógica Combinatoria
  - Y
  - NAND
  - Y-O
  - Y-O-INVERTIR
  - OR-XOR
  - O-XNOR
- Pestillos
  - RS
  - Reloj D con Set y Reset
  - D transparente con Set y Reset
  - JK cronometrado con reinicio

Videotutorial de CLC

Este video presenta la celda lógica configurable (CLC) para dispositivos MCU de 8 bits de Microchip y muestra cómo usarla.

Configuración de CLC

El periférico CLC tiene cuatro secciones que deben configurarse antes de poder usarse. Esto implica configurar ocho registros en su programa de software. Una vez que se configuran estos registros, el CLC funcionará independientemente del control del software hasta que los registros se cambien a través del software.

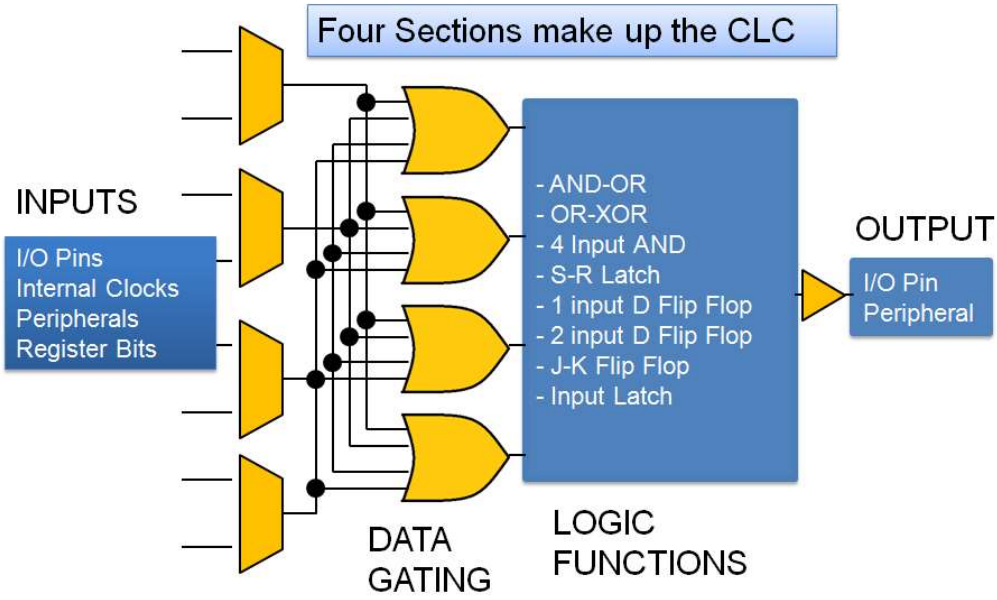
Incluyen:

- CLCxCON
- CLCxSEL0
- CLCxSEL1
- CLCxGLS0
- CLCxGLS1
- CLCxGLS2
- CLCxGLS3
- CLCxPOL

A **PIC®** device can have multiple CLCs so each CLC module has its own set of eight registers. The x in the register names above represent the CLC number (e.g., CLC1 uses the CLC1CON register).

To simplify the setup, the CLC can be broken down into four sections that need to be configured. They include:

- Inputs
- Data Gating
- Logic Function
- Output Setting



(/local--files/8bit:clc/clcsetup.png)

Inputs

Inputs can come from 8-16 different sources, depending on the PIC device, and from this list, up to four can be chosen to feed the data gating section.
They can include:

- I/O pins
- Internal clock outputs
- Peripherals outputs
- Register bits

The inputs are selected by bits in the CLCxSEL0 and CLCxSEL1 registers.

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Each input has an associated 3-bit code that is placed in the CLCxSEL registers to enable the input.

CLC 1 Input	Source
CLC1IN[0] CLC1IN[1]	CLC1IN0 PIN CLC1IN1 PIN
CLC1IN[2] CLC1IN[3]	SYNCC1OUT SYNCC2OUT
CLC1IN[4] CLC1IN[5]	Fosc TMR0IF
CLC1IN[6] CLC1IN[7]	TMR1IF TMR2 = PR2
CLC1IN[8] CLC1IN[9]	lc1_out lc2_out
CLC1IN[10] CLC1IN[11]	lc3_out lc4_out
CLC1IN[12] CLC1IN[13]	NCO1OUT HFINTOSC
CLC1IN[14] CLC1IN[15]	PWM3OUT PWM4OUT

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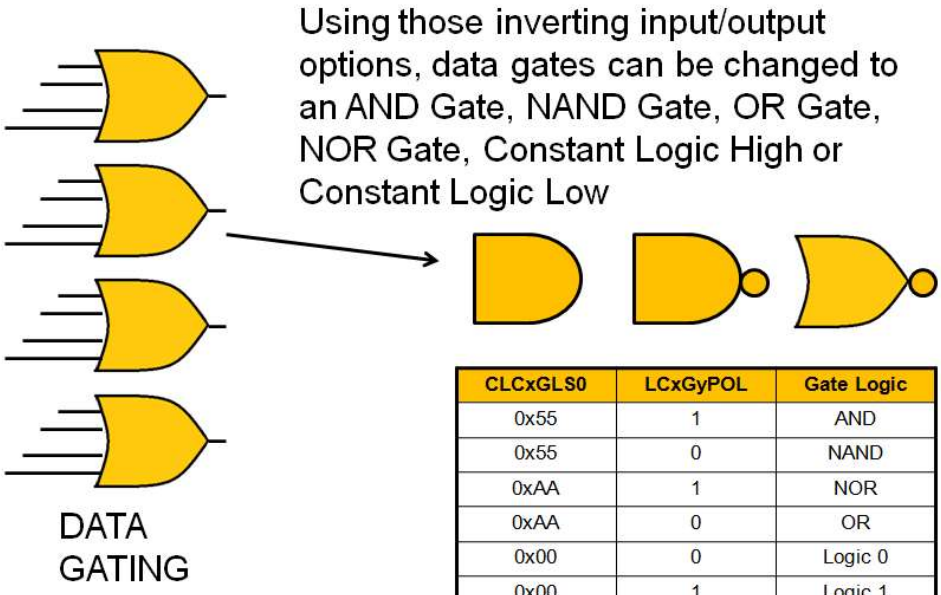
Data Gating

The Data Gating section has four logic gates that need to be set up. This requires five separate registers to be set up. They configure the inverted or non-inverted connection from the inputs that control the CLC peripheral. The five registers include:

- CLCxGLS0
- CLCxGLS1
- CLCxGLS2
- CLCxGLS3
- CLCxPOL

Each gate starts off as a base OR gate, but each input and output can be individually inverted or not inverted.
This allows AND, NAND, OR, and NOR gates to be created. The gates can also be set up to drive a constant 1 or 0 logic level.



CLCxGLS0	LCxGyPOL	Gate Logic
0x55	1	AND
0x55	0	NAND
0xAA	1	NOR
0xAA	0	OR
0x00	0	Logic 0
0x00	1	Logic 1

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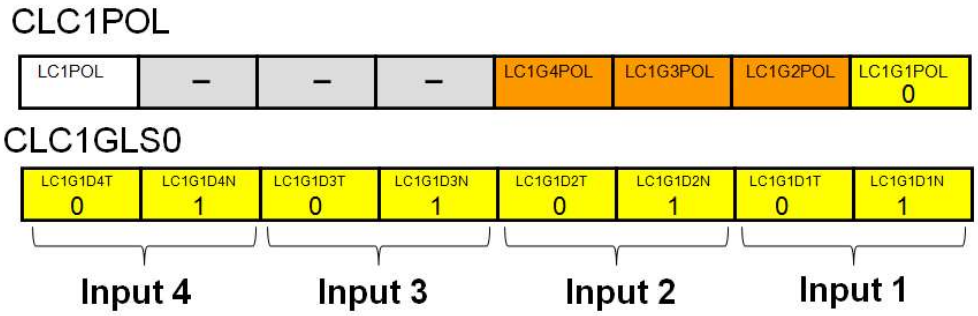
Each input to a data gate has a pair of bits in one of the CLCxGLSx registers. The two bits include a non-inverted (T) bit and an inverted (N) bit that needs to be set up. If the T bit is set, then the input is non-inverted. If the N bit is set, then the input is inverted. If both are set to zero, then the input is not connected to the gate.



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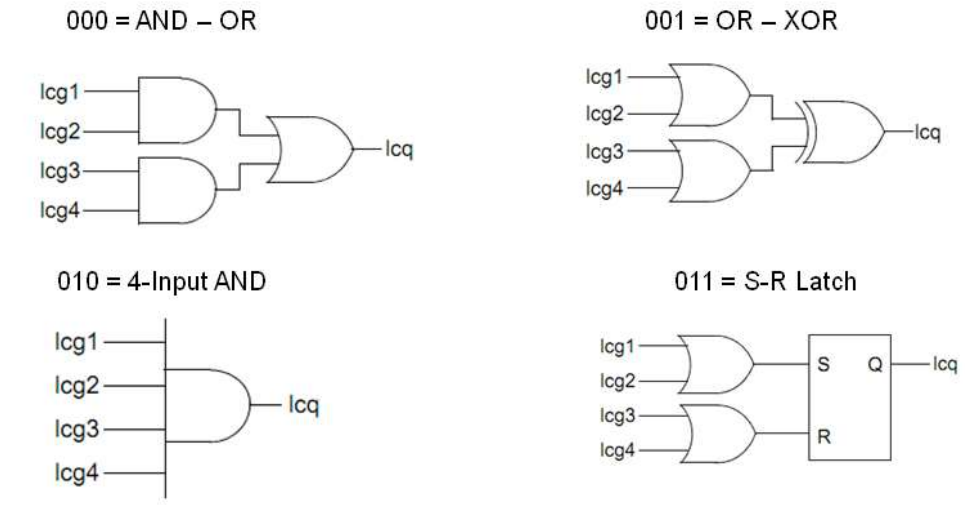
The CLCxPOL register bit, LCxGxPOL bit, will invert or not invert the output of the gate.
0 - non-inverted
1 - inverted

Logic Function

The Logic Function has eight options to choose from. It is selected in the CLCxCON register. Each Logic Function has a 3-bit code associated with it.



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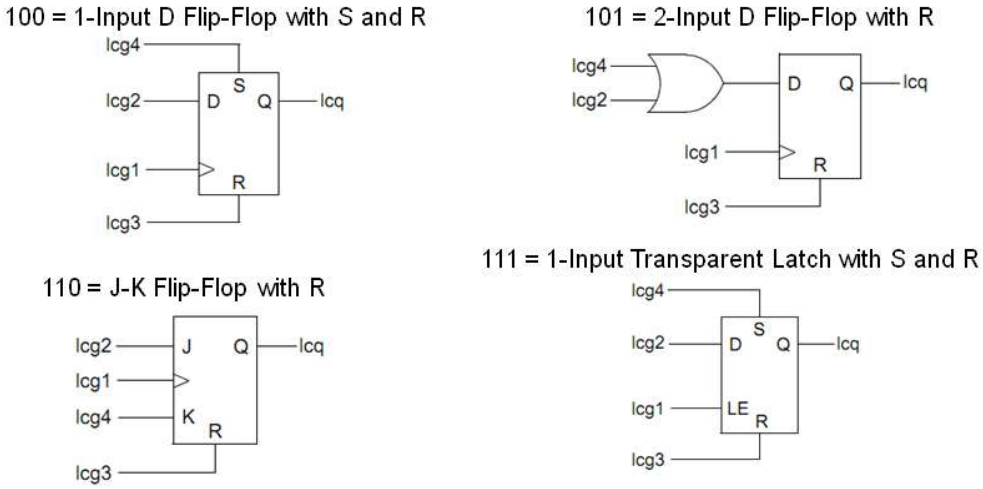

(/local--files/8bit:clc/logic2.png)

The 3-bit code is set in the CLCxCON register LCxMODE bits to enable the selected Logic Function.

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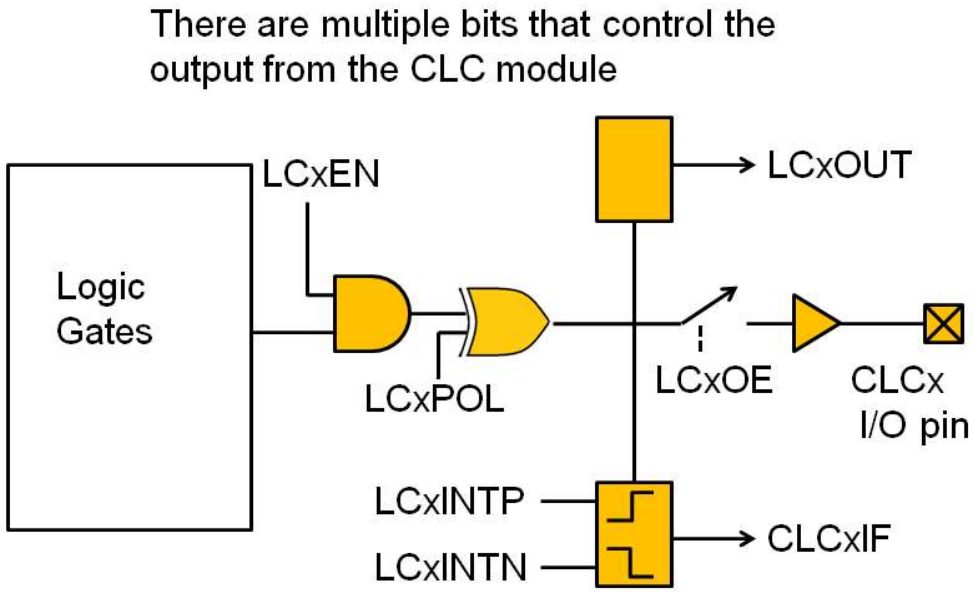
Output

All of the CLC sections reduce down to a single output that can drive an I/O pin, feed another CLC module or internal peripheral, or can also trigger a rising or falling edge interrupt. These various options are set up in the CLCxCON and CLCxPOL registers.



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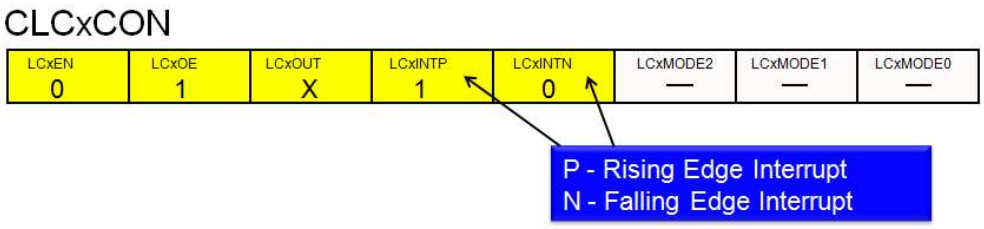
The bits in the CLCxCON register control the output settings.

LCxEN – CLC module enable bit (1 - CLC On, 0 - Off)
LCxOE – Output enable bit (1 – Enable, 0 – Disable)
LCxOUT - Internally monitor output via software (Read Only Bit)
LCxINTP – Rising edge interrupt enable (1-CLCxIF set on Rising Edge)
LCxINTN – Falling edge interrupt enable (1-CLCxIF set on Falling Edge)



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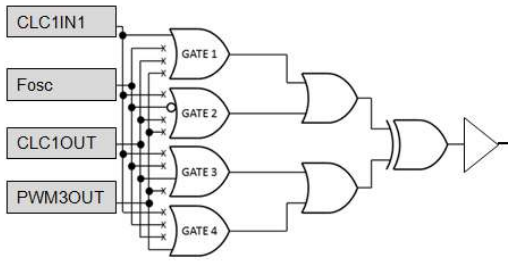
CLC Example

Here is a simple example that shows the eight registers set up in software to create the CLC setup shown in the picture.

The example below shows a setup for the CLC1 module. The eight register settings are shown for this example in a format for the XC8 compiler.




```
// CLC 1 Setup
CLC1SEL0 = 0x01;   // CLC1IN1 Pin, Fosc Inputs
CLC1SEL1 = 0x02;   // CLC1OUT, PWM3OUT Inputs
CLC1GLS0 = 0x01;   // Input 1 not inverted
CLC1GLS1 = 0x04;   // Input 2 inverted
CLC1GLS2 = 0x20;   // Input 3 not inverted
CLC1GLS3 = 0x80;   // Input 4 not inverted
CLC1POL  = 0x00;   // Output of CLC1 is not inverted
CLC1CON = 0xD2;   // Enable OR-XOR, Rising Edge Interrupt, Output Pin Enabled, CLC enabled
```

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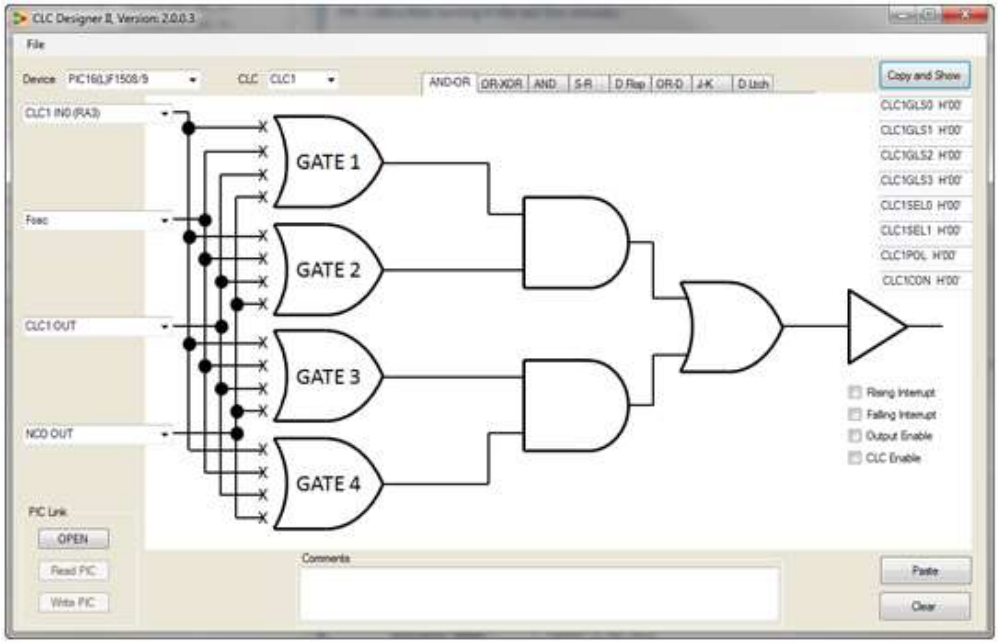
CLC Designer Tool

The CLC Designer Tool is a GUI based tool that makes creating the CLC structure much easier. Through a series of setup options, the tool will automatically output the eight register settings so you can include it in your **MPLAB® X** project.

The CLC Designer Tool is part of MPLAB Code Configurator (MCC) MPLAB® X Plugin.



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