Descripción general del temporizador AVR® MCU

Los temporizadores son una característica muy útil de un microcontrolador para contar pulsos en un pin de entrada. Cuando son impulsados por el reloj de instrucciones, pueden convertirse en una base de tiempo precisa. Los dispositivos AVR® tienen temporizadores de 8 y 16 bits de ancho y ofrecen diferentes funciones según el dispositivo. Un conjunto muy típico de temporizadores se puede encontrar en el microcontrolador AVR **ATmega328PB** . Este dispositivo tiene cinco temporizadores/contadores, como se describe aquí:

Temporizador 0	TC0	Temporizador/contador de 8 bits con modulación de ancho de pulso (PWM)
Temporizador 1	TC1	Temporizador/contador de 16 bits con PWM y funcionamiento asíncrono
Temporizador 2	TC2	Temporizador/contador de 8 bits con PWM y funcionamiento asíncrono
Temporizador 3	TC3	Temporizador/contador de 16 bits con PWM y funcionamiento asíncrono
Temporizador 4	TC4	Temporizador/contador de 16 bits con PWM y funcionamiento asíncrono

Definiciones:

Nomenclatura de registro

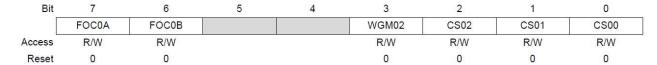|	
ABAJO	El contador llega al FONDO cuando llega a cero (0x00 para contadores de 8 bits y 0x0000 para contadores de 16 bits)
MÁX.	El contador alcanza su valor máximo cuando pasa a ser 0x0F (15 decimal) para contadores de 8 bits y 0x00FF (255 decimal) para contadores de 16 bits
PARTE SUPERIOR	El contador llega al TOP cuando su valor llega a ser igual al valor más alto posible. Al valor TOP se le puede asignar un valor fijo MAX o el valor almacenado en el registro OCRxA. Esta asignación depende del modo de funcionamiento

TC0 - Temporizador/Contador de 8 bits con PWM

Timer/Counter0 (TC0) es un módulo de temporizador/contador de uso general de 8 bits, con dos unidades de comparación de salida independientes y compatibilidad con PWM.

Registros TC0

El registro del temporizador/contador 0 (TCNT0) y los registros de comparación de salida TC0x (OCR0x) son registros de 8 bits. Todas las señales de solicitud de interrupción son visibles en el registro de bandera de interrupción del temporizador 0 (TIFR0). Todas las interrupciones se enmascaran individualmente con el registro de máscara de interrupción del temporizador 0 (TIMSK0).

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Name:      TCCR0B
Offset:    0x45
Reset:     0x00
Property:  When addressing as I/O Register: address offset is 0x25
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Bit	7	6	5	4	3	2	1	0
	FOC0A	FOC0B			WGM02	CS02	CS01	CS00
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

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Fuentes de reloj del temporizador/contador TC0

TC0 can be clocked by an internal or an external clock source. The clock source is selected by writing to the Clock Select (CS02:0) bits in the Timer/Counter Control Register (TCCR0B).

Bits 2:0 – CS0n: Clock Select [n = 0..2]

The three Clock Select bits select the clock source to be used by the Timer/Counter.

CS02	CS01	CS00	Description
0	0	0	No Clock source (Timer stopped)
0	0	1	clkio/1 (No prescaling)
0	1	0	clkio/8 (From prescaler)
0	1	1	clkio/64 (From prescaler)
1	0	0	clkio/256 (From prescaler)
1	0	1	clkio/1012 (From prescaler)

1	1	0	External clock source on T0 pin (clock on falling edge)
1	1	1	External clock source on T0 pin (clock on rising edge)

TC0 Counter Unit

Depending on the mode of operation used, T0 is cleared, incremented, or decremented at each timer clock (clkT0). clkT0 can be generated from an external or internal clock source, selected by the Clock Select bits (CS0[2:0]).

The counting sequence is determined by the setting of the WGM01 and WGM00 bits located in the T0 Control Register A (TCCR0A) and the WGM02 bit located in the Timer/Counter Control Register B (TCCR0B).

Bits 1:0 – WGM0n: Waveform Generation Mode [n = 1:0]

Combined with the WGM02 bit found in the TCCR0B Register, these bits control the counting sequence of the counter, the source for maximum (TOP) counter value and what type of waveform generation to be used. Modes of operation supported by the Timer/Counter unit are: Normal mode (counter), Clear Timer on Compare Match (CTC) Mode and two types of Pulse Width Modulation (PWM) modes.

Table 1-2 Waveform Generation Mode Bit Description

Mode	WGM2:0	Mode of Operation	TOP	OCR0x Update	TOV flag set on
0	0 0 0	Normal	0xFF	Immediate	MAX
1	0 0 1	PWM Phase Correct	0xFF	TOP	BOTTOM
2	0 1 0	CTC	OCRA	Immediate	MAX
3	0 1 1	Fast PWM	0xFF	BOTTOM	MAX
4	1 0 0	Reserved	~	~	~
5	1 0 1	PWM Phase Correct	OCRA	TOP	BOTTOM
6	1 1 0	Reserved	~	~	~
7	1 1 1	Fast PWM	OCRA	BOTTOM	MAX

Note:
1. MAX = 0xFF
2. BOTTOM = 0x00

Modes of Operation for TC0

The mode of operation determines the behavior of TC0 and the Output Compare pins. It is defined by the combination of the Waveform Generation mode bits and Compare Output mode bits in the Timer/Counter control Registers A and B (TCCR0B.WGMn2, TCCR0A.WGM01, TCCR0A.WGM00 and TCCR0A.COM0x[1:0]).

Available modes of operation for TC0 are:

- Normal Mode
- Clear Timer on Compare Match (CTC) Mode
- Fast PWM Mode
- Phase Correct PWM Mode

Clear Timer on Compare Match Mode

In Clear Timer on Compare or CTC mode (WGM0[2:0]=0x2), the **OCR0A Register** is used to manipulate the counter resolution: the counter is cleared to ZERO when the counter value (TCNT0) matches the OCR0A. The OCR0A defines the top value for the counter, hence also its resolution.

The counter value (TCNT0) increases until a compare match occurs between TCNT0 and OCR0A and then counter (TCNT0) is cleared. An interrupt can be generated each time the counter value reaches the TOP value by setting the OCF0A Flag. If the interrupt is enabled, the interrupt handler routine can be used for updating the TOP value.

The waveform frequency is defined by the following equation:

$$f_{OCnx} = \frac{f_{clk\_I/O}}{2 \cdot N \cdot (1 + OCRnx)}$$

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N represents the prescaler factor (1, 8, 64, 256, or 1024).

TC1, TC3, & TC4 - 16-bit Timer/Counters with PWM

The 16-bit Timer/Counter units allow accurate program execution timing (event management), wave generation and signal timing measurement.

Registers (TC1, TC3, TC4)

- The Timer/Counter (TCNTn), Output Compare Registers (OCRA/B) and Input Capture Register (ICRn) are all 16-bit registers.
- The Timer/Counter Control Registers (TCCRnA/B) are 8-bit registers and have no CPU access restrictions.
- Interrupt requests (abbreviated to Int.Req. in the block diagram) signals are all visible in the Timer Interrupt Flag Register (TIFRn). All interrupts are individually masked with the Timer Interrupt Mask Register (TIMSKn).
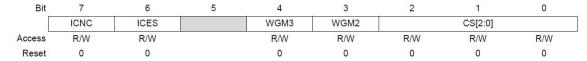
Timer/Counter Clock Sources (TC1, TC3, TC4)

The Timer/Counter can be clocked by an internal or an external clock source. The clock source is selected by the Clock Select logic which is controlled by the Clock Select bits in the timer/Counter control Register B (TCCRnB.CS[2:0]).

Name: TCCR1B, TCCR3B, TCCR4B
Offset: 0x81 + n*0x10 [n=0..2]
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ICNC	ICES		WGM3	WGM2	CS[2:0]		
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

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Bits 2:0 – CS[2:0]: Clock Select [n = 0..2]

The three Clock Select bits select the clock source to be used by the Timer/Counter.

CS02	CS01	CS00	Description
0	0	0	No Clock source (Timer stopped)
0	0	1	clkio/1 (No prescaling)
0	1	0	clkio/8 (From prescaler)
0	1	1	clkio/64 (From prescaler)
1	0	0	clkio/256 (From prescaler)
1	0	1	clkio/1012 (From prescaler)
1	1	0	External clock source on T0 pin (clock on falling edge)
1	1	1	External clock source on T0 pin (clock on rising edge)

Counter Unit (TC1, TC3, TC4)

TC1, TC3 and TC4 are programmable 16-bit bi-directional counters.

Each 16-bit counter is mapped into two 8-bit I/O memory locations: **Counter High** (TCNTnH) containing the upper eight bits of the counter and **Counter Low** (TCNTnL) containing the lower eight bits.

Depending on the selected mode of operation, the counter is cleared, incremented, or decremented at each timer clock (clkTn). The clock clkTn can be generated from an external or internal clock source, as selected by the Clock Select bits in the Timer/Counter Control Register B (TCCRnB.CS[2:0]).

The counting sequence is determined by the setting of the Waveform Generation mode bits in the Timer/Counter Control Registers A and B (TCCRnB.WGM[3:2] and TCCRnA.WGM[1:0]).

Modes of Operation (TC1, TC3, TC4)

The mode of operation is determined by the combination of the Waveform Generation mode (WGM[3:0]) and Compare Output mode (TCCRnA.COMx[1:0]) bits.

Available modes of operation are:

- Normal Mode
- Clear Timer on Compare Match (CTC) Mode
- Fast PWM Mode
- Phase Correct PWM Mode
- Phase and Frequency Correct PWM Mode

Fast PWM Mode

The Fast Pulse Width Modulation or Fast PWM modes (modes 5, 6, 7, 14,and 15, WGM[3:0]= 0x5, 0x6, 0x7, 0xE, 0xF) provide a high frequency PWM waveform generation option. The Fast PWM differs from the other PWM options by its single-slope operation. The counter counts from BOTTOM to TOP then restarts from BOTTOM.

In Fast PWM mode the counter is incremented until the counter value matches either one of the fixed values 0x00FF, 0x01FF, or 0x03FF (WGM[3:0] = 0x5, 0x6, or 0x7), the value in ICRn (WGM[3:0]=0xE), or the value in OCRnA (WGM[3:0]=0xF). The counter is then cleared at the following timer clock cycle.

The PWM frequency for the output can be calculated by the following equation:

$$f_{OCnxPWM} = \frac{f_{clk\_I/O}}{N \cdot (1 + TOP)}$$

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Note:

• The "n" in the register and bit names indicates the device number (n = 0 for Timer/Counter 0) and the "x" indicates Output Compare unit (A/B).

• N represents the prescale divider (1, 8, 64, 256, or 1024).

TC2 - 8-bit Timer/Counter2 with PWM and Asynchronous Operation

Timer/Counter2 (TC2) is a general purpose, dual channel, 8-bit Timer/Counter module.

TC2 Registers

The Timer/Counter (TCNT2) and Output Compare Register (OCR2A and OCR2B) are 8-bit registers. Interrupt request signals are all visible in the Timer Interrupt Flag Register (TIFR2). All interrupts are individually masked with the Timer Interrupt Mask Register (TIMSK2).

Name: TCCR2B
Offset: 0xB1
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	FOC2A	FOC2B			WGM22	CS22	CS21	CS20
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

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TC2 Clock Sources

TC2 can be clocked by an internal synchronous or an external asynchronous clock source: The three Clock Select bits (CS2:CS0) select the clock source to be used by the Timer/Counter.

CS02	CS01	CS00	Description
0	0	0	No Clock source (Timer stopped)
0	0	1	clkio/1 (No prescaling)
0	1	0	clkio/8 (From prescaler)
0	1	1	clkio/64 (From prescaler)
1	0	0	clkio/256 (From prescaler)

1	0	1	clkio/1012 (From prescaler)
1	1	0	External clock source on T0 pin (clock on falling edge)
1	1	1	External clock source on T0 pin (clock on rising edge)

TC2 Counter Unit

Depending on the mode of operation used, the counter is cleared, incremented, or decremented at each timer clock (clkT2). clkT2 can be generated from an external or internal clock source, selected by the Clock Select bits (CS2[2:0]).

The counting sequence is determined by the setting of the WGM21 and WGM20 bits located in the Timer/Counter Control Register (TCCR2A) and the WGM22 bit located in the Timer/Counter Control Register B (TCCR2B).

TC2 Modes of Operation

The mode of operation, i.e., the behavior of the Timer/Counter and the Output Compare pins, is defined by the combination of the Waveform Generation mode (WGM2[2:0]) and Compare Output mode (COM2x[1:0]) bits.

Available modes of operation are:

- Normal Mode
- Clear Timer on Compare Match (CTC) Mode
- Fast PWM Mode
- Phase Correct PWM Mode

Normal Mode

In the Normal mode (WGM22:0 = 0) the counting direction is always up (incrementing) without having the counter cleared. The counter will roll over to 0c00 when it passes its maximum 8-bit value (TOP = 0xFF).

In normal operation, the Timer/Counter Overflow Flag (TOV2) will be set in the same timer clock cycle as the TCNT2 becomes zero. The TOV2 Flag, in this case, behaves like a ninth bit, except that it is only set, not cleared. However, combined with the timer overflow interrupt that automatically clears the TOV2 flag, the timer resolution can be increased by software. There are no special cases to consider in the Normal mode, a new counter value can be written at any time.

> ⚠ Regardless of which mode is used the programmer needs to remember two things:
> 1. The timer has to be started by selecting the clock source.
> 2. If interrupts are used, they must be enabled.