Registros CLCxSELn

Los registros CLCxSEL, contenidos en la celda lógica configurable (CLC) (https://microchip-dev.wikidot.com/8bit:clc) , controlan qué entradas se usan con el CLC.

Fuentes de entrada CLC

El CLC tendrá múltiples entradas para seleccionar y cada una tendrá un código de 3 bits asociado, como se muestra en la siguiente tabla. Cada entrada se puede conectar a una de las dos puertas de datos de entrada a través de un multiplexor controlado por los registros CLCxSEL0 y CLCxSEL1.

Data Input	lcxd1 D1S	lcxd2 D2S	lcxd3 D3S	lcxd4 D4S	CLC 1	CLC 2
CLCxIN[0]	000	—	—	100	CLC1IN0	CLC2IN0
CLCxIN[1]	001	—	—	101	CLC1IN1	CLC2IN1
CLCxIN[2]	010	—	—	110	Reserved	Reserved
CLCxIN[3]	011	—	—	111	Reserved	Reserved
CLCxIN[4]	100	000	—	—	Fosc	Fosc
CLCxIN[5]	101	001	—	—	TMR0IF	TMR0IF
CLCxIN[6]	110	010	—	—	TMR1IF	TMR1IF
CLCxIN[7]	111	011	—	—	TMR2 = PR2	TMR2 = PR2
CLCxIN[8]	—	100	000	—	lcx1_out	lcx1_out
CLCxIN[9]	—	101	001	—	lcx2_out	lcx2_out
CLCxIN[10]	—	110	010	—	lcx3_out	lcx3_out
CLCxIN[11]	—	111	011	—	lcx4_out	lcx4_out
CLCxIN[12]	—	—	100	000	NCO1OUT	LFINTOSC
CLCxIN[13]	—	—	101	001	HFINTOSC	ADCFRC
CLCxIN[14]	—	—	110	010	PWM3OUT	PWM1OUT
CLCxIN[15]	—	—	111	011	PWM4OUT	PWM2OUT

(/local--files/8bit:clcsel/CLCInputs.png)

De la hoja de datos PIC16F1507

(http://ww1.microchip.com/downloads/en/DeviceDoc/40001586D.pdf) .

Las selecciones de entrada están controladas por los registros CLCxSEL0 y CLCxSEL1 configurando el código de entrada de 3 bits.

- El registro CLCxSEL0 controla las puertas de entrada de datos 1 y 2. Los bits 0-2

controlan la entrada 1 y los bits 4-6 controlan la entrada 2.

CLCxSEL0: MULTIPLEXOR DATOS 1 Y 2 SELECCIONAR REGISTRO

U-0	R/W-x/u	R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u
—	LCxD2S<2:0>			—	LCxD1S<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **LCxD2S<2:0>:** Input Data 2 Selection Control bits(1)

111 = CLCxIN[11] is selected for lcxd2
110 = CLCxIN[10] is selected for lcxd2
101 = CLCxIN[9] is selected for lcxd2
100 = CLCxIN[8] is selected for lcxd2
011 = CLCxIN[7] is selected for lcxd2
010 = CLCxIN[6] is selected for lcxd2
001 = CLCxIN[5] is selected for lcxd2
000 = CLCxIN[4] is selected for lcxd2

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **LCxD1S<2:0>:** Input Data 1 Selection Control bits(1)

111 = CLCxIN[7] is selected for lcxd1
110 = CLCxIN[6] is selected for lcxd1
101 = CLCxIN[5] is selected for lcxd1
100 = CLCxIN[4] is selected for lcxd1
011 = CLCxIN[3] is selected for lcxd1
010 = CLCxIN[2] is selected for lcxd1
001 = CLCxIN[1] is selected for lcxd1
000 = CLCxIN[0] is selected for lcxd1

(/local--files/8bit:clcsel/CLCSEL0.png)

De la hoja de datos PIC16F1507

(http://ww1.microchip.com/downloads/en/DeviceDoc/40001586D.pdf) .

- El registro CLCxSEL1 controla las puertas de entrada de datos 3 y 4. Los bits 0-2 controlan la entrada 3 y los bits 4-6 controlan la entrada 4.

CLCxSEL1: MULTIPLEXOR DATOS 3 Y 4 SELECCIONAR REGISTRO

U-0	R/W-x/u	R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u
—	LCxD4S<2:0>			—	LCxD3S<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **LCxD4S<2:0>:** Input Data 4 Selection Control bits(1)

111 = CLCxIN[3] is selected for lcxd4
110 = CLCxIN[2] is selected for lcxd4
101 = CLCxIN[1] is selected for lcxd4
100 = CLCxIN[0] is selected for lcxd4
011 = CLCxIN[15] is selected for lcxd4
010 = CLCxIN[14] is selected for lcxd4
001 = CLCxIN[13] is selected for lcxd4
000 = CLCxIN[12] is selected for lcxd4

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **LCxD3S<2:0>:** Input Data 3 Selection Control bits(1)

111 = CLCxIN[15] is selected for lcxd3
110 = CLCxIN[14] is selected for lcxd3
101 = CLCxIN[13] is selected for lcxd3
100 = CLCxIN[12] is selected for lcxd3
011 = CLCxIN[11] is selected for lcxd3
010 = CLCxIN[10] is selected for lcxd3
001 = CLCxIN[9] is selected for lcxd3
000 = CLCxIN[8] is selected for lcxd3

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(http://ww1.microchip.com/downloads/en/DeviceDoc/40001586D.pdf) .