Conjunto de instrucciones de rango medio mejorado

Esto se aplica a las familias de microcontroladores PIC ® PIC16F1xxx y PIC16LF1xxx .

Operaciones orientadas a bytes

Mnemónicos, Operandos		Descripción	Ciclos	Código de operación de 14 bits MSb……LSb	Estado Afectado	notas
ADDWF	f, d	Añadir W y f	1	00 0111 ffff ffff	C, CC, Z	2
AÑADIRWFC	f, d	Suma con Carry W y f	1	11 1101 ffff ffff	C, CC, Z	2
ANDWF	f, d	Y W con f	1	00 0101 ffff ffff	Z	2
ASRF	f, d	Desplazamiento aritmético a la derecha	1	11 0111 ffff ffff	C, Z	2
LSLF	f, d	Desplazamiento lógico a la izquierda	1	11 0101 ffff ffff	C, Z	2
LSRF	f, d	Desplazamiento lógico a la derecha	1	11 0110 ffff ffff	C, Z	2
CLRF	F	Borrar f	1	00 0001 1fffffff	Z	2
CLRW		Borrar W	1	00 0001 0000 00xx	Z	
COMF	f, d	Complemento f	1	00 1001 ffff ffff	Z	2
DECF	f, d	Decremento f	1	00 0011 ffff ffff	Z	2
FIN	f, d	Incremento f	1	00 1010 ffff ffff	Z	2

IORWF	f, d	Inclusivo OR W con f	1	00 0100 dfff ffff	Z	2
MOVF	f, d	Move f	1	00 1000 dfff ffff	Z	2
MOVWF	f	Move W to f	1	00 0000 1fff ffff	None	2
RLF	f,d	Rotate left f through Carry	1	00 1101 dfff ffff	C	2
RRF	f,d	Rotate right f through Carry	1	00 1100 dfff ffff	C	2
SUBWF	f,d	Subtract with Borrow W from f	1	11 1011 dfff ffff	C,DC,Z	2
SUBWFB	f,d	Subtract W from f	1	00 0010 dfff ffff	C,DC,Z	2
SWAPF	f,d	Swap nibbles in f	1	00 1110 dfff ffff	None	
XORWF	f,d	Exclusive OR W with f	1	00 0110 dfff ffff	Z	2

Byte Oriented Skip Instructions

Mnemonic, Operands		Description	Cycles	14-bit Opcode MSb……LSb	Status Affected	Notes
DECFSZ	f,d	Decrement f, Skip if 0	1(2)	00 1011 dfff ffff	None	1,2
INCFSZ	f,d	Increment f, Skip if 0	1(2)	00 1111 dfff ffff	None	1,2

Bit Oriented File Register Operations

Mnemonic, Operands		Description	Cycles	14-bit Opcode MSb……LSb	Status Affected	Notes
BCF	f,b	Bit Clear f	1	01 00bb bff ffff	None	2
BSF	f,b	Bit Set f	1	01 01bb bfff ffff	None	2

Bit Oriented Skip Operations

Mnemonic, Operands		Description	Cycles	14-bit Opcode MSb……LSb	Status Affected	Notes
BTFSC	f,b	Bit Test f, Skip if Clear	1(2)	01 10bb bfff ffff	None	1,2
BTFSS	f,b	Bit Test f, Skip if Set	1(2)	01 11bb bfff ffff	None	1,2

Literal Operations

Mnemonic, Operands		Description	Cycles	14-bit Opcode MSb……LSb	Status Affected	Notes
ADDLW	k	Add literal and W	1	11 1110 kkkk kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11 1001 kkkk kkkk	Z	
IORLW	k	Inclusive OR literal with W	1	11 1000 kkkk kkkk	Z	
MOVLB	k	Move literal to BSR	1	00 0000 001k kkkk	None	
MOVLP	k	Move literal to PCLATH	1	11 0001 1kkk kkkk	None	
MOVLW	k	Move literal to W	1	11 0000 kkkk kkkk	None	
SUBLW	k	Subtract W from literal	1	11 1100 kkkk kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11 1010 kkkk kkkk	Z	

Control Operations

Mnemonic, Operands		Description	Cycles	14-bit Opcode MSb……LSb	Status Affected	Notes
BRA	k	Relative Branch	2	11 001k kkkk kkkk	None	
BRW		Relative Branch with W	2	00 0000 0000 1011	None	
CALL	k	Call Subroutine	2	10 0kkk kkkk kkkk	None	
CALLW		Call Subroutine with W	2	00 0000 0000 1010	None	
GOTO	k	Goto address	2	10 1kkk kkkk kkkk	None	
RETFIE	k	Return from interrupt	2	00 0000 0000 1001	None	
RETLW	k	Return, place literal in W	2	11 0100 kkkk kkkk	None	
RETURN	k	Return from subroutine	2	00 0000 0000 1000	None	

Inherent Operations

Mnemonic, Operands		Description	Cycles	14-bit Opcode MSb……LSb	Status Affected	Notes
CLRWDT		Clear Watchdog Timer	1	00 0000 0110 0100	$\overline{TO}$,$\overline{PD}$	
NOP		No Operation	1	00 0000 0000 0000	None	
OPTION		Load OPTION register with W	1	00 0000 0110 0010	None	
RESET		Software device Reset	1	00 0000 0000 0001	None	
SLEEP		Go into standby mode	1	00 0000 0110 0011	$\overline{TO}$, $\overline{PD}$	
TRIS	f	Load TRIS register	1	00 0000 0110 0fff	None	

C-Compiler Optimized

Mnemonic, Operands	Description	Cycles	14-bit Opcode MSb……LSb	Status Affected	Notes
ADDFSR	Add Literal to FSRn	1	11 0001 0nkk kkkk	None	
MOVIW	Move Indirect FSRn to W	1	00 0000 0001 0nnn	Z	2
MOVWI	Move W to Indirect FSRn	1	00 0000 0001 1nnnn	Z	2

Notes

1. If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.
2. If this instruction addresses an INDF register *and* the MSb of the corresponding FSR is set, the instruction requires one additional instruction cycle.