05 Hardware Design II (VLSI)

Engr 399/599: Hardware Security

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Indiana University

Adapted from: Mark Tehranipoor of University of Florida

Agenda

- Review some of last class.
- Questions on P1?
- Finish VLSI Unit?
- Next unit - PUFs!!!
- First Project Assigned: Due 2/17/25

Course Website

engr99.github.io

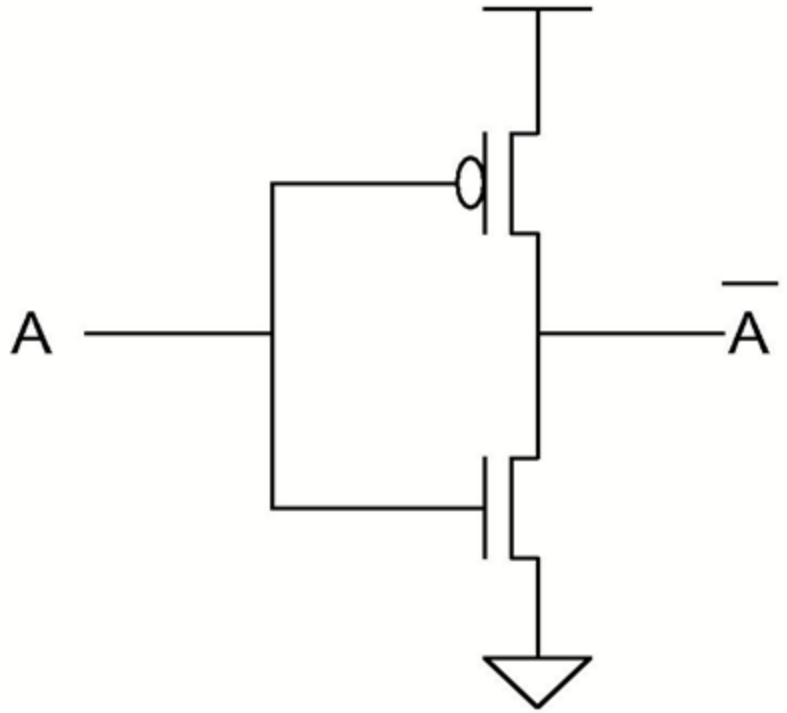
Side Quest: Seagate Controversy UPDATE

The plot thickens!!!!

"A widespread scandal involving used Seagate hard drives fraudulently sold as new has continued to escalate, with new evidence suggesting that the drives originated from Chinese cryptocurrency mining farms. The drives, many of which had logged 15,000 to 50,000 hours of prior use, were reportedly altered to appear unused before re-entering the retail supply chain"

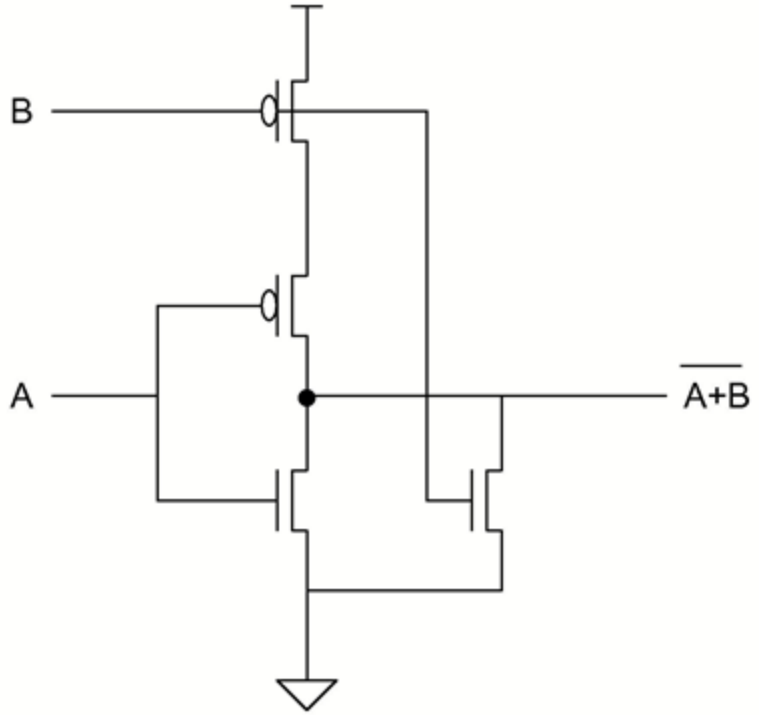
CMOS Logic Implementations

- Inverter



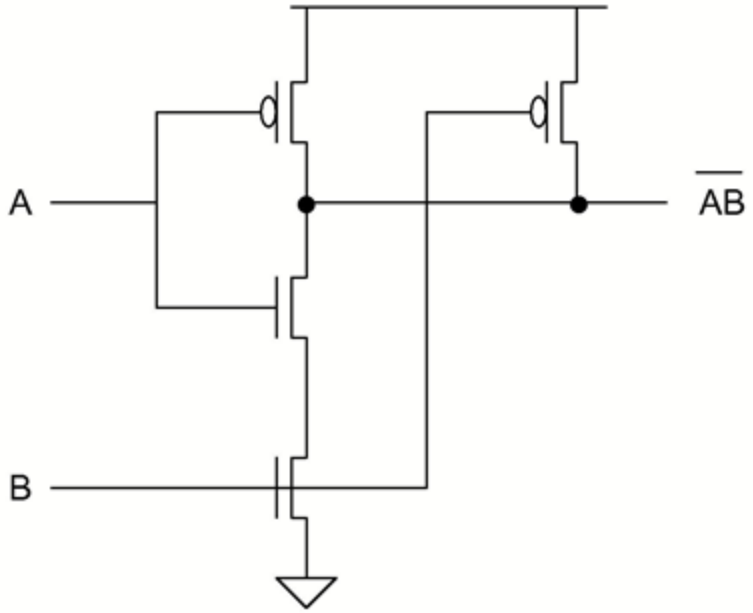
CMOS Logic Implementations

- NOR



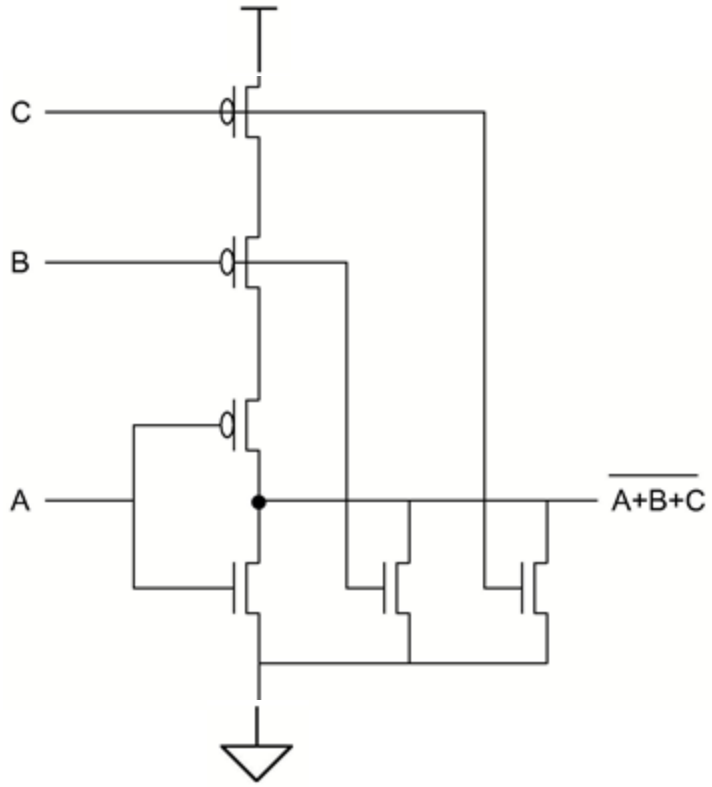
CMOS Logic Implementations

- NAND



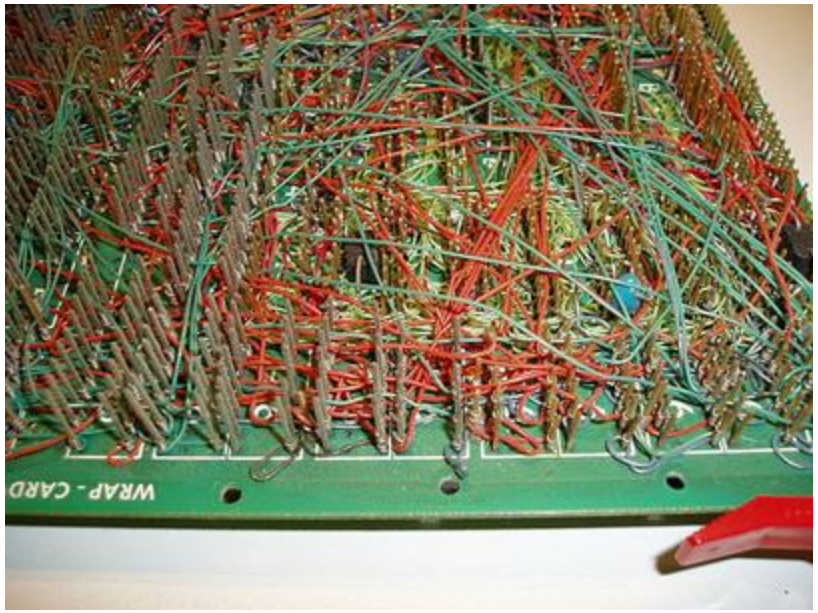
CMOS Logic Implementations

- Multi-input NOR



What is VLSI design?

- The process of creating an integrated circuit from specifications to fabrication

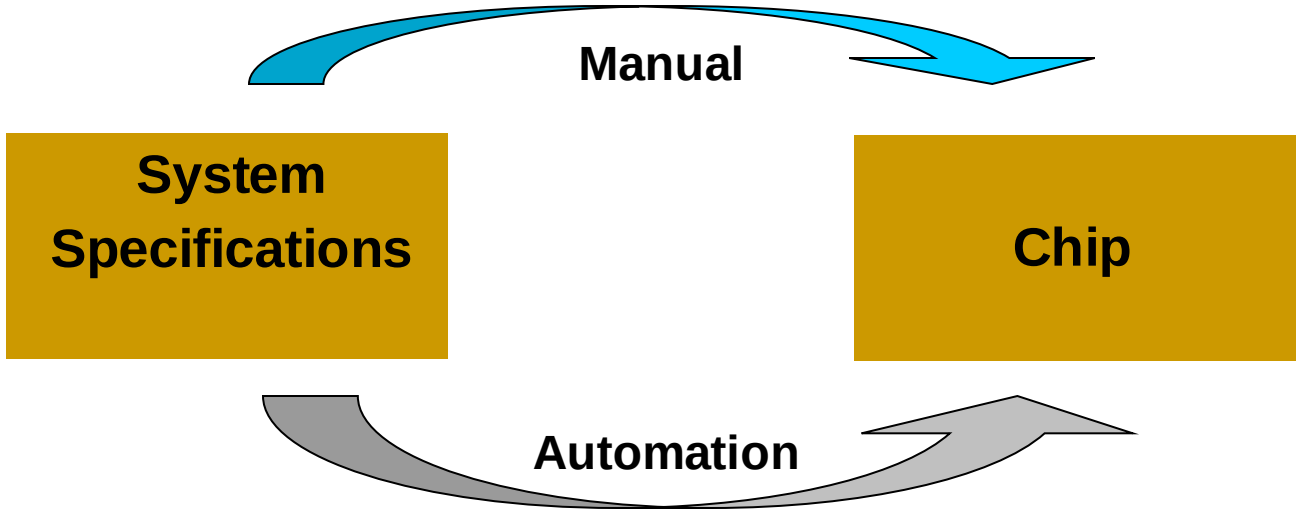


What is an integrated circuit?

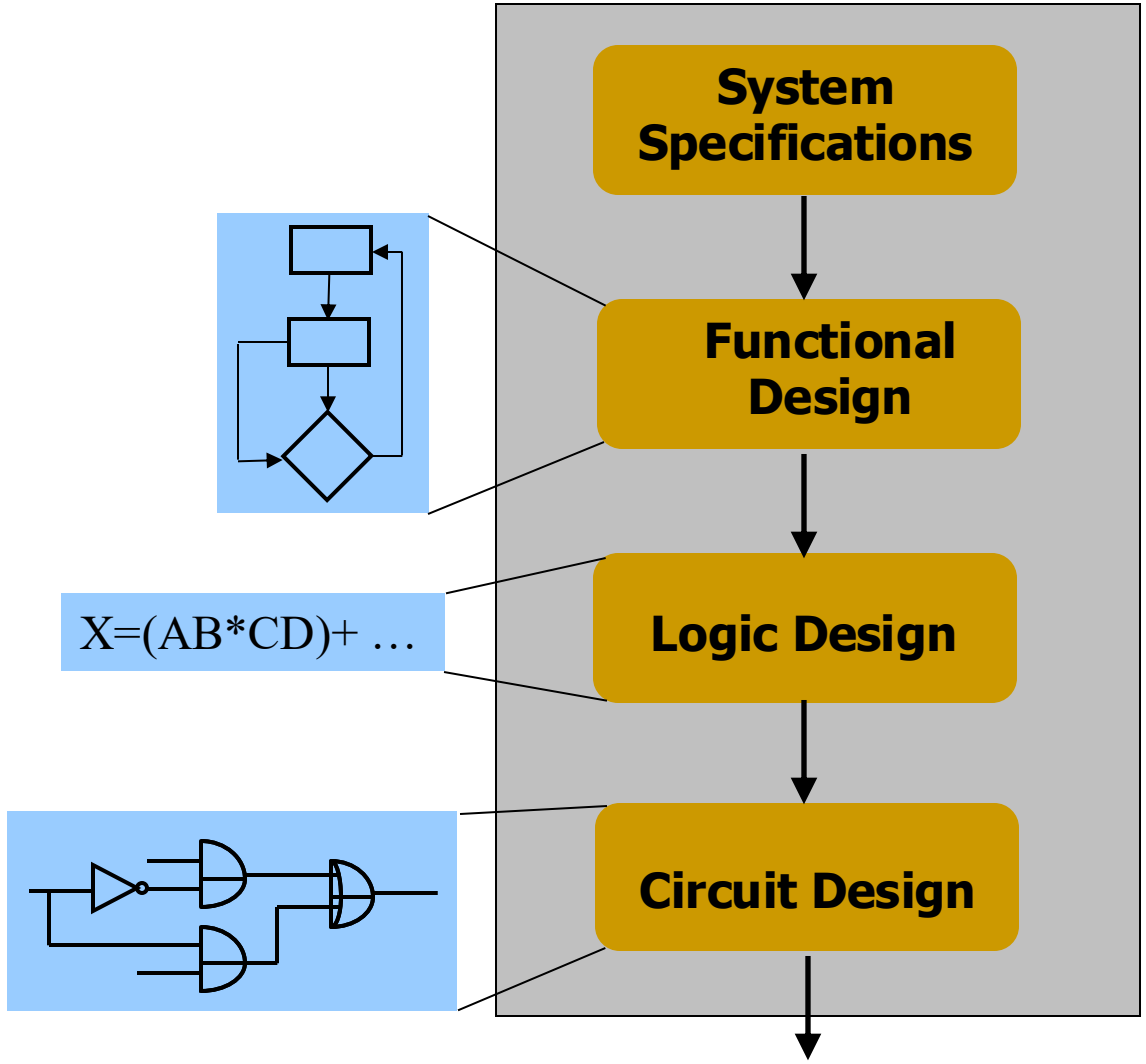
- A single integrated component that contains all the primary elements of an electrical circuit: transistors, wiring, resistors, capacitors, etc.
- What is NOT an integrated circuit?

VLSI Design Automation

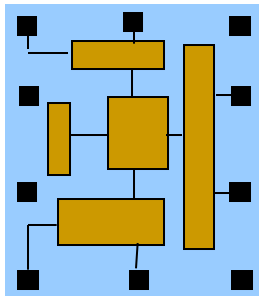
- Large number of components
- Optimize requirements for higher performance
  - Performance relates to speed, power and size. (SWaP)
- Time to market competition
- Cost
  - Using computer makes it cheaper by reducing time-to-market.

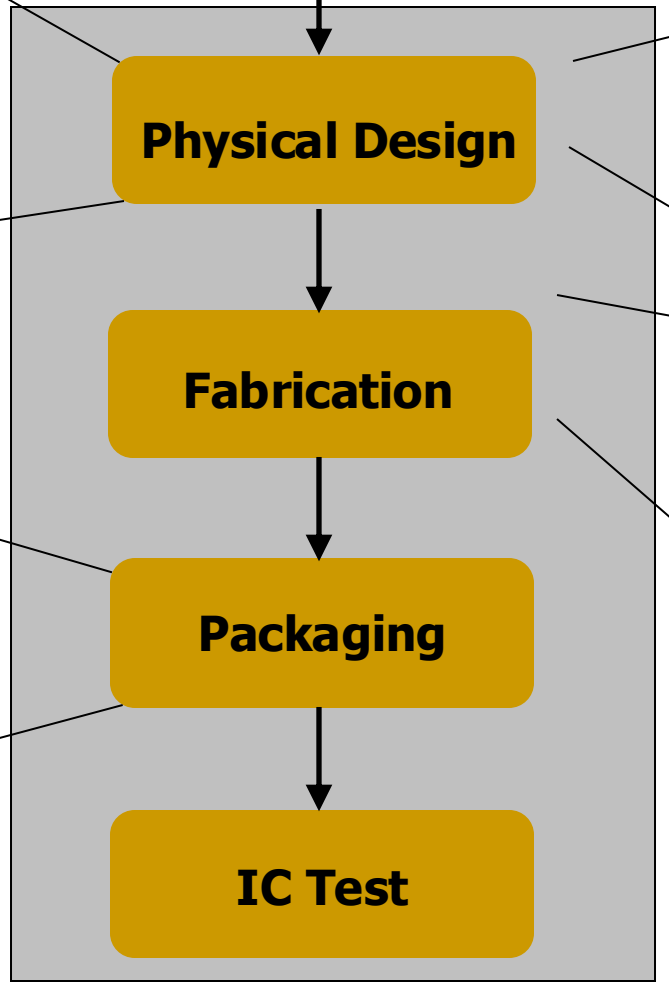


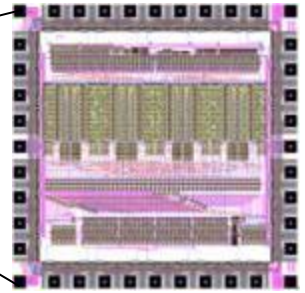
VLSI Design Cycle

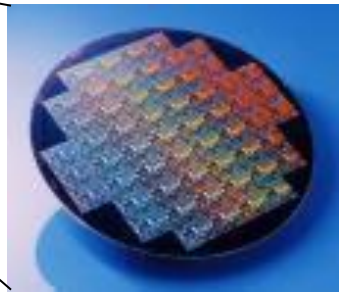


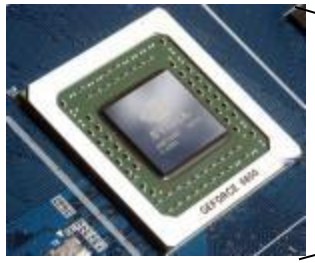
VLSI Design Cycle





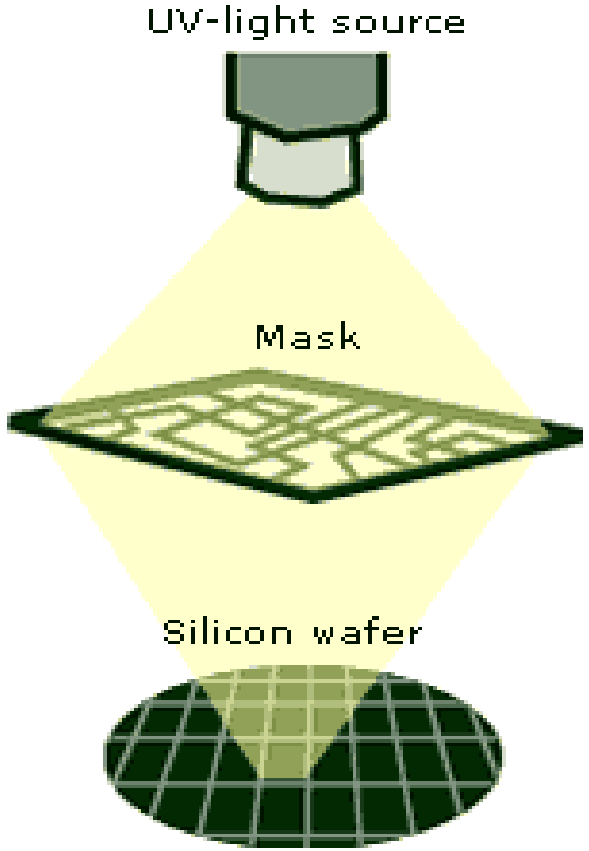






Semiconductor Processing

- How do we make a transistor?

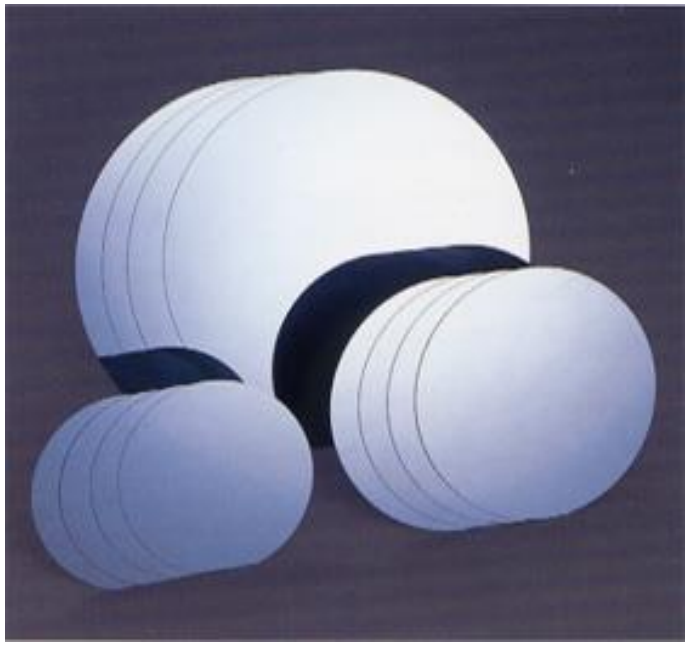


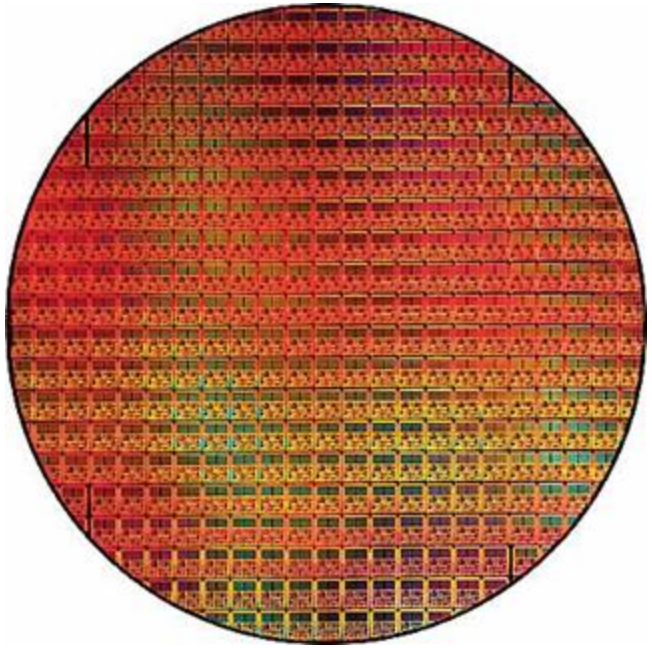
- How do you control where the features get placed?
  - Photo lithography masks

Extreme Ultraviolet Lithography (EUV)

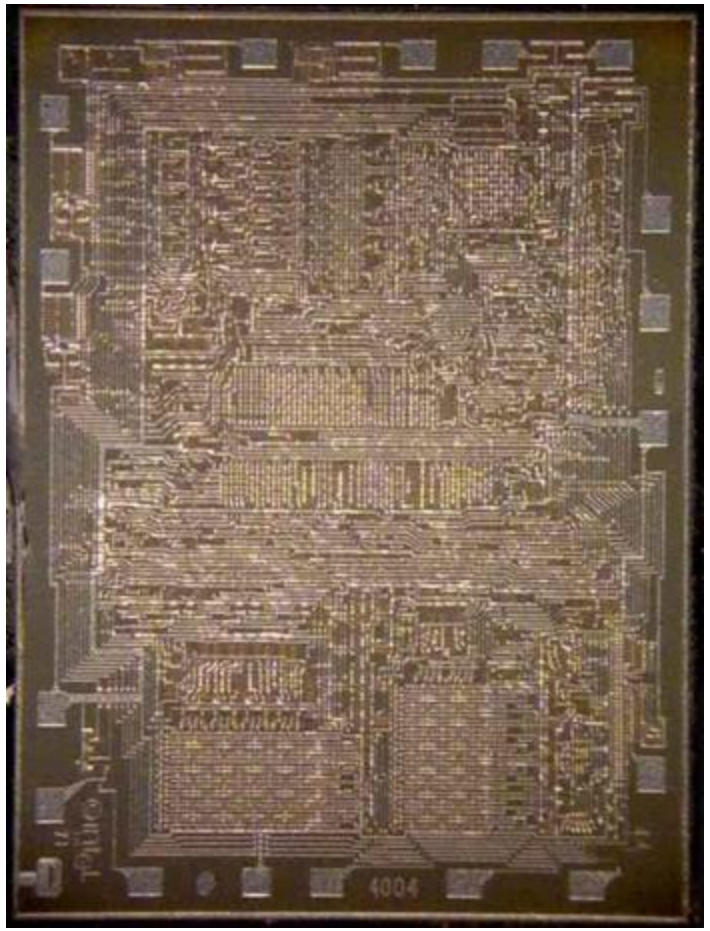
Excellent Youtube series on Semiconductor Manufacturing history.

Wafer Processing



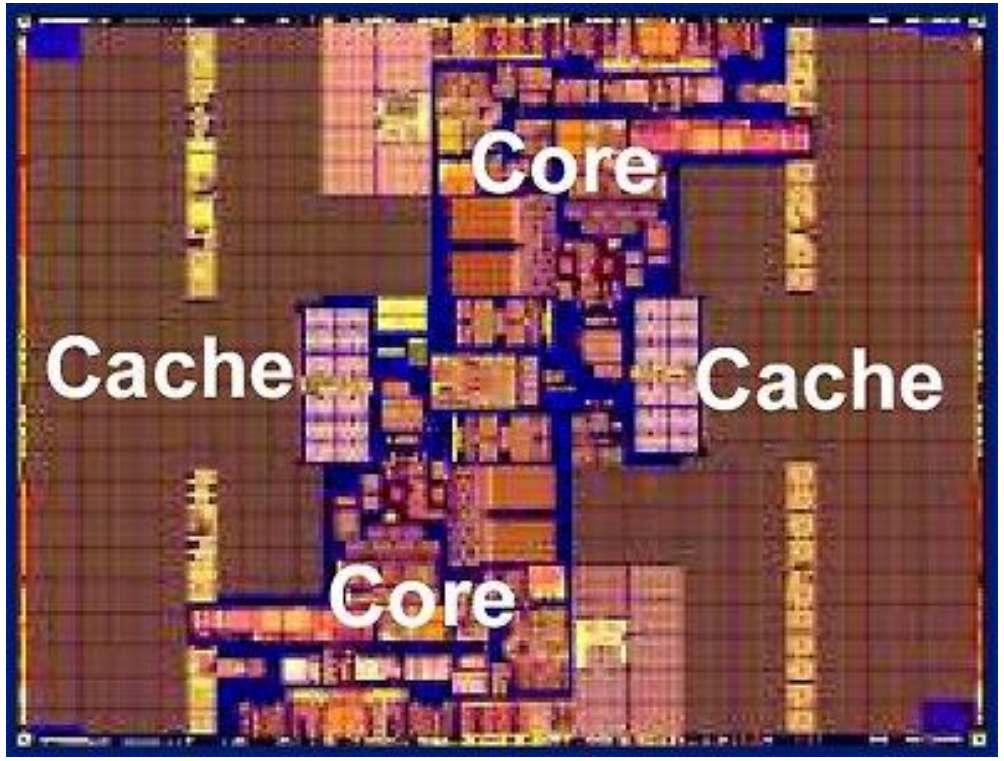


Intel 4004



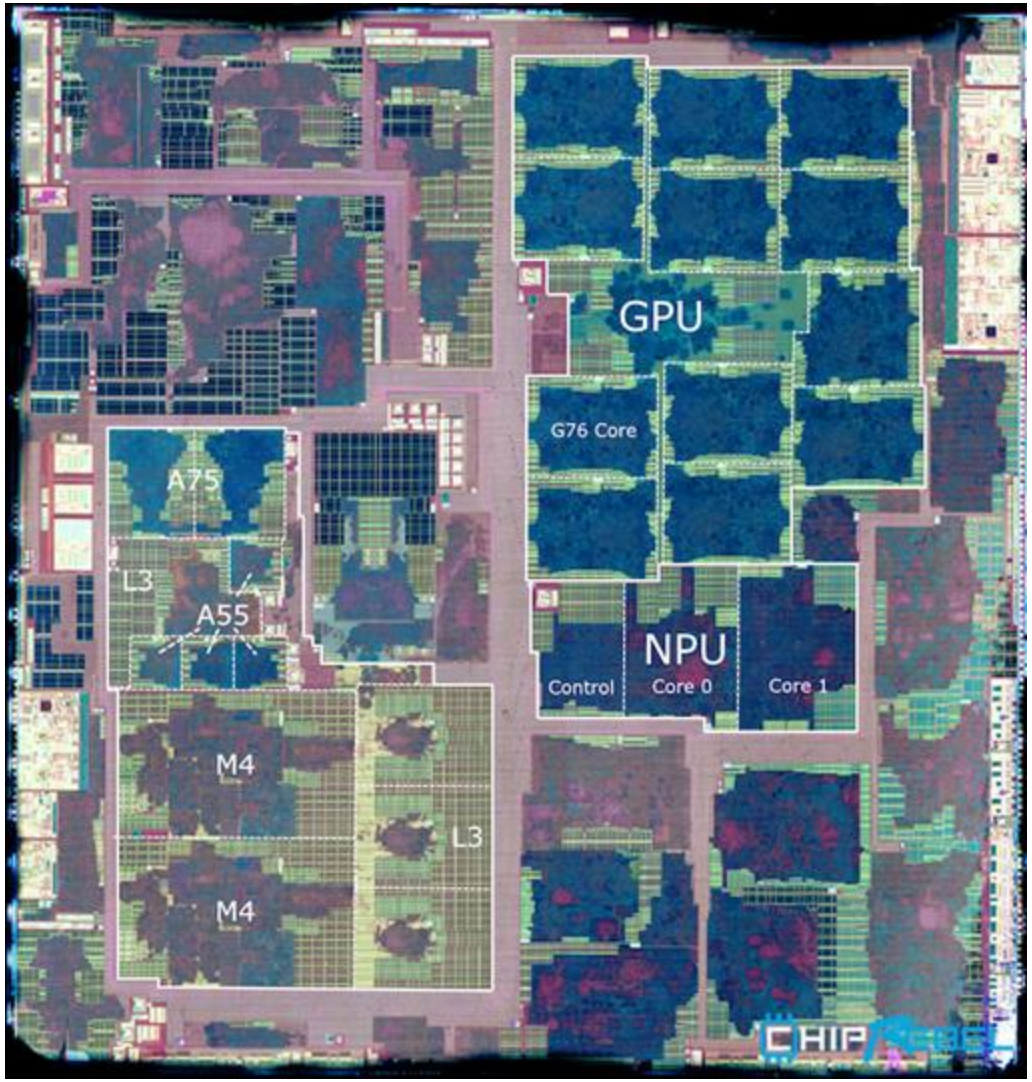
- First microprocessor
- Designed in 1971
- 2300 transistors
- 10-um process
- ~100 KHz

Intel Itanium Processor



- Released in 2005
- 1.72 Billion transistors
- 90-nm process
- 2 GHz

Samsung Exynos 9820 SoC



- Released in 2019
- 2.75 GHz
- TSMC 7nm LPP

Design Methodology

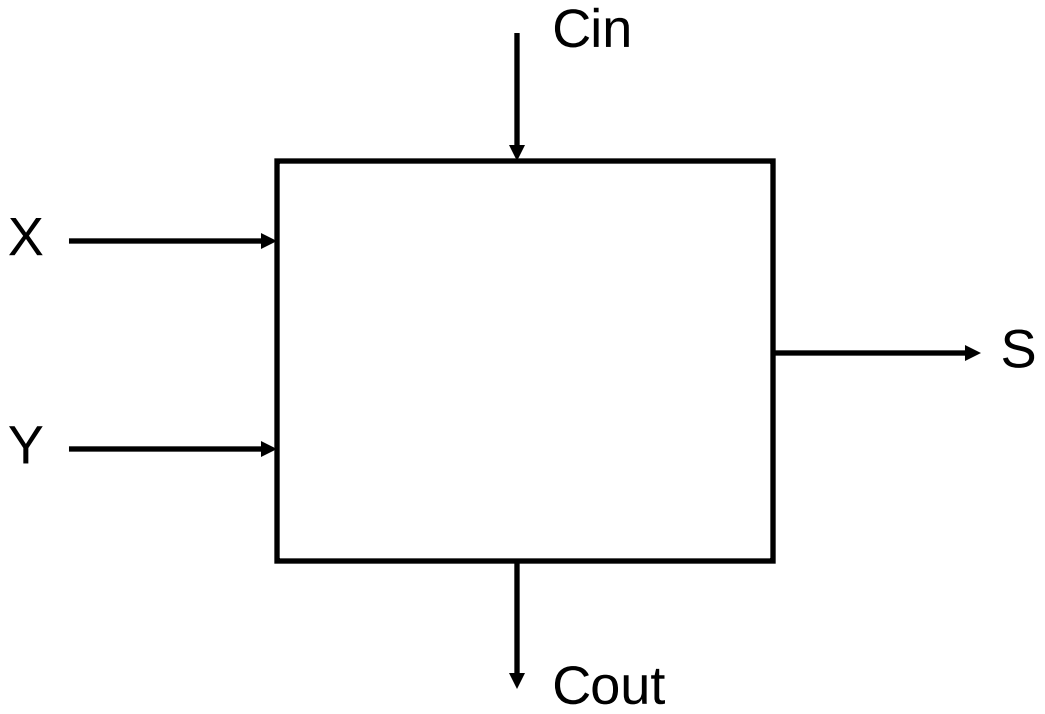
- Functional specification
  - What does the chip do?
- Behavioral specification
  - How does it do it? (abstractly)
- Logic design
  - How does it do it? (logically)
- Layout
  - How does it do it? (physically)

Design Constraints

- Budget
  - Total cost
- Silicon area
- Power requirements
  - Dynamic
  - Static
- Speed
  - Performance
- Schedule
  - Time to market

Functional Specification

- Full adder



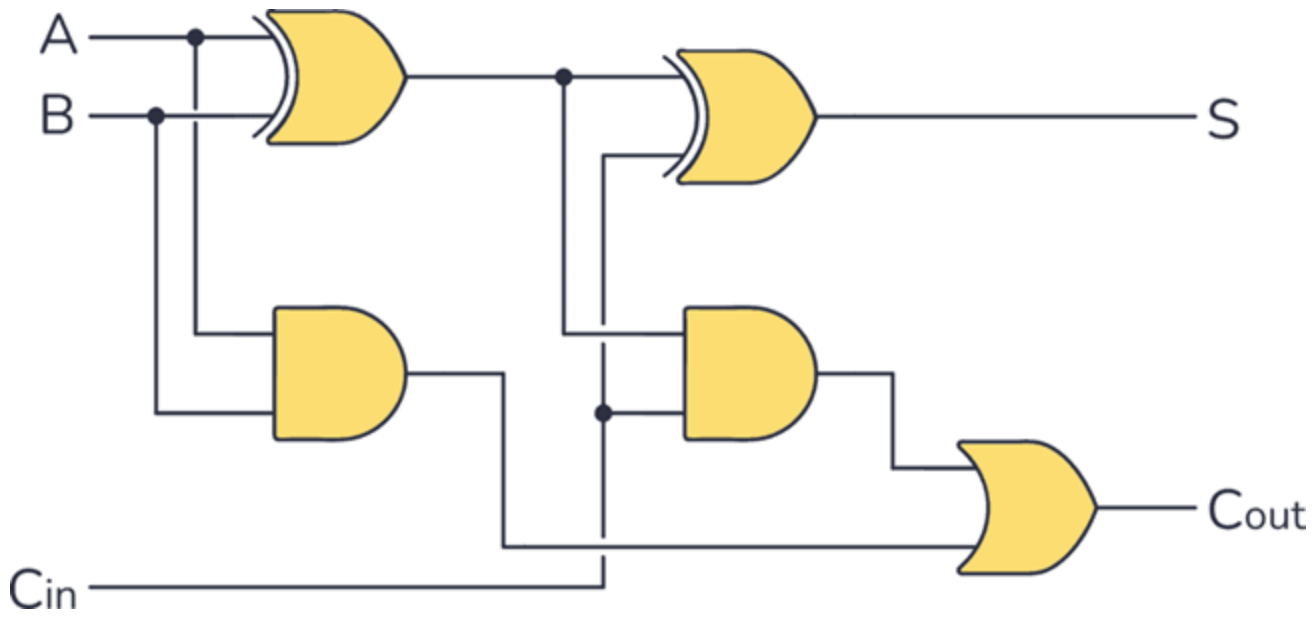
Behavioral Specification

- VHDL
- Verilog

```
entity adder is
        -- i0, i1 and the carry-in ci are inputs of the adder.
        -- s is the sum output, co is the carry-out.
        port (i0, i1 : in bit; ci : in bit; s : out bit; co : out bit);
 end adder;
 architecture rtl of adder is
        begin -- This full-adder architecture contains two concurrent assignment.
         -- Compute the sum. s <= i0 xor i1 xor ci;
        -- Compute the carry. co <= (i0 and i1) or (i0 and ci) or (i1 and ci);

end rtl;
```

Behavioral Specification

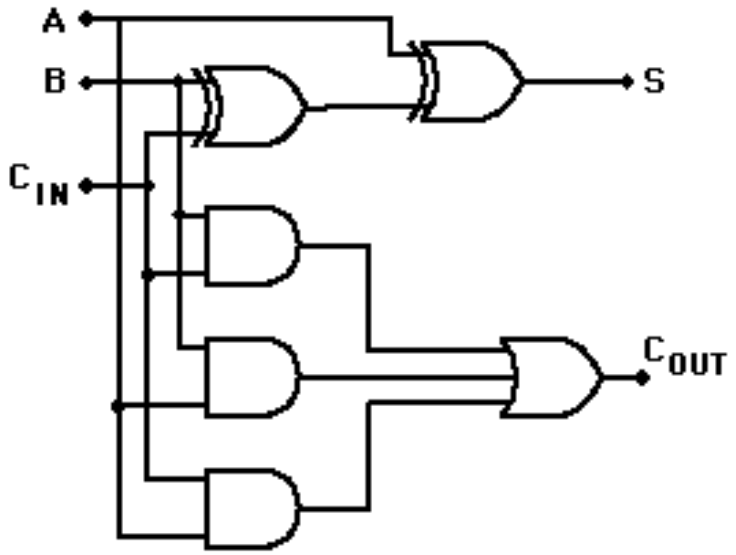
```
module fulladder (a,b,cin,sum,cout);
    input a,b,cin;
    output sum,cout;

    reg sum,cout;
    always @ (a or b or cin)
    begin
       sum <= a ^ b ^ cin;
       cout <= (a & b) | (a & cin) | (b & cin);
    end
endmodule
```



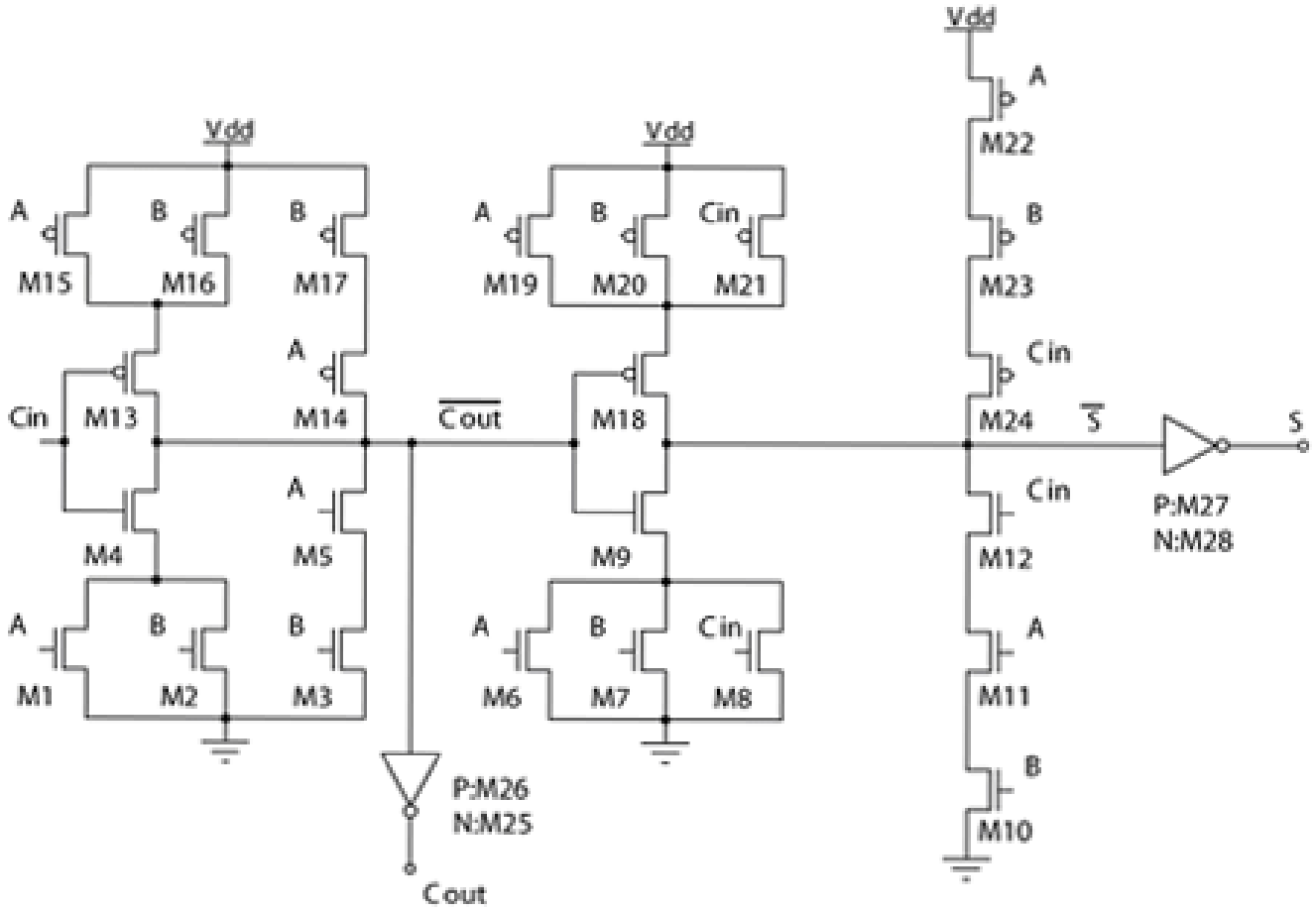
Logic Design

Full Adder Truth Table

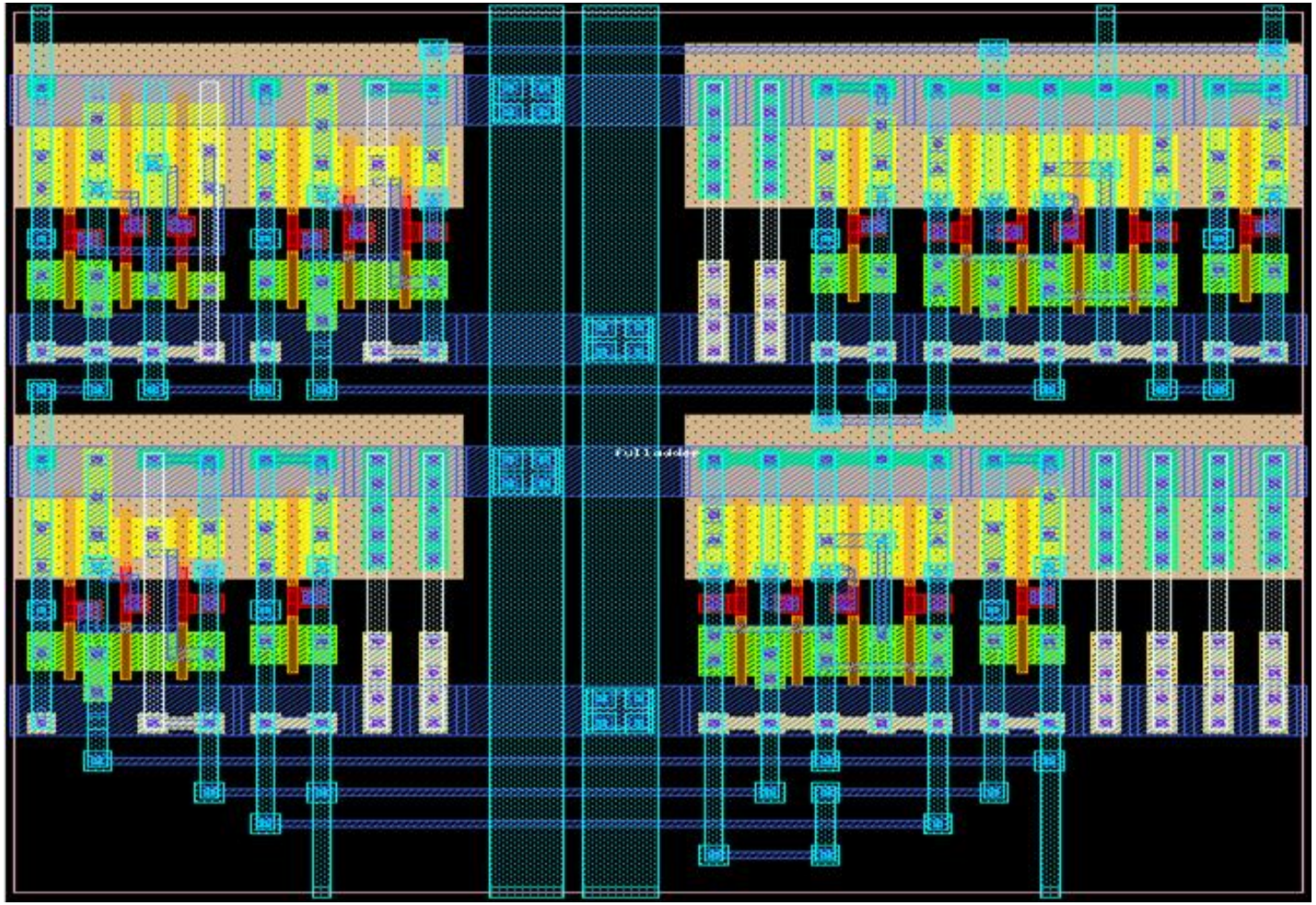
CARRY IN	*input B*	*input A*	*CARRY OUT*	*SUM digit*
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



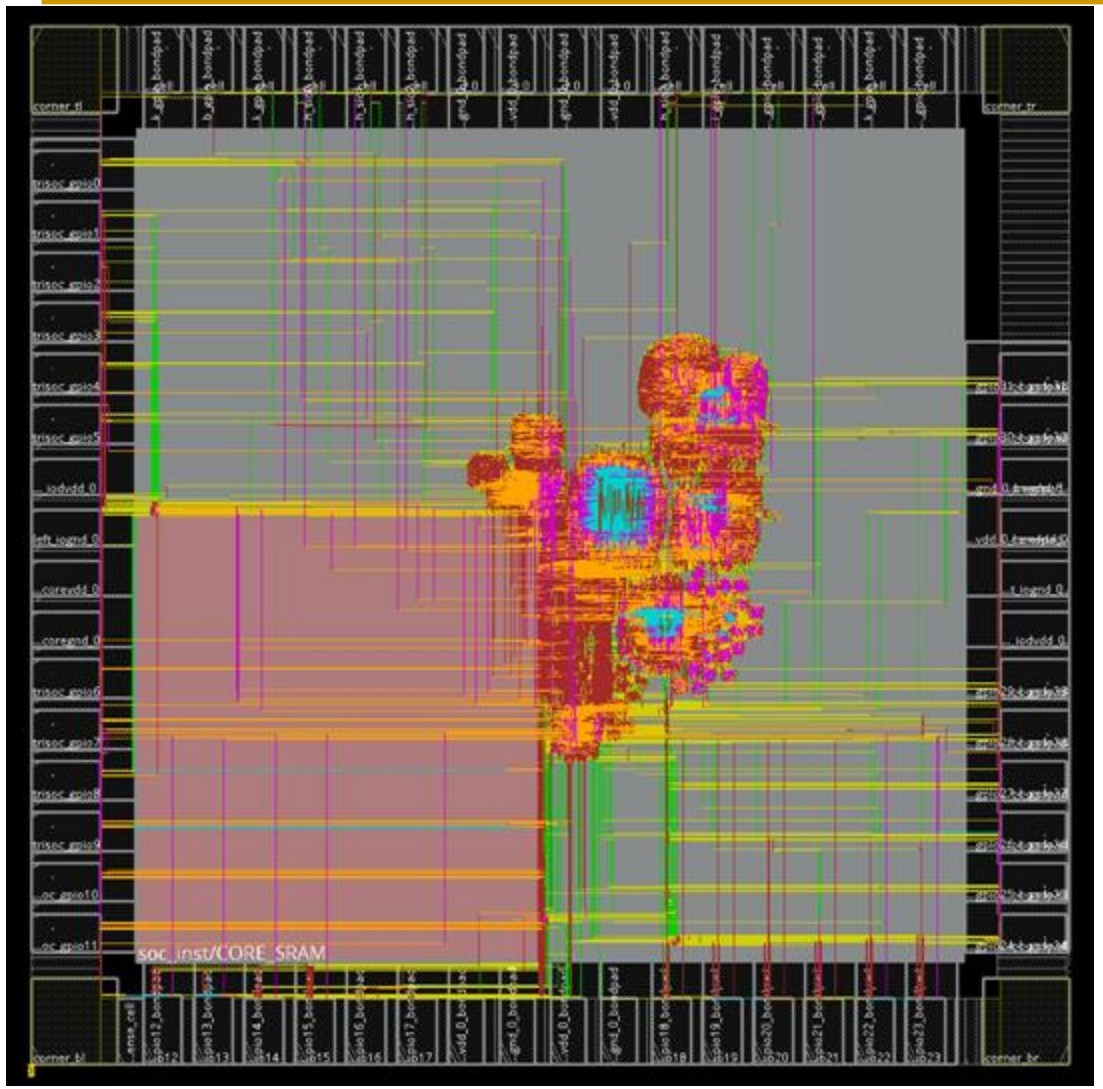
Transistor Schematic

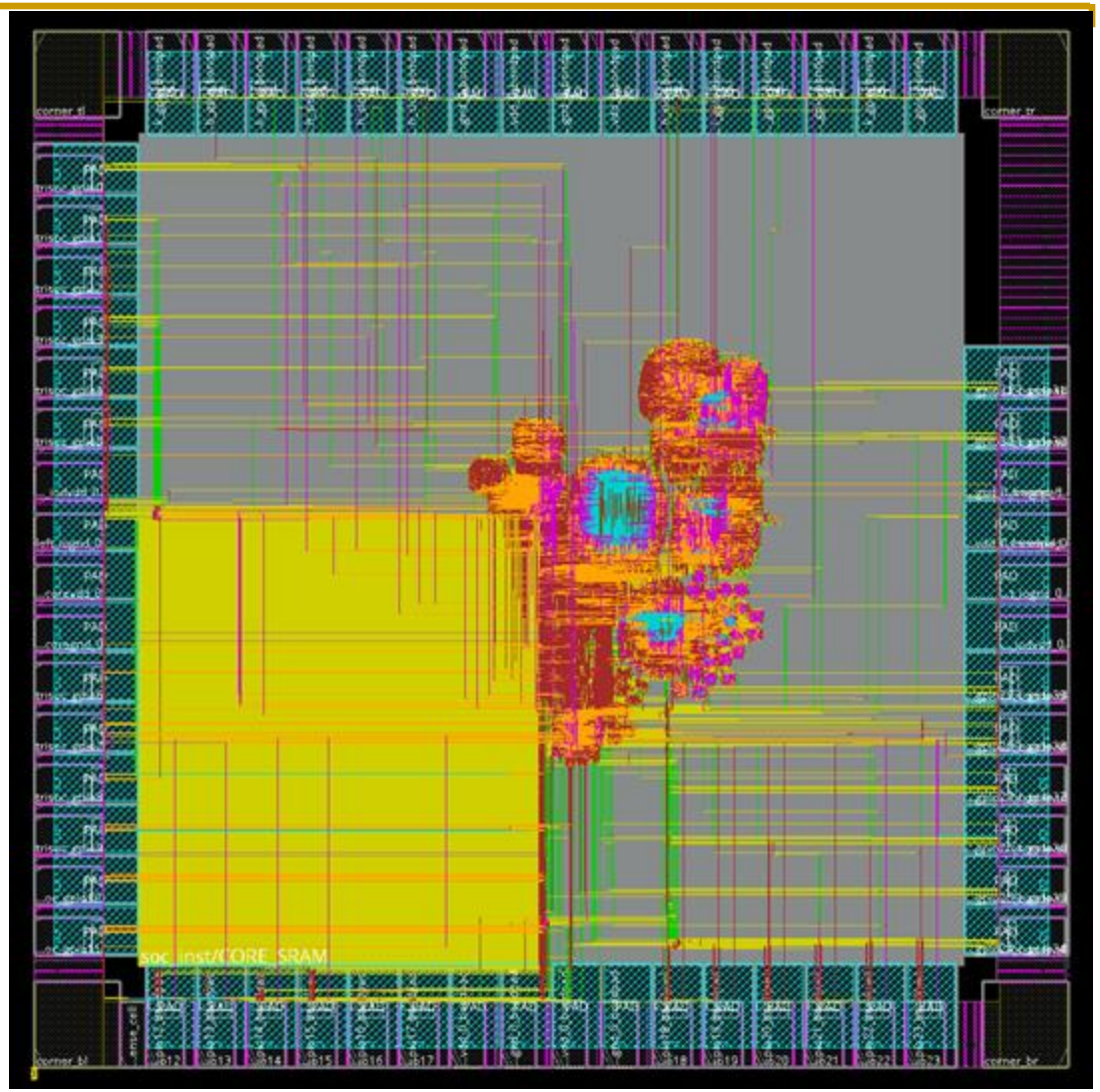


Layout



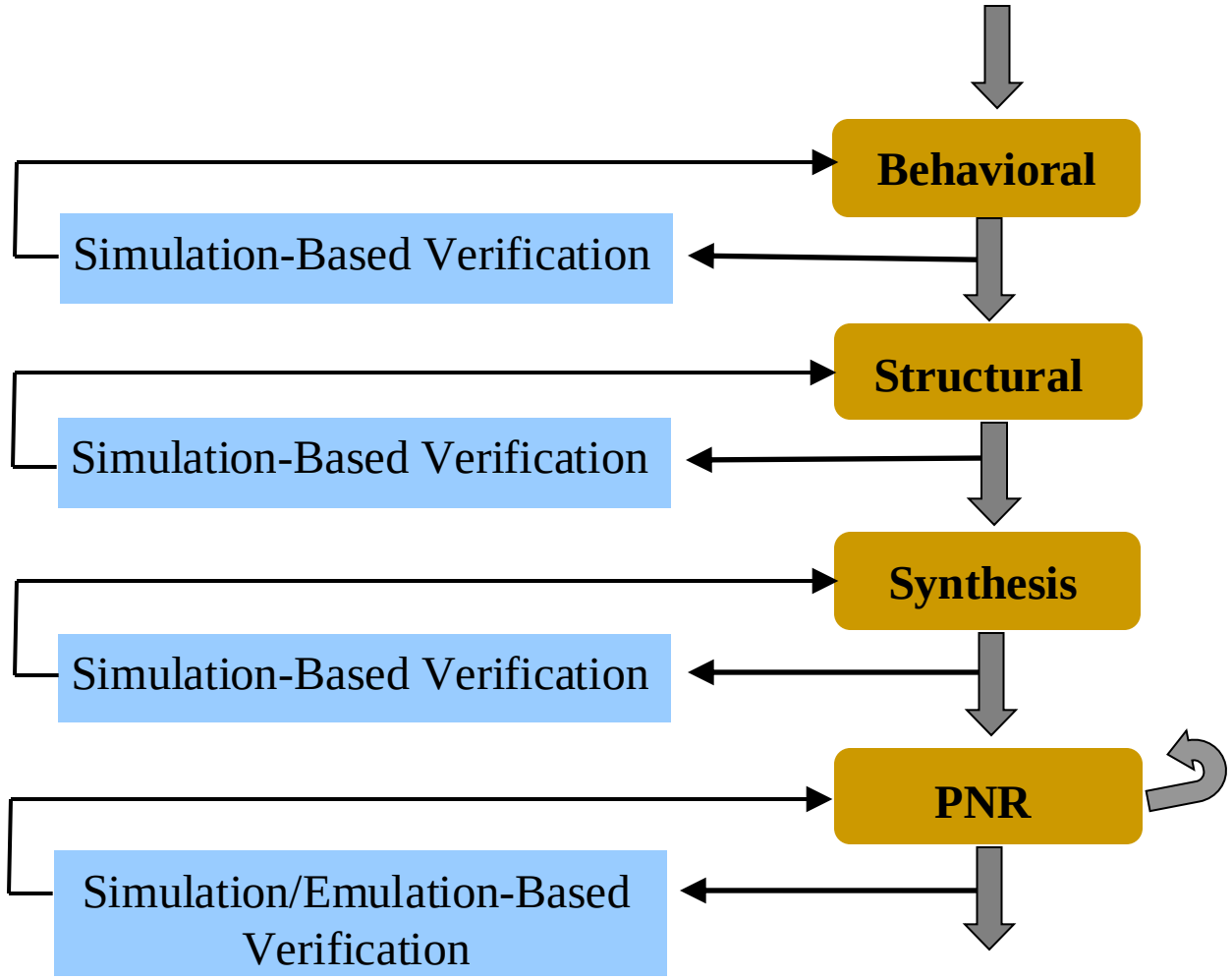
Layout





GF 12LP, 344,000 SCs 1500k Transistors

Design Process is Iterative



PNR: Placement and routing

VLSI Design Methodologies

- Full custom
  - Design for performance-critical cells
  - Very expensive
- Standard cell
  - Faster
  - Performance is not as good as full custom
- Gate array
- Field Programmable Gate Array

Comparison of Design Styles

	Full Custom	Standard Cell	Gate Array	FPGA
Area	Compact	Moderate	Moderate	Large
Performance	High	Moderate	Moderate	Low

Production Volume:	**Mass Production Volume**	**Medium Production Volume**	**Medium Production Volume**	**Low Production Volume**
Complexity:	**High**			**Low**

VLSI Chip Yield

- A manufacturing defect in the fabrication process causes electrically malfunctioning circuitry.
- A chip with no manufacturing defect is called a **good chip**.
  - The defective ones are called **bad chips**.
- Percentage of good chips produced in a manufacturing process is called the ***yield***.
- Yield is denoted by symbol *Y*.

$$Y = \frac{\text{\# of good die}}{\text{\# total manufactured die}}$$

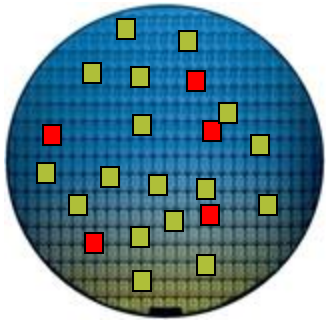
- How to separate bad chips from the good?
  TEST ALL CHIPS

Why Does Test Matter ?

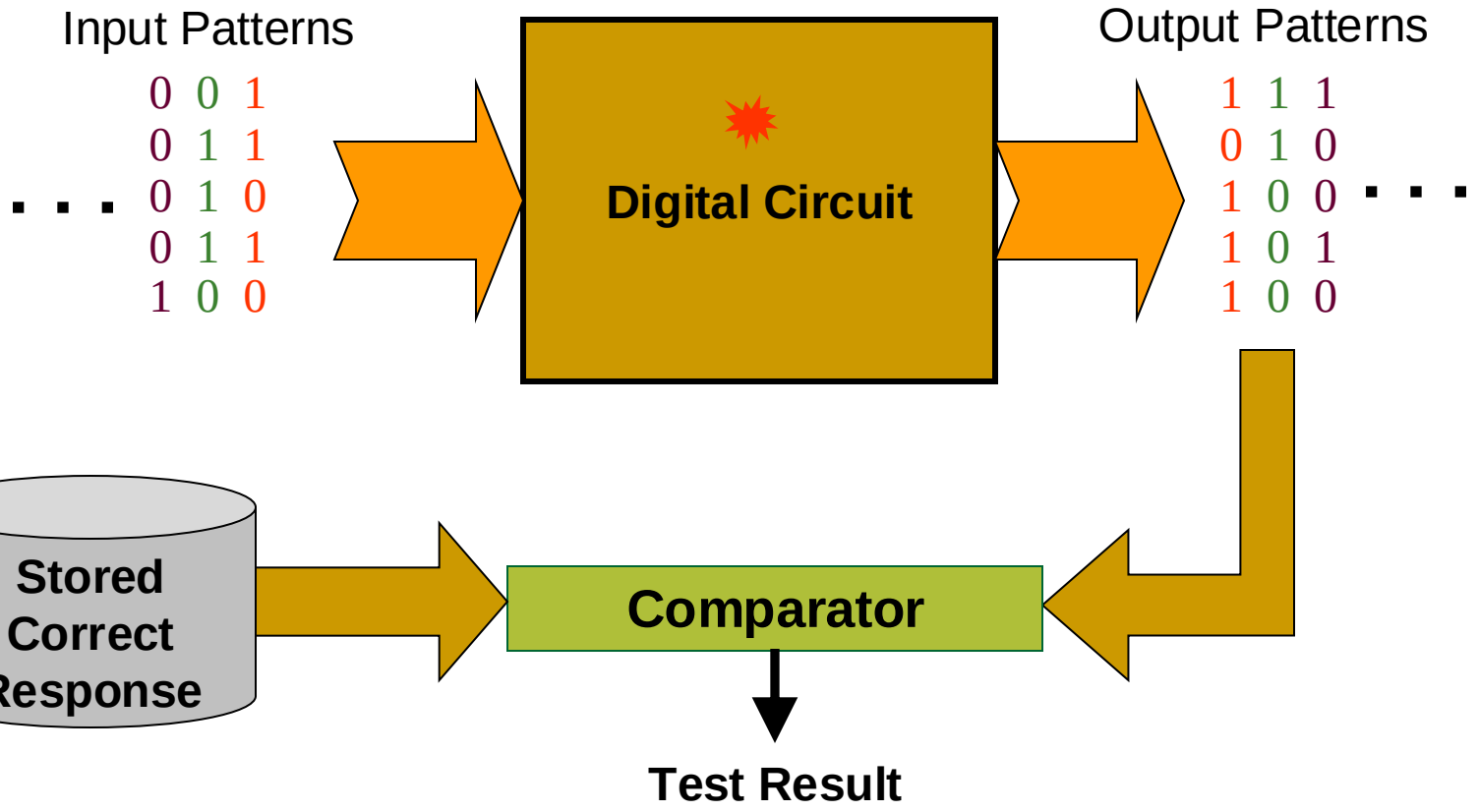
- In simple terms, TEST identifies the defective chips
- Some bad chips ( ) are easy to find

- Some other are difficult ( )
- Test is associated with
  - Cost
  - Return On Investment (ROI)
    - ¥ € $ - Money

Wafer



Testing Principle



Functional Test Method – Not very efficient

Contract between design house and fab vendor

- Design is complete and checked (verified)
- Fab vendor: How will you test it?
- Design house: I have checked it and …
- Fab vendor: But, how would you test it?
- Design house: Why is that important?
- *complete the story*

- That is one reason for design-for-testability (DFT), test generation etc.

Contract between design …

Hence:

- "Test" must be comprehensive
- It must not be "too long"

Issues:

- Model possible defects in the process
  - Understand the process
- Develop simulator and fault simulator
- Develop test generator
- Methods to quantify the test efficiency
  - Fault coverage

Ideal Tests

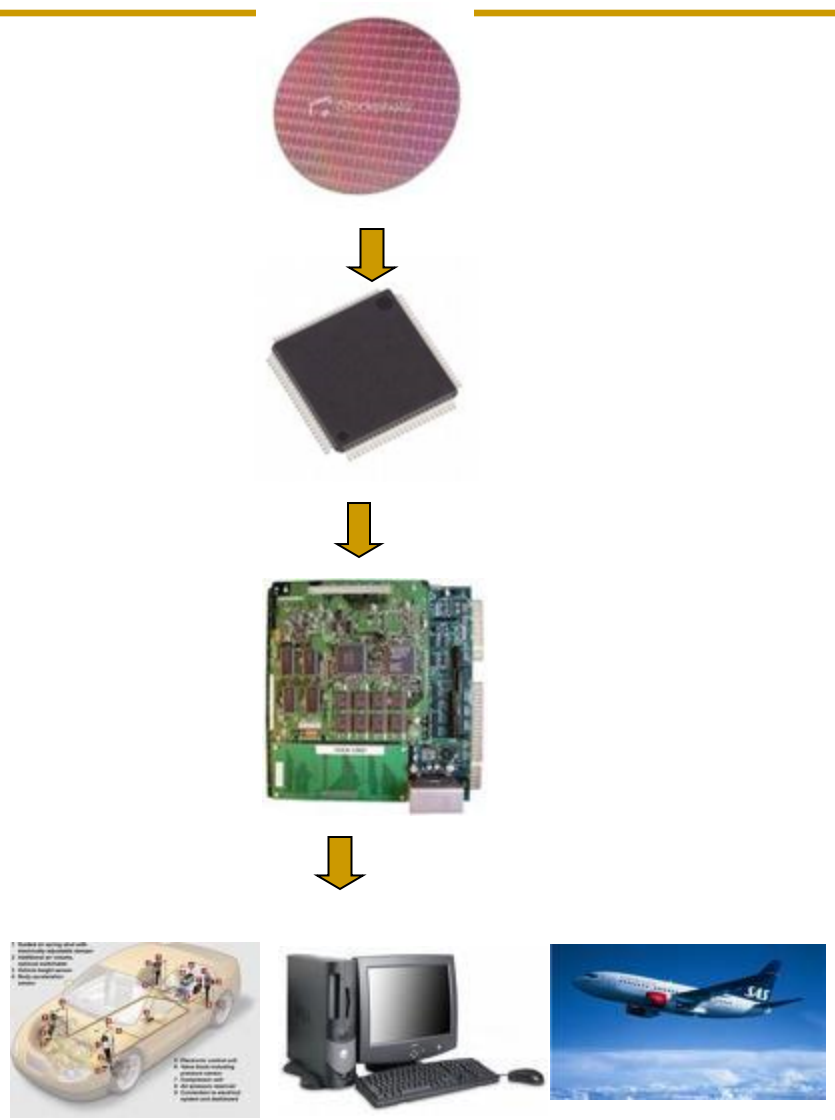
- Ideal tests detect **all** defects produced in the manufacturing process.
- Ideal tests pass all functionally good devices.
- Very large numbers and varieties of possible defects need to be tested.
- Difficult to generate tests for some real defects. *Defect-oriented testing is an open problem.*

Real Tests

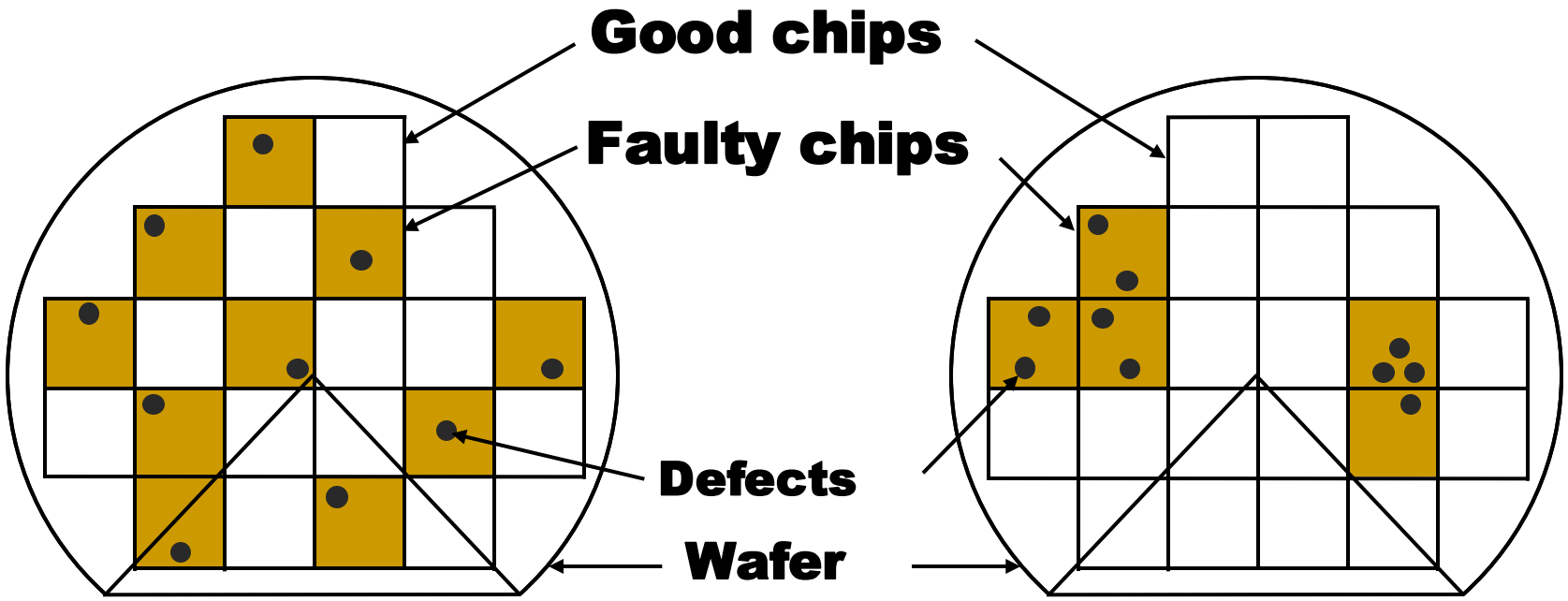
- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected. The fraction (or percentage) of such chips is called the **yield loss**.
- Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the **defect level**.

Level of testing (1)

- Levels
  - Chip
  - Board
  - System
    - Boards put together
    - System-on-Chip (SoC)
  - System in field
- Cost – Rule of 10
  - It costs 10 times more to test a device as we move to higher level in the product manufacturing process



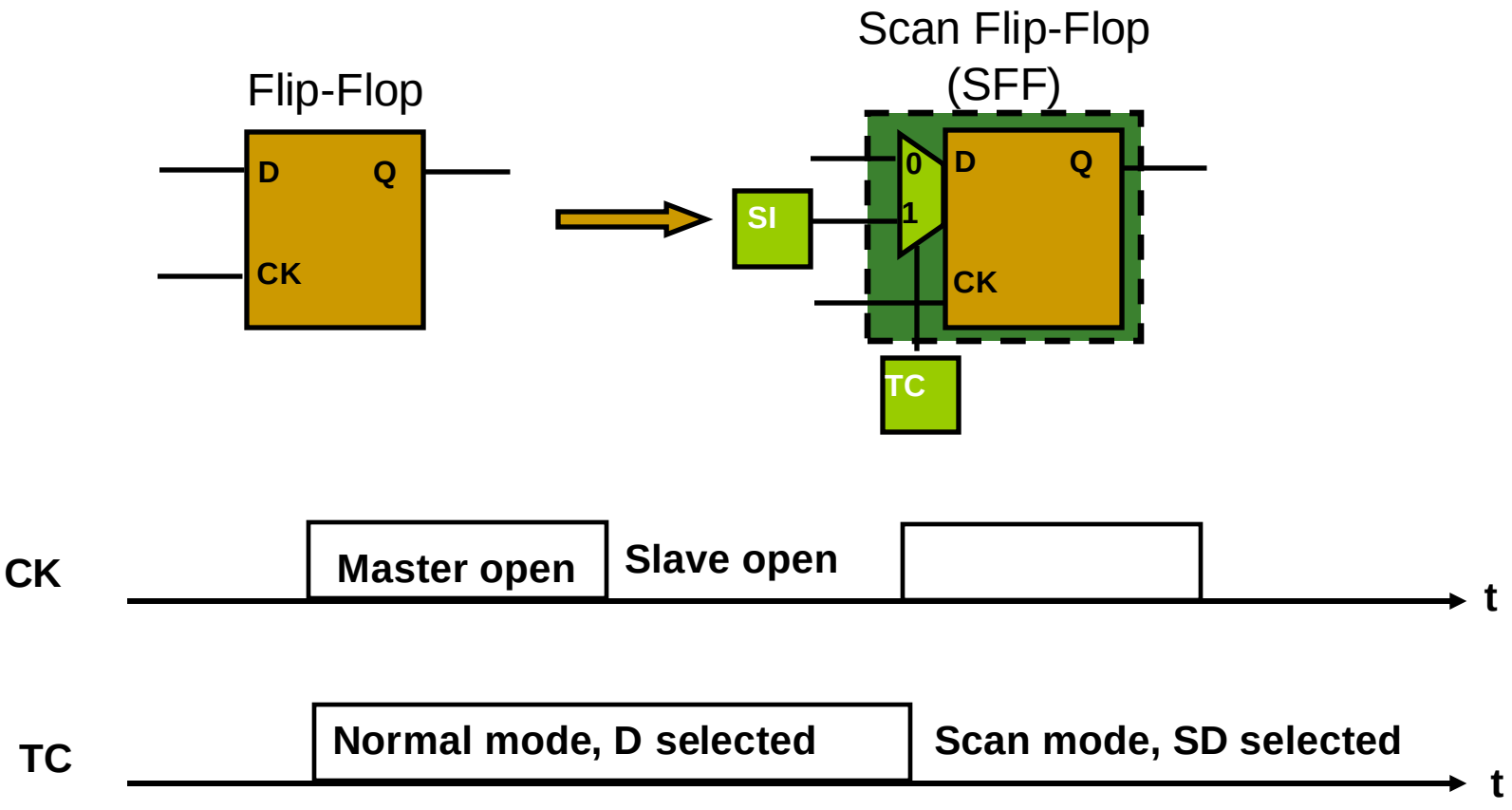
VLSI Defects



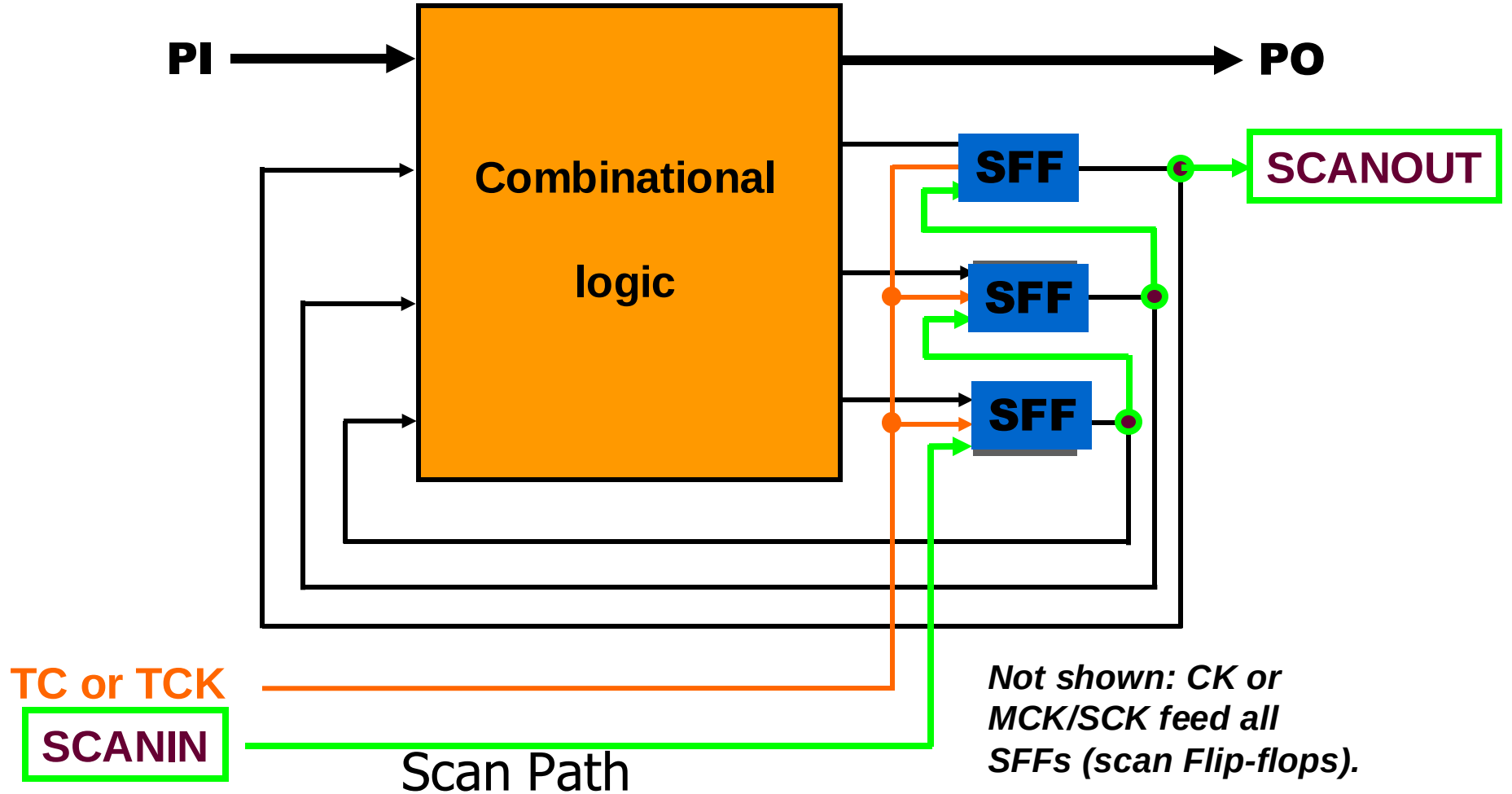
Unclustered defects
Wafer yield = 12/22 = 0.55

Clustered defects (VLSI)
Wafer yield = 17/22 = 0.77

Scan Flip-Flop

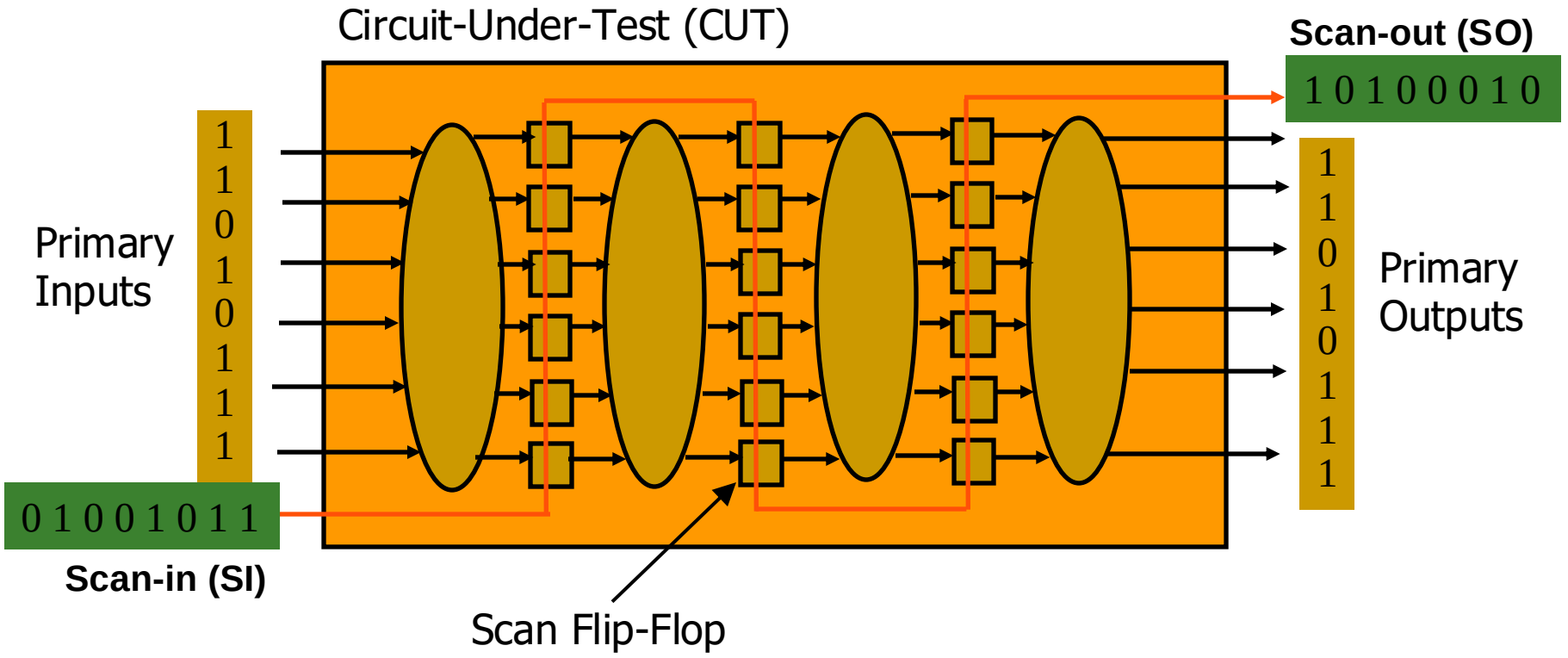


Adding Scan Structure



Scan Path
Also called Scan Chain

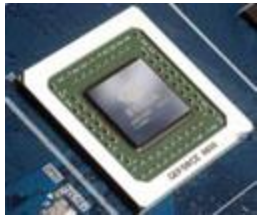
Scan Design



Structural Test Method – Extremely efficient

ADVANTEST Model T6682 ATE

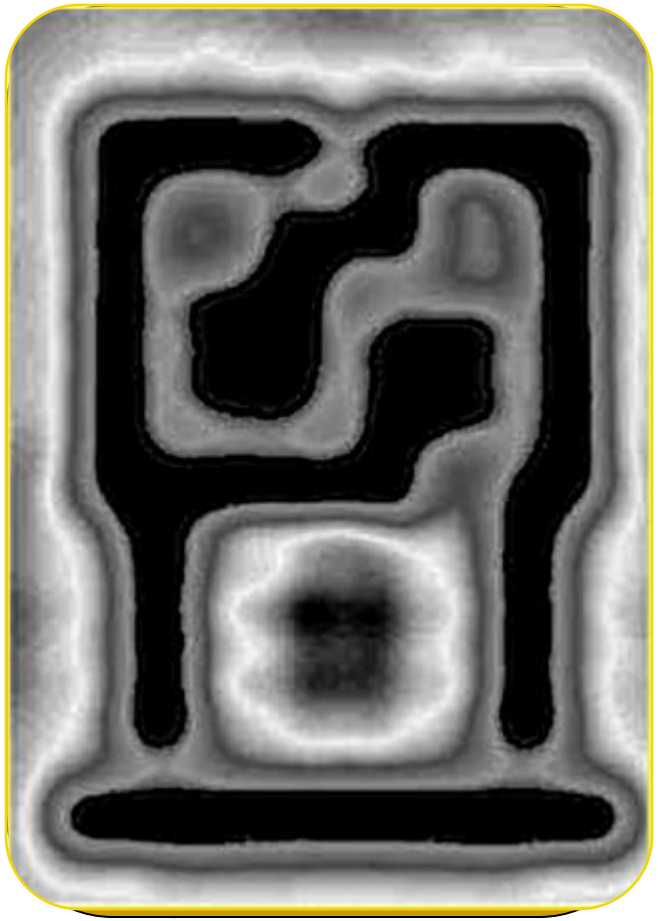
Test Head



Testers are very expensive ($150K – $20M)

WYSINWYG

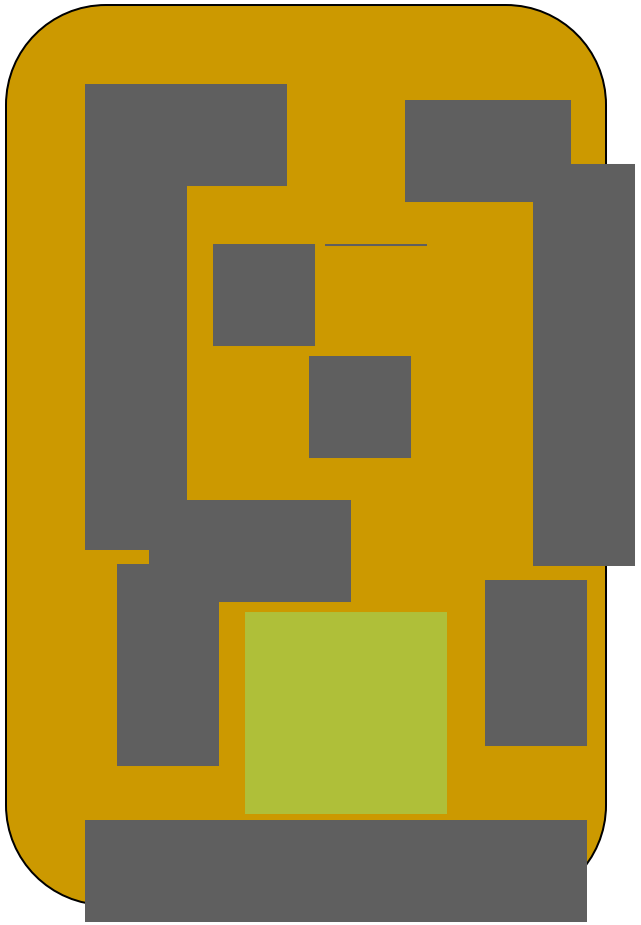
Sub-Wavelength WYSINWYG

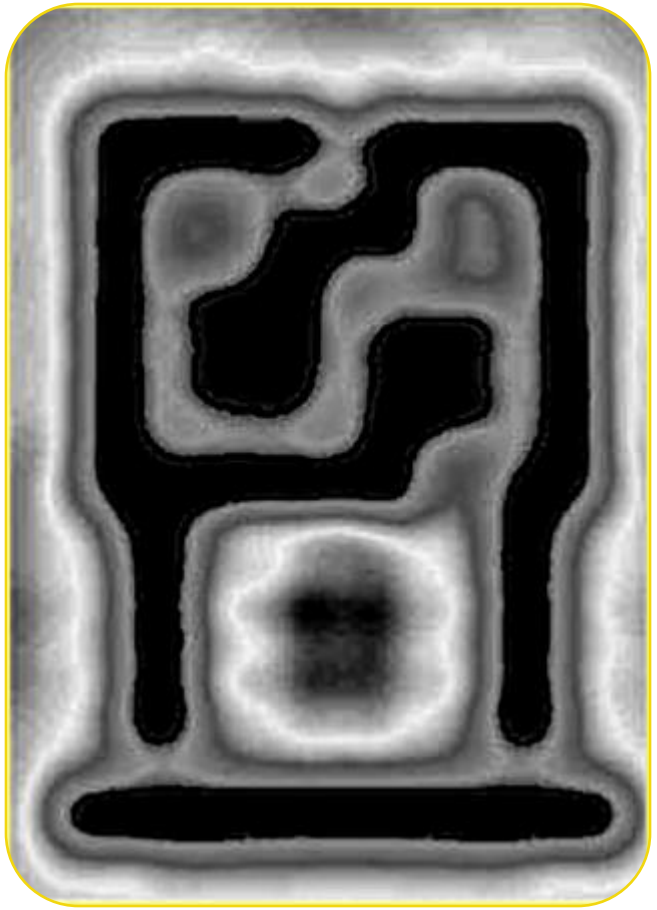


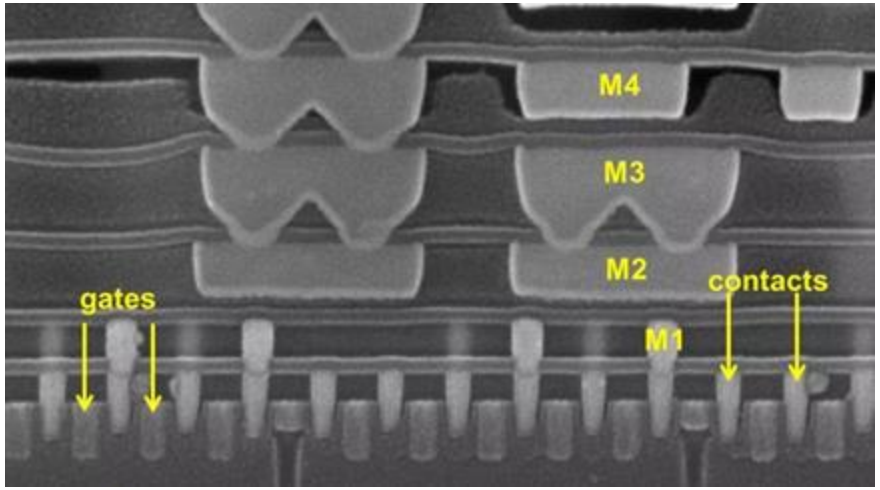
What You See Is Not What You Get

Process variations

No two transistors have the same parameters






M4
M3
M2
M1
gates
contacts