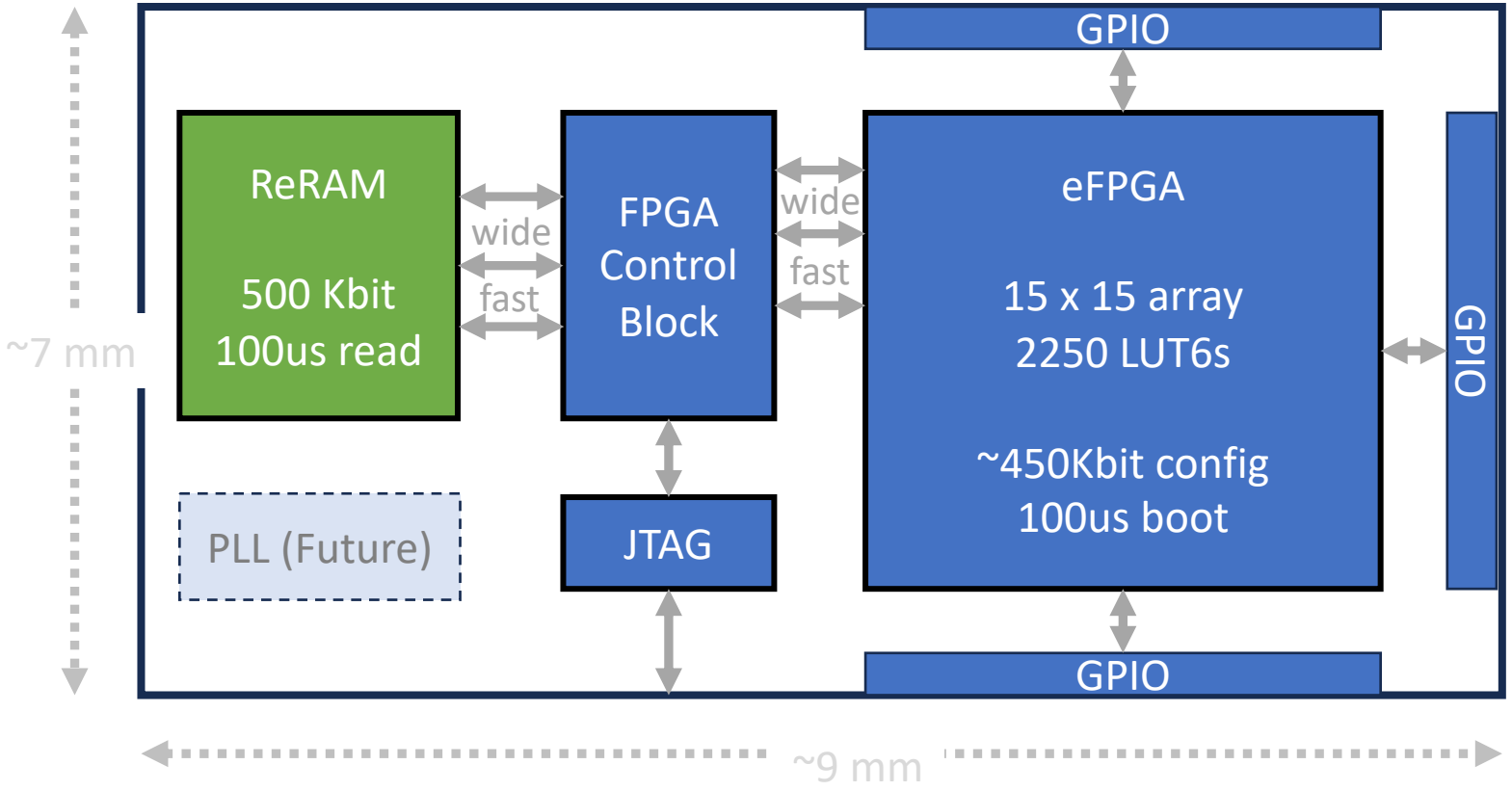
Skywater s130

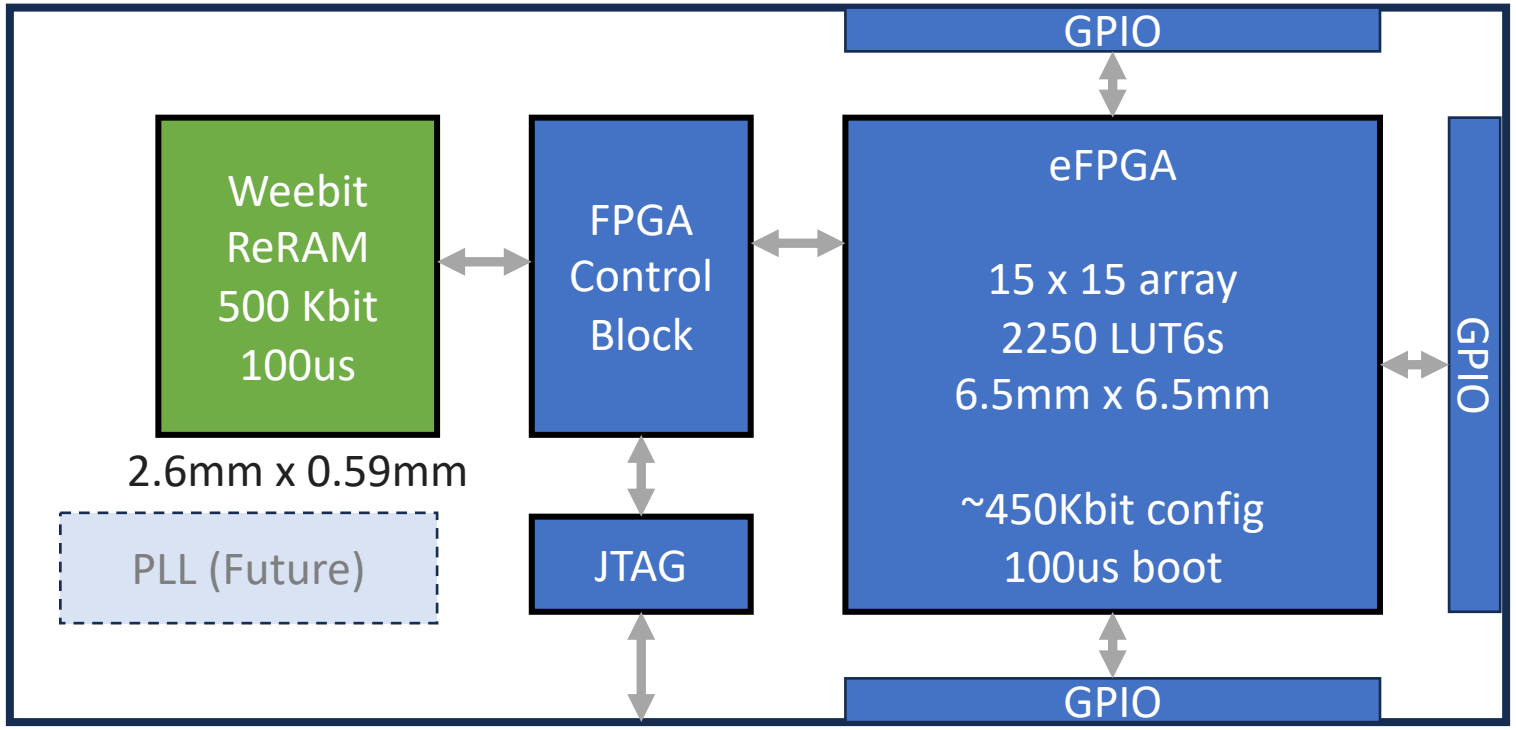
Ram Compiler?

Green: Weebit Designed Blue: QuickLogic Designed



Block Diagram

Green: Weebit Deliverable
Blue: QuickLogic Deliverable



@Andrew: smaller FPGA, RAM block (maybe KC)? TRL6/7?

12 x 12 =

438 cm/tile ⇒ 5.256 mm/side

144 tiles = 1440 cuts

288,000 bits

@ 0.5 def/cm²

= 0.3 cm² ~ 90% yield

Fudge Math based on KU8@130 & KU10@90
is ~192,280μm² / tile or ~438μm/side

15×15 CLBs is 6.577 mm/side
= 225 CLBs ≈ 2250 LUT6's
(excludes BRAMs + DSPs)

225 · 2000 bits/tile = 450 Kbit
0.5 def/cm²

= 0.43 cm² ~ 80% yield

$20 \times 20 =$

20 tiles · 438 mm/tile = 8,760 mm/side

20×20 CLBs · 10 LUTs/CLB = 4000 LUTs

excludes BRAM & DSPs

20×20 × 2k bits/tiles =

$0.5\ defect/cm^2$ 800 Kbit

$0.61\ cm^2 \Rightarrow$ 60-70% yield

Assumptions from KC/Tim:
12LP: 1 Tile: 1CLB + Routing, 10 LUT6s, 86um x 68um, ~2K bits
Not Optimized: ~60% utilization, hoping for 95%.

20K LUT: 2K Tiles, 44x45 array:
3.7mm x 3.06mm

200K LUT: 20K Tiles, 141x142 array
12mm x 9.6mm

300K LUT: 30K Tiles, 150x200 array
13mm x 13.6mm

400K LUT: 40K Tiles, 180x222
15.5mm x 15mm

500K LUT: 50K Tiles, 200 x 250
17.2mm x 17mm.

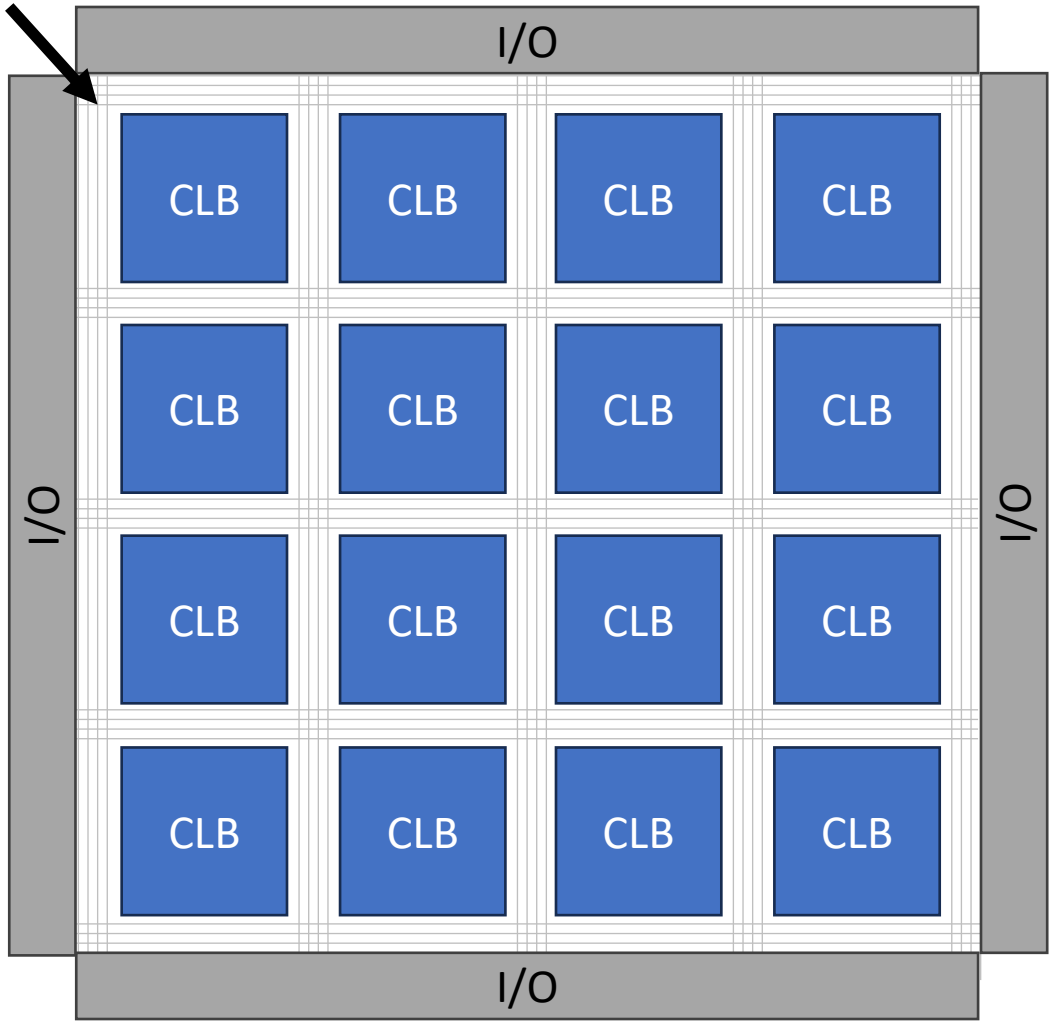
K4N8 @ 130: tile: 209um x 184um, 8 LUT4s

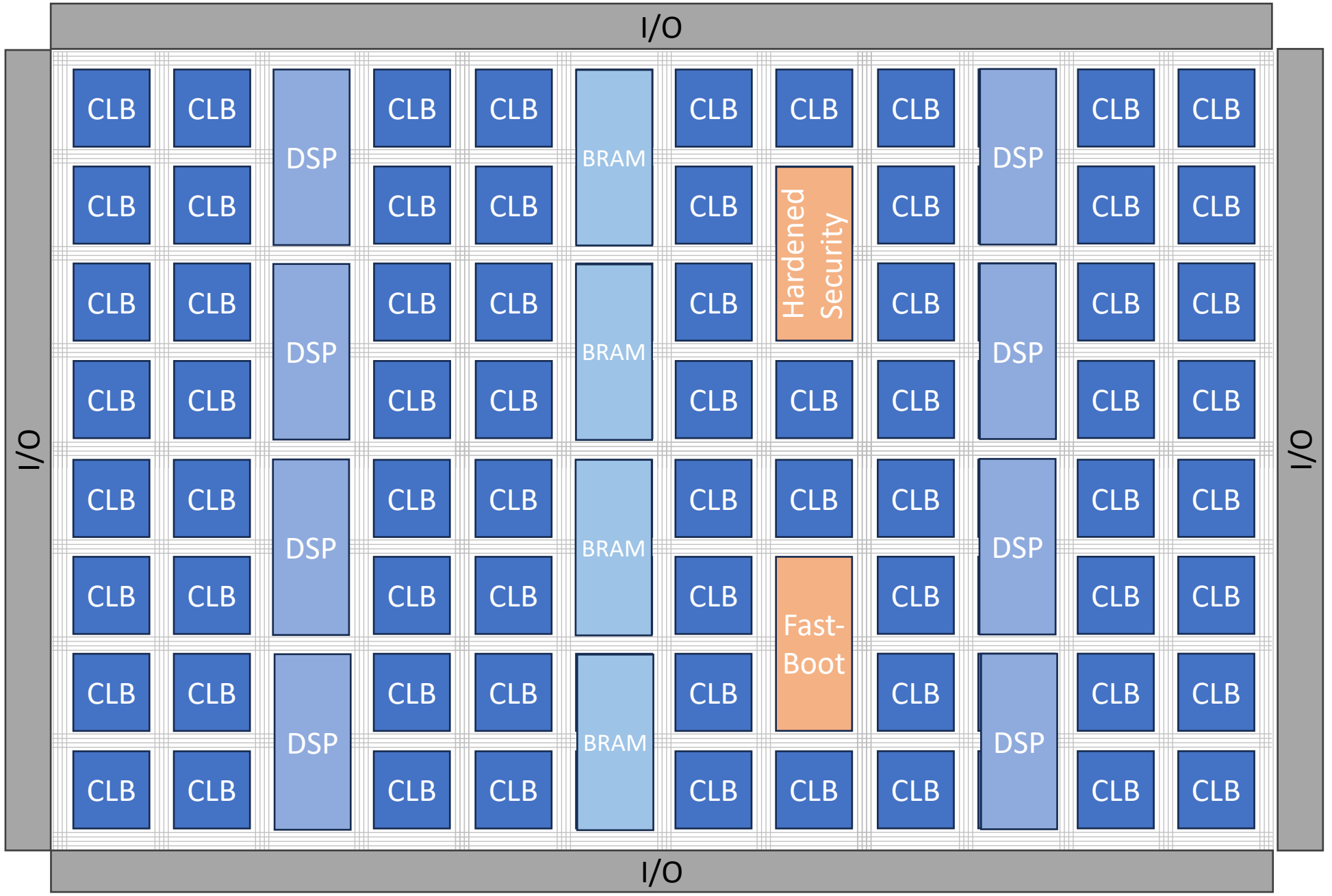
20x20 tile: 4.2mm x 3.7mm, 3200 LUT4s or 2K LUT6’s

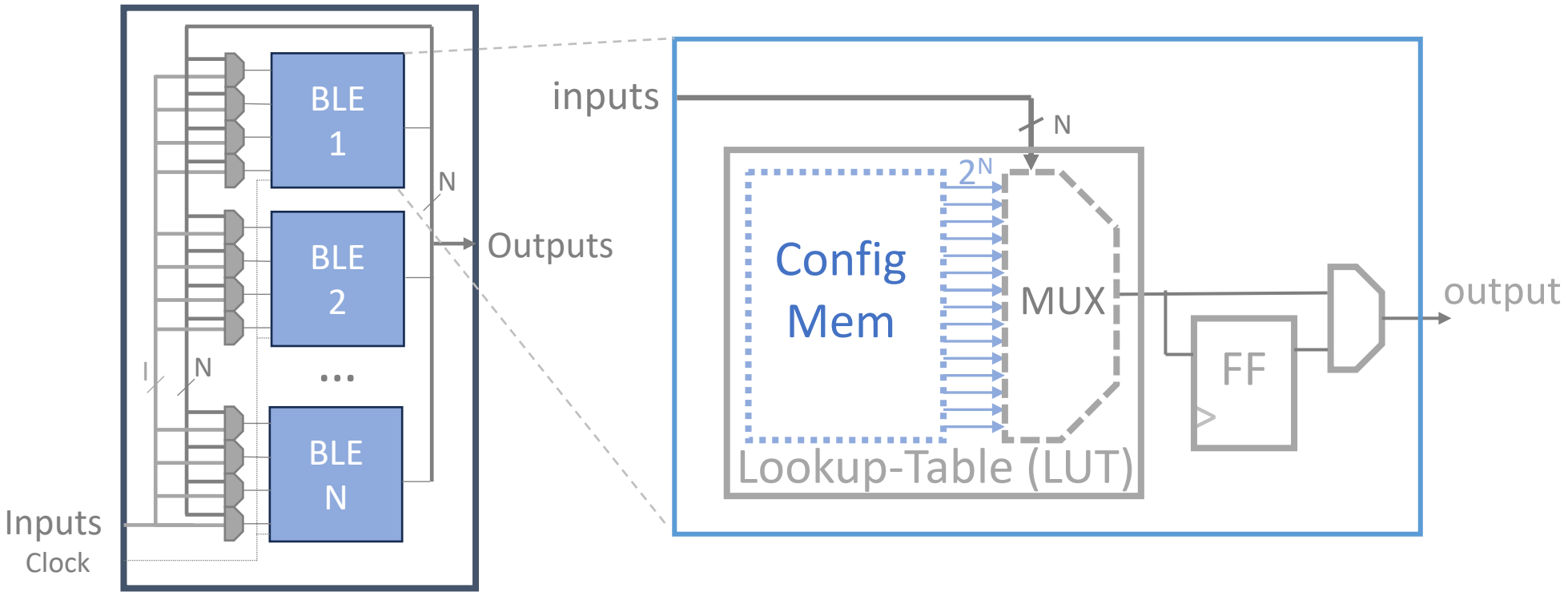
25 x 25 tile: 5.2mm x

Just say “~2K LUT6”.

Routing

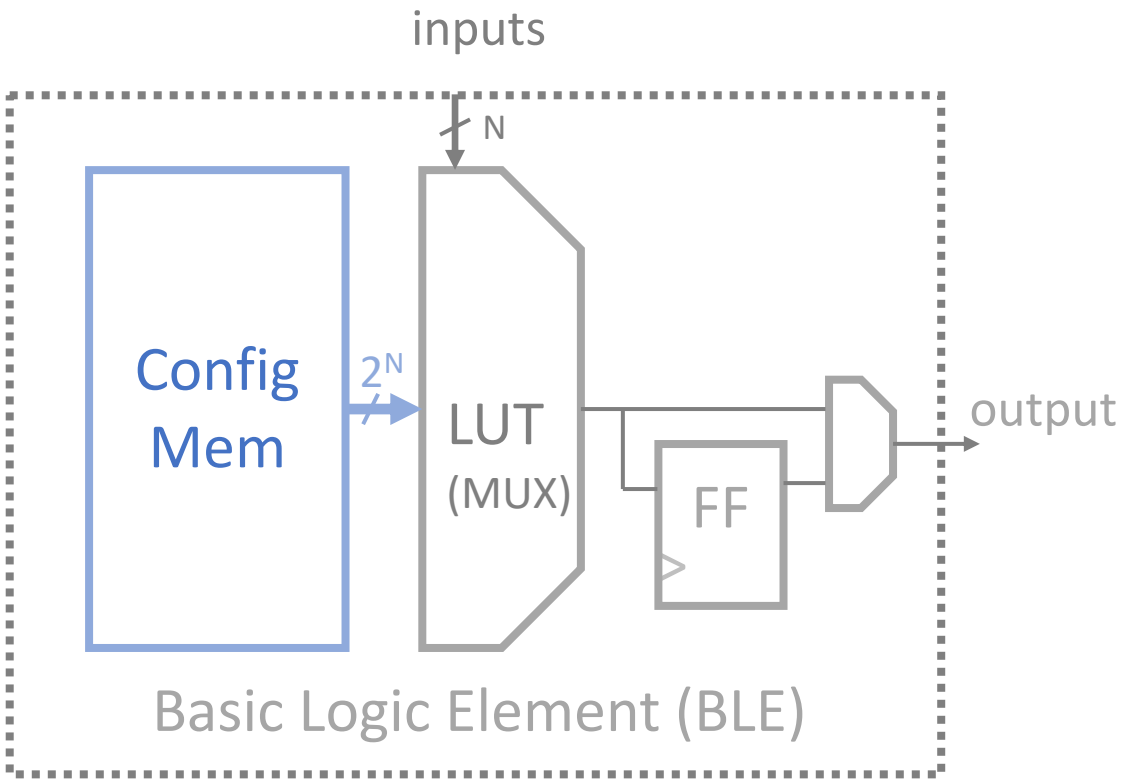

I/O
I/O
I/O
I/O
CLB
CLB
CLB
CLB
CLB
CLB
CLB
CLB
CLB
CLB
CLB
CLB
CLB
CLB
CLB
CLB

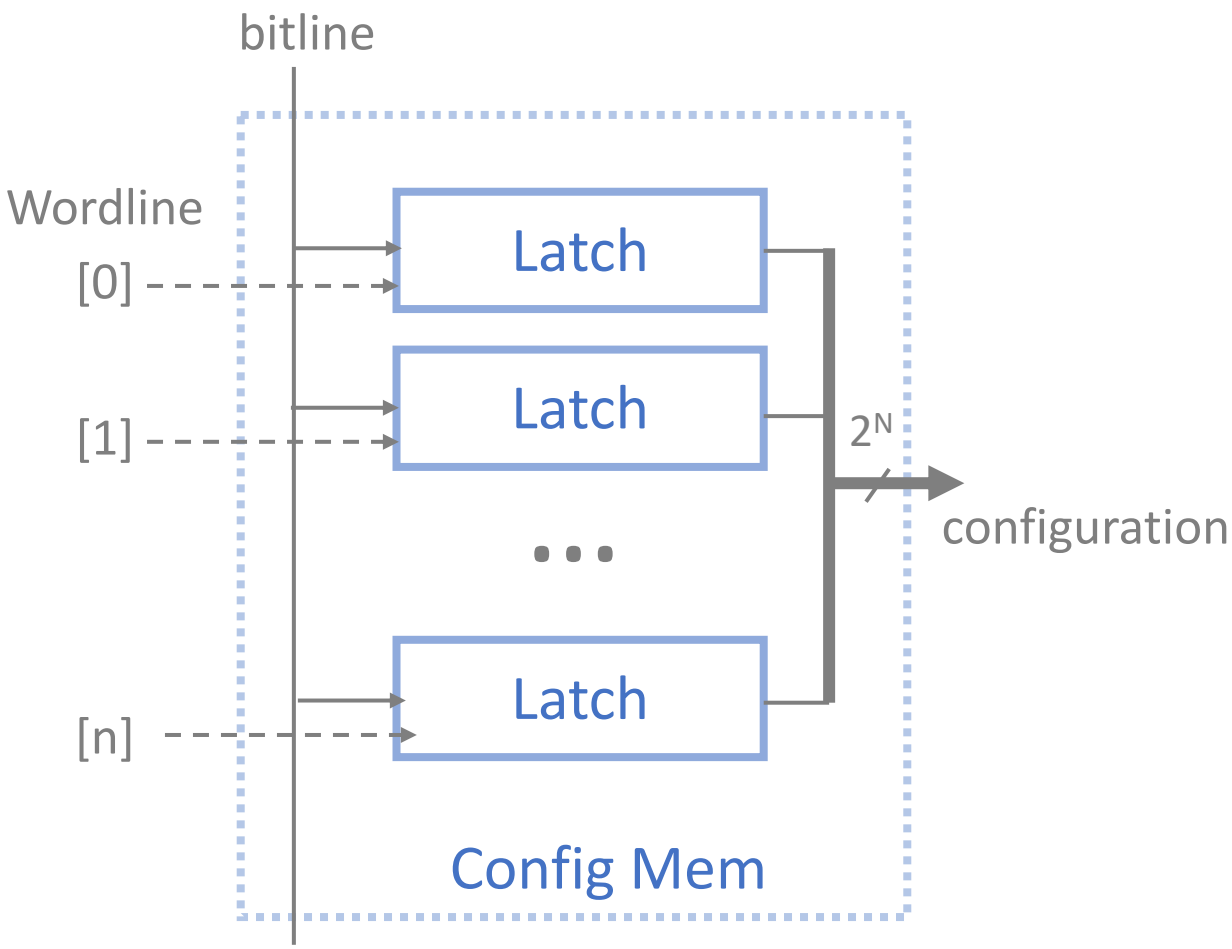

I/O
I/O
I/O
I/O
CLB
DSP
BRAM
Hardened Security
Fast-Boot

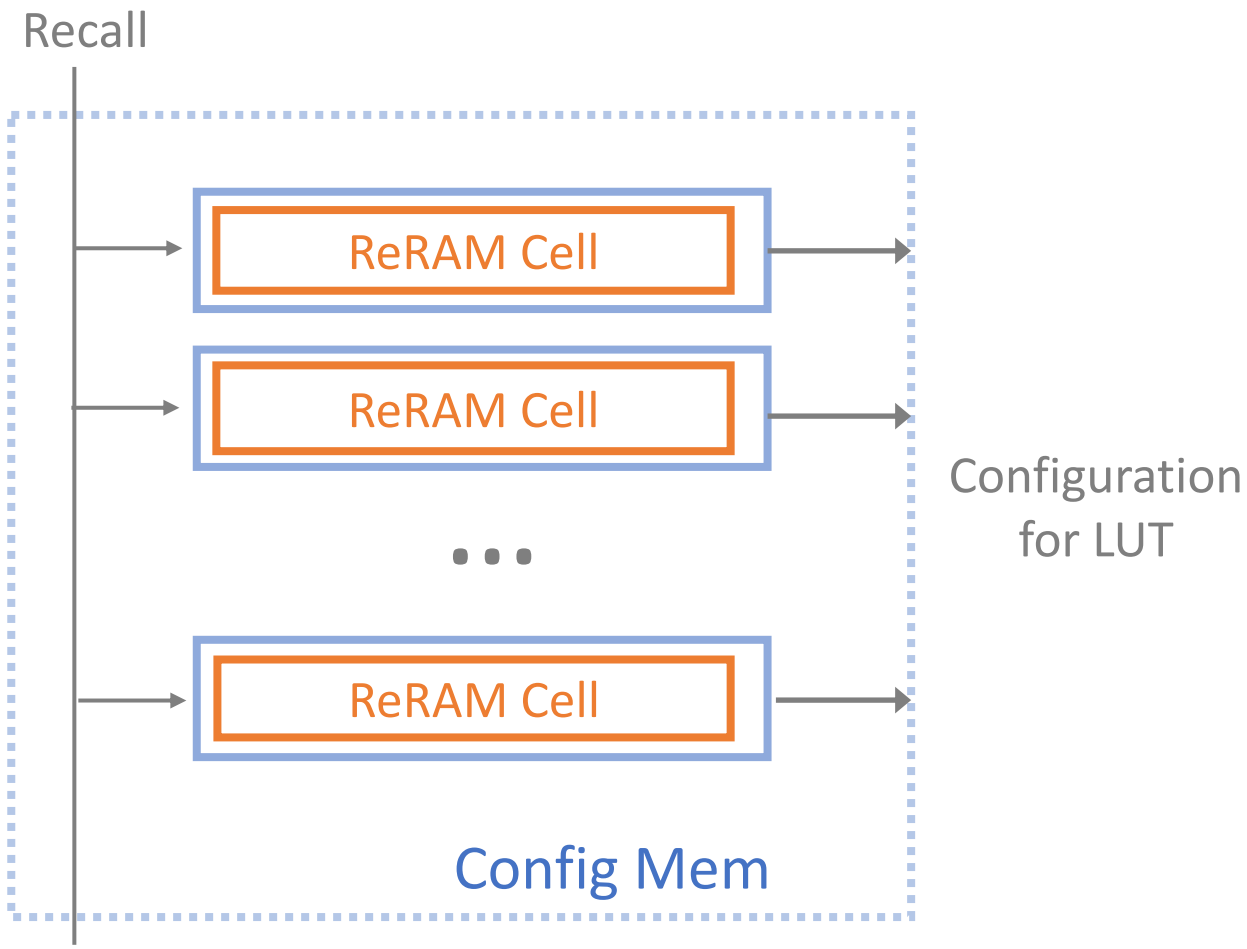


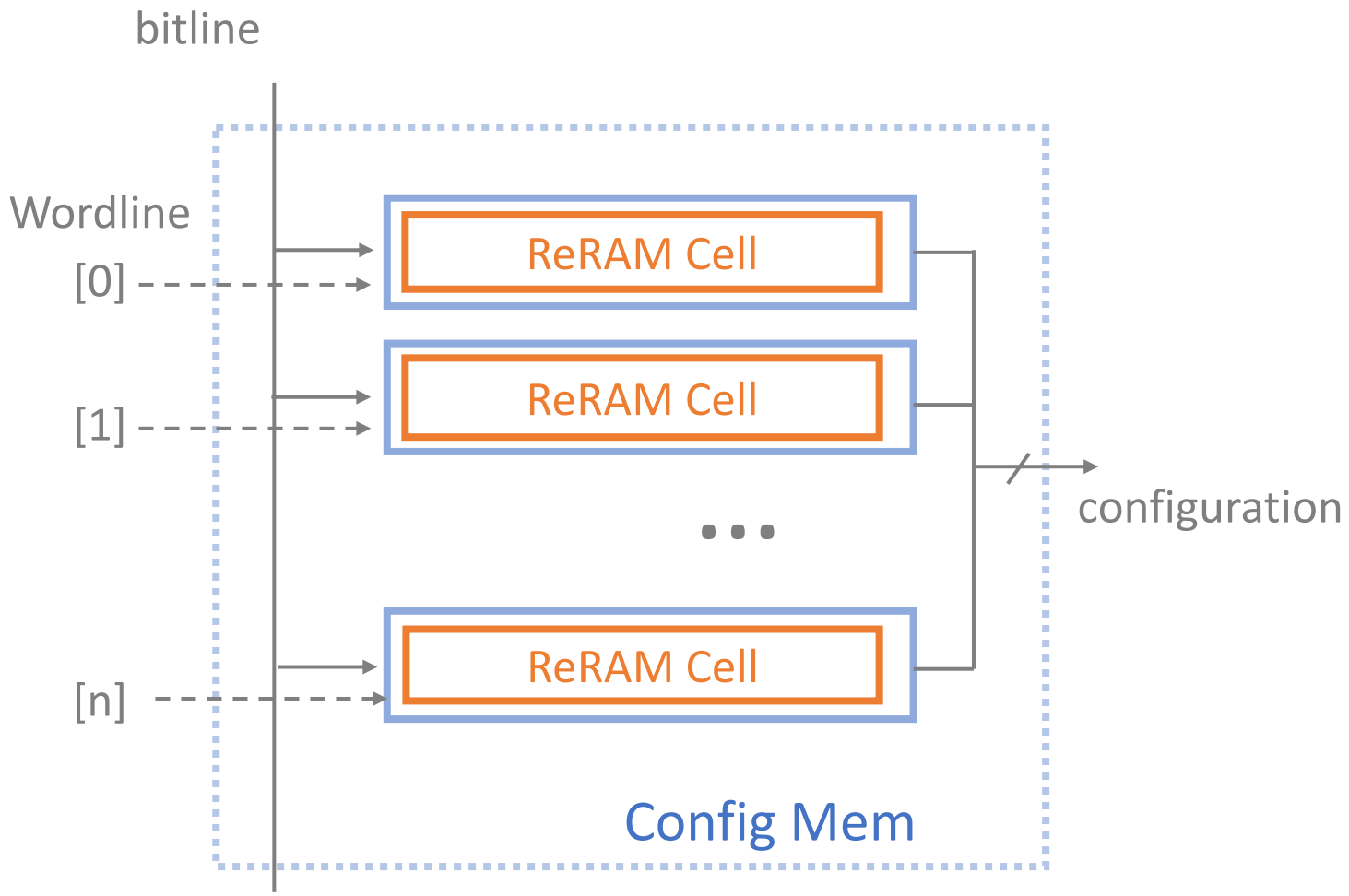
Configurable Logic Block (CLB)

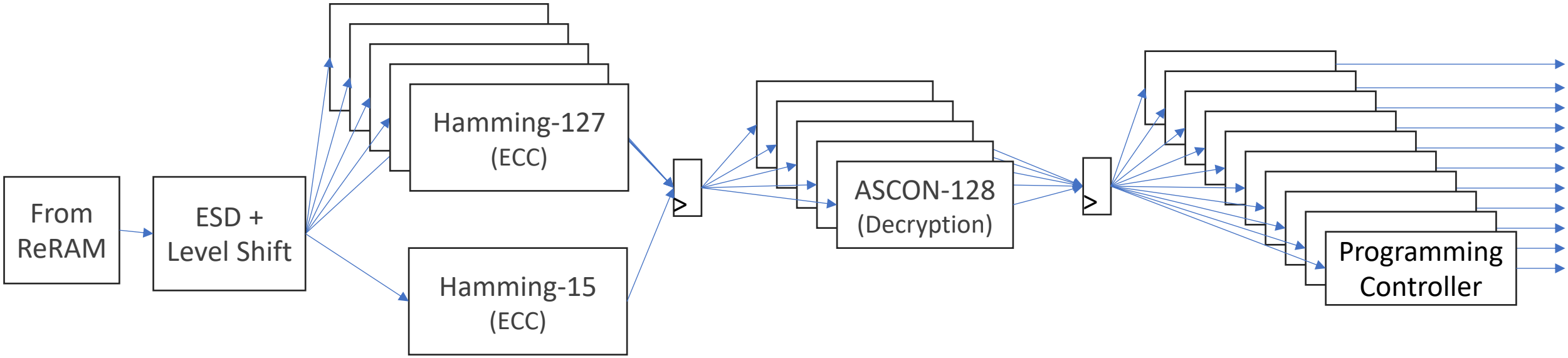
Basic Logic Element (BLE)


inputs
N
Config Mem
2^N
LUT
(MUX)
FF
output
Basic Logic Element (BLE)

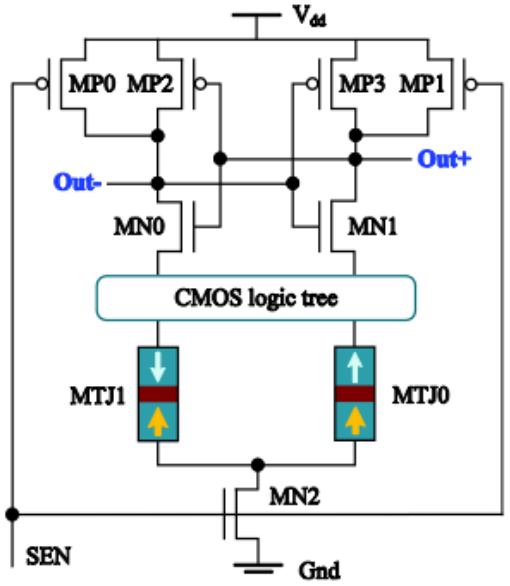

bitline
Wordline
[0]
[1]
[n]
Latch
Latch
Latch
2^N
configuration
Config Mem

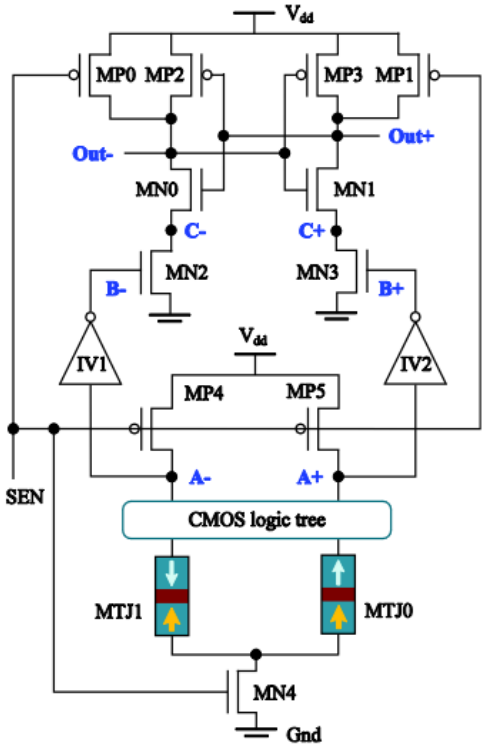

Recall
ReRAM Cell
ReRAM Cell
ReRAM Cell
Configuration
for LUT
Config Mem

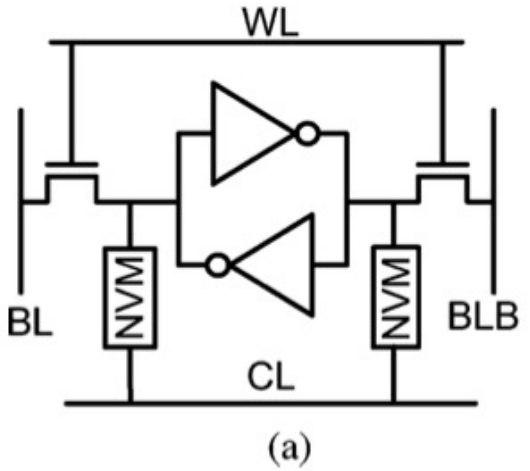

bitline
Wordline
[0]
[1]
[n]
ReRAM Cell
ReRAM Cell
ReRAM Cell
configuration
Config Mem

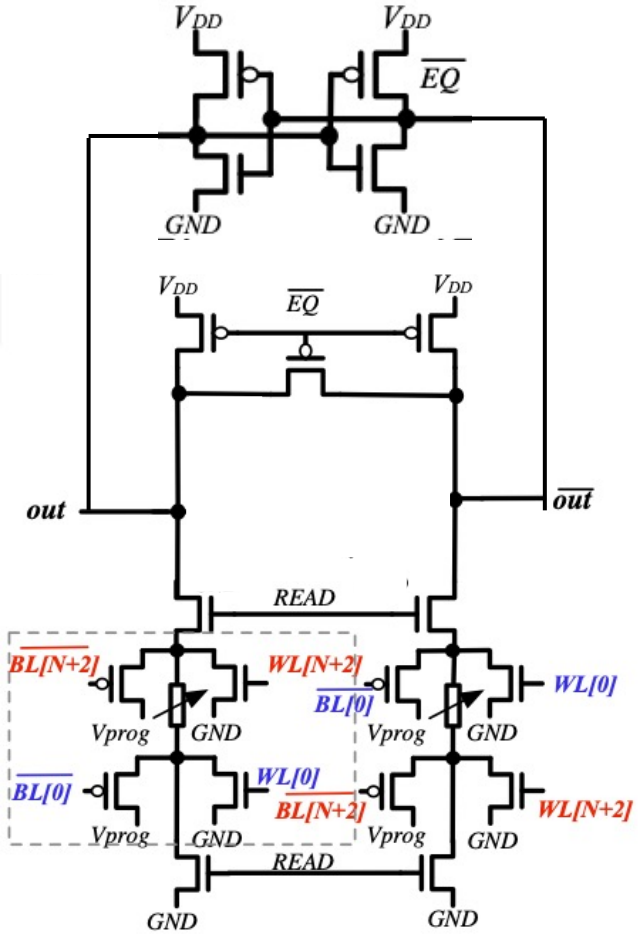

From ReRAM
ESD + Level Shift
Hamming-127 (ECC)
Hamming-15 (ECC)
ASCON-128 (Decryption)
Programming Controller

- ReDraw


Vdd
MP0 MP2
MP3 MP1
Out-
Out+
MN0
MN1
CMOS logic tree
MTJ1
MTJ0
MN2
SEN
Gnd

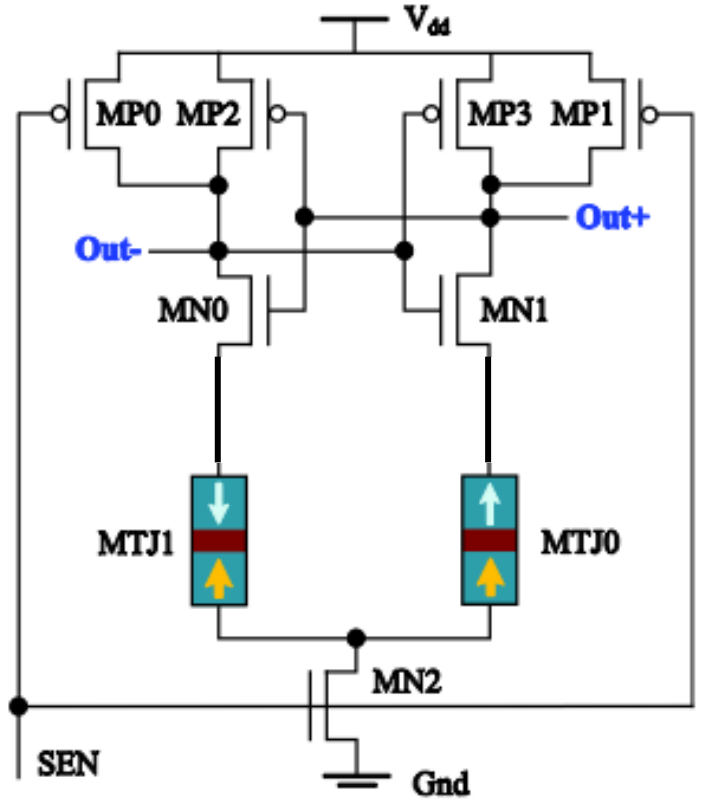

Vdd
MP0 MP2
MP3 MP1
Out-
Out+
MN0
MN1
C-
C+
MN2
MN3
B-
B+
IV1
IV2
Vdd
MP4
MP5
A-
A+
SEN
CMOS logic tree
MTJ1
MTJ0
MN4
Gnd


WL
BL
NVM
NVM
BLB
CL
(a)

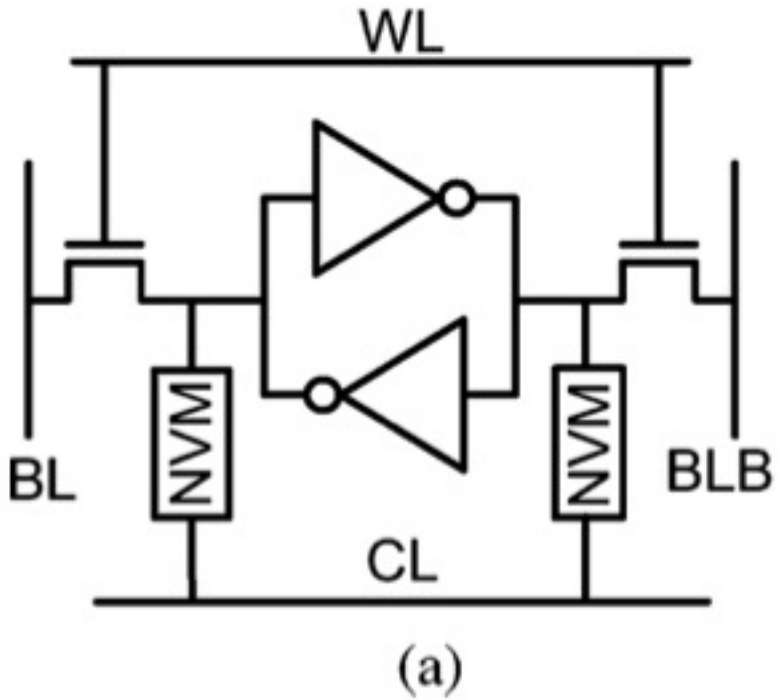

VDD
VDD
EQ
GND
GND
VDD
EQ
VDD
out
out
READ
BL[N+2]
WL[N+2]
WL[0]
BL[0]
Vprog
GND
Vprog
GND
BL[0]
WL[0]
WL[N+2]
BL[N+2]
Vprog
GND
Vprog
GND
READ
GND
GND

The basic idea is to integrate differential ReRAM cells with the latch.

Use ReRAM (not MTJs) here. ReRAM has higher yield, better resistance differences, and is cheaper to manufacture



Separated Precharge Sensing Amplifier for Deep Submicrometer MTJ/CMOS Hybrid Logic Circuits

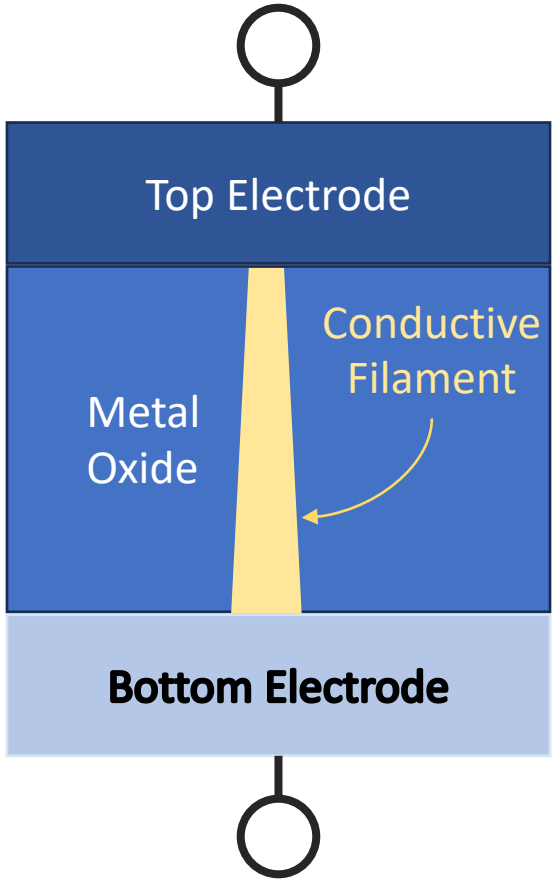


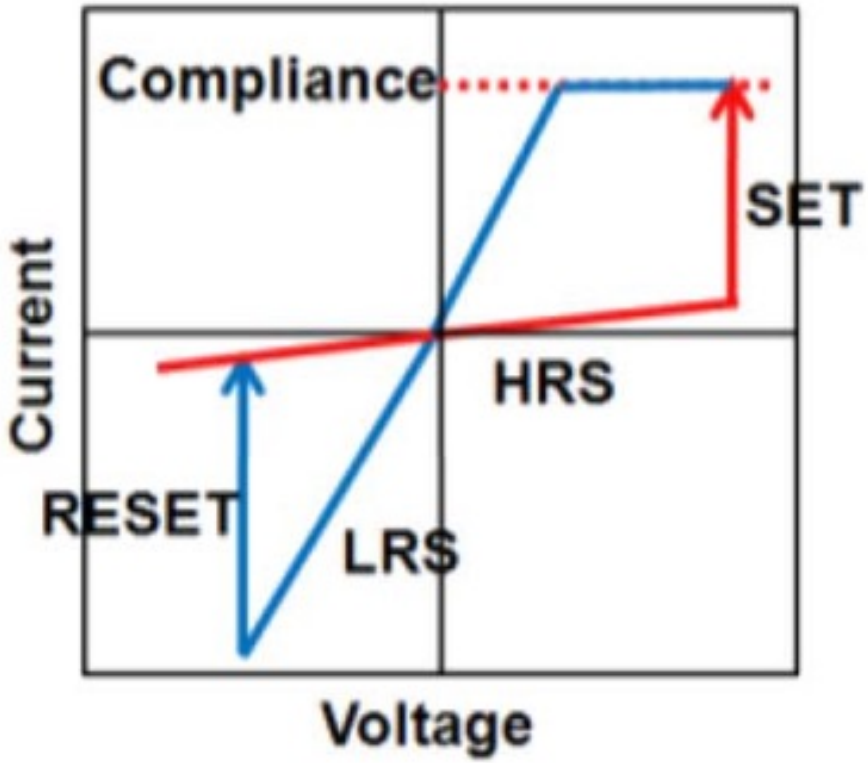
(a)

https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6197240

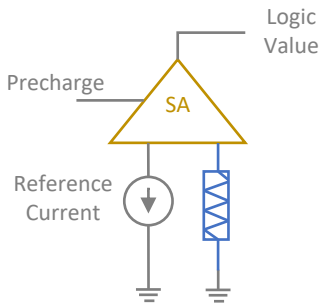
References

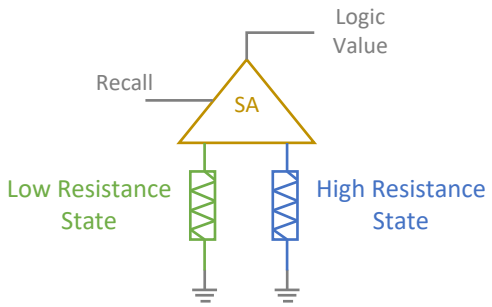
- Low Store Energy, Low VDDmin, 8T2R Nonvolatile Latch and SRAM With Vertical-Stacked Resistive Memory (Memristor) Devices for Low Power Mobile Applications
- Ultra-low-power RRAM-based FPGA: A Road towards Reconfigurable Edge Computing
- Energy/Reliability Trade-Offs in Low-Voltage ReRAM-Based Non-Volatile Flip-Flop Design

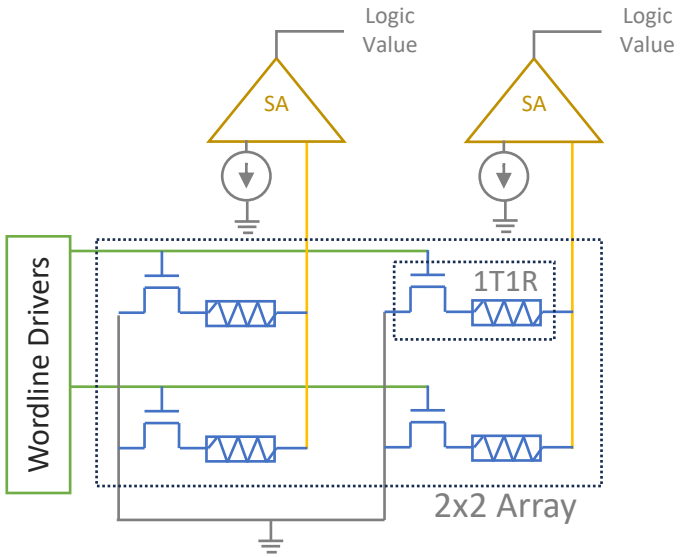

Top Electrode
Conductive
Filament
Metal
Oxide
Bottom Electrode


Compliance
SET
HRS
RESET
LRS
Current
Voltage

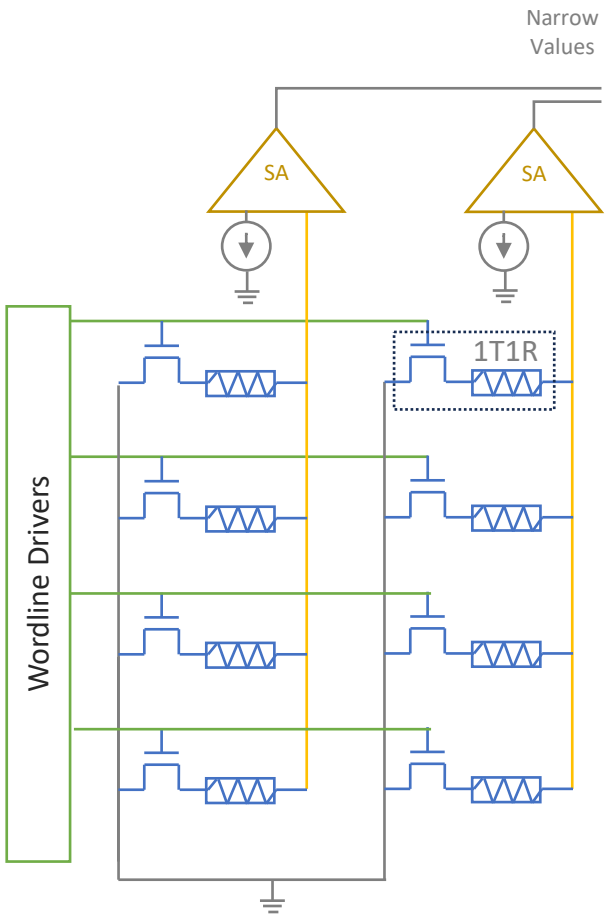
(c)


Logic
Value
Precharge
SA
Reference
Current

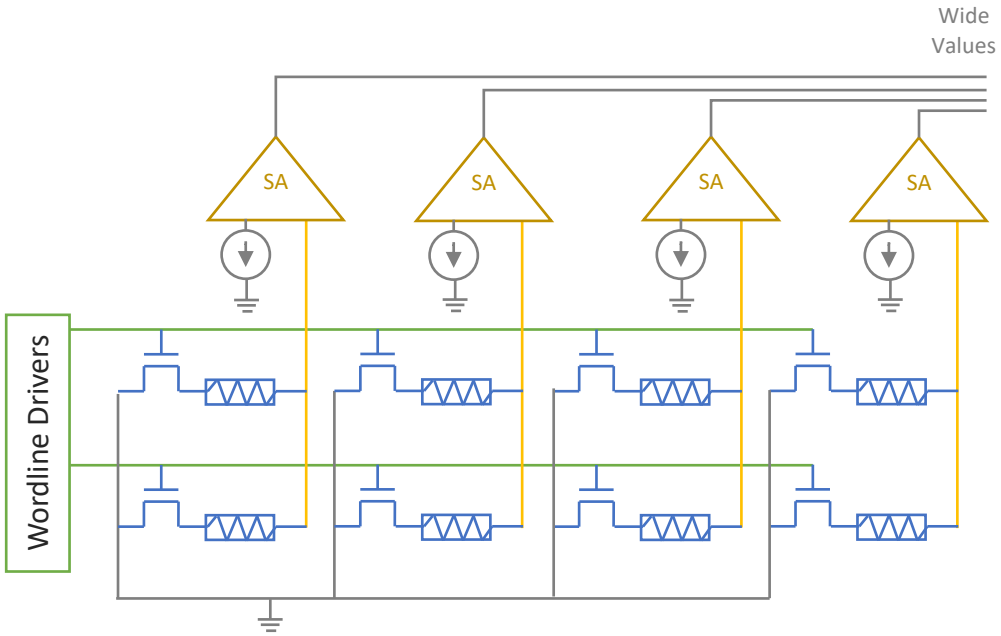

Logic
Value
Recall
SA
Low Resistance
State
High Resistance
State



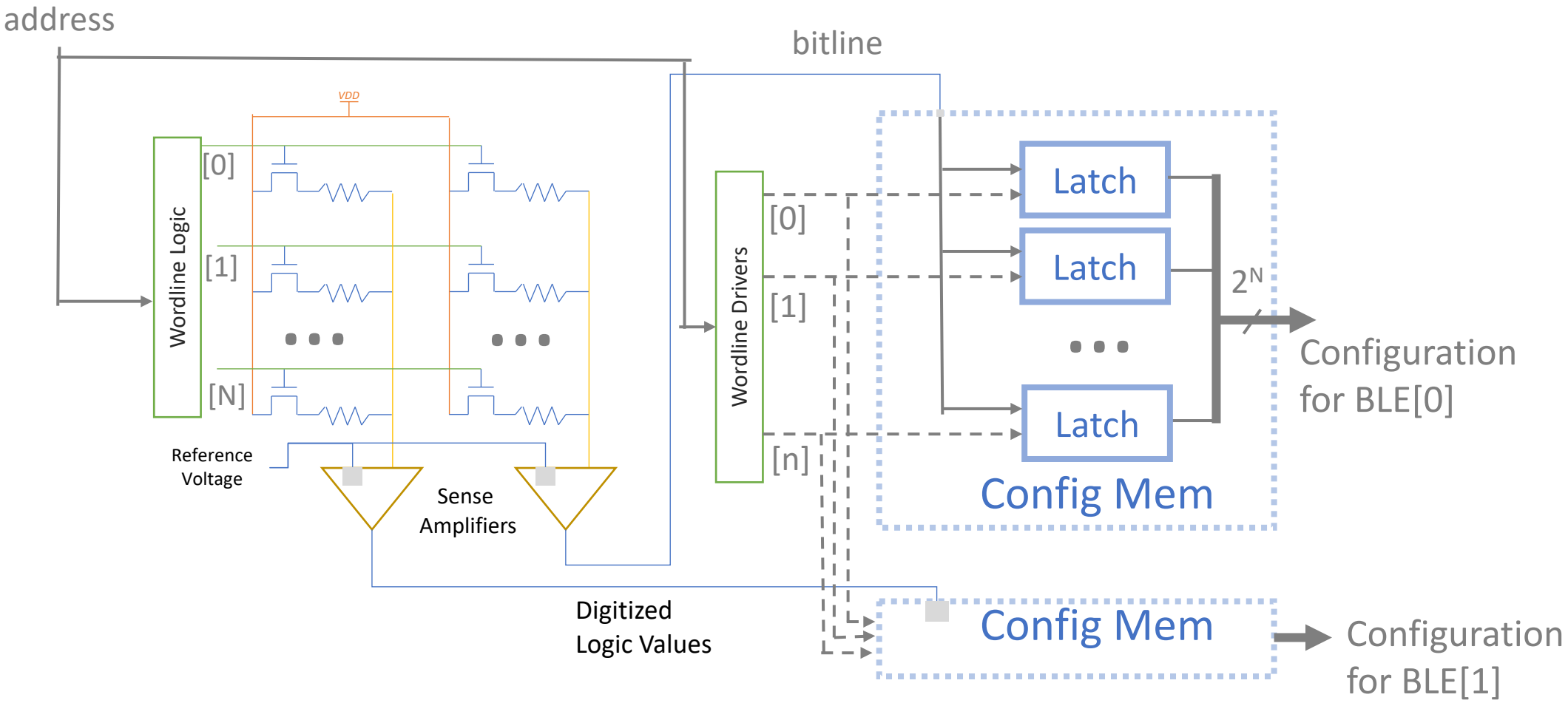
Logic
Values



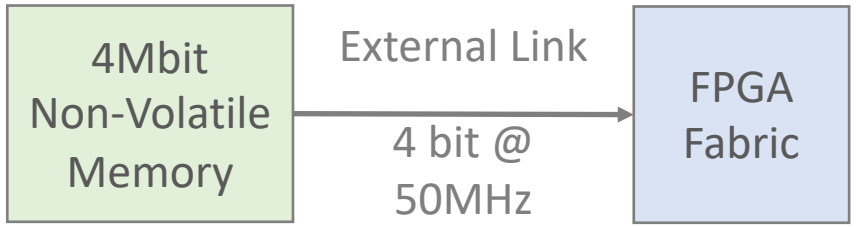
a) Typical ReRAM array
(low area overheads)



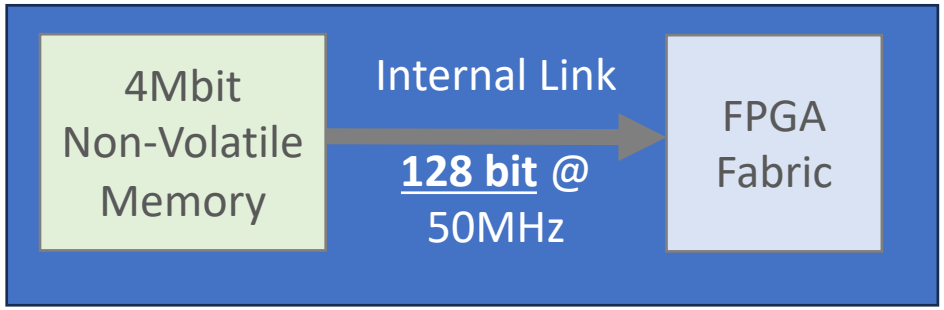
a) High-Bandwidth ReRAM array
(increases area overheads)


address
bitline
VDD
Wordline Logic
[0]
[1]
[N]
Reference
Voltage
Sense
Amplifiers
Wordline Drivers
[0]
[1]
[n]
Latch
Latch
Latch
2^N
Config Mem
Configuration
for BLE[0]
Digitized
Logic Values
Config Mem
Configuration
for BLE[1]

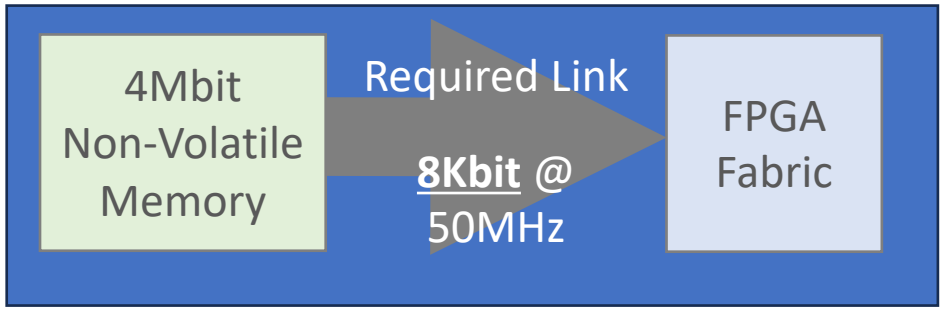
Off-Chip Connection
20ms



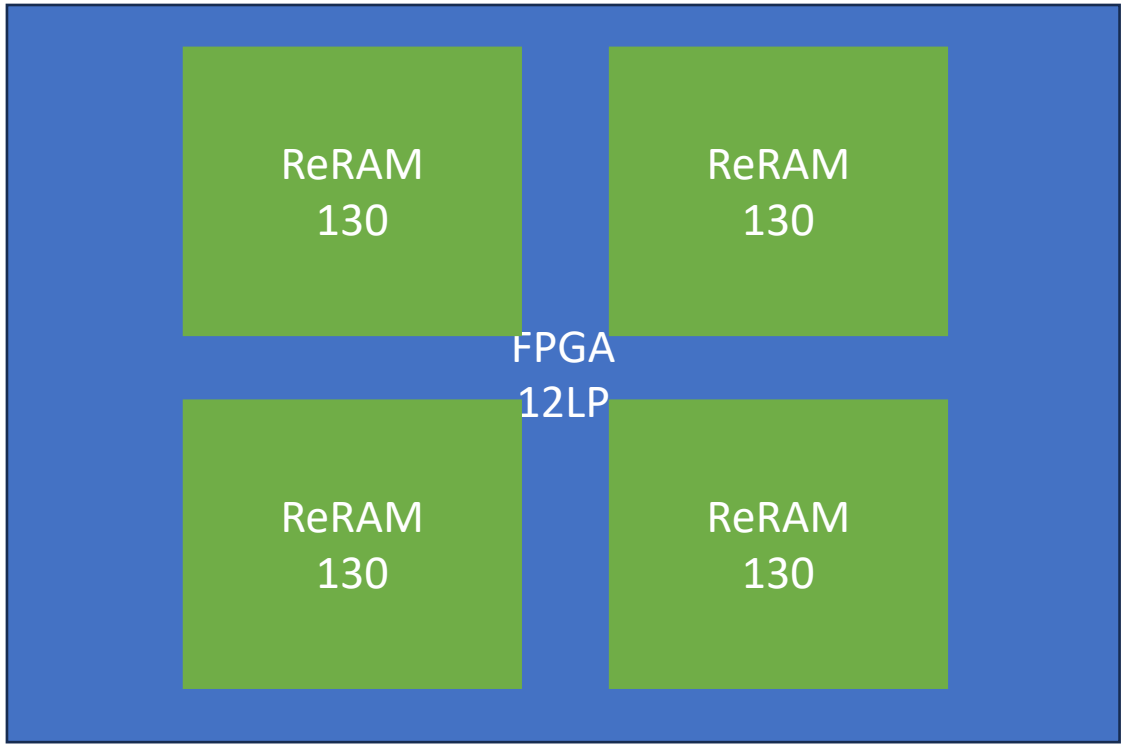
On-Chip Connections
625us



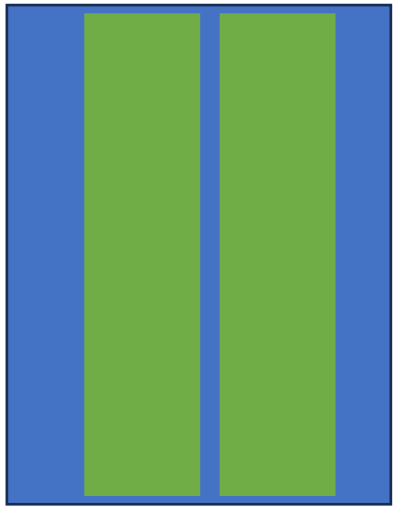
Required Link
10us




ReRAM- 130
ReRAM - 130
FPGA - 12LP


ReRAM
130
ReRAM
130
FPGA
12LP
ReRAM
130
ReRAM
130

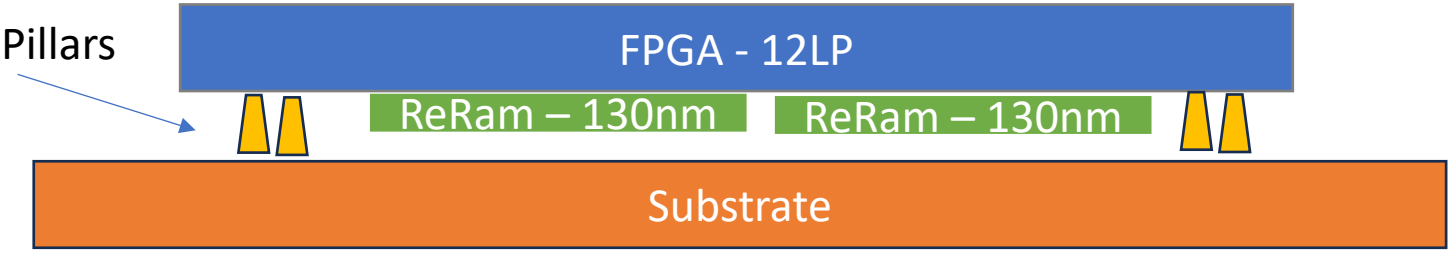
Top View:



FPGA:
12LP

ReRAM – 130nm

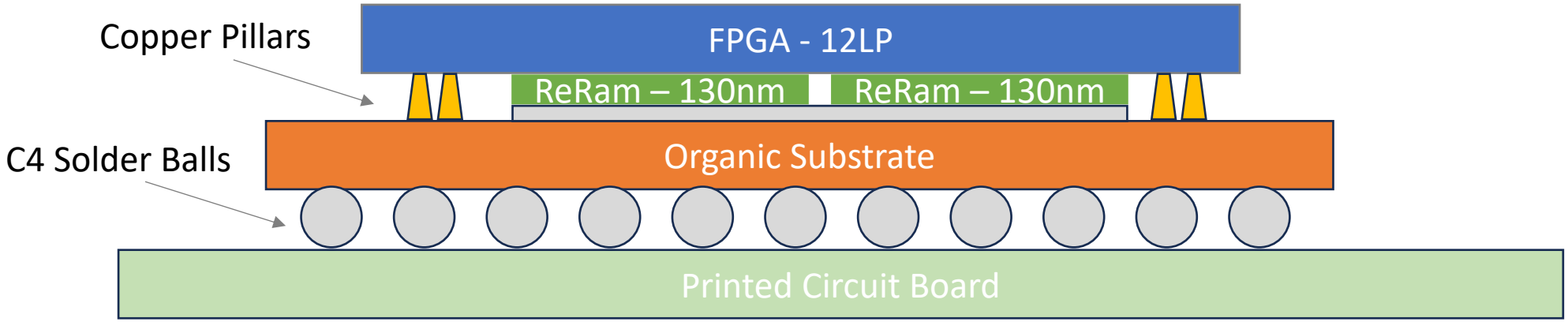
Copper Pillars

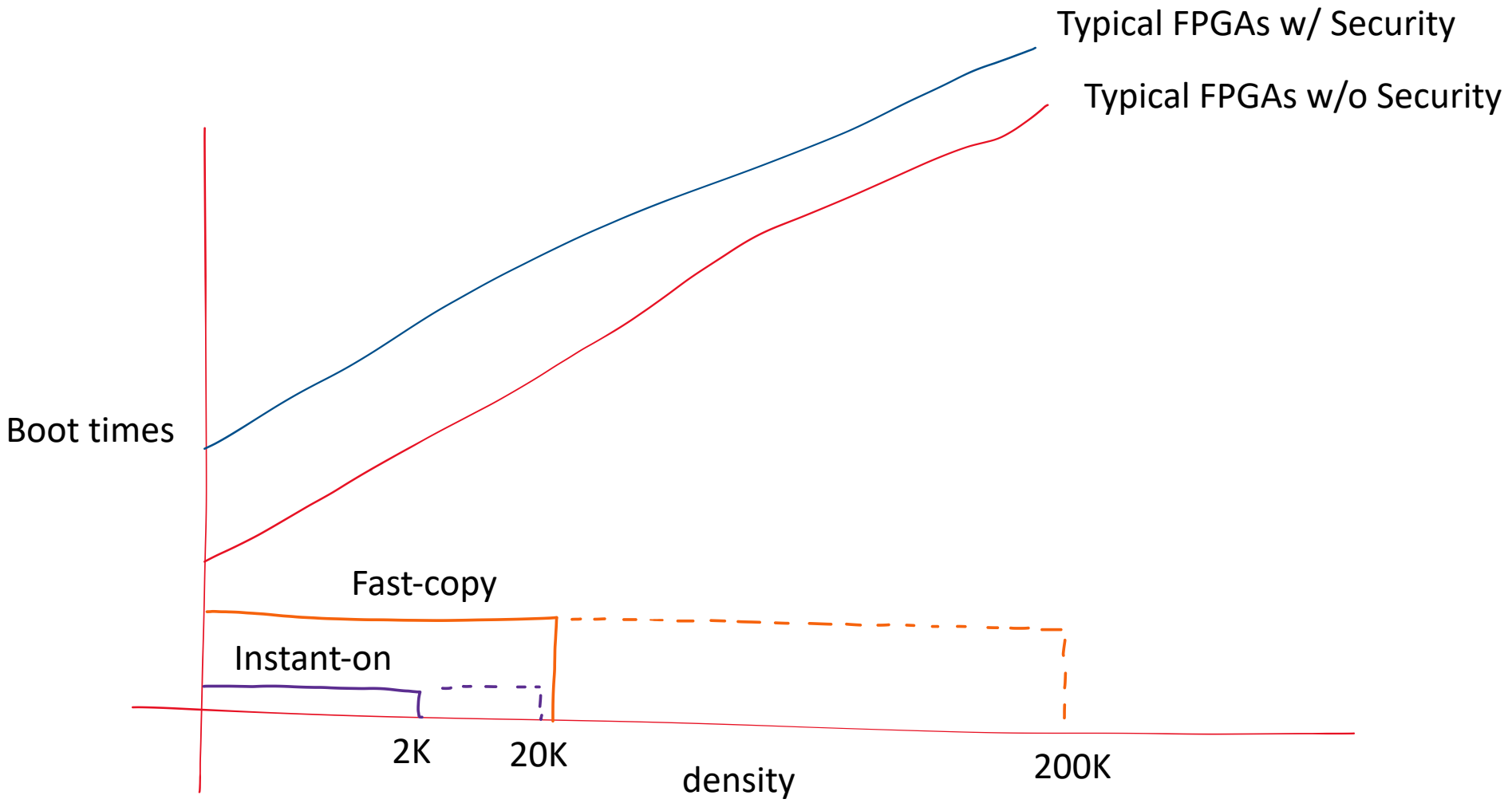


Side View:

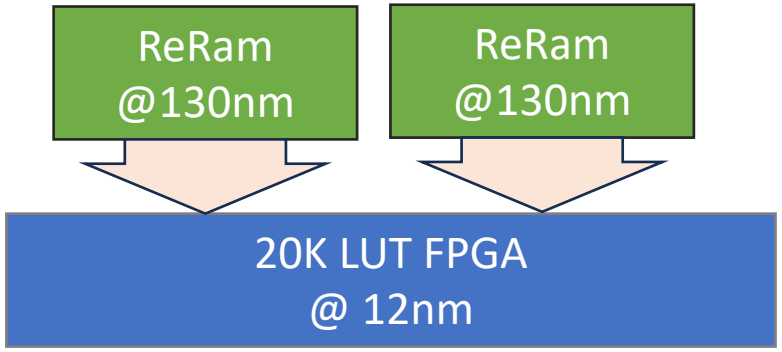
ReRAM: 2.6mm x 0.6 mm
FPGA die: 2.7mm x 2.2mm
Connectivity: ~150 signals from ReRAM die to FPGA (x2 ReRAM die)


ReRam @ 130nm
640 bit
Fast Copy
@ Boot
ReRam @ 130nm
640 bit
FPGA Die @ 12nm

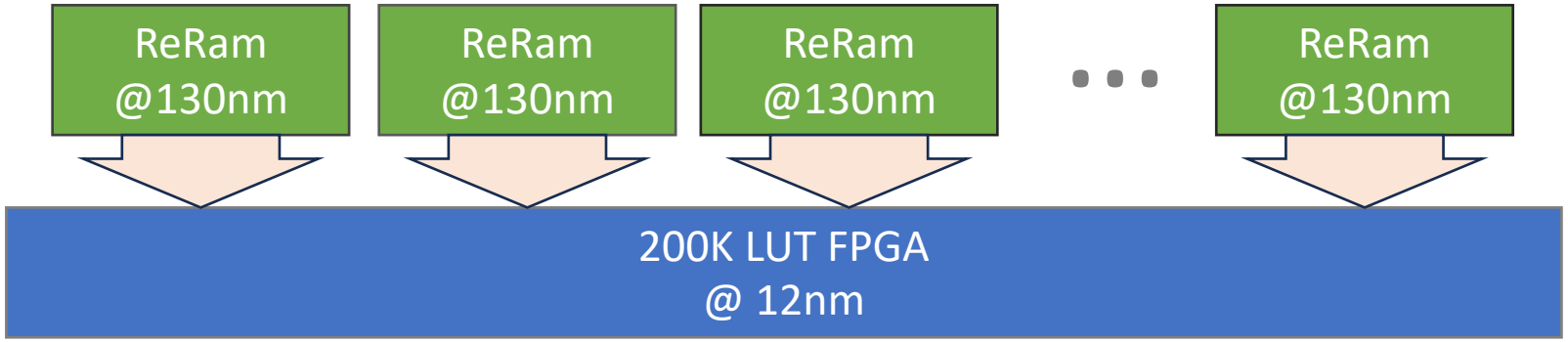

Copper Pillars
FPGA - 12LP
ReRam – 130nm
ReRam – 130nm
C4 Solder Balls
Organic Substrate
Printed Circuit Board

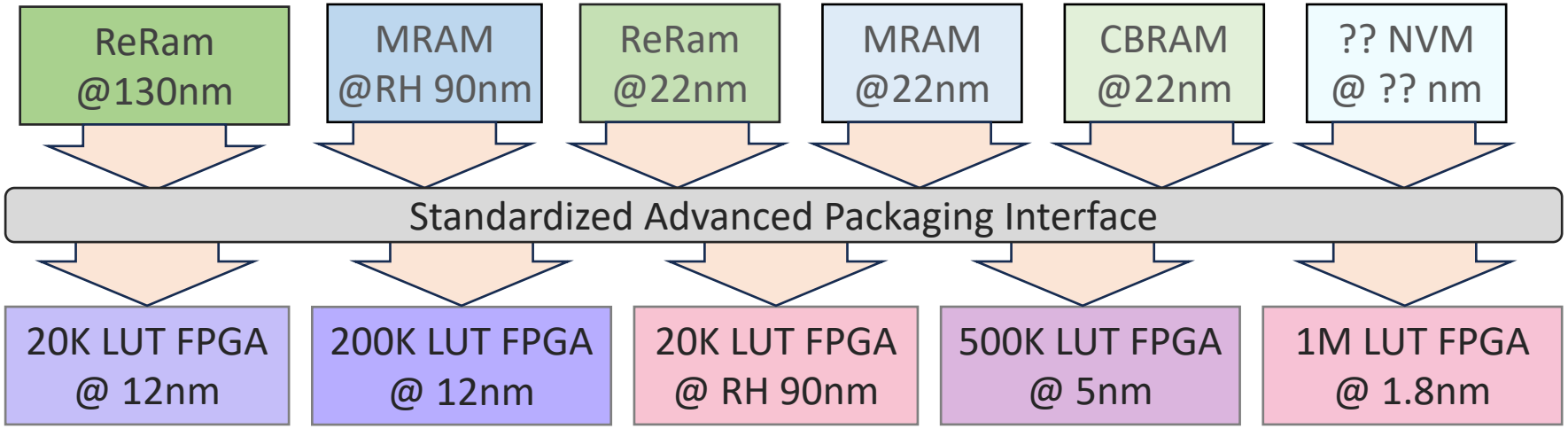

Typical FPGAs w/ Security
Typical FPGAs w/o Security
Boot times
Fast-copy
Instant-on
2K
20K
density
200K

Demonstration System
<100us boot



Production System
<100us boot

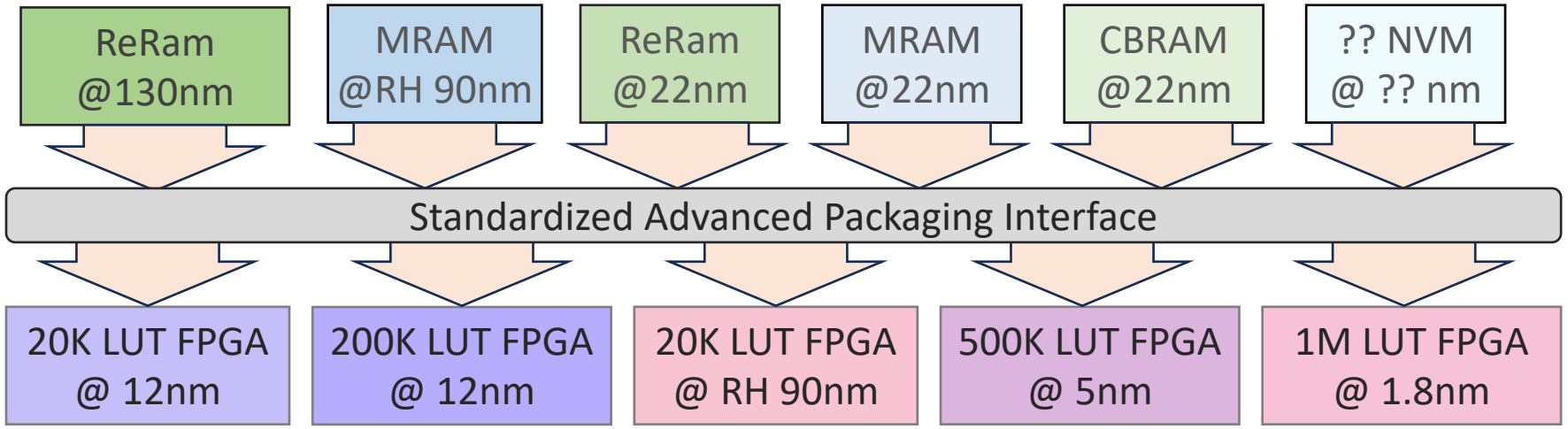


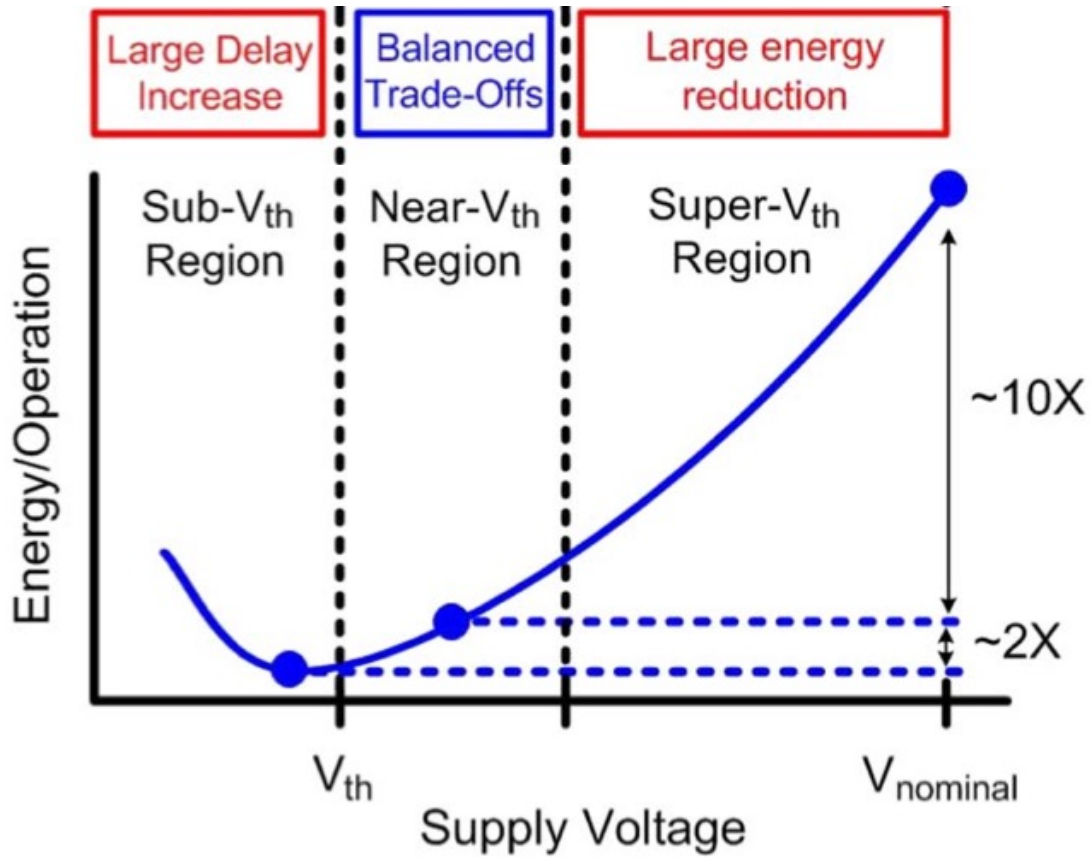


Any Non-Volatile Memory

\+ Any FPGA Fabric

Boots in <100us




Large Delay Increase
Balanced Trade-Offs
Large energy reduction
Sub-Vth Region
Near-Vth Region
Super-Vth Region
Energy/Operation
~10X
~2X
Vth
Vnominal
Supply Voltage