PLL, Reset and Clocks

Monday, December 09, 2024 11:40 AM

Reset and Power Up

- Power applied. system clock stable
- E21 boot
- PHY (IPM, PCIe, DDR, D2D) FW download
- PHY (IPM, PCIe, DDR, D2D) init
- PHY output clock stable (IPM, D2D, PCIe clock)
- I3C, D2D LL sync
- Functional unit init
    - PCIe MAC
    - IPM, DDR MC
    - FLC
  - RISC-V system bring up
    - Code download
    - ETM

Chip Reset and Clock Ports

- `CB_nPOR`: Active low, power on reset. Reset PLL and clock circuitry
- `CB_nRST`: Active low, global chip reset
- `CORERSTn`: Active low, reset embedded uC
- External reset chip required to detect stable voltage level and reset timing
- OSC: 25MHz single ended reference clock for SOC PLL
- `Ref_100m_p/n`[4:0] 100MHz reference (CML/differential) for D2D high speed PLL
- `Ref_ipm`[4:0] 133.33Mhz reference single end clock for IPM PHY

External Clock Sources

Frequency	Part Number	Comment
25MHz	ASD3-25.000MHZ-LR-T	±25ppm
133.33MHz	SIT8009BI-13-18E-133.333333	±50ppm
100MHz	Si52204-A01BGMR	0.085ps rms, PCIe Gen 6

SOC Clocks

Name	Working Frequency	Source	Comment
clk1g (clk1g_slice[3:0])	1GHz ->600M	Mockingbird PLL	Main clock for each slice.
clk1g_noc, clk1g_noc_lp	1GHz -> 600M	Mockingbird PLL	NOC clock
clk_riscv	1Ghz	Mockingbird PLL	Andes CPU
clk1g_axi4tg	1Ghz	Mockingbird PLL	AXI4 traffic gen
clk_uc	200MHz	Mockingbird PLL	uC subsystem
clk_ipm	1066MHz	IPM PHY	
clk_flc1_slave	Up to 1Ghz	Mockingbird PLL or PCIe EP PHY	FLC1 slave port
clk_flc1	1Ghz	Mockingbird PLL	FLC1 core clock
clk_flc2	1Ghz	Mockingbird PLL	FLC2 core clock
clk_rc_x8[1:0]	Up to 1Ghz	RC x8 PHY	
clk_rc_x4[1:0]	Up to 1Ghz	RC x4 PHY	
ref_100m_p[1:0], ref_100m_n[1:0]	100MHz	External	100MHz differential clock for D2D PLL
ref_ipm[3:0]	133.33MHz	External	IPM PLL reference clock
ep_cxl_ref_p[3:0], ep_cxl_ref_n[3:0]	100MHz	External	PCIe/CXL endpoint PHY reference clock
rc_cxl_ref_p[1:0], rc_cxl_ref_n[1:0]	100MHz	External	PCIe/CXL RC PHY reference clock
clk25m	25MHz	External	

FLC Slice Clocks

Clock	Value	Type	Description
FLC1_axi_slv_config	00	RW	00 = CXL.mem -> flc1 01 = CXL.io -> flc1 1x = Reserved

Table below defines the clock, when FLC1_axi_slv_config == 2'b00.

Clock Source Selection

Ipm_mc_axi_p0_sync	flc1_axi_slave_sync	flc1_axi_slave	flc1
x	1	ep_cxl_clk	ep_cxl_clk

ep_cxl_clk	PCIe PHY generated clock.

Frequency variations are based on mode negotiation.

Table below defines the clock, when FLC1_axi_slv_config != 2'b00.

Clock Source Selection

Ipm_mc_axi_p0_sync	flc1_axi_slave_sync	flc1_axi_slave	flc1
x	1	clk_nic (clk1g)	clk_nic (clk1g)

Clocks and resets review:

	Reset	Clock	
1.	CB_nPOR	Ref clk - 25MHz	Power on reset -
2.	CB_nRST	Uc clk- 200MHz	Post PLL lock
3.	CORERSTn	Uc clk - 200Mhz	Reset to core- post PLL lock with 200MHz
4.	rc_x8_resetn[1:0]	Clk_rc_x8 – 4.687 MHz	Post PLL lock
5.	rc_x4_resetn[1:0]	Clk_rc_x4 – 4.687 Mhz	Post PLL lock

mockingbird_uc_top_wrapper		
CB_nRST	200MHz clk	Post PLL Lock. To release reset on UC subsystem
CB_nPOR	Clk 25MHz	Power on Reset before PLL Lock
CORERSTn	200MHz clk	Post PLL lock. reset in u_mockingbird_uc_top
sysrst_n	200MHz	UC generated system reset for internal modules. Post CB_nRST and before CORERSTn
ep_perstn_in[3:0]		
axi4tg_resetn		