DDR5 Server Low Current PMIC on DIMM

M88P5010

Data Sheet

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Terms and Abbreviations

Term	Definition
ADC	Analog-to-Digital Conversion
CCC	Common Command Codes
COT	Constant On Time
DCM	Discontinuous Conduction Mode
DDR	Double Data Rate. A description of contemporary synchronous DRAM characterized by data communications at a rate of two bits per clock cycle per wire.
DDR5	Double Data Rate, Fifth Generation
DIMM	Dual In-Line Memory Module. A packaging arrangement of memory devices on a socketable substrate.
DVS	Dynamic Voltage Scaling
FCCM	Forced Continuous Conduction Mode
FCQFN	Flip-Chip Quad Flat No-Lead Package
FSM	Finite State Machine
Host	Memory controller agent on a DDR channel
JEDEC	JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council)
LDO	Low Dropout Regulator
OCL	Over-Current Limit
OTP	Over-Temperature Protection
OVP	Over-Voltage Protection
PEC	Packet Error Code
RCD	Registering Clock Driver
SCL	Serial Clock
SDA	Serial Data
SPD	Serial Presence Detect
TS	Temperature Sensor
UVP	Under-Voltage Protection

Revision History

Revision Number	Revision Date	Changes	
		Page Number	Description
1.0	June 7, 2022		• Removed “Preliminary” on Front page.
0.98	October 27, 2021	11, 12, 13, 14, 28	• Made some minor changes to Table 5, and removed critical temperature hysteresis threshold in Table 6. No silicon changes. • Corrected the Notes sequence of Table 5.
0.97	June 18, 2021		• Updated Page 1. • Removed one note for Tables 72 and 122. • Updated Table 128.
0.96	April 21, 2021		• Changed Silicon Revision from C0 to C3. • Inclusive terminology updated throughout the document, for example, replaced with Host/Controller or Target, or changed S0-S6 with TE0-TE6 in Section 4.1.4.8; including Table 5, Figures 20 to 26. • Changed “I3C” to “I3C Basic” throughout the whole document. • Updated Items 3&9 in Features. • Updated Application and General Description. • Updated the 5th paragraph of General Description. • Changed signal PWR_GOOD to CAMP, VIN_BULK_PGH_th to VINx_PG_RS throughout the whole document. • Updated the notes of Figures 3&4. • Updated Figure 5, and deleted the note. • Updated Tables 1, 2, 3, 4, 5, 6, 9. • Added new 6 Figures to Section 2. • Updated 2 Figures “Power On/Off Sequence with...”. • Updated the previous Figure 9 “VIN_MGMT Input Supply to VIN_BULK Input Supply Switchover Function”. • Updated Sections 3.3, 3.5, 3.6. • Deleted the previous Sections 3.7&3.8,and added new Sections 3.7, 3.8, 3.9 & 3.10. • Updated Sections 3.10, 3.11, 3.12... to 3.29, and added Sections 3.18, 3.31 & 3.31. • Updated Sections 4.1.1, 4.1.3. • Added input power requirements to Sections 4.4.2&4.4.3. • Added a paragraph to Section “DIMM Vendor Region Registers”. • Deleted the RW attribute of R34. • Updated Tables 20, 24, 33, 34, 50, 51, 52, 55, 57, 58, 60, 61, 64, 69, 71, 72, 73, 74; deleted the previous Tables 47&48 • Added new sections “Host Region Register” & “Clear Registers” and “Mask Register”. • Updated the duration from 100ms to 200ms after Tables R04, R05 and R06. • Updated Tables R0A, R0B, R10-R2F, R30, R32, R34, R35, R3B, R3C, R3D, R40, R50. • Some minor formats modification.
0.91	December 8, 2020		• Updated the remote Caps in Figures 3&4 and related notes; • Updated the value of capacitors per phase to “JEDEC defined 350µF” in Section 3.28.

Revision Number	Revision Date	Changes	
		Page Number	Description
0.9	July 9, 2020	-	• Updated Page 1; • Added Description “Montage Evaluation Board” after Figure 3 & Figure 4, respectively; • Added Note to Figure 5; • Added a new Table 8 ‘PMIC Operation; PWR_GOOD Type: Output Only‘; • Updated Tables 2, 3, 4, 5, 6; Figures 6, 9; • Updated 4.1V for VIN_BULK_UV_FL to 4.0V in Tables 5, R33 and throughout the document; • Changed S to ‘S or Sr’ in Tables of 4.1.4.3.2, 4.1.4.3.3; • Updated/added Figures of Section 4.1.4.3.4; • Added new sections 4.1.4.9 ‘CCC Packet Error Handling’; 4.1.4.12 ‘IO Operation’; 4.1.4.13 ‘Bus Clear’; • Updated Items 2, 3, 5, 6 in Table 6; • Updated Sections 3.7, 3.11, 3.15, 3.17, 3.23, 3.25, 3.26, 3.27, 3.28; • Updated [b3] in Tables R1A; [b7] in R2F; [b1-b0] in R30; [b3] in R33 • Adjusted the sections order in Chapter 4; • In Chapter 4, updated Table ‘Register Base Attributes’; removed 4.5 ’I2C/I3C Register Map’; added sections ‘Register Map Breakdown’, ‘Register Memory Protection’; added ‘Attribute’ column to Tables R04-R5E.
0.8	October 14, 2019	-	• Added I3C interface, and added/adjusted related description; • Updated EC tables and Registers information.
0.5	March 20, 2019	-	Initial revision

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DDR5 Server Low Current PMIC on DIMM

M88P5010

Features

- Compliant with JEDEC DDR5 server low current PMIC5010 DIMM application
  - 4 buck converters (SWA, SWB, SWC and SWD) with per phase current capability of 3A full load / 3.5A peak load, and two LDOs of VLDO_1.8V and VLDO_1.0V
  - SWA and SWB can be also configured into one-output converter with dual-phase to provide 6A full load/ 7A peak load
  - For VDD (1.1V), VDDQ (1.1V) and VPP (1.8V) voltage regulators on DIMM application
- Wide VIN_BULK (VINA,VINB,VINC and VIND) voltage range to support 12V power supply in normal case and 5V power supply mainly in Switch Over case
- COT structure to provide fast transient load response
- Selectable FCCM or DCM operation
- Configurable Power On and Power Off sequence with programmable Soft Start / Soft Stop time
- Voltage, output current, output power and temperature reporting
- Input supply Switch Over function to provide uninterrupted operation
- I²C and I3C Basic interfaces
- Non-Write Protect mode for debug and validation
- Protection functions, such as OVP, UVP, OCL and OTP with error log counter and data storage
- 5x5 35-pin FCQFN package

Applications

- DDR5 Server DIMM Devices, such as low current RDIMM

General Description

The M88P5010 is a Power Management IC (PMIC) compliant with JEDEC JESD301-1 DDR5 server low current DIMM application. Refer to Table 5 for M88P5010 electrical characteristics.

The device contains 4 DC-DC buck converters of SWA, SWB, SWC and SWD, among which phase SWA and SWB can be configured into one power rail with dual-phase or two power rails with two isolated phases. Each phase is designed to offer 3A continuous full current and 3.5A peak current. In addition, it also has two LDOs of VLDO_1.8V and VLDO_1.0V.

The device adopts Constant On Time (COT) mode control approach to realize the fast response to the transient load. Also, it simplifies the loop stability design with fewer external compensation components.

The device also provides the flexibility of operating in either Forced Continuous Conduction Mode (FCCM) or Discontinuous Conduction Mode (DCM) at light load.

The M88P5010 works as a target device, and is intended to operate up to 12.5MHz on a 1.0V I3C Basic bus or up to 1MHz on a 1.0V to 3.3V I²C bus.

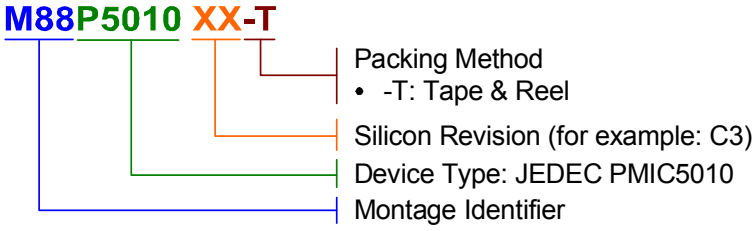
The M88P5010 provides various protection functions, including Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), Over-Current Limit (OCL) and Over-Temperature Protection (OTP).

The M88P5010 is available in a 5mm x 5mm, 35-pin FCQFN package.

Ordering Information

Full Part Number	Mode Name	Package (Green)[1]
M88P5010XX-T	JEDEC DDR5 Server Low Current PMIC5010 on DIMM	FCQFN5x5-35, Tape & Reel

1. Green: Lead Free / Halogen Free.



Block Diagram

Figure 1. Function Logic Diagram

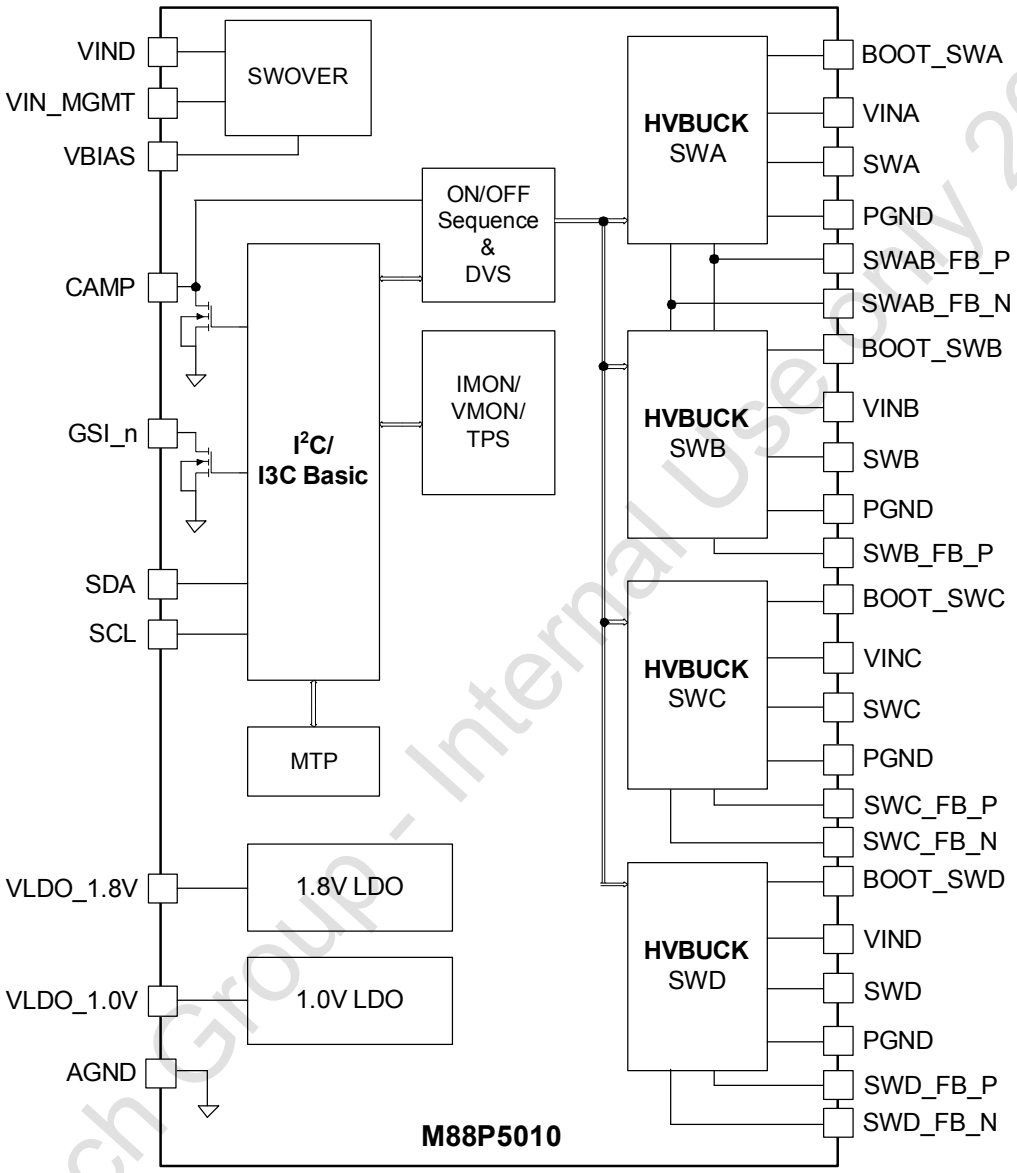
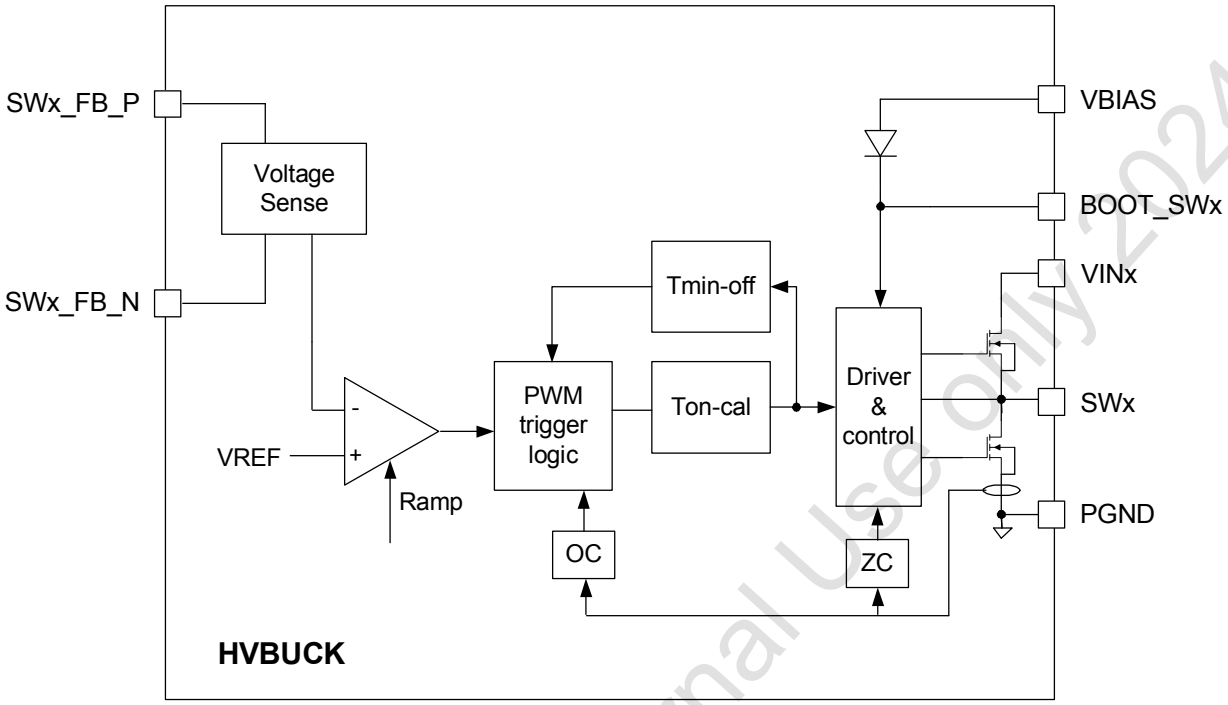
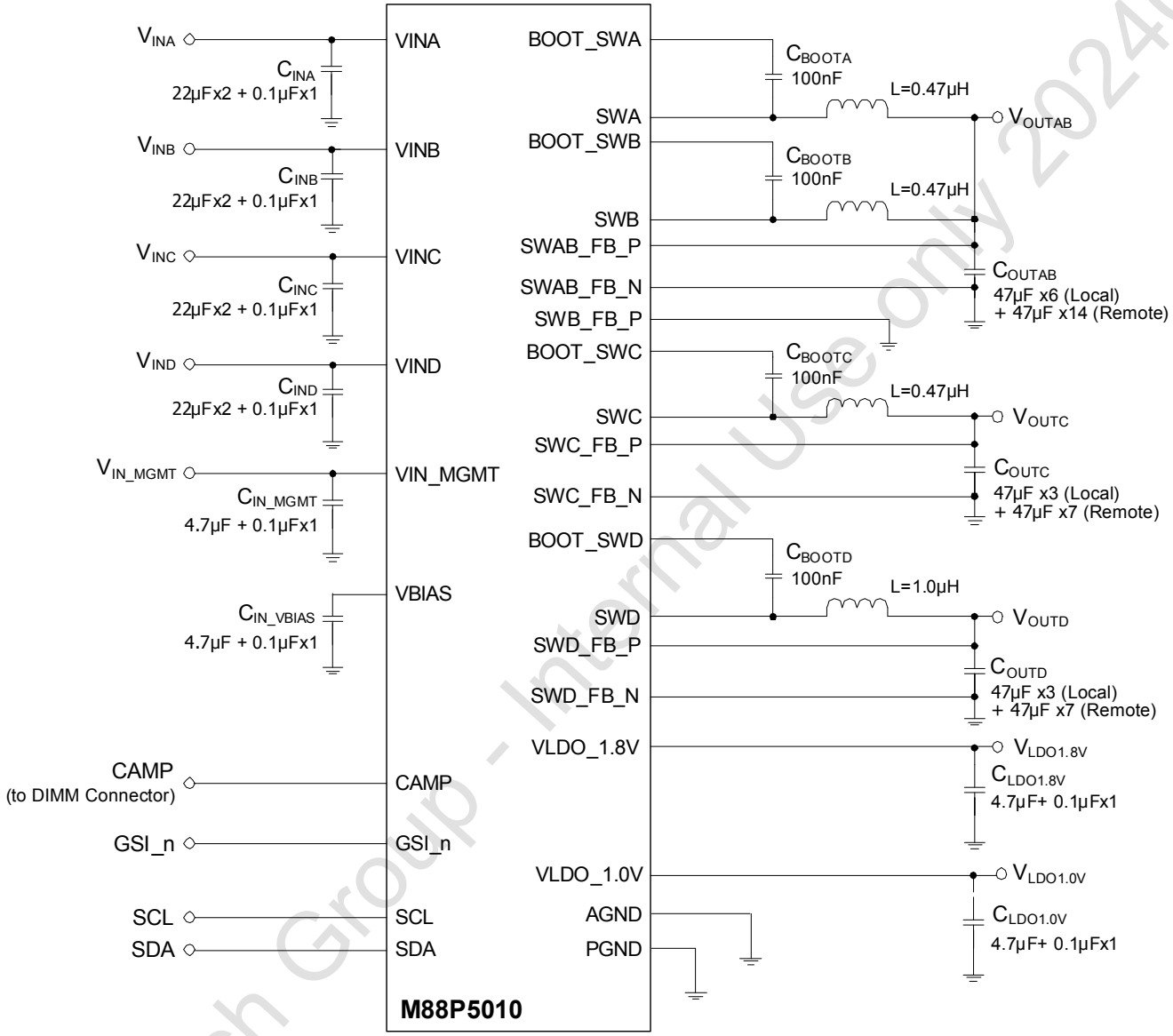


Figure 2. HVBUCK Block Diagram



Reference Application

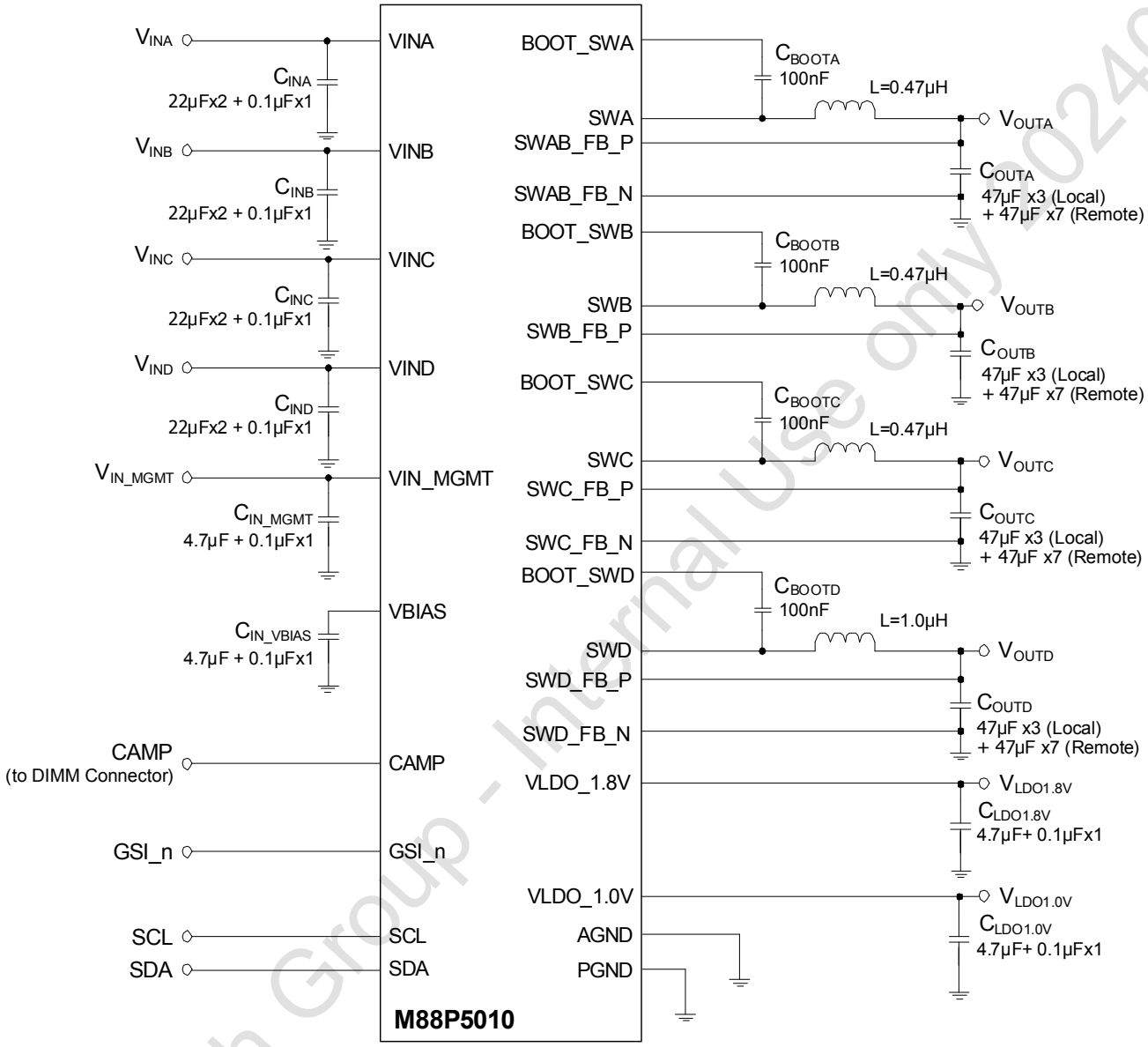
Figure 3. Application Circuit (SWAB dual-phase, 3 output rails)



Montage Evaluation Board

- Switching Frequency of Each Phase: 750kHz
- Load Current per Phase: 3A
- Inductor: 0.47µH for SWA/B/C; 1.0µH for SWD
- Input Cap per Phase: 22µFx2 + 0.1µFx1
- Output Cap per Phase: 47µF x3 at PMIC local side, and 47µF x7 equivalent capacitance at remote DRAMs load side

Figure 4. Application Circuit (SWA, SWB separated, 4 output rails)



Montage Evaluation Board

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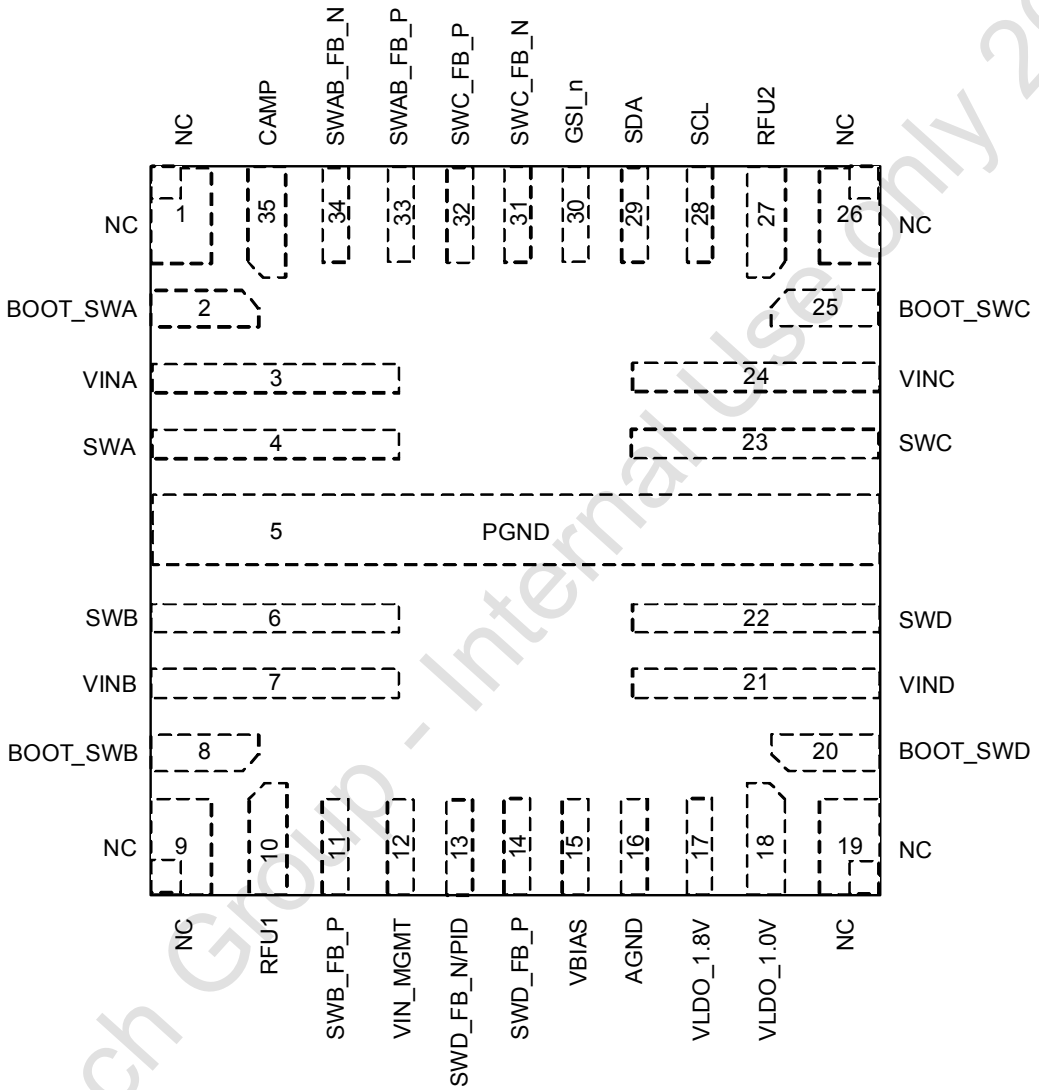
- Inductor: 0.47µH for SWA/B/C; 1.0µH for SWD
- Input Cap per Phase: 22µFx2 + 0.1µFx1
- Output Cap per Phase: 47µF x3 at PMIC local side, and 47µF x7 equivalent capacitance at remote DRAMs load side

1 Pin Information

1.1 Pin Configuration and Assignment

Figure 5. 35-Pin FCQFN, 5 mm x 5 mm (Top View)



1.2 Pin Description

Table 1. Pin Description

Pin No.	Pin Name	Function
2	BOOT_SWA	Bootstrap cap node for SWA phase. This pin is connected to SWA through a 100nF ceramic capacitor.
3	VINA	One of 4 VIN_BULK pins used as input power source of SWA regulator. All the VIN_BULK pins must be connected to the 12V input supply even if one or more output regulators are not intended to be used.
4	SWA	SWA switch node.
5	PGND	Power ground.
6	SWB	SWB switch node.
7	VINB	One of 4 VIN_BULK pins used as input power source of SWB regulator. All the VIN_BULK pins must be connected to the 12V input supply even if one or more output regulators are not intended to be used.
8	BOOT_SWB	Bootstrap cap node for SWB phase. This pin is connected to SWB through a 100nF ceramic capacitor.
10	RFU1	Reserved for future use, and connected to ground plane.
11[1]	SWB_FB_P	Single-ended positive feedback pin for SWB rail when SWB is configured as an independent output power rail. This pin must be connected to GND when SWA and SWB are in the dual-phase and single output operation mode.
12	VIN_MGMT	3.3V supply input pin, and used as power source of VLDO_1.8V, VLDO_1.0V and other internal circuit.
13	SWD_FB_N/PID	SWD rail negative sense feedback return, or PMIC device ID.
14[1]	SWD_FB_P	SWD rail positive sense feedback
15	VBIAS	Internal bias supply
16	AGND	Analog ground
17	VLDO_1.8V	1.8V LDO output
18	VLDO_1.0V	1.0V LDO output
20	BOOT_SWD	Bootstrap cap node for SWD phase. This pin is connected to SWD through a 100nF ceramic capacitor.
21	VIND	One of 4 VIN_BULK pins used as input power source of SWD regulator. All the VIN_BULK pins must be connected to the 12V input supply even if one or more output regulators are not intended to be used.
22	SWD	SWD switch node
23	SWC	SWC switch node
24	VINC	One of 4 VIN_BULK pins used as input power source of SWC regulator. All the VIN_BULK pins must be connected to the 12V input supply even if one or more output regulators are not intended to be used.
25	BOOT_SWC	Bootstrap cap node for SWC phase. This pin is connected to SWC through a 100nF ceramic capacitor.

Table 1. Pin Description

Pin No.	Pin Name	Function
27	RFU2	Reserved for future use, and connected to ground plane.
28	SCL	I²C/I3C Basic serial clock interface.
29	SDA	I²C/I3C Basic bi-directional serial data interface.
30	GSI_n	Status interrupt/indication output pin, open drain output. Connected to ground plane or kept floating if it is not used.
31	SWC_FB_N	SWC rail negative sense feedback return.
32[1]	SWC_FB_P	SWC rail positive sense feedback.
33[1]	SWAB_FB_P	SWA/B rail positive sense feedback when SWA and SWB are combined as 2-phase, single output rail. When SWA and SWB are separated for 2 output rails, this pin is used as SWA positive sense feedback.
34	SWAB_FB_N	SWA/B rail negative sense feedback return when SWA and SWB are combined as 2-phase, single output rail. When SWA and SWB are separated for 2 output rails, this pin is used as SWA negative sense feedback return.
35	CAMP	Control and Monitor Port. Output: Open drain driver to indicate power good signal of DC-DC regulators and LDOs; Input: The PMIC disables DC-DC output regulators when this pin transitions from High to Low; Input: The PMIC enters Write Protect mode when this pin is High.
1, 9, 19, 26	NC	No connection; connected to ground plane or kept floating.

1. If a series resistor has to be added between a SWx_FB_P pin and output voltage sense point of VDD,VDDQ or VPP, please ensure the resistor value is 0Ω to avoid the ramp-up issue.

2 Electrical Specifications

2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings[1]

Parameter	Min	Max	Unit
V_{INx} (V_{IN_BULK})	-0.3	+18	V
SWx (DC)	-0.3	+18	V
SWx (Pulse < 25 ns)	-5	+22	V
BOOT_SWx (DC)	-0.3	+23.5	V
BOOT_SWx (Pulse < 25 ns)	-1.0	+26	V
BOOT_SWx – SWx	-0.3	+6	V
V_{IN_MGMT}[2], V_{BIAS}[2]	-0.3	+6	V
SWx_FB_P	-0.3	+5.5	V
SWx_FB_N, PID	-0.3	+5.5	V
VLDO_1.8V, VLDO_1.0V	-0.3	+5.5	V
SCL, SDA	-0.3	+5.5	V
GSI_n, CAMP[3], RFU1, RFU2	-0.3	+5.5	V
Thermal Resistance from Junction to Ambient, θ_{JA}[4]	25		°C/W
Thermal Resistance from Junction to Case θ_{JC}[4]	8.5		°C/W
Thermal Resistance from Junction to Baseboard, θ_{JB}[4]	13.5		°C/W
Junction Temperature T_J	-40	+150	°C
Storage Temperature Range T_{STG}	-55	+150	°C
Re-flow Temperature (Soldering, 10 sec)	+260		°C
ESD Susceptibility[5] (HBM)	±2000		V
ESD Susceptibility[5] (CDM)	±500		V
EOS Requirement[6,7,8,9]			
V_{INx} (V_{IN_BULK})	37		V
V_{IN_MGMT}	10		V

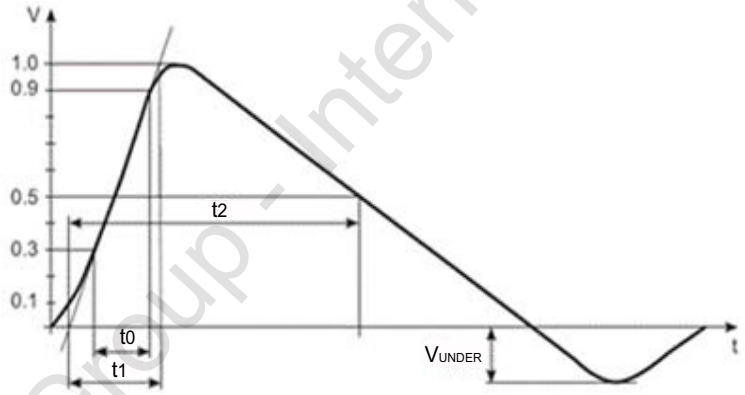
1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The maximum voltage is under the condition of SWx regulators shut-down.
3. CAMP pins shall withstand the stress when connected to maximum of 15V DC source through a 250Ω series resistor for 10 seconds. M88P5010 is also able to withstand the stress mentioned above without series resistor added.

4. This thermal rating is calculated on JEDEC 51 standard 4-layer board with dimensions 3” x 4.5” in still air conditions. Actual thermal resistance is affected by the PCB size, solder joint quality, layer count, copper thickness, air flow, altitude and other unlisted variables.
5. Device is ESD sensitive. Handling precaution recommended. The Human Body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.
6. The test is performed on DDR5 DIMM module without any input capacitor at VIN_BULK and VIN_MGMT pins.
7. The input source needs to follow the waveform and condition as shown in Figure 6 and Table 3.
8. Probing is performed at the VIN_BULK and VIN_MGMT pins of PMIC.
9. Each net test is performed individually.

Table 3. Input Source Condition

Parameter	Description	Value	Notes
t0	Rise from 30% to 90% of peak	0.72µs (+ 30%)	
t1	Rise time	1.2µs (+ 30%)	t1 = 1.67 * t0
t2	Duration time to half value	50µs (+ 20%)	
R_{OUT}	Output impedance	2Ω	
$V_{UNDERSHOOT}$	Undershoot Voltage	30% Max.	

Figure 6. Impulse Waveform for EOS Test (IEC 61000-4-5)



2.2 Recommended Operating Conditions

Table 4. Recommended Operating Conditions[1]

Parameter	Min	Max	Unit
V_{INx} (V_{IN_BULK})[2,3]	4.25	15	V
V_{IN_MGMT}	3.0	3.6	V
Full Load Continuous Current, I_{OUT_SWA}, I_{OUT_SWB} (per phase)[4]	0	3	A
Full Load Continuous Current, I_{OUT_SWC}[4]	0	3	A
Full Load Continuous Current, I_{OUT_SWD}[4]	0	3	A
Full Load Continuous Current, $I_{OUT\_LDO\_1.8V}$	0	25	mA
Full Load Continuous Current, $I_{OUT\_LDO\_1.0V}$	0	20	mA
Operating Junction Temperature T_J	-40	+125	°C
Operating Ambient Temperature T_A[5]	-40	+85	°C

1. Functional operation of the device beyond the conditions of “Recommended Operating Conditions” is not implied.
2. V_{INx} (V_{IN_BULK}) is connected to 12V input power supply, and the PMIC SWx regulators will not ramp up until V_{INx} reaches 5.25V (typical value, when R1A[7:5] is set to ‘110’). One of the actual applications to support 5V input power supply is Switch Over mode. In this mode, V_{INx} power supply may be switched from 12V to 5V automatically.
3. Per JEDEC spec, it may trigger V_{INx} power not good status when V_{INx} is less than 4.25V.
4. The maximum load peak current is 3.5A per phase, which lasts for 20µs to 50µs.
5. Operating Junction Temperature T_J still needs to be met.

2.3 Electrical Characteristics

Table 5. Electrical Characteristics[1, 2] (Sheet 1 of 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General						
$V_{INx\_UV\_FL}$	VINx UV Falling Threshold	VINx falling, R1A[7:5]=’xxx’	3.85	4.0	4.15	V
$V_{INx\_UV\_RS}$	VINx UV Rising Threshold	VINx rising, (R1A[7:5]=’110’) + 1V	5.05	5.25	5.65	V
		Other settings tolerance	-0.3	-	+0.3	V
$V_{INx\_PG\_FL}$	VINx Power Good Falling Threshold	VINx falling, R1A[7:5]=’110’	3.95	-	4.25	V
		VINx falling, R1A[7:5]=’001’	9.2	9.5	9.8	V
		Other settings tolerance	-0.3	-	+0.3	V
$V_{INx\_PG\_RS}$	VINx Power Good Rising Threshold	VINx rising, (R1A[7:5]=’110’) + 1V	5.05	5.25	5.65	V
		Other settings tolerance	-0.3	-	+0.3	V
$V_{INx\_OV\_RS}$	VINx OV Rising Threshold	VINx rising, R1B[7]=’0’	14.4	14.5	15.2	V
		VINx rising, R1B[7]=’1’	15.8	16	16.6	V
$V_{INx\_OV\_FL}$	VINx OV Falling Threshold	VINx falling, R1B[7]=’0’	12.8	13.6	14.4	V
		VINx falling, R1B[7]=’1’	14.2	15	15.8	V

Table 5. Electrical Characteristics[1, 2] (Sheet 2 of 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IN\_MGMT\_UV\_FL}$	VIN_MGMT UV Falling Threshold[3]	VIN_MGMT falling	2.6	2.7	2.8	V
$V_{IN\_MGMT\_UV\_RS}$	VIN_MGMT UV Rising Threshold	VIN_MGMT rising	2.7	2.8	2.9	V
$V_{IN\_MGMT\_OV\_RS}$	VIN_MGMT OV Rising Threshold	VIN_MGMT rising, R1B[5]='0'	3.7	3.8	3.95	V
		VIN_MGMT rising, R1B[5]='1'	3.6	3.7	3.8	V
$V_{IN\_MGMT\_OV\_FL}$	VIN_MGMT OV Falling Threshold	VIN_MGMT falling	3.4	3.5	3.65	V
$V_{BIAS\_UV\_FL}$	VBIAS UV Falling Threshold	VBIAS falling	2.43	2.55	2.65	V
$V_{BIAS\_UV\_RS}$	VBIAS UV Rising Threshold	VBIAS rising	2.65	2.8	2.95	V
$V_{BIAS\_PG\_FL}$	VBIAS Power Good Falling Threshold	VBIAS falling, R1A[3]='0'	2.5	2.6	2.75	V
$V_{BIAS\_PG\_RS}$	VBIAS Power Good Rising Threshold	VBIAS rising	2.65	2.8	2.95	V
V_{SWO_FL}	Switch Over Falling Threshold	VIN_MGMT falling, R2F[7]='0'	2.7	2.8	2.9	V
		VIN_MGMT falling, R2F[7]='1'	2.65	2.75	2.85	V
V_{SWO_RS}	Switch Over Rising Threshold	VIN_MGMT rising	2.8	2.9	3.0	V
I_{VIN_SD}	VINx Shutdown Current	VR_ENABLE, R32[7]='0'; ADC Disabled, R30[7]='0'	-	10	30	µA
$I_{VIN\_MGMT\_SD}$	VIN_MGMT Shutdown Current	VR_ENABLE, R32[7]='0'; ADC Disabled, R30[7]='0'	-	550	700	µA
$I_{VIN\_MGMT\_Q}$	VIN_MGMT Quiescent Current	VR_ENABLE, R32[7]='1' ADC_ENABLE, R30[7]='1' No-switching	-	2800	3400	µA
I/O Pin (CAMP, GSI_n, SDA, SCL)						
I_{IO_LC}	I/O Leakage Current	IO pins forced to 'H' or GND	-2	-	2	µA
V_{IH}	SDA, SCL Input High Voltage	SDA, SCL high threshold	0.7	-	-	V
V_{IL}	SDA, SCL Input Low Voltage	SDA, SCL low threshold	-	-	0.3	V
V_{OH}	SDA Output High Voltage	Pull high to 1.0V, I_{OH} = 3mA	0.75	-	-	V
V_{OL}	SDA, CAMP and GSI_n Output Low Voltage	I_{OL} = 3mA	-	-	0.3	V
V_{CAMP_IH}	CAMP Logic-Input Threshold	High threshold	1.26	-	-	V
V_{CAMP_IL}		Low threshold	-	-	0.3	V
R_{ON_SDA}	SDA Output Pull-up and Pull-down Driver Impedance[4]	SDA	20	-	100	Ω
$R_{ON\_GSI\_n}$, R_{ON_CAMP}	GSI_n, CAMP Output Pull-down Driver Impedance	GSI_n, CAMP output	40	-	100	Ω
C_{IN_BUS}	Input Capacitance[3]	SCL, SDA	-	-	5	pF

Table 5. Electrical Characteristics[1, 2] (Sheet 3 of 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SP}	Pulse Width of spikes which must be suppressed by the input filter in I²C mode[3]	Single glitch, f ≤ 100kHz	-	-	-	ns
		Single glitch, f > 100kHz	0	-	50	ns
K_{OUT_SDA}	Output Slew Rate[3,5]	Rising, SDA	0.1	-	1	V/ns
		Falling, SDA	0.1	-	3	V/ns
HV Buck Converter (SWx)						
$I_{BIAS\_Q\_SWx}$	Quiescent Current (VBIAS supply)	Enable, no switching	-	500	620	µA
t_{SSTRT}	Soft-Start Internal	R2C[7:5], R2C[3:1], R2D[7:5], R2D[3:1] = '001'	1.78	2	2.29	ms
		Other settings tolerance	-11	-	+14	%
t_{SSTOP}	Soft-Stop Internal	R22[1:0], R24[1:0], R26[1:0] = '00'	0.44	0.5	0.57	ms
		R28[1:0] = '00'	0.89	1	1.14	ms
		Other settings tolerance	-11	-	+14	%
$\%V_{SWx\_SP}$	SWx Regulator Feedback Set Point Reference Voltage Accuracy without Load	SWx Output Voltage ≥ 1V	-0.75	-	+0.75	%
		0.8V ≤ SWx Output Voltage <1V	-1	-	+1	%
V_{OUT_SWx}	Output Voltage Range	SWA when R2B[5] = '0' SWB when R2B[4] = '0' SWC when R2B[3] = '0'	800	-	1435	mV
		SWD when R2B[0] = '0'	1500	-	2135	mV
V_{OUT_STEP}	Output Voltage Programmable Step		-	5	-	mV
K_{DVS_SR}	Slew Rate of Dynamic Output Voltage Scaling in Non-Write Protect mode		0.8	1.0	1.2	mV/µs
R_{ON_HS}	HS-MOS ON Resistance[6]	HS-MOS ON Resistance	-	30	45	mΩ
R_{ON_LS}	LS-MOS ON Resistance[6]	LS-MOS ON Resistance	-	15	22.5	mΩ
I_{LIM_Valley}	Valley Current Limit [6]	R20[7:6], R20[5:4], R20[3:2], R20[1:0] = '00'	1.7	2	2.5	A
		R20[7:6], R20[5:4], R20[3:2], R20[1:0] = '01'	2.25	2.5	3.0	A
		R20[7:6], R20[5:4], R20[3:2], R20[1:0] = '10'	2.7	3	3.6	A
		R20[7:6], R20[5:4], R20[3:2], R20[1:0] = '11'	3.15	3.5	4.2	A
f_{SW}	Switching Frequency	R29[5:4], R29[1:0], R2A[5:4], R2A[1:0] = '01'	675	750	825	kHz
		R29[5:4], R29[1:0], R2A[5:4], R2A[1:0] = '10'	900	1000	1100	kHz

Table 5. Electrical Characteristics[1, 2] (Sheet 4 of 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{OFF_MIN}	Minimum Off-Time[3]	Open loop. FB_P = 95% * target	150	195	240	ns
$\%V_{UVP}$	Under-Voltage Protection Threshold	R22[3:2], R24[3:2], R26[3:2], R28[3:2] = '00'	87	90	93	%
		Other settings	typ. - 3	typ.	typ. + 3	%
$\%V_{OVP}$	Over-Voltage Protection Threshold	R22[5:4], R24[5:4], R26[5:4], R28[5:4] = '10'	109.5	112.5	115.5	%
		Other settings	typ. - 3	typ.	typ. + 3	%
$\%V_{PGL}$	Power Good Low-Side Threshold	SWx Output Voltage Falling. R21[0], R23[0], R25[0], R27[0] = '0'	92	95	97.5	%
		Other settings	typ. - 3	typ.	typ.+ 2.5	%
$\%V_{PGH}$	Power Good High-Side Threshold	SWx Output Voltage Rising. R22[7:6], R24[7:6], R26[7:6], R28[7:6] = '01'	105	107.5	110.5	%
		Other settings	typ.- 2.5	typ.	typ. + 3	%
$\%_{PG\_HYS}$	Power Good Hysteresis		1.0	2.5	4.0	%
R_{DISCHG}	Discharge Resistance		10	25	40	Ω
LDO (VLDO_1.8V, VLDO_1.0V)						
%LDOx_ACC	LDOx Regulation Voltage Accuracy		-2.0	-	+2.0	%
V_{LDOx_RANGE}	Output Voltage Setting Range	VLDO_1.8V	1.7	-	1.9	V
		VLDO_1.0V	0.9	-	1.2	V
V_{LDR}	Load Regulation	VLDO_1.8V, I_{LOAD} = 0mA to 25mA	-	2.0	5.0	mV
		VLDO_1.0V, I_{LOAD} = 0mA to 20mA	-	2.0	5.0	mV
I_{LIM_LDOx}	Current Limit	VLDO_1.8V	40	60	80	mA
		VLDO_1.0V	35	50	65	mA
V_{PG_LDOx}	Power Good Threshold	VLDO_1.8V, falling, R1A[2] = '0'	1.55	1.6	1.65	V
		VLDO_1.0V, falling, R1A[0] = '0'	-14	-10	-6.5	%
		VLDO_1.0V, falling, R1A[1] = '1'	-18.5	-15	-12	%
V_{UV_LDOx}	Invalid Threshold	VLDO_1.8V, falling	1.1	1.2	1.3	V
		VLDO_1.0V, falling	0.55	0.6	0.65	V
$PSRR_{LDOx}$	Power Supply Rejection Rate[3]	f = 100 Hz, I_{OUT} = 20mA	-	-60	-	dB
		f = 10 kHz, I_{OUT} = 20mA	-	-40	-	dB
R_{DIS_LDOx}	Discharge Resistance		15	30	55	Ω
Voltage Monitoring ADC						
N_{R_V}	Resolution		-	8	-	bits

Table 5. Electrical Characteristics[1, 2] (Sheet 5 of 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INL_V	Integral Nonlinearity	SWA/B/C Output range: 1.05V to 1.16V	-1	-	1	LSB
		SWD Output range: 1.75V to 1.85V				
		Others	-3	-	3	LSB
t_{CT_V}	Conversion Time		174	200	235	µs
Current Monitoring ADC						
N_{R_C}	Resolution		-	6	-	bits
INL_C	Integral Nonlinearity[6]	<0.5A	-4	-	4	LSB
		≥0.5A	-3	-	3	LSB
I_{DCR_C}	ADC Decoding Current Range		0	-	8	A
t_{CT_C}	Conversion Time		174	200	235	µs
Temperature Monitoring ADC						
N_{R_T}	Resolution		-	3	-	bits
INL_T	Integral Nonlinearity[3]		-1	-	1	LSB
T_{DTR}	ADC Decoding Temperature Range		80	-	140	°C
t_{CT_T}	Conversion Time[3]		-	1	-	µs
Thermal Protection						
T_{WARN}	Thermal Warning Threshold[3]	R1B[2:0]='101'	-	125	-	°C
ΔT_{WARN_HYS}	Thermal Warning Hysteresis[3]		-	10	-	°C
T_{OTP}	Thermal Shutdown Threshold[3]	R2E[2:0]='100'	-	145	-	°C
I²C Interface [6,7] - Open Drain						
f_{SCL}	SCL Operating Frequency		0.01	-	1	MHz
t_{HIGH}	SCL Clock High Pulse Width Time		260	-	-	ns
t_{LOW}	SCL Clock Low Pulse Width Time		500	-	-	ns
$t_{TIMEOUT}$	Detect Clock Input Low Time		10	-	50	ms
t_R	Clock/Data Rise Time		-	-	120	ns
t_F	Clock/Data Fall Time		-	-	120	ns
$t_{SU:DAT}$	Data in Setup Time		50	-	-	ns
$t_{HD:DI}$	Data in Hold Time		0	-	-	ns
$t_{SU:STA}$	Start Condition Setup Time		260	-	-	ns
$t_{HD:STA}$	Start Condition Hold Time		260	-	-	ns
$t_{SU:STO}$	Stop Condition Setup Time		260	-	-	ns

Table 5. Electrical Characteristics[1, 2] (Sheet 6 of 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{BUF}	Time Between Stop Condition and next Start Condition		500	-	-	ns
$t_{HD:DAT}$	SDA Data Out Hold Time		0.5	-	350	ns
$t_{DEVCTRLCCC\_DELAY\_PEC\_DIS}$	DEVCTRL CCC Followed by DEVCTRL CCC or Register Read/ Write Command Delay[8]		3	-	-	µs
$t_{I2C\_CCC\_UPDATE\_DELAY}$	SETHID CCC or SETAASA CCC followed by any other CCC or Read/ Write Command Delay		2.5	-	-	µs
I3C Basic Interface [6,7,9] - Push Pull						
f_{SCL}	SCL Operating Frequency		0.01	-	12.5	MHz
t_{HIGH}	SCL Clock High Pulse Width Time		35	-	-	ns
t_{LOW}	SCL Clock Low Pulse Width Time		35	-	-	ns
$t_{TIMEOUT}$	Detect Clock Input Low Time		10	-	50	ms
t_R	Clock/Data Rise Time		-	-	5	ns
t_F	Clock/Data Fall Time		0	-	5	ns
$t_{SU:DAT}$	Data in Setup Time		8	-	-	ns
$t_{HD:DI}$	Data in Hold Time		3	-	-	ns
$t_{SU:STA}$	Start Condition Setup Time		12	-	-	ns
$t_{HD:STA}$	Start Condition Hold Time		30	-	-	ns
$t_{SU:STO}$	Stop Condition Setup Time		12	-	-	ns
t_{BUF}	Time Between Stop Condition and next Start Condition[10]		500	-	-	ns
t_{DOUT}	SCL Falling Clock In to Valid SDA Data Out Time		0.5	-	12	ns
t_{DOFFT}	SCL Rising Clock In to Target SDA Output Off		0.5	-	12	ns
t_{DOFFC}	SCL Rising Clock In to Controller SDA Output Off		0.5	-	30	ns
$t_{CL\_r\_DAT\_f}$	SCL Rising Clock In to Host Driving Data Signal Low[11]		40	-	-	ns
t_{AVAL}	Bus Available Time (no edges seen on SCL and SDA)		1	-	-	µs
t_{IBI_ISSUE}	Time to issue IBI after an event is detected when Bus is available			-	15	µs

Table 5. Electrical Characteristics[1, 2] (Sheet 7 of 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{CLR\_I3C\_CMD\_DELAY}$	Time from Clear Register Status to any I3C Basic operation with Start condition to avoid false IBI generation; PEC disabled		4	-	-	µs
	Time from Clear Register Status to any I3C Basic operation with Start condition to avoid false IBI generation; PEC enabled		15			µs
$t_{DEVCTRLCCC\_DELAY\_PEC\_DIS}$	DEVCTRL CCC Followed by DEVCTRL CCC or Register Read/ Write Command Delay[8]		3	-	-	µs
$t_{WR\_RD\_DELAY\_PEC\_EN}$	Register Write Command Followed by Register Read Command Delay in PEC Enable Mode[12]		8	-	-	µs
$t_{I3C\_CCC\_UPDATE\_DELAY}$	RSTDAA CCC or ENEC CCC or DISEC CCC to any other CCC or Read/Write Command Delay		2.5	-	-	µs
t_{CCC_DELAY}	Any CCC followed by RSTDAA CCC delay		2.5	-	-	µs

1. V_{INx} = 12 V, V_{IN_MGMT} = 3.3V, T_J = -40°C to +125°C, unless otherwise noted.
2. The device is not guaranteed to function outside its operating conditions.
3. Guaranteed by design and/or characterization.
4. The R_{ON_SDA} min. value is 19Ω when T_J is -40°C.
5. The reference load and the timing measurement points are shown as Figure 7 and Figure 8. For slew rate measurement, V_{OH} = {1.0/(R_{ON} +50)}*50.
6. Tested under 25°C and 125°C. -40°C is guaranteed by design and/or characterization.
7. Check input/output timing from Figure 9 to Figure 12.
8. From STOP condition of DEVCTRL CCC to START condition for Register Read or Register Write Command Data Packet delay. The PMIC sends NACK if Host does not satisfy $t_{DEVCTRLCCC\_DELAY\_PEC\_DIS}$ timing parameter. For I3C basic mode, this timing parameter restriction is only applicable when PEC function is disabled in PMIC. If PEC is enabled, this timing parameter does not apply.
9. I3C Basic mode with Open Drain operation follows timing values as shown in I²C Mode.
10. If PEC is enabled, $t_{WR\_RD\_DELAY\_PEC\_EN}$ timing parameter applies.
11. See Figure 23.
12. From STOP condition for Register Write Command Data Packet to START condition for Register Read Command Data Packet delay. This timing parameter restriction is only applicable when PEC function is enabled in PMIC. If PEC is disabled, this timing parameter does not apply. The PMIC sends NACK if Host does not satisfy $t_{WR\_RD\_DELAY\_PEC\_EN}$ timing parameter.

Figure 7. Output Slew Rate and Output Timing Reference Load

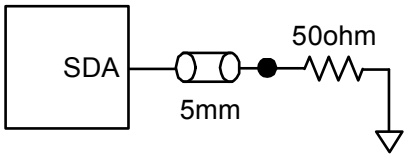


Figure 8. Output Slew Rate Measurement Points

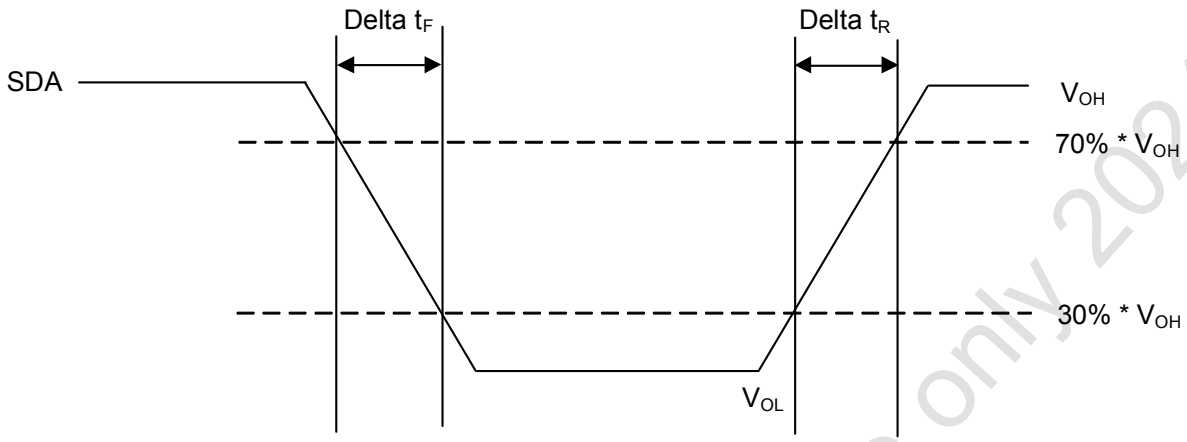


Figure 9. I²C or I3C Basic Bus AC Input Timing Parameter Definition

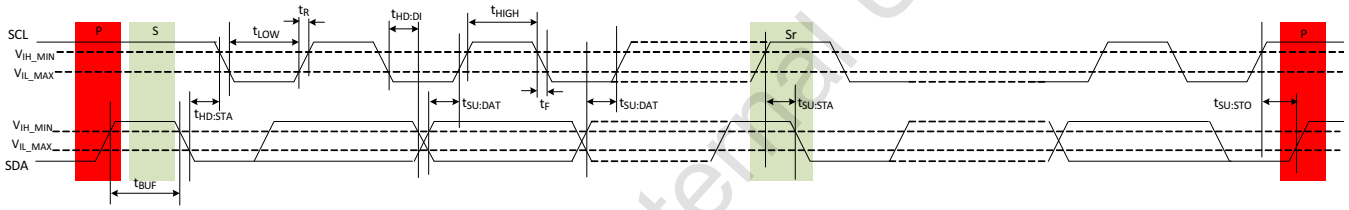


Figure 10. I3C Basic Bus AC Data Output Timing Parameter Definition

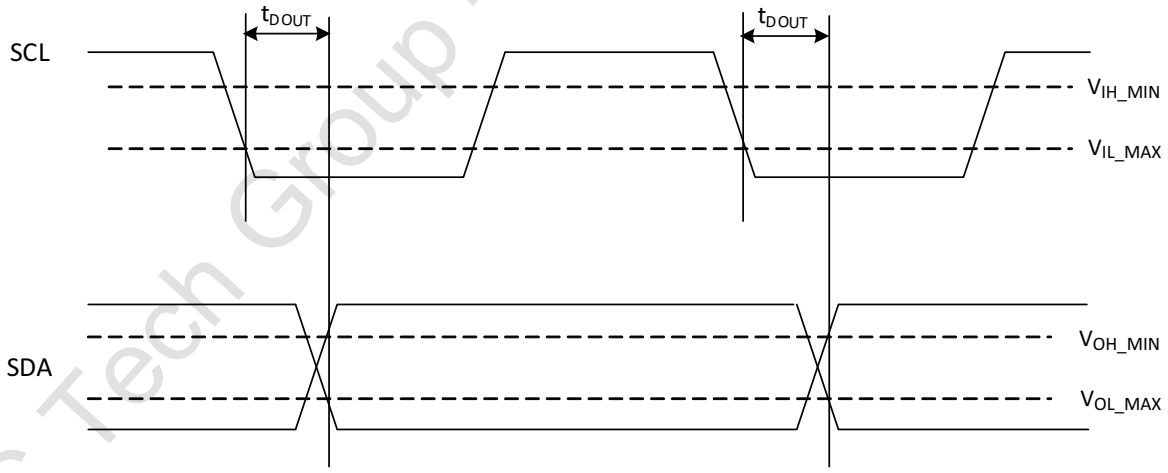


Figure 11. I²C Bus AC Data Output Timing Parameter Definition

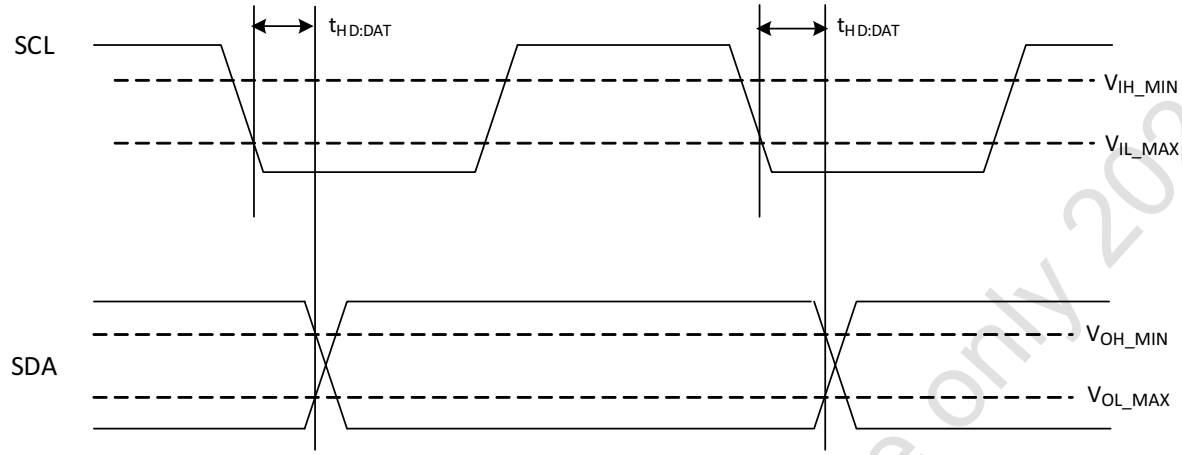
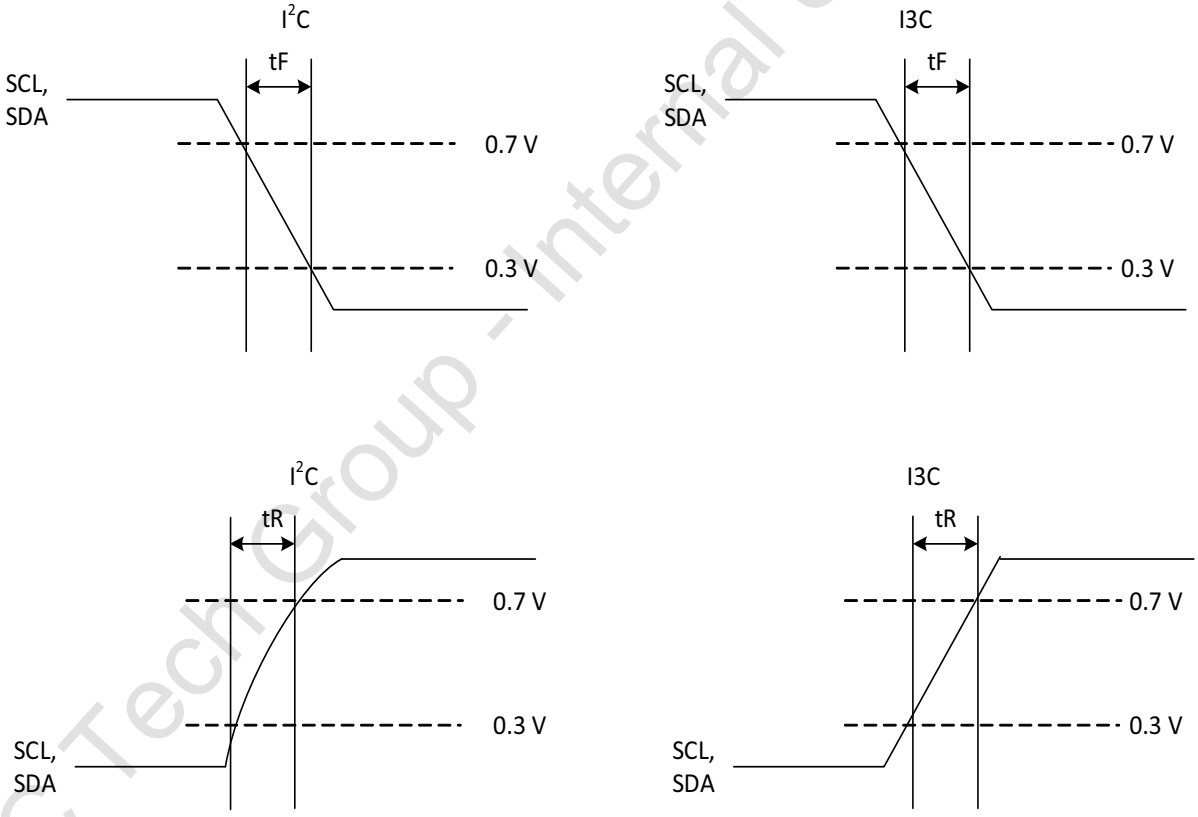


Figure 12. Rise and Fall Timing Parameter Definition



3 Function Description

The M88P5010 is a Power Management IC (PMIC) containing four buck converters (SWA/SWB/SWC/SWD) and two LDOs (VLDO_1.8V and VLDO_1.0V) with necessary protection functions. The buck converters adopt Constant On Time (COT) control to realize the fast transient response. Two of the buck converters (SWA and SWB) can be configured to operate in dual-phase and single output power rail. Two ADCs are implemented to monitor the current consumptions of the buck converters and the voltage information of the input/output rails. The PMIC is designed to meet power requirements of DDR5 server low current PMIC with high efficiency and small form factor.

3.1 Constant On Time Control

The COT control algorithm can be described briefly as follows: the high-side switch On time is determined by a one-shot whose period is inversely proportional to the input voltage and directly proportional to the output voltage. Another one-shot determines the minimum Off time. The On-time one-shot can be triggered when the following conditions occur: the output voltage is lower than the reference voltage, the low-side switch current is below the current-limit threshold, and the minimum Off-time one-shot has timed out.

3.2 Buck Converter Current Limit

The PMIC uses an internal current sense circuit and does not need the external current sense resistor. If the current sense voltage is above the current-limit threshold, the pulse modulator is not allowed to initiate a new cycle. The actual inductor peak current is the current-limit threshold plus the inductor peak-to-peak ripple current. The former can be set through I^2C/I3C Basic, and the latter depends on the output inductance, VIN_BULK (VINx) voltage, output voltage and phase switching frequency.

3.3 Power Up Sequence

The DDR5 PMIC has two input supplies from the platform: VIN_BULK (VINx) and VIN_MGMT.

The VIN_MGMT supply is used to generate the internal bias voltage for reading operation from its internal non-volatile memory content and to supply VLDO_1.8V & VLDO_1.0V. At power on, the VIN_MGMT supply shall reach a minimum of 2.8V before it can be detected as a valid input supply to the PMIC. The VIN_MGMT supply is strictly a voltage input.

The VIN_BULK supply is used by the PMIC for all buck regulators, and it may also be used to generate the internal bias voltage in Switch Over mode. At power on, the VIN_BULK input supply shall reach a minimum threshold VINx_PG_RS (R1A[7:5] + 1V) before it can be detected as a valid input supply to the PMIC. The PMIC tolerates any non-monotonic input supply once it crosses this threshold.

Figure 13 and Figure 14 show the PMIC power up sequence when the power is first applied. The platform can power up VIN_BULK and VIN_MGMT supply in any sequence. Figure 13 shows that VIN_MGMT supply ramps up first prior to VIN_BULK supply. Figure 14 shows that VIN_BULK supply ramps up first prior to VIN_MGMT supply. The PMIC does not mandate any specific timing relationship between VIN_BULK and VIN_MGMT supply.

Figure 13. VIN_MGMT Ramps Up First

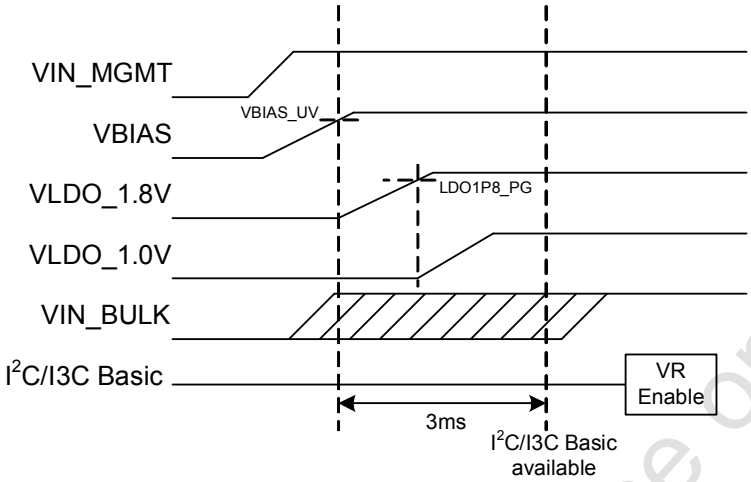
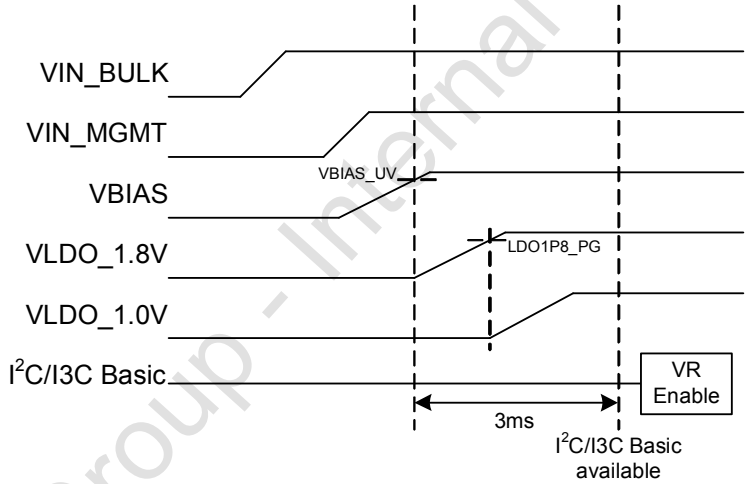


Figure 14. VIN_BULK Ramps Up First



Once the VBIAS supplied by VIN_MGMT is valid and stable, the PMIC shall drive VLDO_1.8V & VLDO_1.0V supply, and it shall enable I²C/I3C Basic bus interface function and read the MTP data within 3ms. The host shall not attempt to access the PMIC's memory registers until the 3ms timing requirement is satisfied. The PMIC allows access to its memory registers as long as VIN_MGMT input supply is valid and the PMIC does not require VIN_BULK input supply. The host may read PMIC's own internal memory content prior to ramping VIN_BULK supply.

During power on, the host shall:

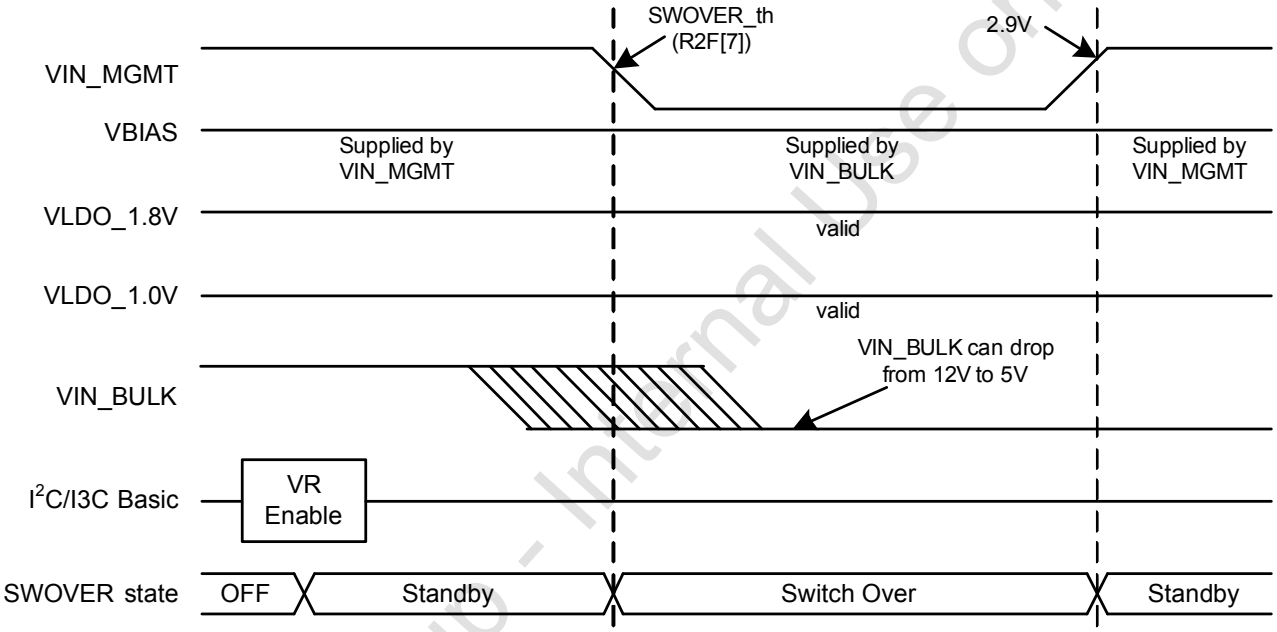
- Ramp up VIN_MGMT supply; ramp up VIN_BULK supply; (No timing relationship between the two supplies)
- Send VR Enable command by setting register R32[7] = '1'.

The host, prior to issuing VR Enable command, must keep VIN_MGMT input supply valid as long as VLDO_1.8V & VLDO_1.0V LDO outputs are required. If VIN_MGMT input supply is removed or drops below 2.7V, the PMIC does not guarantee any operation including VLDO_1.8V & VLDO_1.0V LDO outputs as well as its I²C/I3C Basic interface regardless of VIN_BULK input supply status.

3.4 Switch Over Function (SWOVER)

After the host issues VR Enable command to the PMIC, the PMIC offers the input supply Switch Over (SWOVER) function. The PMIC has an automatic internal input supply Switch Over function from VIN_MGMT input supply to VIN_BULK input supply. The PMIC triggers the switchover to VIN_BULK input supply when VIN_MGMT input supply drops below the threshold set in Register R2F[7]. The VBIAS is supplied by VIN_BULK after switchover. The PMIC's VLDO_1.8V & VLDO_1.0V LDO outputs and I²C/I3C Basic interface (SCL/SDA) continue to operate as normal. While the PMIC is in the Switch Over mode to VIN_BULK, VIN_MGMT input supply can re-power backup at any time and the PMIC switches back to VIN_MGMT input supply for its LDO outputs and I²C/I3C Basic interface continues to operate as normal. Figure 15 shows automatic internal Switch Over function.

Figure 15. Input Supply Switch Over Function



3.5 Switching Regulators Power ON Sequence

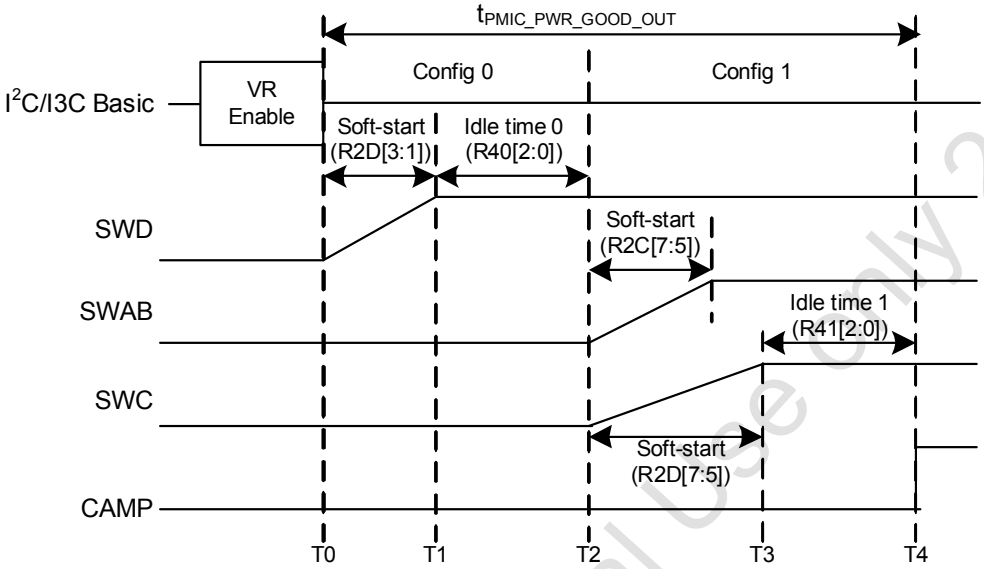
After VR Enable command is registered, the PMIC shall complete the following power up steps:

1. Begin to execute Power On sequence as programmed in Power On sequencing registers of R40 (Config 0) to R43 (Config 3) etc.;
2. Power up all enabled output switching regulators and be ready for normal operation;
3. Update status registers and float CAMP output signal;

Power On sequencing registers of R40 to R43 are allocated in PMIC's DIMM vendor registers region (password protected).

Figure 16 shows the specific sequence of ramping up the output regulators as an example. The specific ramp up sequence is configurable through the registers.

Figure 16. Power On Sequence with Config 0 and Config 1 Enabled (SWA, SWB Operated in 2-Phase) (R40[7:0]=10001xxx; R41[7:0]=11111xxx; R42=0x00; R43=0x00)



Assuming that SWA and SWB are configured into dual-phase and single output power rail per setting in R4F[0]. Power on sequencing registers are configured as R40[7:0]=10001xxx; R41[7:0]=11111xxx; R42=0x00; R43=0x00. The sequence shown in Figure 16 is described as following:

The host issues VR_ENABLE command. At time 'T0', the SWD regulator begins to ramp up with its soft-start time set in R2D[3:1]. At time 'T1', SWD completes the soft-start time after reaching the preset voltage. From time 'T1', the PMIC waits for the 'idle time 0' set in R40[2:0]. At time 'T2', the next group of regulators of SWAB and SWC begin to ramp up with their related soft-start time set in R2C[7:5] and R2D[7:5]. At time 'T3', both SWAB and SWC complete the soft-start time after reaching the relevant preset voltage. From time 'T3', the PMIC waits for the 'idle time 1' set in R41[2:0]. At time 'T4', the PMIC keeps the CAMP signal floating (i.e it remains High). The total power-On time should be $t_{PMIC\_PWR\_GOOD\_OUT}$.

After power On, the PMIC allows VIN_BULK input supply to vary and go as low as VIN_BULK min value (4.25V), while it continues to operate as normal. The VIN_MGMT input supply can drop and may recover at any time.

If PMIC CAMP signal is not pulled High after the Power On Sequence is completed, the host can access the PMIC status registers for detailed information after $t_{PMIC\_PWR\_GOOD\_OUT}$ time. The PMIC may NACK for any host request on I2C or I3C Basic bus after VR Enable command until $t_{PMIC\_PWR\_GOOD\_OUT}$ time expires.

3.6 Switching Regulators Power Off Sequence

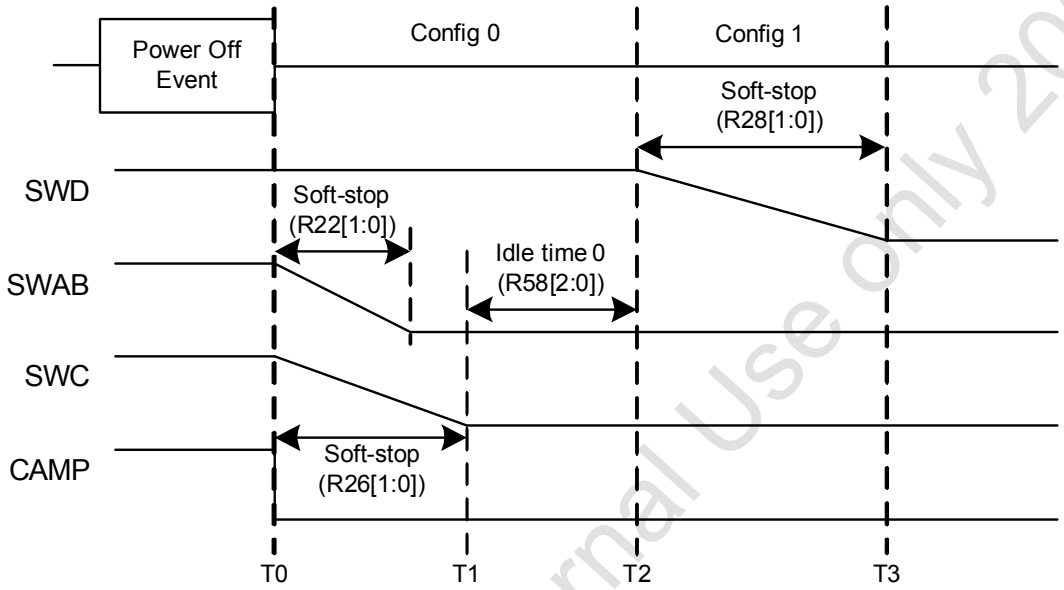
The Power Off Sequence for all four buck regulators is activated when one of the following events occurs:

1. Setting control register bit VR_ENABLE (R32[7]) to 1'b0 (Only in Non-Write Protect mode);
2. Removing PMIC's 12 V input supply;
3. PMIC detecting CAMP input signal transition from High to Low logic (R32[4]="0");
4. PMIC detecting some events under column of VR Disable Trigger in Table 6.

The behavioral of the Power Off Sequence is similar to the Power On sequence, and the settings can be programmed in registers from R58 (Config 0) to R5B (Config 3) which are allocated in the password-protected DIMM vendor register region.

Figure 17 shows the specific sequence of ramping down the output regulators (SWAB, SWC and SWD) as an example. The specific ramp down sequence is configurable through the registers.

Figure 17. Power Off Sequence with Config 0 and Config 1 Enabled (SWA, SWB Operated in 2-Phase) (R58[7:0]=11110xxx; R59[7:0]=11111000; R5A=0x00; R5B=0x00)



In addition, in Non-Write Protect mode, the host can configure one or more bits in R2F [6:3] to '0' in any specific Power Off Sequence. The PMIC keeps the CAMP signal floating (i.e it remains High) because this is intentional command from the host and not a fault condition. Note that host can re-enable any of disabled output regulators by configuring one or more bits in R2F [6:3] to '1' in any specific sequence.

3.7 CAMP Signal

The CAMP (Control AND Monitor Port) signal provides three different functions.

1. Register Write Protect function
2. Fail_n function
3. Status function

3.7.1 Register Write Protect Function

By default, the PMIC register Write Protect function is enabled (R2F[2]='0'). The CAMP input signal level determines when PMIC enters or exits the Write Protect mode. The PMIC enters the Write Protect mode when CAMP signal is at logic level High. PMIC exits the Write Protect mode when CAMP signal is at logic Low. In Write Protect mode, the PMIC does not allow to modify all R15 to R2F, R32 and R35 in the host region as well as R40 to R6F in the DIMM region. The PMIC simply ignores the host request for write operation in Write Protect mode. The PMIC allows all register read access in Write Protect mode.

If R2F[2]='1', the PMIC does not enter Write Protect mode. The PMIC CAMP input signal has no effect on Write Protect function. The PMIC allow write and read access to all registers.

Caution: The operation of Non-write Protect mode should be limited to lab and debug environment instead of normal system operation.

3.7.2 Fail_n Function

By default, PMIC Fail_n function is enabled (R32[4]='0'). When PMIC CAMP input signal transitions from High to Low, the PMIC executes VR Disable command, asserts CAMP signal low (if R32[3]='0'), exits the Write Protect mode and clears R32[7] to '0'.

If R32[4]='1', the PMIC Fail_n function is disabled. The Fail_n function is independent of PMIC's Write Protect function.

3.7.3 Status Function

The PMIC CAMP output signal indicates status of VIN_BULK input supply and all output regulators (SWx power rails, VLDO_1.8V, VLDO_1.1V and VBIAS). Once PMIC receives VR Enable command, the PMIC floats CAMP pin when VIN_BULK input supply is valid and all enabled output regulator's tolerances are maintained. Note that CAMP pin is not effected based on VIN_MGMT input supply.

At first power up, with the stable & valid input supply VIN_MGMT as well as VLDO_1.8V & VLDO_1.0V LDO outputs, the PMIC asserts CAMP pin Low.

Once PMIC receives VR Enable command from the host, the PMIC enables all appropriate output regulators and updates corresponding status registers and enters state called as “Regulation”. At this point, PMIC floats CAMP output and the external board pullup resistor pulls the CAMP pin high. Once the CAMP pin is pulled high (i.e no other PMIC is driving the CAMP pin low), the PMIC enters state stated called as “online” state.

Once the CAMP pin is High, if PMIC detects any condition either on VIN_BULK input supply or any of the output regulators (SWx power rails, VLDO_1.8V, VLDO_1.0V, and VBIAS) that causes the PMIC to update it status registers to indicate the power status is not good, then PMIC asserts CAMP pin low and keeps it asserted until the host explicitly takes a specific action corresponding to it. The PMIC does not automatically let the CAMP pin float even if the condition that triggered the PMIC to assert the CAMP pin no longer exists. In other words, the PMIC’s CAMP pin is latched and once latched, it must be explicitly addressed by the host.

Regardless of whether PMIC is operating in Write Protect mode or not, the PMIC always asserts CAMP signal low to indicate the status if there is a fault event.

3.8 GSI_n Signal

General Status Interrupt (GSI_n) is an Open Drain output signal. By default at power on, GSI_n output is disabled. The host can enable the GSI_n output by setting R1B[3]=‘1’. Typically, GSI_n output is pulled up to 1 kΩ resistor to 1.8V or 3.3V. The PMIC asserts GSI_n output for the events as described in Table 6.

3.9 Finite State Machine (FSM)

Finite State Machine is implemented within the PMIC to control different operating states. Figure 18 shows high-level simplified state diagram. Specific transition details are function of PMIC's configuration register settings (e.g. R2F, R32, etc. as well as CAMP signal and input/output supplies). Please refer to detailed functional description and configuration register definition for PMIC operation.

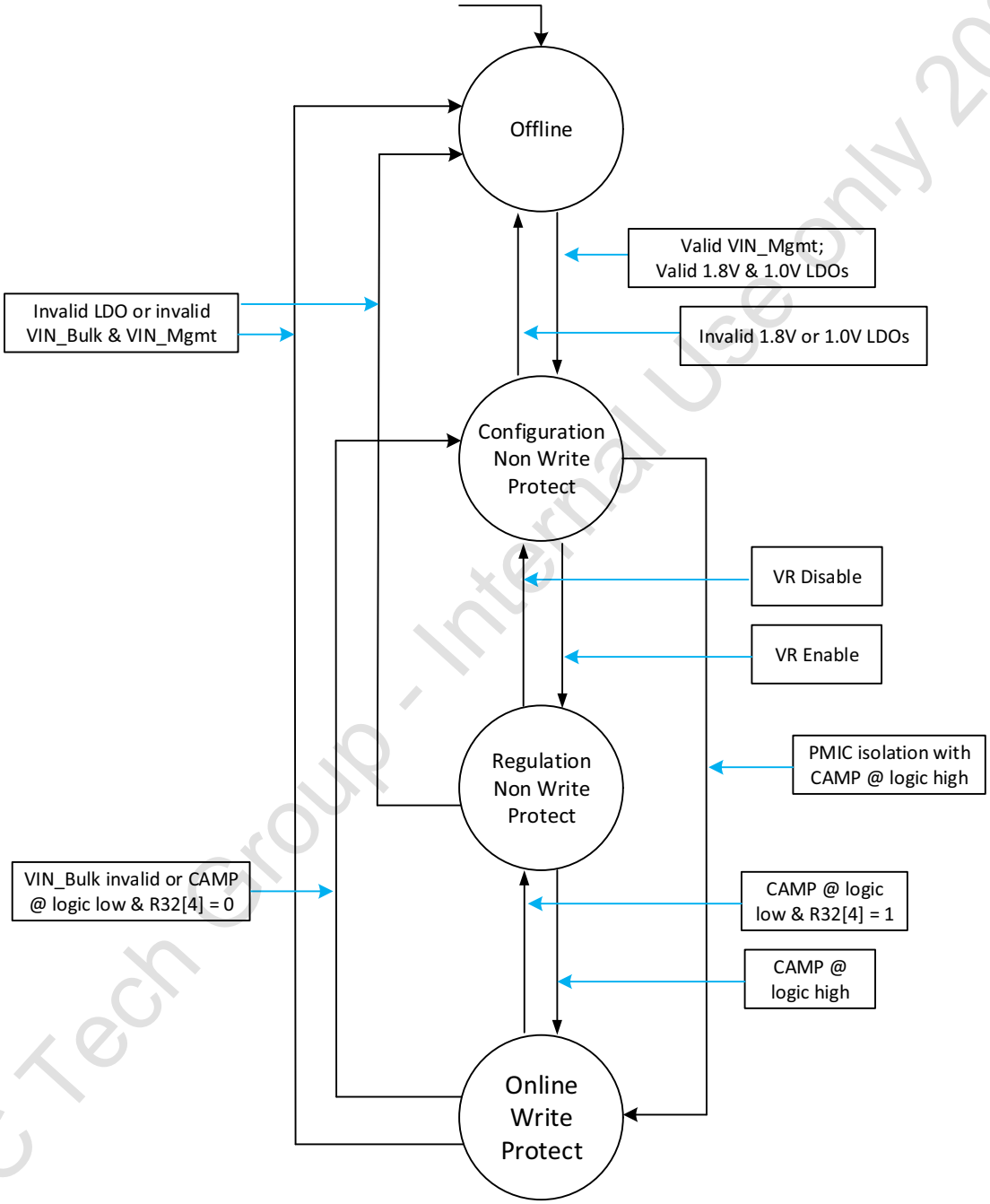
The detailed state descriptions of the FSM are as below:

- **Offline State:** All registers are reset to specified default values. VLDO_1.8V, VLDO_1.0V and DCDC SWx regulators are off. CAMP is Hi-Z.
- **CONFIGURATION (Non-Write Protect) State:** All registers are writable and readable. PMIC downloads the data from MTP when the first time entering the CONFIGURATION State. The I^2C/I3C Basic bus interface is alive and running. LDOs are valid; switch regulators are off. CAMP is low.
- **REGULATION (Non-Write Protect) State:** All registers are writable and readable. All enabled output rails are

active. Internal power good is floated, external CAMP is low.

- **Online (Write Protect) State:** All registers are readable. All non protect registers are writable. All enabled output rails are active. CAMP is high.

Figure 18. PMIC FSM



3.10 PMIC Response to Function Interrupt

Table 6 lists the PMIC behaviors in response to various interrupt events when mask register bits are not set.

Table 6. PMIC Events Interrupt Summary (Sheet 1 of 2)

Status Event	Status Bit	Clear Bit	Mask Bit	Threshold Setting	Hysteresis Threshold	NVM Error Log	GSI_n Output	CAMP (Output)	VR Disable Trigger
VIN_BULK Power Good	R08[7]	R10[7]	R15[7]	R1A[7:5]	R1A[7:5] + 1 V	N/A	Low	Low	No
VIN_BULK Over Voltage	R08[0]	R10[0]	R15[0]	R1B[7]	R1B[7] - 1.2 V	R04[5], R05[2:0]	Low	Low	Yes
VIN_BULK Under Voltage	R33[3]	R14[3]	R19[3]	4 V	R1A[7:5] + 1 V	N/A	Low	Low	Yes
VIN_MGMT Over Voltage	R08[1]	R10[1]	R15[1]	R1B[5]	3.5 V	N/A	Low	High	No
VBIAS Power Good	R09[6]	R11[6]	R16[6]	R1A[3]	2.8 V	N/A	Low	Low	No
VBIAS Under Voltage	R33[3]	R14[3]	R19[3]	2.55 V	2.8 V	N/A	Low	Low	Yes
VIN_MGMT to VIN_BULK Switch Over	R09[4]	R11[4]	R16[4]	R2F[7]	2.9 V	N/A	Low	High	No
Valid VIN_MGMT in Switch Over	R33[4]	R14[4]	R19[4]	2.9 V	-	N/A	Low	High	No
1.8V LDO Power Good	R09[5]	R11[5]	R16[5]	R1A[2]	1.66 V	N/A	Low	Low	No
1.0V LDO Power Good	R33[2]	R14[2]	R19[2]	R1A[0]	R1A [0] + 6%	N/A	Low	Low	No
SWA Output Power Good	R08[5]	R10[5]	R15[5]	R21[0], R22[7:6]	R21[0] + 2.5% R22[7:6] - 2.5%	N/A	Low	Low	No
SWB Output Power Good	R08[4]	R10[4]	R15[4]	R23[0], R24[7:6]	R23[0] + 2.5% R24[7:6] - 2.5%	N/A	Low	Low	No
SWC Output Power Good	R08[3]	R10[3]	R15[3]	R25[0], R26[7:6]	R25[0] + 2.5% R26[7:6] - 2.5%	N/A	Low	Low	No
SWD Output Power Good	R08[2]	R10[2]	R15[2]	R27[0], R28[7:6]	R27[0] + 2.5% R28[7:6] - 2.5%	N/A	Low	Low	No
SWA Output Over Voltage	R0A[7]	R12[7]	R17[7]	R22[5:4]	-	R04[6], R05[6,2:0], R06[3]	Low	Low	Yes
SWB Output Over Voltage	R0A[6]	R12[6]	R17[6]	R24[5:4]	-	R04[6], R05[5,2:0], R06[2]	Low	Low	Yes
SWC Output Over Voltage	R0A[5]	R12[5]	R17[5]	R26[5:4]	-	R04[6], R05[4,2:0], R06[1]	Low	Low	Yes

Table 6. PMIC Events Interrupt Summary (Sheet 2 of 2)

Status Event	Status Bit	Clear Bit	Mask Bit	Threshold Setting	Hysteresis Threshold	NVM Error Log	GSI_n Output	CAMP (Output)	VR Disable Trigger
SWD Output Over Voltage	R0A[4]	R12[4]	R17[4]	R28[5:4]	-	R04[6], R05[3,2:0], R06[0]	Low	Low	Yes
SWA Output Under Voltage	R0B[3]	R13[3]	R18[3]	R22[3:2]	-	R04[6], R05[6,2:0], R06[7]	Low	Low	Yes
SWB Output Under Voltage	R0B[2]	R13[2]	R18[2]	R24[3:2]	-	R04[6], R05[5,2:0], R06[6]	Low	Low	Yes
SWC Output Under Voltage	R0B[1]	R13[1]	R18[1]	R26[3:2]	-	R04[6], R05[4,2:0], R06[5]	Low	Low	Yes
SWD Output Under Voltage	R0B[0]	R13[0]	R18[0]	R28[3:2]	-	R04[6], R05[3,2:0], R06[4]	Low	Low	Yes
SWA Output Current Limit	R0B[7]	R13[7]	R18[7]	R20[7:6]	-	N/A	Low	High	No
SWB Output Current Limit	R0B[6]	R13[6]	R18[6]	R20[5:4]	-	N/A	Low	High	No
SWC Output Current Limit	R0B[5]	R13[5]	R18[5]	R20[3:2]	-	N/A	Low	High	No
SWD Output Current Limit	R0B[4]	R13[4]	R18[4]	R20[1:0]	-	N/A	Low	High	No
SWA Output High Current/ Power	R09[3]	R11[3]	R16[3]	R1C[7:2]	-	N/A	Low	High	No
SWB Output High Current/ Power	R09[2]	R11[2]	R16[2]	R1D[7:2]	-	N/A	Low	High	No
SWC Output High Current/ Power	R09[1]	R11[1]	R16[1]	R1E[7:2]	-	N/A	Low	High	No
SWD Output High Current/ Power	R09[0]	R11[0]	R16[0]	R1F[7:2]	-	N/A	Low	High	No
High Temperature Warning	R09[7]	R11[7]	R16[7]	R1B[2:0]	R1B[2:0] - 10 °C	N/A	Low	High	No
Critical Temperature	R08[6]	N/A	N/A	R2E[2:0]	-	R04[4], R05[2:0]	Low	Low	Yes
PEC Error	R0A[3]	R12[3]	R17[3]	N/A	-	-	Low	High	No
Parity Error	R0A[2]	R12[2]	R17[2]	N/A	-	-	Low	High	No

The host is expected to read appropriate status registers to determine and isolate the cause of the GSI_n signal assertion or CAMP signal assertion. The host may attempt to clear or mask the appropriate corresponding interrupt event. The PMIC keeps the GSI_n signal asserted or CAMP signal asserted until the appropriate corresponding registers are explicitly cleared or masked by the host. Table 7 and Table 8 show the PMIC's response of GSI_n signal and CAMP output signal for each event before and after host issues the Clear command. Table 7 and Table 8 assumes that all mask bits are either '0' or '1' for simplicity.

Table 7. PMIC Response for Clear Command by Host - 1

	Event Occurred; All Mask Bits = '0'		Clear Command; Event Not Present; All Mask Bits = '0'		Event Occurred; All Mask Bits = '1'		Clear Command; Event Not Present; All Mask Bits = '1'	
			R2F[1:0] = '00' or '01' or '10'		R2F[1:0] = '00'		R2F[1:0] = '00'	
Event	**CAMP Output**	**GSI_n Output**	**CAMP Output**	**GSI_n Output**	**CAMP Output**	**GSI_n Output**	**CAMP Output**	**GSI_n Output**
VIN_BULK Power Good	Low	Low	High	High	Low	High	High	High
VIN_BULK Over Voltage	Low	Low	Low	High	Low	High	Low	High
VIN_MGMT Over Voltage	High	Low	High	High	High	High	High	High
SWA Output Power Good SWB Output Power Good SWC Output Power Good SWD Output Power Good	Low Low Low Low	Low Low Low Low	High High High High	High High High High	Low Low Low Low	High High High High	High High High High	High High High High
1.8 V LDO Power Good 1.0 V LDO Power Good VBIAS LDO Power Good	Low Low Low	Low Low Low	High High High	High High High	Low Low Low	High High High	High High High	High High High
SWA Output Over Voltage SWB Output Over Voltage SWC Output Over Voltage SWD Output Over Voltage	Low Low Low Low	Low Low Low Low	Low Low Low Low	High High High High	Low Low Low Low	High High High High	Low Low Low Low	High High High High
SWA Output Under Voltage SWB Output Under Voltage SWC Output Under Voltage SWD Output Under Voltage	Low Low Low Low	Low Low Low Low	Low Low Low Low	High High High High	Low Low Low Low	High High High High	Low Low Low Low	High High High High
VBIAS LDO Output or VIN_BULK Input Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit SWB Output Current Limit SWC Output Current Limit SWD Output Current Limit	High High High High	Low Low Low Low	High High High High	High High High High	High High High High	High High High High	High High High High	High High High High
SWA Output High Current/Power SWB Output High Current/Power SWC Output High Current/Power SWD Output High Current/Power	High High High High	Low Low Low Low	High High High High	High High High High	High High High High	High High High High	High High High High	High High High High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	P/C	P/C	Low	Low	P/C	P/C
VIN_MGMT to VIN_BULK Switch Over	High	Low	High	High	High	High	High	High
Valid VIN_MGMT in Switch Over	High	Low	High	High	High	High	High	High
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Table 8. PMIC Response for Clear Command by Host - 2

Event	Event Occurred; All Mask Bits = '1'		Clear Command; Event Not Present; All Mask Bits = '1'		Event Occurred; All Mask Bits = '1'		Clear Command; Event Not Present; All Mask Bits = '1'	
	R2F[1:0] = '01'		R2F[1:0] = '01'		R2F[1:0] = '10'		R2F[1:0] = '10'	
	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output	CAMP Output	GSI_n Output
VIN_BULK Power Good	High	Low	High	High	High	High	High	High
VIN_BULK Over Voltage	Low	Low	Low	High	Low	High	Low	High
VIN_MGMT Over Voltage	High	Low	High	High	High	High	High	High
SWA Output Power Good SWB Output Power Good SWC Output Power Good SWD Output Power Good	High High High High	Low Low Low Low	High High High High	High High High High	High High High High	High High High High	High High High High	High High High High
1.8 V LDO Power Good 1.0 V LDO Power Good VBIAS LDO Power Good	High High High	Low Low Low	High High High	High High High	High High High	High High High	High High High	High High High
SWA Output Over Voltage SWB Output Over Voltage SWC Output Over Voltage SWD Output Over Voltage	Low Low Low Low	Low Low Low Low	Low Low Low Low	High High High High	Low Low Low Low	High High High High	Low Low Low Low	High High High High
SWA Output Under Voltage SWB Output Under Voltage SWC Output Under Voltage SWD Output Under Voltage	Low Low Low Low	Low Low Low Low	Low Low Low Low	High High High High	Low Low Low Low	High High High High	Low Low Low Low	High High High High
VBIAS LDO Output or VIN_BULK Input Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit SWB Output Current Limit SWC Output Current Limit SWD Output Current Limit	High High High High	Low Low Low Low	High High High High	High High High High	High High High High	High High High High	High High High High	High High High High
SWA Output High Current/Power SWB Output High Current/Power SWC Output High Current/Power SWD Output High Current/Power	High High High High	Low Low Low Low	High High High High	High High High High	High High High High	High High High High	High High High High	High High High High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	P/C	P/C	Low	Low	P/C	P/C
VIN_MGMT to VIN_BULK Switch Over	High	Low	High	High	High	High	High	High
Valid VIN_MGMT in Switchover	High	Low	High	High	High	High	High	High
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Note that when host masks any of the event in appropriate register, it only masks the assertion of GSI_n output signal or assertion of CAMP output signal. The PMIC functional behavior remains the same as noted for each event other than assertion of GSI_n output signal and assertion of CAMP output signal.

3.11 VIN_BULK Power Good Status

When VIN_BULK goes below VINx_PG_FL set by R1A[7:5], the PMIC will set the VIN_BULK status in R08[7] and de-assert CAMP output signal, and continue to operate as normal. The PMIC allows access to all registers. The host is responsible for taking any specific action, and may query the PMIC register space to determine and identify the cause of the CAMP de-assertion.

3.12 VIN_BULK UV Protection

When VIN_BULK goes below VINx_UV_FL(4V), the PMIC will set the VIN_BULK under-voltage lockout status in R33[3] and de-assert CAMP output signal, and start the Power Down sequence (Config 0 to Config 3) to disable its regulator outputs (SWA/B/C/D).

3.13 VIN_BULK OV Protection

When VIN_BULK goes above VINx_OV_RS set by R1B[7], PMIC will set the VIN_BULK over-voltage lockout status in R08[0]. PMIC allows access to all registers, and continues to operate as normal. If VIN_BULK OV condition remains greater than the deglitch time (typ. 13 µs), PMIC will de-assert CAMP output signal and internally generate VR Disable command, and start the Power Down sequence (Config 0 to Config 3) to disable its regulator outputs (SWA/B/C/D). PMIC keeps its VLDO_1.8V and VLDO_1.0V outputs active, and continues to allow access to all registers.

3.14 VIN_MGMT OV Protection

When VIN_MGMT goes above VIN_MGMT_OV_RS set by R1B[5], the PMIC will set the status R08[1]. The PMIC allows access to all registers and continues to operate as normal.

3.15 VBIAS Power Good Status

When VBIAS goes below VBIAS_PG_FL set by R1A[3], the PMIC will set Register R09[6] and drive CAMP output signal. The PMIC continues to operate as normal, and allows access to all registers. The host is responsible for taking any specific action, and may query the PMIC register space to determine and identify the cause of the CAMP de-assertion.

3.16 VBIAS UV Protection

When VBIAS goes below VBIAS_UV_FL(2.55 V), the PMIC will shut down all of its switching output regulators without going through the power-off sequence. The VLDO_1.8V and VLDO_1.0V are no longer active and all the registers will be reset to the default value.

3.17 VLDO_1.8V and VLDO_1.0V Power Good Status

When VLDO_1.8V goes below $V_{PG\_LDO1P8\_L}$ set by R1A[2] or VLDO_1.0V goes below $V_{PG\_LDO1P0\_L}$ set by R1A[0], PMIC will set Register R09[5] or R33[2] accordingly and drive CAMP output signal. PMIC continues to operate as normal, and allows access to all registers. Host is responsible for taking any specific action, and may query PMIC register space to determine and identify the cause of the CAMP de-assertion.

3.18 LDO Output Failure

When LDO VLDO_1.8V or VLDO_1.0V goes below their related threshold of V_{UV_LDOx}, the PMIC returns to the "offline" state.

3.19 DC/DC Power Good Status

When any output (SWA/B/C/D) goes below SWx_PGL_th set by R21[0], R23[0], R25[0], R27[0] or goes above SWx_PGH_th set by R22[7:6], R24[7:6], R26[7:6], R28[7:6], the PMIC will set Register R08[5:2] accordingly and drive CAMP output signal to Low. The PMIC continues to operate as normal, and allows access to all registers. The host is responsible for taking any specific action, and may query the PMIC register space to determine and identify the cause of the CAMP de-assertion.

3.20 DC/DC OV Protection

When any output (SWA/B/C/D) goes above SWx_OV_th set by R22[5:4], R24[5:4], R26[5:4], R28[5:4], the PMIC will set Register R0A[7:4] accordingly. If DCDC_OV condition remains greater than the deglitch time (Typ 13µs), the PMIC will de-assert CAMP output signal and start the Power Down sequence (Config0 to Config3) to disable its regulator outputs (SWA/B/C/D) (under R4F[7]='0'). The PMIC keeps its VLDO_1.8V and VLDO_1.0V outputs active, and continues to allow access to all registers.

3.21 DC/DC UV Protection

When any output (SWA/B/C/D) goes below SWx_UV_th set by R22[3:2], R24[3:2], R26[3:2], R28[3:2], the PMIC will set Register R0B[3:0] accordingly. If DCDC_UV condition remains greater than the deglitch time (Typ 13µs), the PMIC will de-assert CAMP output signal and start the Power Down sequence (Config0 to Config3) to disable its regulator outputs (SWA/B/C/D) (under R4F[7]='0'). The PMIC keeps its VLDO_1.8V and VLDO_1.0V outputs active, and continues to allow accessing to all registers.

3.22 High Temp Warning and Critical Temp Protection

If the PMIC temperature goes above T_{WARN} set by R1B[2:0], the PMIC will set the warning status Register R09[7]. The PMIC continues to operate as normal, and allows access to all registers. The host is responsible for taking any specific action, and may query the PMIC register space to determine and identify the cause. If the PMIC temperature goes above T_{OTP} set by R2E[2:0], the PMIC will shut down all of its switching regulators without going through the Power-Off sequence. However, the PMIC keeps VBIAS and LDO regulators (VLDO_1.8V and VLDO_1.0V) active and allows access to all registers. When the temperature drops below the threshold, the host must re-start the PMIC by going through the power cycle of the VIN_MGMT and VIN_BULK input supply.

3.23 Output Current Limit

The PMIC has an output current limiter mechanism to limit the current on the PMIC output voltage regulators. The cycle-by-cycle over-current conditions are detected and handled by the PMIC. When the inductor valley current goes above I_{LIM_Valley} set by R20[7:6], R20[5:4], R20[3:2], R20[1:0], the next t_{ON} cycle is blocked until the inductor current falls below I_{LIM_Valley}. The maximum valley current is therefore clamped to I_{LIM_Valley}. If the current limit event continuously exists, the PMIC will set the warning status Register R0B[7:4] appropriately.

3.24 Reverse Output Current Limit

The PMIC has a reversed output current limiter mechanism to limit the current on the PMIC output voltage regulators. The cycle-by-cycle reversed over-current conditions are detected and handled by the PMIC. When the inductor current goes below about -4.5A, the next t_{ON} cycle is forcedly started. The minimum valley current is therefore clamped to about -4.5A.

3.25 Dynamic Voltage Scaling (DVS)

In the Non-Write Protect mode, the output voltage of switching regulators SWA, SWB, SWC and SWD can be set dynamically by Host I²C/I3C Basic command. The voltage ramping up/down slew rate is typical 1mV/µs.

3.26 Analog-to-Digital Conversion

The PMIC supports analog-to-digital converter (ADC) to monitor the voltage of both the input supply power rails (VIN_BULK and VIN_MGMT) and the output voltage regulators (SWA, SWB, SWC, SWD, VBIAS, VLDO_1.8V, VLDO_1.0V). The general purpose of ADC interface is summarized in Table 9.

The register R30[7:3] allows to enable the ADC and select the desired input supply voltage or output supply voltage. The register R31[7:0] provides the actual voltage measurement. The PMIC also monitors the current or power of output voltage regulators (SWA, SWB, SWC and SWD) and updates registers R0C[7:2] for SWA, R0D[7:2] for SWB, R0E[7:2] for SWC and R0F[7:2] for SWD. The register R1B[6] allows the host to select whether the PMIC should report current measurements or power measurements.

Table 9. ADC Interface General Purpose Summary

Default Monitoring (5-channel) + User Selection (1-channel)			
Channel Sensor	**Monitor Type**	**Monitor Register**	**Current or Power Measurement Selector**
SWA Output Current	Default monitor	R0C/R1B	R1B[6]=0 Set for current R1B[6]=1 Set for power R1A[1]=0 Report power for single switcher output R1A[1]=1 Report the sum of power for all switcher outputs (SWA, SWB, SWC, SWD)
SWB Output Current		R0D/R1B	
SWC Output Current		R0E/R1B	
SWD Output Current		R0F/R1B	
PMIC die Temp.		R33	
SWA Output Voltage	User selection	R30/R31	
SWB Output Voltage			
SWC Output Voltage			
SWD Output Voltage			
VIN_BULK Input Voltage			
VIN_MGMT Input Voltage			
VBIAS Output Voltage			
VLDO_1.8V Output Voltage			
VLDO_1.0V Output Voltage			

3.27 PMIC Error Injection

The PMIC offers error injection function for the purpose of debug, test and validation at various stages.

- Error Injection Function Usage prior to VR Enable:

  Prior to VR Enable command, the Error injection function may be invoked by setting R35[7]='1' during the configuration state. The PMIC shall not execute power on sequence and shall not enable PMIC output

regulators when PMIC receives VR Enable command. The PMIC shall not update error log registers (R04 to R06).

- Error Injection Function Usage after VR Enable:

  After PMIC output regulators are enabled with VR Enable command and PMIC is in Non-Write Protect mode, the error injection function may be invoked by setting R35[7]='1'. The R35[7]='1' is disallowed if PMIC is in Write Protect mode.

The Indicated error injection will only occur when the outputs are enabled. The injected error will assert the PMIC fault sensor. The PMIC will respond with the appropriate output control and set the status bits. To exit from Error Injection Mode, the PMIC must go through power cycle of both VIN_BULK and VIN_MGMT input supply.

3.28 Application Note

The discrete components, such as inductors and capacitors, and PMIC design parameters, such as switching frequency, contribute a lot to the performance of DC-DC regulators, such as efficiency and load transient response. This section provides some design recommendations based on the Montage evaluation board.

3.28.1 Inductor Selection

Inductors with package size of 4.3mm(max) x 4.3mm (max) x 2.0mm (max) can be used for small form factor purpose. Inductor DCR and ACR are critical parameters for good efficiency. 0.47µH inductors for SWA/B/C and 1.0µH inductor for SWD are used on the Montage evaluation board with information as shown in Table 10.

Table 10. Evaluation Board Inductors

Power Rail	Inductance	SAMSUNG ELECTRO-MECHANICS P/N	ALPS ALPINE P/N
SWA/B/C	0.47µH	CIGW404020KMR47MLF	GLVSRR4701A
SWD	1.0µH	CIGW404020KM1R0MLF	GLVSR1R001A

3.28.2 Capacitor Selection

The PMIC is designed to use ceramic capacitors for its input and output filters. DC bias characteristics of the capacitor must be considered for the selection of the voltage rating and case size of the capacitor. To achieve better load transient performance for 3A per channel application, JEDEC defines 350µF distributed capacitance per phase to be placed nearby DRAMs load sides, besides 3x47µF local ceramic capacitors nearby PMIC. See Section "Reference Application" for the input/output capacitors selection. Table 11 shows capacitors used on Montage evaluation board.

Table 11. Evaluation Board Capacitors[1,2] (Sheet 1 of 2)

Item	Qty (per channel)	Value	Description	Part Number
VINx	2	22µF	0805 MLCC, X5R, 25V	GRT21BR61E226ME13L
	1	0.1µF	0402 MLCC, X6S, 25V	GRM155C81E104KA12D
VIN_MGMT	1	4.7µF	0402 MLCC,X6S, 6.3V	GRM155C80J475MEAAD
VBIAS	1	4.7µF	0402 MLCC,X6S, 6.3V	GRM155C80J475MEAAD
Bootstrap	1	100nF	0402 MLCC,X6S, 25V	GRM155C81E104KA12D

Table 11. Evaluation Board Capacitors[1,2] (Sheet 2 of 2)

Item	Qty (per channel)	Value	Description	Part Number
SWx Power Rail Output	3 (PMIC local side caps)	47µF	0805 MLCC,X6S, 4V	GRT21BC80G476ME13L
	7 (Remote equivalent caps)			
VLDO_1.0V	1	4.7µF	0402 MLCC,X6S, 6.3V	GRM155C80J475MEAAD
VLDO_1.8V	1	4.7µF	0402 MLCC,X6S, 6.3V	GRM155C80J475MEAAD

1. Actual DIMM may use X6S or X7R caps which depends on the real system temperature.
2. 0.1µF decoupling caps, such as GRM152C80J104KE19, can be placed closely to VIN_MGMT,VBIAS and VLDO_1.x LDOs.

3.28.3 Other Design Highlights

- Switching frequency: To make tradeoff between efficiency and load transient response, the phase switching frequency is set to 750kHz on Montage evaluation board.
- DCM mode: DCM mode may be selected for better efficiency at light load.
- Dual-Phase configuration: SWA and SWB can be set to dual-phase single regulator mode (R4F[0]="1") as JEDEC DIMM schematic does.
- Valley current limit: To support 3A TDC per phase application, The valley current limit of each phase needs to be set to 3.5A (R50="FF").
- VLDO_1.8V and VLDO_1.0V: The output voltage of two LDOs shall be set to 1.8V and 1.0V respectively to provide the right supply voltage for other components on the DIMM.

3.29 Method to Identify & Map Out DIMM with a PMIC Fault in Shared CAMP Topology

A typical DDR5 server platform may have up to 32 DDR5 DIMM sockets. It is possible that 8 DDR5 DIMMs share CAMP signal. The exact number of DDR5 DIMMs that share CAMP signal is beyond the scope of this section. It is assumed that CAMP signal is pulled up on the platform or on the controller via a 1kΩ pull-up resistor to either 3.3V or 1.8V.

In a DDR5 server platform, it is possible that one or more DDR5 DIMMs may have encountered one of PMIC faults as listed below, which has generated the VR Disable event. Also refer to Table 6.

- SWx Over Voltage
- SWx Under Votlage
- VIN_Bulk Over Voltage
- VIN_Bulk Under Voltage
- Critical Temperature

In this environment, it is desired to let the platform continue to power up and that faulty PMIC does not interfere with the platform operation. This section describes a BIOS or appropriate software method to identify the faulty PMIC/DDR5 DIMM and then to map out the faulty PMIC/DDR5 DIMM from the memory subsystem. The fault scenario noted here is one example of fault scenario. Note that initial failure may occur during operation, hence BIOS needs to determine and log fault condition and then execute the map out routine.

Faulty PMIC Identification:

1. Power up the platform (i.e. DDR5 DIMMs) by applying VIN_Bulk and VIN_Mgmt input supplies.

2. Broadcast VR Enable command to all PMICs.
3. If all PMICs power up their regulators successfully, all PMICs float the CAMP signal and the pull-up resistor pulls the CAMP signal high, which indicaties that all PMICs (i.e. DDR5 DIMMs) have powered up successfully.
4. However, if one PMIC (or more PMICs) fails to power up their regulators, then that PMIC continues to hold the CAMP signal low, while other PMICs that do power up their regulators successfully float the CAMP signal. The net effect is that CAMP signal remains low.
5. BIOS eventually times out as the CAMP signal is not pulled up high, and interrogates all PMIC's status registers one at a time. The interrogation process of PMIC status registers allows BIOS to identify which PMICs regulators are successfully powered up and which PMICs are faulty.

Once BIOS identifies the faulty PMIC, BIOS stores the faulty PMIC (DDR5 DIMM) identification in its non-volatile memory.

Isolating and Securing Faulted PMIC:

1. Once the faulty PMIC is identified, the platform may recycle the power by simultaneously removing VIN_Bulk and VIN_Mgmt input supply and then re-applying VIN_Bulk and VIN_Mgmt input supplies. This puts PMIC in configuration mode,
   a. BIOS reads PMIC error log registers to determine 'bad' PMIC. The BIOS also has a prior knowledge of a faulty PMIC.
2. BIOS performs the following steps to the faulty PMIC.
   a. Write R32 = 0x08 (Floats CAMP signal; prevents PMIC interference)
   b. Ensure R2F[2] = '0'.
3. Broadcast VR Enable command to all PMICs.
4. All good PMIC executes Power On Sequence and floats the CAMP signal. The faulty PMIC is already floating the CAMP signal and does not execute Power On Sequence.
5. At this point, BIOS sees the CAMP signal pulled High and moves to the next operation.
6. By the above process, the faulty PMIC is mapped out of the memory system in a secure state and it does not interfere with platform operation. Good PMICs allow the server system to power up normally and operate in a secure state.

4 Registers Space

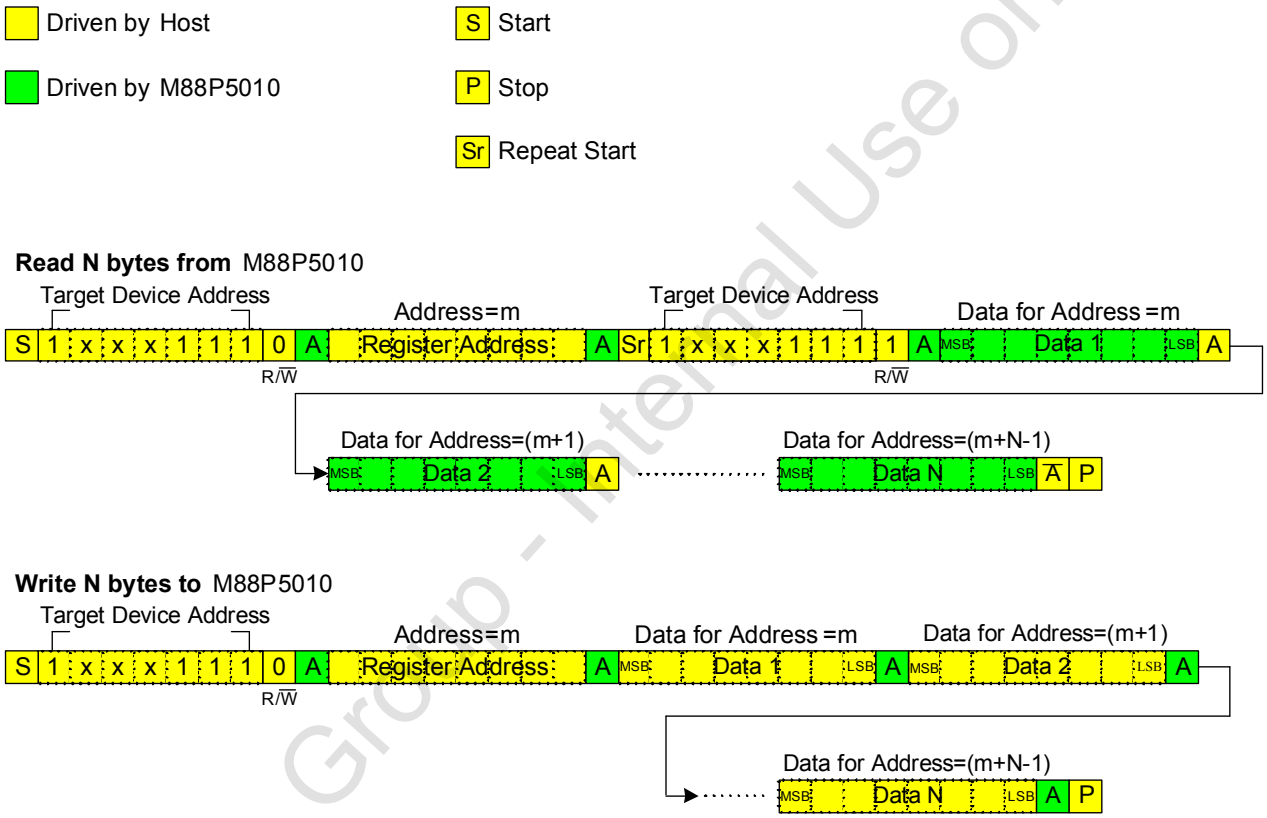
This chapter describes all configuration and status registers in detail.

4.1 Register Read/Write Mechanism

4.1.1 I²C Interface

The DDR5 PMIC address is 7'bxxxxyyy, where xxxx = 1000 or 1001 or 1100 depending on the PMIC ID (LID), yyy is a 3-bit code set by R34[3:1] (HID). The Write or Read bit stream (N ≥ 1) is shown in Figure 19:

Figure 19. I²C Interface Write/Read Bit Stream



4.1.2 PMIC Address ID (PID)

The PMIC has a PID input pin which allows to assign up to three different unique IDs for I²C/I3C Basic interface. The PID input pin is shared with the SWD_FB_N pin.

At the first power on, when the VLDO_1.8V output is ready, the PMIC automatically senses its ID. The PMIC also checks the configuration register R4F[1].

If the SWD output regulator is enabled and intended to operate in a single-ended remote sensing mode, the PMIC offers three different IDs as shown in Table 12. If the SWD output regulator is not enabled, the PMIC still offers three different IDs.

If SWD output regulator is enabled and intended to operate in a differential remote sensing mode like DDR5 RDIMM or DDR5 LRDIMM, there is only one default ID for the PMIC as shown in Table 12. This means, there is only one PMIC on the DIMM I²C/I3C Basic bus.

Table 12. Default ID for I²C/I3C Basic Interface.

R4F[1]	PID Pin Connection on DIMM Board	PMIC 4-bit Local Device Type ID (LID)	Host ID (HID)
'0'	Tied to GND	LID = 1001	Default = 111
	Tied to VLDO_1.8V	LID = 1100	Default = 111
	Floating	LID = 1000	Default = 111
'1'	Connect to Differential Sensing GND	LID = 1001	Default = 111

The selected LID code either '1001' or '1100' or '1000' is merged with a 3-bit HID code R34[3:1] to establish a 7-bit address code for the device. For example, with the default setting in R34[3:1] = '111', if the PID pin is connected to GND, the device address shall be '1001 111'.

4.1.3 I²C and I3C Basic Interface Operation

At Power On, by default, the PMIC device comes up in the legacy I²C mode of operation. There is no pull-up resistor inside PMIC on I²C bus.

The following applies to I²C mode:

1. The max operation speed is limited to 1MHz
2. In-band Interrupt is not supported
3. Bus reset is supported.
4. Parity Check is not supported except for supported CCCs.
5. Packet Error Check is not supported.

The PMIC device shall operate in the legacy I²C mode until it is put into I3C Basic mode via command.

Host may put the PMIC device in I3C Basic mode by issuing SETAASA CCC.

The following applies to I3C Basic mode:

1. The operation speed is up to 12.5MHz
2. In-band Interrupt is supported
3. Bus reset is supported.
4. Parity Check is always enabled by default.
5. Packet Error Check is supported and is disabled by default.

4.1.4 Device Interface - Protocol

The 7-bit serial address of the PMIC device applies to both I²C mode and I3C Basic mode of operation identically.

Table 13. 7-bit Address of PMIC Device

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	X	0	X	1	1	1	R/W
PMIC Device Type ID (LID)				Host ID (HID)			Read/Write

4.1.4.1 Switch from I2C Mode to I3C Basic Mode

By default, when PMIC first powers on, it operates in the legacy I2C mode. The PMIC device shall operate in I2C mode until it is put into I3C Basic mode via command.

In I2C mode, Host is allowed to issue only 3 CCCs (DEVCTRL, SETHID, SETAASA). All other CCCs are not supported and the PMIC device may simply ignore them. Host must issue DEVCTRL & SETHID CCC first (if required) followed by SETAASA CCC.

Host puts the PMIC device in I3C Basic mode by issuing SETAASA CCC.

When SETAASA CCC is registered by the PMIC device, it updates the R32[6] to '1'.

When SETHID CCC is registered by the PMIC device, it updates the R34[3:1].

4.1.4.2 Switch from I3C Basic Mode to I2C Mode

Host can put the PMIC device back to I2C mode from I3C Basic mode at any time by issuing RSTDAA CCC. When RSTDAA CCC is registered by the PMIC device, it updates the R32[6] to '0'.

4.1.4.3 I2C Target Protocol

The PMIC device operates on a standard I2C serial interface. Transactions where the PMIC device is the targeted target device begin with Host issuing a START condition followed by a 7-bit PMIC device address then a Read or Write bit, RW. All data are transmitted with the most-significant bit MSB first. During the address followed by R/W bit transmission, the PMIC device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK.

The PMIC device accepts 1 byte of address which covers 256 bytes of registers. The PMIC device register space does not require page selection process as all registers are within first 256 bytes.

4.1.4.3.1 Write Operation – Data Packet

Table 14. I2C - Write Command Data Packet

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr[1]	1	X	0	X	HID			W = 0	A	
	Address[7:0]								A	
	Data								A	
	---								A	
	Data								A	P

1. In I2C mode, Start or Repeat Start operation followed by 7'h7E with W = 0 is only allowed for the purpose of issuing CCCs that are allowed in I2C mode. Any other operation including another Repeat Start is considered an illegal operation.

4.1.4.3.2 Read Operation - Data Packet

Table 15. I²C - Read Command Data Packet

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr[1]	1	X	0	X	HID			W = 0	A	
	Address[7:0]								A	
Sr[1]	1	X	0	X	HID			R = 1	A[2]	
	Data								A	
	---								A	
	Data								N[3]	P

1. In I²C mode, Start or Repeat Start operation followed by 7'h7E with W = 0 is only allowed for the purpose of issuing CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered an illegal operation.
2. If the target device NACKs during Repeat Start for any reason, Host may retry Repeat Start again. Host can do Repeat Start as many times as it may desire. The PMIC may eventually ACK.
3. When the PMIC device reaches the last byte within the region (either Host region or DIMM vendor region), it will continue to return data but the returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches R255, it will reset to address R00 and continue to return the data. Only Host can perform STOP operation.

4.1.4.3.3 Default Read Address Pointer Mode

During normal operation of the DDR5 DIMM, Host periodically may poll critical information from the same location. An example may be the PMIC device's status registers or current or power measurement register Readout. To help improve the efficiency of the I²C bus protocol, the PMIC offers a default Read address pointer mode so that whenever the PMIC device sees the STOP operation on its SCL and SDA bus, its Read address pointer is always resets to the default address. The default Read pointer address mode is enabled through Register R3A[6] and the default starting address for Read operation is selectable through Register R3A[5:4]. This allows Host to read the Read command data packet as shown in Table 16. The default Read address pointer reduces the packet overhead by 2 bytes. Host typically enables this mode at last after VR Enable command when the normal operation of the DDR5 DIMM begins.

Table 16. I²C - Read Command Data Packet w/ Default Address Pointer Mode

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr	1	X	0	X	HID			R=1	A	
	Data								A	
	---								A	
	Data								N[1]	P

1. When PMIC device reaches last byte within the region (either Host region or DIMM vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches R255, it will reset to address R00 and it will continue to return the data. Only Host can perform STOP operation.

4.1.4.4 I3C Basic Target Protocol

The PMIC device operates on a standard I3C Basic serial interface. Transactions where the PMIC device is the targeted target device begin with Host issuing a START condition followed by a 7-bit PMIC device address then a Read or Write

bit, RW. All data are transmitted with the most-significant bit MSB first. During the address followed by R/W bit transmission, the PMIC device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See Table 17. The “T” bit carries Parity information from Host for each byte.

The Packet Error Code (PEC) function is disabled by default when the PMIC device is put in I3C Basic mode. Host may optionally enable this function through R34[7] or DEVCTRL CCC. If enabled, PEC is appended at the end of all transactions. If PEC is enabled, Host must complete the burst length as indicated in CMD field. In other words, Host must not interrupt the burst length pre-maturely for Write operation.

4.1.4.4.1 Write Operation - Data Packet

Table 17. I3C Basic - Write Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W = 0	A[1,2,3]	
	Address[7:0]								T	
	Data								T	
	---								T	
	Data								T	Sr[4] or P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
2. The PMIC device NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device Select code issued by Host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7’h7E.

Table 18. I3C Basic - Write Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1,2,3]	
	Address[7:0]								T	
	CMD			W=0	0000				T	
	Data								T	
	---								T	
	Data								T	
	PEC								T	Sr[4] or P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
2. The PMIC device NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device Select code issued by Host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7’h7E.

The host may optionally allow PMIC device to request IBI. For this case, the transactions to the PMIC device begin with the I3C host issuing a START condition followed by 7'h7E and then the Write bit. If PMIC device has a pending IBI, it transmits its 7-bit device Select code followed by R = 1. If the PMIC device has no pending IBI, there is no action taken by PMIC. Table 19 & Table 20 show the I3C Basic bus Write command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in Table 20, PEC calculation does not include IBI header byte (7'h7E followed by W = 0).

Table 19. I3C Basic - Write Command Data Packet w/ IBI Header; No Pending IBI, PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,2]	
Sr	1	X	0	X	HID			W=0	A[2,3,4]	
	Address[7:0]								T	
	Data								T	
	---								T	
	Data								T	Sr[5] or P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. See Figure 22 to see how the transition occurs from Host Push Pull Operation (W=0) to Target Open Drain (ACK) and See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
4. The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device Select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
5. Repeat Start or Repeat Start with 7'h7E.

Table 20. I3C Basic - Write Command Data Packet w/ IBI Header; No Pending IBI, PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,2]	
Sr	1	X	0	X	HID			W=0	A[2,3,4]	
	Address[7:0]								T	
	CMD			W=0	0000				T	
	Data								T	
	---								T	
	Data								T	
	PEC								T	Sr[5] or P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. See Figure 22 to see how the transition occurs from Host Push Pull Operation (W=0) to Target Open Drain (ACK) and See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).

4. The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device Select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
5. Repeat Start or Repeat Start with 7'h7E.

4.1.4.4.2 Read Operation - Data Packet

The PMIC device operates on a standard I3C Basic serial interface. Transactions where the PMIC device is the targeted target device begin with the host issuing a START condition followed by a 7-bit PMIC device address then a Read or Write bit, RW. All data are transmitted with the most-significant bit MSB first. During the address followed by R/W bit transmission, the PMIC device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See Table 21. The "T" bit carries Parity information from the host for each byte prior to Repeat START. After Repeat START, the "T" bit carries information from the PMIC device to the host indicating Continuous ('1') or Stop ('0') whether it is transmitting the last byte or not.

The Packet Error Code (PEC) function is disabled by default when the PMIC device is put in I3C Basic mode. The host may optionally enable this function through R34[7] or DEVCTRL CCC. If enabled, PEC is appended as shown in Table 21. If PEC is enabled, the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length pre-maturely for Read operation.

Table 21. I3C Basic - Read Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W = 0	A[1,2,3]	
	Address[7:0]								T	
Sr	1	X	0	X	HID			R = 1	A/N[4]	
	Data								T = 1	
	---								T = 1	
	Data								T = 1[5,6]	Sr[7] or P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
2. The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device Select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
4. If the target device NACKs during Repeat Start for any reason, The host may retry Repeat Start again. The host can do the Repeat Start as many times as it may desire. If the target device NACKs due to the parity error in previous bytes, it will always NACK regardless of how many times the host tries Repeat Start. If there are no parity errors, PMIC may eventually ACK.
5. See Figure 23 to see how the host ends target device operation.
6. When the PMIC device reaches the last byte within the region (either Host region or DIMM vendor region), it will continue to return data, but the returned data will be 0x00 if there is no valid password for the DIMM vendor region or Vendor specific region. Once the address counter reaches R255, it will reset to address R00 and it will continue to return the data. Only the host can perform STOP operation.
7. Repeat Start or Repeat Start with 7'h7E.

Table 22. I3C Basic - Read Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1,2,3]	
	Address[7:0]								T	
	CMD			R=1	0000				T	
	PEC								T	
Sr	1	X	0	X	HID			R=1	A/N[4]	
	Data								T=1	
	---								T=1	
	Data								T=1	
	PEC								T=0[5]	Sr[6] or P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
2. The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device Select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
4. If the target device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do the Repeat Start as many times as it may desire. If the target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the host tries Repeat Start. If there are no parity or PEC errors, PMIC may eventually ACK. The PEC calculation by the target device only includes the device Select code of ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operations, the target device includes the device Select of only the last Repeat Start from the host when it ACKs in PEC calculation and all other NACK responses of the device Select code of Repeat Start are not included in PEC calculation.
5. See Figure 24 to see how the target device ends the operation followed by the host STOP operation.
6. Repeat Start or Repeat Start with 7'h7E.

The host may optionally allow the PMIC device to request IBI. For this case, the transactions to the PMIC device begin with I3C Basic the host issuing a START condition followed by 7'h7E and then the Write bit. If the PMIC device has a pending IBI, it transmits its 7-bit device Select code followed by R = 1. If the PMIC device has no pending IBI, there is no action taken by PMIC. Table 23 & Table 24 show the I3C Basic bus Read command data packet with an optional IBI header for PEC disabled and PEC enabled case respectively. Note that in Table 24 PEC calculation does not include IBI header byte (7'h7E followed by W = 0).

Table 23. I3C Basic - Read Command Data Packet w/ IBI Header; No Pending IBI, PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,2]	
Sr	1	X	0	X	HID			W=0	A[2,3,4]	
	Address[7:0]								T	
Sr	1	X	0	X	HID			R=1	A/N[5]	
	Data								T=1	
	...								T=1	
	Data								T=1[6,7]	Sr[8] or P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
2. The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. See Figure 22 to know how the transition occurs from Host Push Pull Operation (W=0) to Target Open Drain (ACK) and See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
4. The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device Select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
5. If the target device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do Repeat Start as many times as it may desire. If the target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the host tries Repeat Start.
6. See Figure 23 to know how the host ends the target device operation.
7. When the PMIC device reaches the last byte within the region (either the Host region or DIMM vendor region), it will continue to return data, but the returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches R255, it will reset to address R00 and continue to return the data. Only the host can perform STOP operation.
8. Repeat Start or Repeat Start with 7'h7E.

Table 24. I3C Basic - Read Command Data Packet w/IBI Header; No Pending IBI, PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,2]	
Sr	1	X	0	X	HID			W=0	A[2,3,4]	
	Address[7:0]								T	
	CMD			R=1	0000				T	
	PEC								T	
Sr	1	X	0	X	HID			R=1	A/N[5]	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0[6]	Sr[7] or P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
2. The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. See Figure 22 to know how the transition occurs from Host Push Pull Operation (W=0) to Target Open Drain (ACK) and See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
4. The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device Select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.
5. If the target device NACKs during Repeat Start for any reason, the host may retry Repeat Start again. The host can do Repeat Start as many times as it may desire. If the target device NACKs due to PEC error or parity error in previous bytes, it will always NACK regardless of how many times the host tries Repeat Start. If there are no parity or PEC errors, PMIC may eventually ACK. PEC calculation by the target device only includes the device Select code of the ACK response of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the target device includes the device Select of only the last Repeat Start from the host when it ACKs in PEC calculation and all other NACK responses of the device Select code of Repeat Start are not included in PEC calculation.
6. See Figure 24 to know how the target device ends the operation followed by the host STOP operation.
7. Repeat Start or Repeat Start with 7'h7E.

4.1.4.4.3 Default Read Address Pointer Mode

Table 25 & Table 26 show the Read command data packet for the PEC function disabled and enabled respectively. When the PEC function is enabled, R3A[3:2] sets the number of bytes that the PMIC device sends out followed by the PEC calculation. If PEC is enabled, the host must complete the burst length as indicated in R3A[3:2] register. In other words, the host must not interrupt the burst length pre-maturely for default address pointer Read operation.

Table 25. I3C Basic - Read Command Data Packet w/ Read Address Pointer Mode; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			R=1	A[1]	
	Data								T=1	
	...								T=1	
	Data								T=1[2,3]	Sr[4] or P

1. The PMIC device NACKs if there is a parity error in a previous transaction when the host performs consecutive transactions with Repeat Start.
2. See Figure 23 to know how the host ends the target device operation.
3. When the PMIC device reaches the last byte within the region (either Host region or DIMM vendor region), it will continue to return data, but the returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches R255, it will reset to address R00 and continue to return the data. Only the host can perform STOP operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 26. I3C Basic - Read Command Data Packet w/ Read Address Pointer Mode; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			R=1	A[1]	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0[2]	Sr[3] or P

1. The PMIC device NACKs if there is a parity or PEC error in a previous transaction when the host performs consecutive transactions with Repeat Start.
2. See Figure 24 to know how the target device ends the operation followed by STOP operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 27. I3C Basic - Read Command Data Packet w/ Read Address Pointer & IBI Header; No Pending IBI; PEC Disabled (Sheet 1 of 2)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,2]	
Sr	1	X	0	X	HID			R=1	A/N[2]	

Table 27. I3C Basic - Read Command Data Packet w/ Read Address Pointer & IBI Header; No Pending IBI; PEC Disabled (Sheet 2 of 2)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
	Data								T=1	
	...								T=1	
	Data								T=1[3,4]	Sr[5] or P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. The PMIC device NACKs if there is a parity error in a previous transaction when the host performs consecutive transactions with Repeat Start.
3. See Figure 23 to know how the host ends the target device operation.
4. When the PMIC device reaches the last byte within the region (either the Host region or DIMM vendor region), it will continue to return data, but the returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches R255, it will reset to address R00 and continue to return the data. Only the host can perform STOP operation.
5. Repeat Start or Repeat Start with 7'h7E.

Table 28. I3C Basic - Read Command Data Packet w/ Read Address Pointer & IBI Header; No Pending IBI; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,2]	
Sr	1	X	0	X	HID			R=1	A/N[2]	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0[3,4]	Sr[4]or P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
2. The PMIC device NACKs if there is a parity or PEC error in a previous transaction when the host performs consecutive transactions with Repeat Start.
3. See Figure 24 to know how the target device ends the operation followed by STOP operation.
4. Repeat Start or Repeat Start with 7'h7E.

Figure 20. Target Open Drain to Controller Push Pull Hand Off Operation

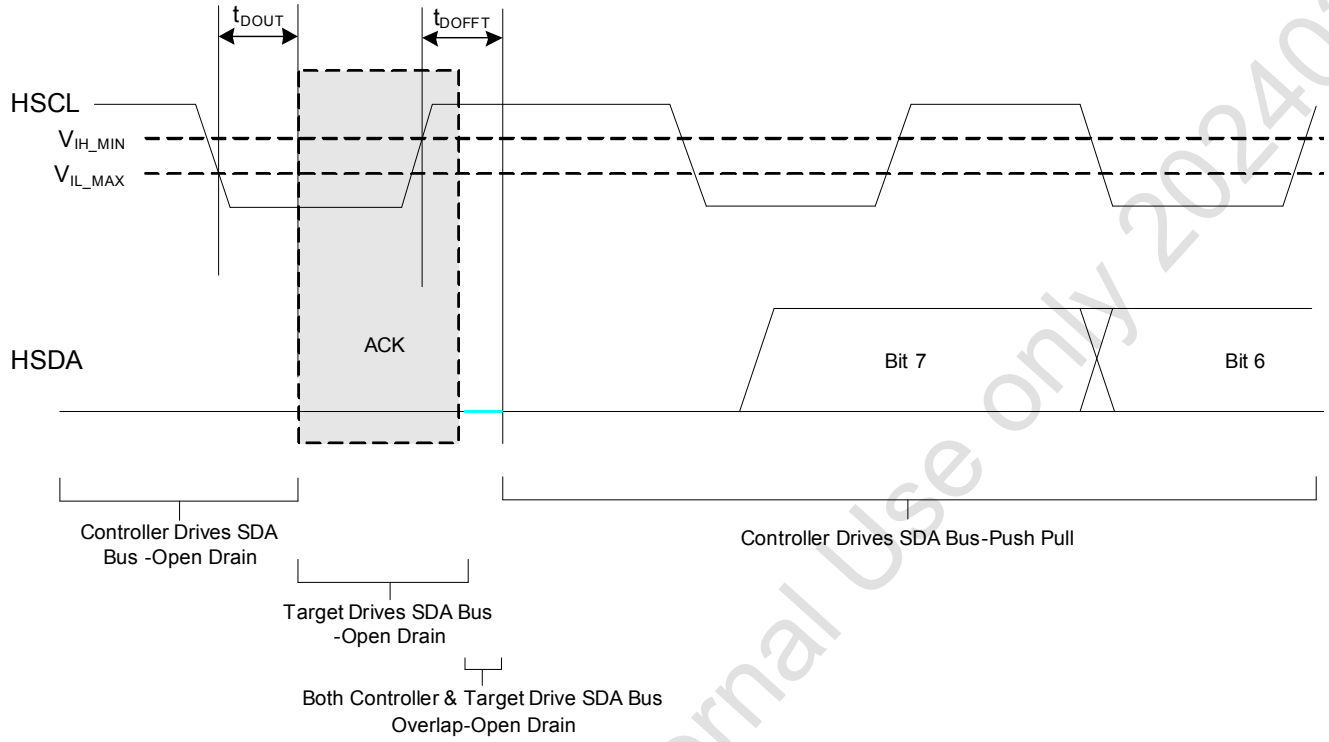


Figure 21. Contorller Open Drain (ACK) to Target Push Pull Hand Off Operation

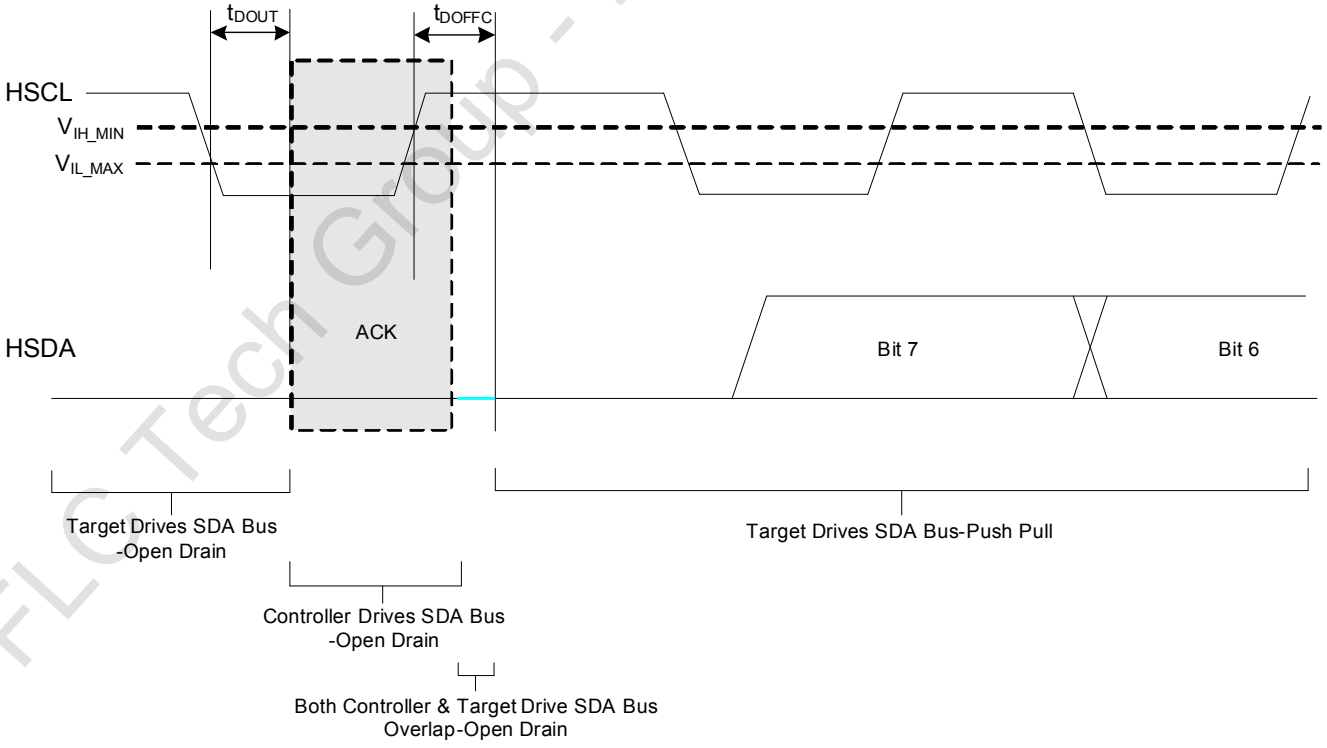


Figure 22. Controller Push Pull to Target Open Drain Hand Off Operation

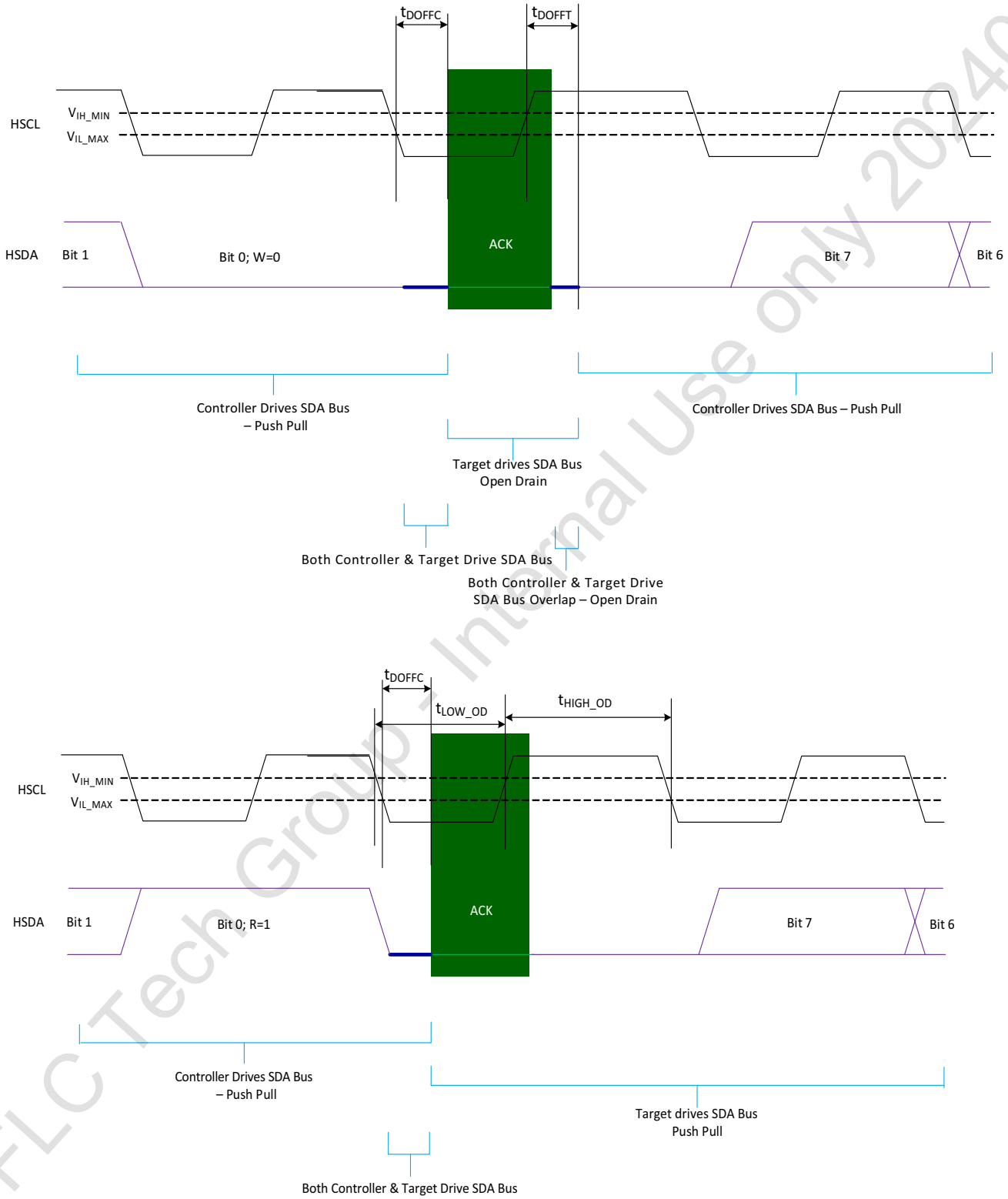


Figure 23. T = 1; Controller Ends Read with Repeated START and STOP Waveform

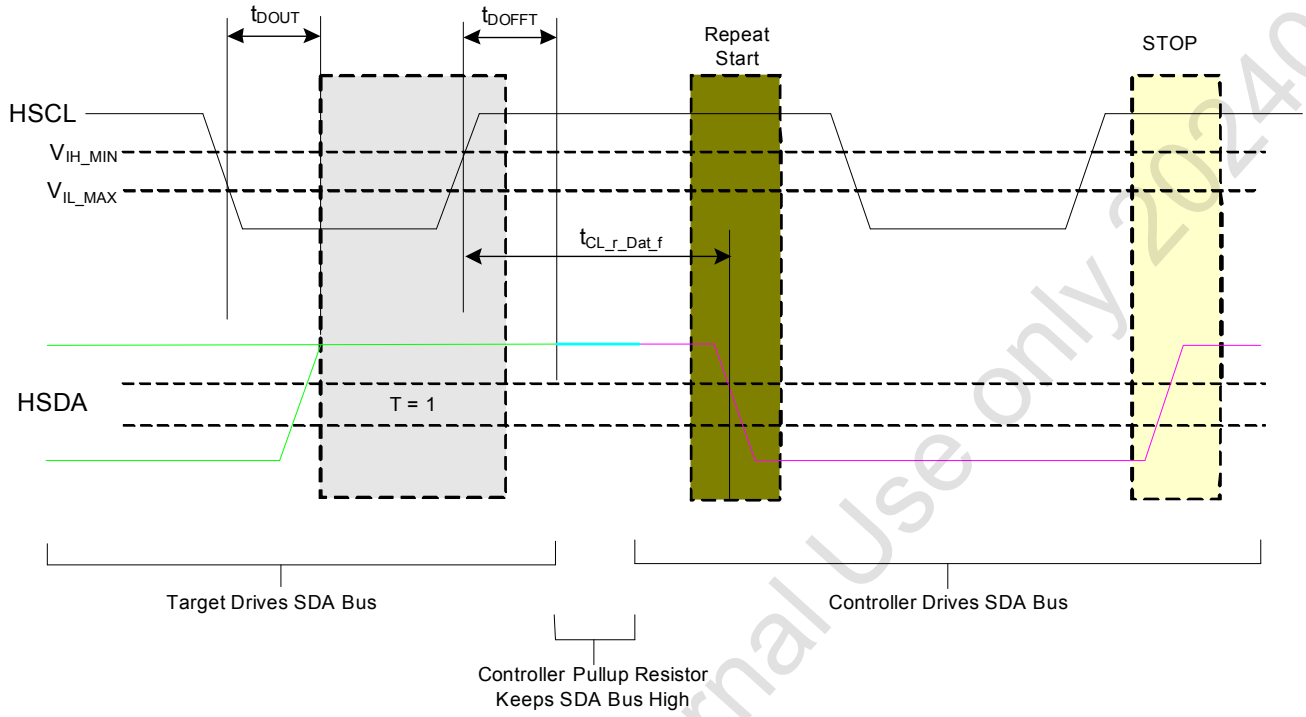
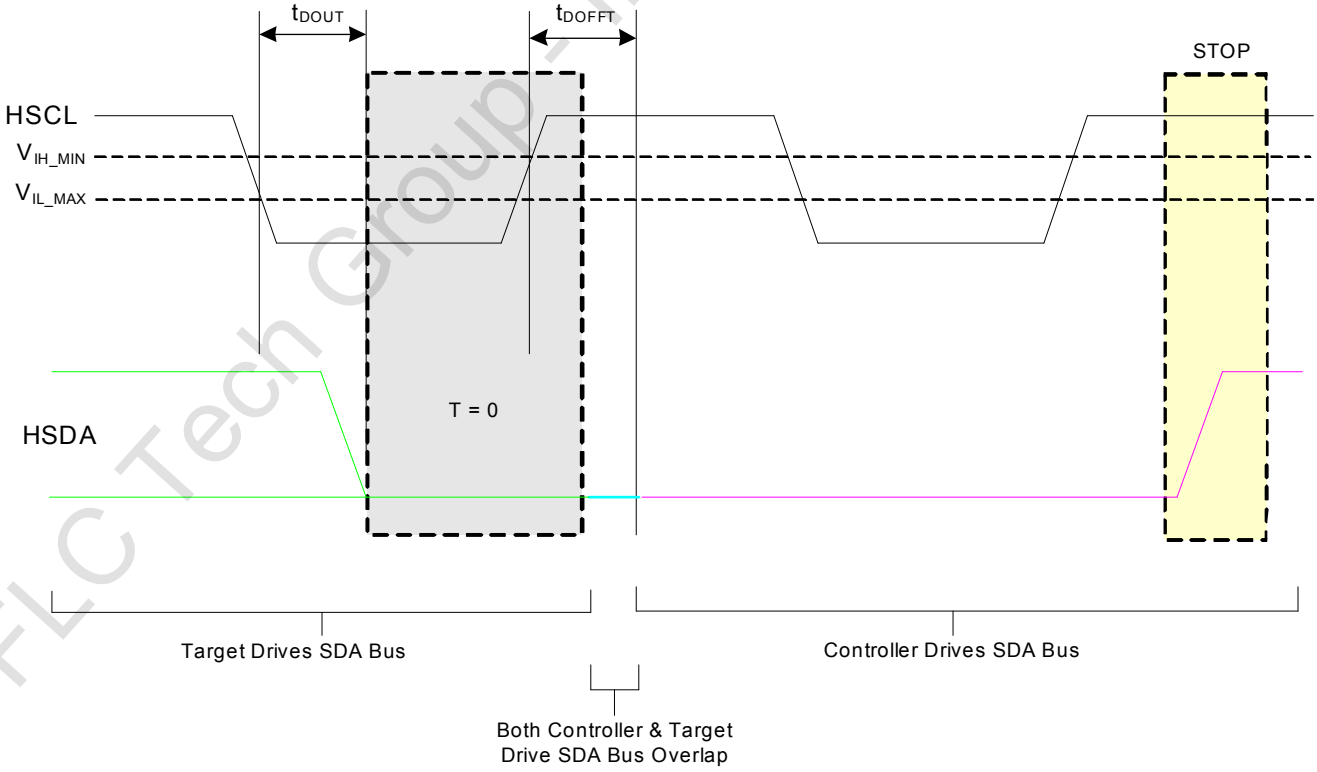


Figure 24. T = 0; Target Ends Read; Controller Generates STOP



4.1.4.5 In-Band Interrupt (IBI)

In I²C mode, the in-band interrupt function is not supported. Only I3C Basic mode supports the in-band interrupt function.

4.1.4.5.1 Enabling & Disabling In-Band Interrupt Function

By default, the IBI function is disabled. The PMIC device enables IBI when it registers ENEC CCC. Once IBI is enabled, the PMIC device sends an IBI when an event occurs.

- When R34[6] = '1', the device sends an IBI at the next available opportunity when any of the register bits in R08[7:0], R09[7:0], R0A[7:2], R0B[7:0] and R33[4:2] is set to '1'. The device also sets R0A[1] to '1' and updates Pending Interrupt Bits[3:0] = '0001' for GETSTATUS CCC.
- When R34[6] = '0', the device does not send the IBI regardless of the register bits in R08[7:0], R09[7:0], R0A[7:2], R0B[7:0] and R33[4:2]. However, the device sets R0A[1] to '1' and updates Pending Interrupt Bits[3:0] = '0001' for GETSTATUS CCC.

4.1.4.5.2 Mechanics of Interrupt Generation

Event interrupts may be generated by the local device if IBI is enabled. If there is a pending interrupt (i.e R0A[1] = '1') and IBI is enabled (i.e. R34[6] = '1'), the PMIC device requests an interrupt after detecting START condition by transmitting its 7-bit binary address (LID bits followed by HID bits) followed by R/W = '1' on the SDA bus serially (synchronized by SCL falling transitions).

If no START condition is detected by the PMIC device, but the I3C Basic bus (SDA and SCL) has been inactive (no edges seen) for t_{AVAL} period, then the PMIC device may assert SDA low to request an interrupt. When the PMIC device requests an interrupt, the host toggles SCL. The PMIC device transmits its 7-bit binary address (LID bits followed by HID bits) followed by R/W bit = '1' to the host.

When the PMIC device requests an interrupt, the host may take one of the two actions below:

1. The host sends ACK on the 9th bit to accept the interrupt request. At this point, if it confirms that it has won the arbitration, the PMIC device transmits the IBI payload as shown in Table 29 and Table 30 for PEC disabled and PEC enabled configuration respectively. Figure 25 shows only the first two data bits of the MDB byte to illustrate the timing. The interrupt payload contains MDB followed by R08", R09", R0A", R0B" & R33" bytes. Host then issues a STOP command. Note the timing waveform in Figure 25. Host then accepts the IBI payload if it sends an ACK on the 9th bit to accept the interrupt request. Host can interrupt the IBI payload at T bit. If Host stops the IBI payload at T bit in the middle of the payload, the PMIC retains the IBI status flag (R0A[1]) and Pending Interrupt Bits[3:0] internally and waits for the next opportunity to request an interrupt. If the PMIC device successfully transmits the entire IBI payload, it then clears the IBI status flag (R0A[1] = '0') and Pending Interrupt Bits[3:0] = '0000' on its own and does not request for an IBI again unless there is another different event occurs; for another same event, the device does not request for an IBI.
2. Host sends NACK on the 9th bit as shown in Figure 26 followed by a STOP command. In this case, the PMIC device does not transmit the IBI payload, but waits for the next opportunity to request an interrupt. At this point, though Host sents an NACK, it has a knowledge of which PMIC device sent the IBI request. The PMIC device retains the IBI status flag (R0A[1] = '1') and Pending Interrupt Bits[3:0]=0001'.

Table 29. Target Device IBI Payload Packet; PEC is Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/T	Stop
S	1	X	0	X	HID			R=1	A[1]	
	MDB=0x00								T=1	
	R08[7:0]								T=1	
	R09[7:0]								T=1	
	R0A[7:0]								T=1	
	R0B[7:0]								T=1	
	R33[7:0]								T=0[2]	P

1. See Figure 21 to see how the transition occurs from Host Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB Byte bit[7]).
2. See Figure 24 to see how the target device ends the operation followed by Host STOP operation.

Table 30. Target Device IBI Payload Packet; PEC is Enable

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/T	Stop
S	1	X	0	X	HID			R=1	A[1]	
	MDB=0x00								T=1	
	R08[7:0]								T=1	
	R09[7:0]								T=1	
	R0A[7:0]								T=1	
	R0B[7:0]								T=1	
	R33[7:0]								T=1	
	PEC								T=0[2]	P

1. See Figure 21 to see how the transition occurs from Host Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB Byte bit[7]).
2. See Figure 24 to see how the target device ends the operation followed by Host STOP operation.

Figure 25. PMIC Requests Interrupt; Host ACK Followed by PMIC Device IBI Payload

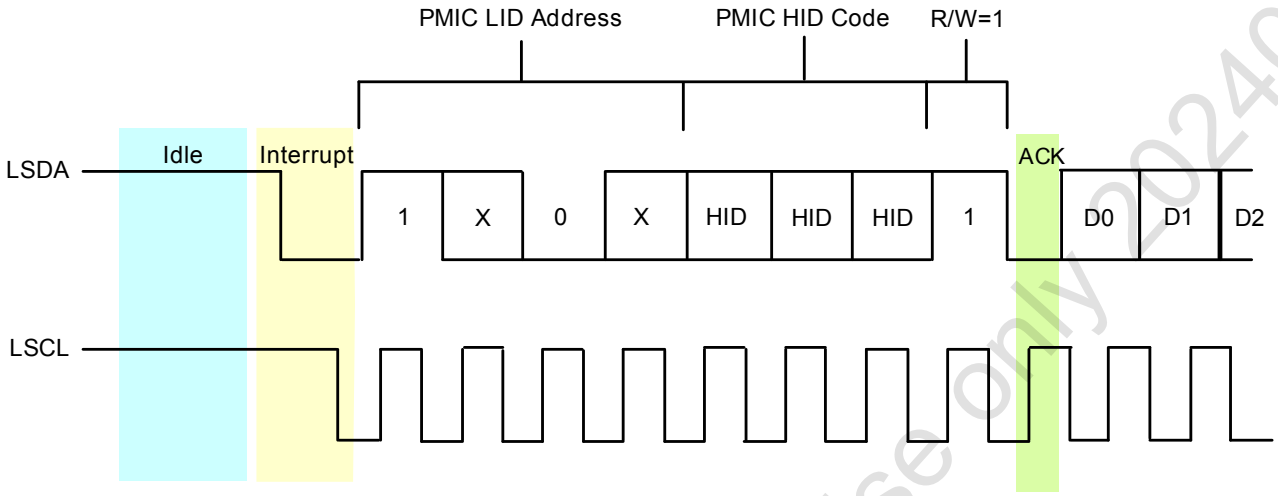
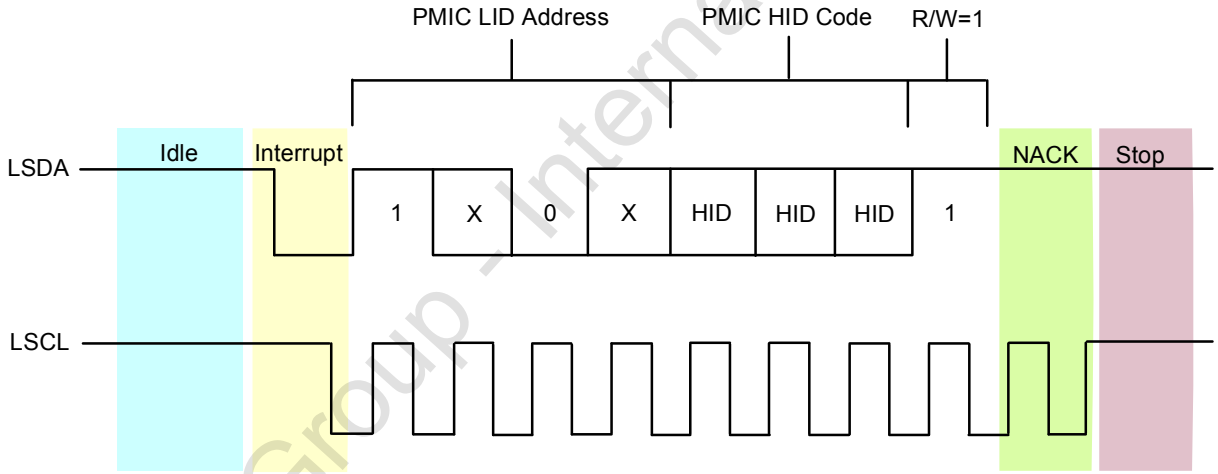


Figure 26. PMIC Requests Interrupt; Host NACK Followed by STOP



4.1.4.5.3 Interrupt Arbitration

As there are multiple devices on an I3C Basic bus, multiple devices may request an interrupt when the Host I3C Basic bus is inactive for t_{AVAL} period. At this time, the arbitration process is required.

For DDR5 DIMM application environment, there could be up to total of 13 different devices including PMIC on an I3C Basic bus.

In a typical DDR5 DIMM application environment, all devices have the same 3-bit HID code. Hence the 4-bit LID code always wins the arbitration. For example, if one target device has a LID code of '0010' and other device (PMIC) has a LID code of '1001', through the arbitration process, the target device LID code of '0010' wins. The PMIC device with a LID code of '1001' must release the bus and wait for the next opportunity to request an interrupt. Table 31 shows the arbitration priority based on the LID code for all devices. The cells in grey color in Table 31 are the likely devices that will be on a standard DDR5 RDIMM or DDR5 LRDIMM.

Table 31. Interrupt Arbitration - Among All Devices

Device	LID Code	HID Code = '111'	Arbitration Priority
N/A	0000	N/A	N/A
RFU	0001	111	1
TS0	0010	111	2
RFU	0011	111	3
RFU	0100	111	4
RFU	0101	111	5
TS1	0110	111	6
RFU	0111	111	7
PMIC1	1000	111	8
PMIC0	1001	111	9
SPD Hub	1010	N/A	N/A
RCD	1011	111	10
PMIC2	1100	111	11
RFU	1101	111	12
RFU	1110	111	13
N/A	1111	N/A	N/A

In an uncommon but possible scenario, would be that, at exact time when Hub or local target devices (i.e PMIC) are requesting an interrupt, Host starts an operation to Hub or local target devices (i.e PMIC). When this happens, Host also is involved in the arbitration process along with Hub or local target devices (PMIC). During the arbitration phase, there is always only one winning device which could be either Hub, the local target device (i.e PMIC) or Host.

If Host wins during the arbitration phase, it continues with normal operation. The losing Hub or local target device (i.e PMIC) waits for the next opportunity to send an interrupt.

If Host looses during the arbitration phase, it must give up the bus. When Host looses during the arbitration, Host must let Hub or the local target device (i.e PMIC) finish sending their 4-bit LID code followed by 3-bit HID code followed by R/W = '1'. At this point, during the 9th bit, Host has two options to take the action as noted below:

- Host sends an ACK to accept the interrupt and hence accepts the IBI payload from the winning Hub or local target device (i.e PMIC). After the IBI payload, Host issues the STOP operation.
- Host sends an NACK followed by STOP operation.

In a rare but still possible scenario, would be that, at exact time when PMIC is requesting an interrupt, Host starts an operation to the same PMIC. When this happens, neither Host nor PMIC knows it is a winner until the 8th bit and Host always wins. This is because, PMIC sends R=1 (the 8th bit) during the interrupt. Host sets W=0 (the 8th bit) during the operation. As a result, Host wins and PMIC must give up the bus and wait for the next opportunity to send an interrupt.

In an extreme rare but still possible scenario, would be that, at exact time when the PMIC device is requesting an interrupt, Host requests a Read operation with the default Read address pointer mode to the PMIC device. When

this happens, there is no winning device. This is the only time there is no winning device. This is because the PMIC device sends R=1 (the 8th bit) during the interrupt and Host also sends R=1 for Read request with the default Read address pointer mode. As a result, there is no winner because Host is waiting for PMIC to ACK and PMIC is waiting for Host to ACK. In this case, neither Host nor PMIC ACKs. Since there is no ACK (i.e NACK) by either device, Host must time out and repeat the Read request with Repeat Start. When Host repeats the Read request with Repeat Start, the PMIC does not send an interrupt because of Repeat Start.

4.1.4.5.4 Clearing Device Status and IBI Status Registers

The PMIC device provides the IBI status in R0A[1] by setting it to '1'. The PMIC device clears the IBI status register R0A[1] to '0' automatically when it sends a complete IBI (including payload and no interruption) and also clears Pending Interrupt Bits[3:0] to '0000'. Once the IBI status register is cleared, the PMIC does not request for an IBI again unless an another event occurs.

The PMIC device provides the device status in R08[7:0], R09[7:0], R0A[7:2], R0B[7:0] and R33[4:2] registers. The status information in R08[7:0], R09[7:0], R0A[7:2], R0B[7:0] and R33[4:2] registers are latched and remains set even after the PMIC device sends IBI payload and clears the IBI status register R0A[1] to '0'. Host must explicitly clear the status register through Clear command by writing '1' for appropriate status or by issuing a Global clear command.

After Host issues a clear command, if the condition is no longer present, the PMIC device clears the appropriate status register, clears the IBI status register to '0' and Pending Interrupt Bits[3:0] to '0000' even if the PMIC device has not sent IBI. After Host issues the clear command, if the condition is still present, the device again sets the appropriate status register, sets the IBI status register to '1' and Pending Interrupt Bits[3:0] to '0001' even if the device has already sent IBI and entire IBI payload.

4.1.4.6 Packet Error Check (PEC) Function

In I^2C mode, Packet Error Check is not supported. Only I3C Basic mode supports the Packet Error Check function.

The PMIC device implements an 8-bit Packet Error Code which is appended at the end of all transactions if PEC is enabled through DEVCTRL CCC or by directly writing '1' to R34[7]. PEC is a CRC-8 value calculated on all the messages bytes except for START, STOP, REPEATED START conditions or T-bits, ACK, NACK and IBI header (7'h7E followed W=0) bits.

The polynomial for CRC-8 calculations is: $C(X) = X^8 + X^2 + X^1 + 1$

The seed value for the PEC function is all zero.

When Host calculates PEC for the PMIC device, it includes LID and HID bits followed by R/W bit.

4.1.4.7 Parity Error Check Function

In I^2C mode, Parity Error Checking is not supported except for supported CCCs. Only I3C Basic mode supports the Parity Error Checking function.

By default, when the PMIC device is put in I3C Basic mode, the Parity Error Check function is automatically enabled. Host can also disable the function with DEVCTRL CCC or by directly writing '1' to R34[5]. When the parity function is disabled, the PMIC device simply ignores the "T" bit information from Host. Host may actually choose to compute the parity and send that information during the "T" bit or simply drive static Low or High in "T" bit.

The PMIC device implements ODD parity. If the odd number bits in the byte are '1', the parity bit value is '0'. If the even number bits in the byte are '1', the parity bit value is '1'. Host computes the parity and sends during "T" bit.

4.1.4.8 Packet Error Check & Parity Error Handling

There are two types of error checking done by the PMIC device: Parity Error Check And Packet Error Check. By default, Parity Error Check is always enabled and Packet Error Check is disabled. Host may enable Packet Error Check at any time. The parity error is checked for each byte in a packet except for the device Select code byte from Host. Host sends parity error information in “T” bit.

I3C Basic mode defines TE0, TE1, TE2, TE3, TE4, TE5 and TE6 error detection for Target devices. Only TE1 and TE2 error detection are supported by PMIC for parity checking. All other errors are not supported and not applicable.

4.1.4.8.1 Write Command Data Packet Error Handling - PEC Disabled

The PMIC device checks for the parity error for each byte in a packet that it receives from Host except for the device Select code byte that it receives from Host as shown in Table 32.

Table 32. Write Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1,2,3]	
	Address[7:0]								T	
	Data								T	
	---								T	
	Data								T	Sr[4] or P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
2. The PMIC device NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device Select code issued by Host does not match with its own device code. The PMIC device ignores the entire packet until STOP or the next Repeat Start operation.
4. Repeat Start or Repeat Start with 7’h7E.

Write command - if there is no parity error:

- The PMIC device executes the command.

Write command - if there are parity error:

- The PMIC device discards the byte in the packet that has a parity error.
- The PMIC device discards all subsequent bytes in the packet until the STOP operation. The PMIC device may or may not check parity for all subsequent bytes in the packet.
- Note that as the packet contains more than one byte, if the first byte has no parity error but the second byte has a parity error, the PMIC device may or may not execute the first byte operation, but the second byte and all subsequent bytes operations are discarded.
- The PMIC device sets the R0A[2:1] to ‘11’ and P_Err in GETSTATUS CCC to ‘1’; updates Pending Interrupt Bits[3:0] in GETSTATUS CCC to ‘0001’; asserts the GSI_n pin if enabled; and waits for the next opportunity to send an in-band interrupt if IBI is enabled.

4.1.4.8.2 Read Command Data Packet Error Handling - PEC Disabled

The PMIC device checks for the parity error for each byte in a packet except for the device Select code byte that it receives from Host prior to Repeat Start as shown in Table 33.

The PMIC device does not compute the parity when it sends the data to Host. It does not check for the parity error for the bytes as shown in Table 33. The device sends Continuous (‘1’) or Stop (‘0’) information during “T” bit when the PMIC device is sending the Read data.

Table 33. Read Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1,2,3]	
	Address[7:0]								T	
Sr	1	X	0	X	HID			R=1	A/N[4]	
	Data								T=1	
	---								T=1	
	Data								T=1[5,6]	Sr[7] or P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
2. The PMIC device NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device Select code issued by Host does not match with its own device code. The PMIC device ignores the entire packet until STOP or the next Repeat Start operation.
4. If the target device NACKs during Repeat Start for any reason, Host may retry Repeat Start again. Host can do Repeat Start as many times as it may desire. If the target device NACKs due to the parity error in previous bytes, it will always NACK regardless of how many times Host tries Repeat Start. If there are no parity errors, PMIC may eventually ACK.
5. See Figure 23 to see how Host ends the target device operation.
6. When the PMIC device reaches the last byte within the region (either Host region or DIMM vendor region), it will continue to return data, but the returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches R255, it will reset to address R00 and continue to return the data. Only Host can perform STOP operation.
7. Repeat Start or Repeat Start with 7’h7E.

Read Command - If there is no parity error:

- The PMIC sends ACK back to Host when Host perform a Start Repeat operation.
- The PMIC device executes the command and sends the data as shown in Table 33.

Read Command - If there is parity error:

- The PMIC device discards the byte in the packet that has a parity error.
- The PMIC device sends NACK back to Host when Host performs a Start Repeat operation, as shown in the grey color cell in Table 33. NACK represents either a parity error in one of the two bytes or that PMIC is not able to start the Read operation. Host may retry Repeat Start again.

  Host may do Repeat Start as many times as it may desire. If the PMIC target device NACKs due to the parity error in a previous byte from Host, it will always NACK regardless of how many times Host tries Repeat Start.
- The PMIC does not send the data shown in Table 33, and instead expects Host to perform STOP operation.
- The PMIC device sets R0A[2:1] to ‘11’ and P_Err in GETSTATUS CCC to ‘1’; updates Pending Interrupt Bits[3:0] in GETSTATUS CCC to ‘0001’; asserts GSI_n pin if enabled; and waits for the next opportunity to send an in-band interrupt if IBI is enabled.

4.1.4.8.3 Write Command Data Packet Error Handling - PEC Enabled

The PMIC device checks for the parity error for each byte in a packet that it receives from Host except for the device select code byte that it receives from Host as shown in Table 34. Further, the PMIC device checks for the

packet error for the entire packet (from Start condition until the last byte of Data) that it receives from Host as shown in Table 34.

Table 34. Write Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1,2,3]	
	Address[7:0]								T	
	CMD			W=0	0	0	0	0	T	
	Data								T	
	---								T	
	Data								T	
	PEC								T	Sr[4] or P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
2. The PMIC device NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device Select code issued by Host does not match with its own device code. The PMIC device ignores the entire packet until STOP or the next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

Write command - If there is no parity error:

- The PMIC device waits for the entire packet. If there is no error in the packet, the PMIC device executes Write command.

  If there is an error in the packet, the PMIC device discards the entire packet and does not execute the packet, and waits for STOP; sets the R0A[3,1] to '11', PEC_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits[3:0] in GETSTATUS CCC to '0001'; asserts the GSI_n pin if enabled; and waits for the next opportunity to send an in-band interrupt if IBI is enabled.

Write command - if there is parity error:

- The PMIC device discards that byte and the entire packet until the STOP operation.
- The PMIC device sets the R0A[2:1] to '11' and P_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits[3:0] in GETSTATUS CCC to '0001'; asserts the GSI_n pin if enabled; and waits for the next opportunity to send an in-band interrupt if IBI is enabled.
- The PMIC device may or may not check error for the packet. If the PMIC device checks error for the packet, it likely detect an error in the packet and the device may also set R0A[3] & PEC_Err in GETSTATUS CCC as well.

4.1.4.8.4 Read Command Data Packet Error Handling - PEC Enabled

The PMIC device checks for the parity error for each byte in a packet except for the device Select code byte that it receives from Host prior to Repeat Start as shown in Table 35.

The PMIC device does not compute the parity when it sends the data to Host. The host does not check for the parity error for the bytes shown in Table 35. The device sends Continuous ('1') or Stop ('0') information during "T" bit when the PMIC device is sending the Read data.

The PMIC device checks for the PEC error in a packet that it receives from Host from Start condition to Repeat Start (from the first device Select code followed by the address offset and CMD byte).

The PMIC device computes the packet error code for the entire packet starting with Repeat Start (device Select code and the data that PMIC device transmits back to Host).

Table 35. Read Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1,2,3]	
	Address[7:0]								T	
	CMD			R=1	0	0	0	0	T	
	PEC								T	
Sr	1	X	0	X	HID			R=1	A/N[4]	
	Data								T=1	
	---								T=1	
	Data								T=1	
	PEC								T=0[5]	Sr[6] or P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr, bit[7]).
2. The PMIC device NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device Select code issued by Host does not match with its own device code. The PMIC device ignores the entire packet until STOP or the next Repeat Start operation.
4. If the target device NACKs during Repeat Start for any reason, Host may retry Repeat Start again. Host can do Repeat Start as many times as it may desire. If the target device NACKs due to the parity or PEC error in previous bytes, it will always NACK regardless of how many times Host tries Repeat Start. If there are no parity or PEC errors, PMIC may eventually ACK. The PEC calculation by the target device only includes the device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the target device includes device Select of only the last Repeat Start from Host when it ACKs in PEC calculation and all other NACK responses of the device Select code of Repeat Start are not included in the PEC calculation.
5. See Figure 24 to see how the target device ends the operation followed by the Host STOP operation.
6. Repeat Start or Repeat Start with 7'h7E.

Read command - If there is no parity error & no PEC error

- The PMIC device sends ACK back to Host when Host perform a Start Repeat operation.
- The PMIC device executes the Read command and sends the data as shown in Table 35.
- The PMIC computes PEC for the bytes (from Start condition to PEC byte prior to Repeat Start) shown in the cells in Table 35.

Read command - if there is parity error or PEC error

- The PMIC device discards the byte in the packet that had a parity error.
- The PMIC device discards second byte in that packet if a parity error occurred in first byte. The PMIC device may or may not check parity for the second byte in that packet.
- The PMIC device discards the packet if there is a PEC error.
- The PMIC sends NACK back to the host when Host perform Start Repeat operation. This is shown in the grey color cell in Table 35. NACK represents either PEC error or a parity error in one of the three bytes or that PMIC

is not able to start the Read operation. Host may retry Repeat Start again. Host may do Repeat Start as many times as it may desire. The PEC calculation by the PMIC device only includes the device Select code of the ACK responses of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the PMIC device includes the device Select of only the last Repeat Start from Host when it ACKs in the PEC calculation and other NACK responses of the device Select codes of Repeat Start are not included in the PEC calculation. If the PMIC target device NACKs due to PEC error or parity error in a previous bytes from Host, it will always NACK regardless of how many times Host tries Repeat Start.

- The PMIC device does not send any data shown in Table 35 and instead expects Host to perform STOP operation.
- The PMIC device sets R0A[3:2] accordingly and R0A[1] to '1', and P_Err, PEC_Err in GETSTATUS CCC to '1' accordingly; updates Pending Interrupt Bits[3:0] in GETSTATUS CCC to '0001'; asserts the GSI_n pin if enabled and waits for the next opportunity to send an in-band interrupt if IBI is enabled.

4.1.4.9 CCC Packet Error Handling

Parity error and PEC error detected in a CCC packet are handled the same way as described for normal Read/ Write operations.

4.1.4.10 Error Reporting

All error conditions detected by the PMIC devices are captured in R08[7:0], R09[7:0], R0A[7:1] R0B[7:0] and R33[4:2] registers.

There are four different possible ways in which the error information can be communicated to the host:

1. Host makes a Read request to R08, R09, R0A, R0B and R33 registers.
2. Host starts any transaction with Start condition followed by 7'h7E IBI header (Only applicable in I3C Basic mode).
3. The PMIC device sends in-band interrupt if enabled, when its SCL and SDA input have been idle for t_{AVAL} time (Only applicable in I3C Basic mode).
4. The PMIC device asserts the GSI_n pin if enabled.

4.1.4.11 I3C Basic Common Command Codes (CCC)

The I3C Basic specification lists a large number of Common Command Codes (CCC). Not all CCC are required to be supported. The PMIC device NACKs for all unsupported CCC. Table 36 lists CCCs supported by the PMIC.

The PMIC device requires a STOP operation in between when switching from a CCC operation to private device-specific Write or Read or Default Read Address Pointer mode operation and vice versa. In other words, any CCC operation must be followed by a STOP operation before continuing to any device-specific Write or Read or Default Read Address Pointer mode operation. Similarly, any device-specific Write or Read or Default Read Address Pointer mode operation must be followed by a STOP operation before continuing to any CCC operation.

The PMIC device does allow Repeat Start operation between any CCC and other CCC or between any private Write or Read or Default Read Address Pointer mode operation and other private Write or Read or Default Read Address Pointer mode operation.

Table 36. PMIC CCC Support Requirement

CCC	Mode	Code	Description	Note
ENEC	Broadcast	0x00	Enable Event Interrupts	
	Direct	0x80		
DISEC	Broadcast	0x01	Disable Event Interrupts	
	Direct	0x81		
RSTDAA	Broadcast	0x06	Put the device in I2C Mode (aka: Reset Dynamic Address Assignment)	
SETAASA	Broadcast	0x29	Put the device in I3C Basic Mode (aka: Set All Addresses to Static Address)	
GETSTATUS	Direct	0x90	Get Device Status	
DEVCAP	Direct	0xE0	Get Device Capability	1
SETHID	Broadcast	0x61	PMIC updates 3-bit HID field	1
DEVCTRL	Broadcast	0x62	Configure SPD Hub and all devices behind Hub	1

1. JEDEC specific CCC.

4.1.4.11.1 ENEC CCC

ENEC CCC is only supported in I3C Basic mode. In I2C mode. it is illegal for Host to issue ENEC CCC. When ENEC CCC is registered by PMIC, it updates R34[6] = '1', and this takes effect at the next Start operation (i.e. after STOP operation).

Table 37 to Table 40 shows an example of a single ENEC CCC. Table 41 shows the encoding definition for ENEC CCC.

If the PEC function is enabled, the PEC calculation starts with a Start or Repeat Start operation, but does not include 7'h7E with W=0 byte.

Table 37. ENEC CCC – Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x00 (Broadcast)								T	
	0x00							ENINT	T	Sr[2] or P

1. The PMIC NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 38. ENEC CCC - Broadcast w/ PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x00 (Broadcast)								T	
	0x00							ENINT	T	
	PEC								T	Sr[2] or P

1. The PMIC NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 39. ENEC CCC – Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x80 (Direct)								T	
Sr	DevID[6:0]							W=0	A[1,2]	
	0x00							ENINT	T	Sr[3] or P

1. The PMIC NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. The PMIC device does not check for the parity error in subsequent bytes when it determines 7-bit device Select code issued by Host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or the next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 40. ENEC CCC - Direct w/ PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x80 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W=0	A[1,2]	
	0x00							ENINT	T	
	PEC								T	Sr[3] or P

1. The PMIC NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. The PMIC device does not check for the parity error in subsequent bytes when it determines 7-bit device Select code issued by Host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or the next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 41. ENEC CCC Byte Encoding

Bit	Encoding	Notes
ENINT	0 = No Action 1 = Enable IBI Interrupt	It is illegal for Host to issue ENEC CCC with ENINT bit = “0”.

4.1.4.11.2 DISEC CCC

DISEC CCC is only supported in I3C Basic mode. In I²C mode, it is illegal for Host to issue this CCC. When DISEC CCC is registered by PMIC, it updates R34[6] = ‘0’, and it takes effect at the next Start operation (i.e. after STOP operation). Table 42 to Table 45 shows an example of a single DISEC CCC. Table 46 shows the encoding definition for DISEC CCC.

If the PEC function is enabled, the PEC calculation starts with a Start or Repeat Start operation but does not include 7’h7E with W=0 byte.

Table 42. DISEC CCC – Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x01 (Broadcast)								T	
	7’h00							DISINT	T	Sr[2] or P

1. The PMIC NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7’h7E.

Table 43. DISEC CCC - Broadcast w/ PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x01 (Broadcast)								T	
	7’h00							DISINT	T	
	PEC								T	Sr[2] or P

1. The PMIC NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7’h7E.

Table 44. DISEC CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x81 (Direct)								T	
Sr	DevID[6:0]							W=0	A[1,2]	
	0x00							DISINT	T	Sr[3] or P

1. The PMIC NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. The PMIC device does not check for the parity error in subsequent bytes when it determines 7-bit device Select code issued by Host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or the next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 45. DISEC CCC - Direct w/PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x81 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W=0	A[1,2]	
	0x00							DISINT	T	
	PEC								T	Sr[3] or P

1. The PMIC NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. The PMIC device does not check for the parity error in subsequent bytes when it determines 7-bit device Select code issued by Host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or the next Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 46. DISEC CCC Byte Encoding

Bit	Encoding	Notes
DISINT	0 = No Action 1 = Disable IBI Interrupt	It is illegal for Host to issue DISEC CCC with DISINT bit = '0'.

4.1.4.11.3 RSTDAA CCC

RSTDAA CCC is only supported in I3C Basic mode. In I²C mode, this CCC is ignored. When RSTDAA CCC is registered by PMIC, it updates R32[6] = '0', and it takes effect at the next Start operation (i.e. after STOP operation). Further it disables the IBI & PEC function (R34[7:6] = '00') and clears the parity function R34[5] = '0'.

Table 47 and Table 48 shows an example of a single RSTDAA CCC.

If the PEC function is enabled, the PEC calculation starts with a Start or Repeat Start operation but does not include 7'h7E with W=0 byte.

Table 47. RSTDAA CCC – Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x06 (Broadcast)								T	Sr[2] or P

1. The PMIC NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 48. RSTDAA CCC - Broadcast w/ PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x06 (Broadcast)								T	
	PEC								T	Sr[2] or P

1. The PMIC NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

4.1.4.11.4 SETAASA CCC

The SETAASA CCC is only supported in I²C mode. In I²C mode, when Host issues this CCC, to guarantee that this CCC is registered by the device without any error, Host shall limit the maximum speed operation for this CCC to 1MHz. In I3C Basic mode, this CCC is ignored. When SETAASA CCC is registered by PMIC, it updates R32[6] = '1', and it takes effect at the next Start operation (i.e. after STOP operation). Table 49 shows an example of a single SETAASA CCC.

SETAASA CCC does not support the PEC function as there is no PEC function in I²C mode.

Table 49. SETAASA CCC – Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x29 (Broadcast)								T	P

4.1.4.11.5 GETSTATUS CCC

GETSTATUS CCC is supported in I3C Basic mode. In I²C mode, this CCC is ignored (i.e. it is not executed internally and the Repeat Start byte arriving after the 0x90 GETSTATUS CCC code is not acknowledged and Host must do the STOP operation. Table 50 to Table 51 show an example of a single GETSTATUS CCC.

If the PEC function is enabled, the PEC calculation starts with a Start or Repeat Start operation but does not include 7'h7E with W=0 byte.

Table 50. GETSTATUS CCC – Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x90 (Direct)								T	
Sr	DevID[6:0]							R=1	A	
	PEC_Err	0	0	0	0	0	0	0	T	
	0	0	P_Err	R32[3]	Pending Interrupt				T	Sr[2] or P

1. The PMIC NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 51. GETSTATUS CCC – Direct w/PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x90 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R=1	A	
	PEC_Err	0	0	0	0	0	0	0	T	
	0	0	P_Err	R32[3]	Pending Interrupt				T	
	PEC								T	Sr[2] or P

1. The PMIC NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 52. GETSTATUS CCC Byte Encoding

Bit	Encoding	Notes
PEC_Err	0 = No Error 1 = PEC Error occurs	This register is cleared when Host issues a clear command to R12[3] for PEC error.
P_Err	0 = No Error 1 = Protocol Error; Parity Error occurs	This register is cleared when Host issues a clear command to R12[2] for Parity error.
R32[3]	See R32 for encoding	PMIC reflects the register status of R32[3] in this bit.
Pending Interrupt	0000 = No Pending Interrupt 0001 = Pending Interrupt All other encodings are reserved.	This register is cleared when Host issues a clear command to any appropriate device status register that causes the IBI status register to be cleared.

After the PMIC device completes the response to GETSTATUS CCC, PEC_Err, P_Err and Pending Interrupt Bits[3:0] are not automatically cleared. Host must explicitly clear the appropriate status register through Clear command by writing '1' to the corresponding register or by issuing Global Clear command. Once the PMIC device clears the appropriate status register, only PEC_Err, P_err and Pending Interrupt Bits[3:0] are cleared.

After Host issues a clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register to '1' and Pending Interrupt Bits[3:0] to '0001'.

4.1.4.11.6 DEVCAP CCC

DEVCAP CCC is only supported in I3C Basic mode. In I^2C mode, it is illegal for Host to issue this CCC.

Table 53 and Table 54 show an example of a single DEVCAP CCC. Table 55 defines the encoding for DEVCAP CCC.

If the PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte.

Table 53. DEVCAP CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0xE0 (Direct)								T	
Sr	DevID[6:0]							R=1	A[1]	
	MSB (Each bit defines capability)								T	
	LSB (Each bit defines capability)								T	Sr[2] or P

1. The PMIC NACKs if there is a parity error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 54. DEVCAP CCC – Direct w/PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0xE0 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R=1	A[1]	
	MSB (Each bit defines capability)								T	
	LSB (Each bit defines capability)								T	
	PEC								T	Sr[2] or P

1. The PMIC NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 55. DEVCAP CCC Byte Encoding

Bit	Encoding	Notes
MSB[7]	RFU	Coded as '0'
MSB[6]	RFU	Coded as '0'
MSB[5]	RFU	Coded as '0'
MSB[4]	RFU	Coded as '0'
MSB[3]	RFU	Coded as '0'
MSB[2]	0 = No Support for Timer based Reset 1 = Supports Timer based Reset	Coded as '1'
MSB[1:0]	RFU	Coded as '00'
LSB[7:0]	RFU	Coded as '0x00'

4.1.4.11.7 SETHID CCC

SETHID CCC is supported only in I²C mode. In I²C mode, when Host issues this CCC, to guarantee that this CCC is registered by the device without any error, Host shall limit the maximum speed operation for this CCC to 1MHz. In I3C Basic mode, it is illegal for Host to issue this CCC.

When SETHID CCC is registered by PMIC, it updates R34[3:1] with the HID code received by PMIC, which takes effect at the next Start operation (i.e. after STOP operation). Table 56 shows an example of a single SETHID CCC. When the device is in I²C mode and SETHID CCC is issued, the PEC function is not supported.

Once PMIC receives SETHID CCC and updates its 3-bit HID code, after the Stop operation, the PMIC device only responds to the updated 7-bit address. The 4-bit LID code of the PMIC device remains as is.

Host may issue SETHID CCC more than one time.

Table 56. SETHID CCC – Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x61 (Broadcast)								T	
	0	0	0	0	HID[2:0]			0	T	P

4.1.4.11.8 DEVCTRL CCC

On a typical I3C Basic bus, there can be up to 120 devices. For DDR5 DIMM application environment, there are up to 8 SPD5 Hub devices, and for each SPD5 Hub device, there are 4 local target devices, totaling up to 40 or more devices on an I3C Basic bus.

For certain operation such as enable or disable functions that are common to all devices (i.e. Packet Error Check), Host must go through one device at a time, which takes significant amount of time at initial power up. Further, it requires additional complexity on Host because it must speak different protocol depending on how it may access the device until all devices are configured identically.

To help expedite this configuration operation and simplify the Host complexity, the device supports DEVCTRL CCC. DEVCTRL CCC is supported either in I²C mode or I3C Basic mode of operation.

In I²C mode, when Host issues this CCC, to guarantee that this CCC is registered by the device without any error, Host shall limit the maximum speed operation for this CCC to 1MHz. Table 57 to Table 58 show an example of a single DEVCTRL CCC.

In I3C mode only, if the PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte.

Host shall pay attention to DEVCTRL CCC. If DEVCTRL CCC is used to access device-specific registers (i.e. RegMod = '1'), Host shall still follow any device-specific register restriction. For example, if the device-specific register requires STOP operation for device to take in the effect of the setting, Host must also use the STOP operation when using DEVCTRL CCC to access the device-specific register.

Table 57. DEVCTRL CCC – Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T[2]	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	Sr[3] or P

1. The PMIC NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
2. An exception is made for DEVCTRL CCC. The PMIC does not report the parity error when it determines the 7-bit device Select code issueed by Host does not match with its own device code. If the 7-bit device Select code does not match but the parity is still valid, the device does not check for the parity error in subsequent bytes, but ignores the entire packet and waits until STOP or Repeat Start operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 58. DEVCTRL CCC – Broadcast w/PEC[1]

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[2]	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T[3]	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	
	PEC								T	Sr[4] or P

1. DEVCTRL CCC with PEC Check is only supported in I3C mode.
2. The PMIC NACKs if there is a parity or PEC error in a previous transaction when Host performs consecutive transactions with Repeat Start.
3. An exception is made for DEVCTRL CCC. The PMIC does not report the parity error when it determines 7-bit device Select code issued by Host does not match with its own device code. The device does not check for PEC as all subsequent bytes are discarded due to parity error. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until STOP or Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 59. DEVCTRL CCC Command Definition

Parameter	Definition
AddrMask[2:0]	Broadcast, Unicast or Multicast Command Selection • 000 = Unicast Command; the PMIC device responds if the DevID[6:0] field matches with the PMIC device own 7-bit address (4-bit LID + 3-bit HID); • 011 = Multicast Command; the PMIC device and possible other device responds if the DevID[6:3] field matches with the PMIC device own 4-bit LID address; • 111 = Broadcast Command; All devices responds to this command. All other encodings are reserved.
StartOffset[1:0]	Only applicable when RegMod = '0'. Identifies the starting Byte (Byte 0 or Byte 1 or Byte 2 or Byte 3) for DEVCTRL CCC. Host can start at any Byte (from Byte 0 to Byte 3) and continue to access the next byte until STOP operation. If Byte 3 is reached, Host is responsible for applying STOP operation. 00 = Byte 0 01 = Byte 1 10 = Byte 2 11 = Byte 3
PEC BL[1:0]	Only applicable when RegMod = '0' and the PEC function is enabled. Identifies the burst length just for this DEVCTRL CCC. The device uses the setting in this field to know when the PEC byte is expected after the data bytes. 00 = 1 Byte 01 = 2 Byte 10 = 3 Byte 11 = 4 Byte
RegMod	Identifies if DEVCTRL will be used for General Registers as identified in Byte 0 to Byte 3 or the device-specific address offset register, if there are different types of devices on the I3C bus. • 0 = Access to General Registers in Byte 0 to Byte 3 (i.e. StartOffset[1:0] = Valid); • 1 = Device-specific Offset Address (i.e Start Offset[1:0] & PECBL[1:0] is a Don't Care and Does not Apply). Host shall NOT use RegMod = '1' with Broadcast Command.
DevID[6:0]	Identifies 7-bit device address. The device responds to the DEVCTRL CCC data packet depending on AddrMask[2:0]. • If AddrMask[2:0] = '111', DevID[6:0] is a Don't Care and device always responds. • If AddrMask[2:0] = '000', DevID[6:0] must match for device to respond • If AddrMask[2:0] = '011', DevID[6:3] must match for device to respond. DevID[2:0] is Don't Care. For any other codes for AddrMask[2:0], the device always NACKs.

Table 60. DEVCTRL CCC Data Payload Definition

Byte #	Bit #	Function	Definition	Comment
Byte 0	[7]	PEC Enable	0 = Disable 1 = Enable	R34[7] is updated
	[6]	Parity Disable	0 = Enable 1 = Disable	R34[5] is updated
	[5:2]	RFU	RFU	
	[1]	VR Enable	0 = VR Disable 1 = VR Enable	R32[7] is updated
	[0]	RFU	RFU	
Byte 1	[7:4]	RFU	RFU	
	[3]	Global & IBI Clear	0 = No Action 1 = Clear All Event and pending IBI[1]	R14[0] is updated
	[2:0]	RFU	RFU	
Byte 2	[7:0]	RFU	RFU	
Byte 3	[7:0]	RFU	RFU	

1. After the target device clears the event, the device can still have certain registers set to '1' if the event is still present in which case, the device will generate an IBI again at the next opportunity.

4.1.4.11.8.1 DEVCTRL CCC Examples - RegMod = '0'

Table 61 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with the PEC function disabled and the parity function enabled. In this example, Host uses DEVCTRL CCC as the Multicast command. Host sends the Multicast command to all devices with 4-bit LID code of '1001' on I3C Basic bus to do VR Enable followed by all devices with 4-bit LID code of '0110' to disable the parity function. Host sends AddrMask = '011' to indicate the Multicast command with DevID[6:3] matching with the PMIC device own 4-bit LID address; StartOffset = '00' to indicate starting Byte 0; and RegMod = '0' to indicates Access to general registers. Upon receiving this command, all devices with DevID[6:3] matching to '1001' will do the VR Enable command; and all devices with DevID[6:3] matching to '0110' will disable the parity function.

Table 62 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with the PEC function disabled and the parity function enabled. In this example, Host uses DEVCTRL CCC as the Broadcast command to enable the PEC function. Host sends AddrMask = '111' to indicate the Broadcast command; StartOffset = '00' to indicate starting Byte 0; and RegMod = '0' to indicate Access to general registers. Upon receiving this command, all devices will enable the PEC function.

Table 61. DEVCTRL CCC Example - Multicast Command to '1001' & '0110' Devices (Sheet 1 of 2)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	1001 000							0	T	
	0000 0010								T	

Table 61. DEVCTRL CCC Example - Multicast Command to '1001' & '0110' Devices (Sheet 2 of 2)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	0110 000							0	T	
	0100 0000								T	P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 62. DEVCTRL CCC Example - Broadcast Command to all Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	111			00		00		0	T	
	0000 000							0	T	
	1000 0000								T	P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 63 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as the Unitcast command to enable VR on DIMM5. Host sends AddrMask = '000' to indicate the Unicast command; StartOffset = '00' to indicate starting Byte 0; and RegMod = '0' to indicates Access to general register. Upon receiving this com- mand, PMIC on DIMM5 will enable its regulator.

Table 63. DEVCTRL CCC Example - Unicast Command to PMIC on DIMM5

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	000			00		00		0	T	
	1001 101							0	T	
	0000 0010								T	P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

4.1.4.11.8.2 DEVCTRL CCC Examples - RegMod = '1'

Table 64 shows an example of DEVCTRL CCC data packet for the purpose of configuring device-specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with the PEC function enabled

and the parity function enabled. In this example, Host sends a Multicast command to all devices with 4-bit LID code of ‘0010’ on the I3C Basic bus to write to address offset of 0x1C and 0x1D with data 0xFF and 0x55 respectively followed by all devices with 4-bit LID of ‘1001’ on the I3C Basic bus to write to address offset of 0x15 with data 0x78.

The PEC calculation starts with Start or Repeat Start operation but does not include 7’h7E with W=0 byte.

Table 65 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with the PEC function disabled and the parity function enabled. In this example, Host sends the Multicast command to all devices with 4-bit LID code of ‘1001’ on the I3C Basic bus to write to address offset of 0x13 with data 0xFF and it continues to write data 0x01 to the next address.

Table 64. DEVCTRL CCC Example - Multicast Command to ‘0010’ & ‘1001’ Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	0010 000							0	T	
	0001 1100 (address offset 0x1C)								T	
	0010 0000 (CMD field = 2 bytes of data)								T	
	1111 1111 (data)								T	
	0101 0101 (data)								T	
	PEC								T	
Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0101 (address offset 0x15)								T	
	0000 0000 (CMD field = 1 byte of data)								T	
	0111 1000 (data)								T	
	PEC								T	P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 65. DEVCTRL CCC Example - Multicast Command to '1001' Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0011 (address offset 0x13)								T	
	1111 1111 (data)								T	
	0000 0001 (data)								T	P

1. See Figure 20 to know how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

4.1.4.12 IO Operation

At Power On, by default, the PMIC device comes up in legacy I2C mode of operation with Open Drain IO for its interface. The maximum speed is limited to 1MHz and the supported IO voltage levels are from 1.0V to 3.3V.

After Power On, Host may put the PMIC device in I3C Basic mode of operation.

In I3C Basic mode, Host may drive the SCL clock input of the PMIC device using either Push-Pull output driver or the open-drain output driver. It is expected that for all DDR5 DIMM family environment, Host may always drive the SCL clock input using a Push-Pull output driver.

To support in-band interrupt, the PMIC device supports dynamic switching between Open Drain mode and Push Pull mode on its SCL and SDA bus for various events. Table 66 describes the different modes of operation by the PMIC device for each cycle.

Table 66. PMIC Device Dynamic IO Operation Mode Switching

	Open Drain Mode	Push Pull Mode
START + Device Select Code	Yes	No
START + 7'h7E IBI Header Byte	Yes	No
REPEAT START + Device Select Code	No	Yes
REPEAT START + 7'h7E Header Byte	No	Yes
CCC Bytes (i.e after 7'h7E+W=0+ACK)	No	Yes
STOP	No	Yes
ACK/NACK Responses	Yes	No
Command, Block Address, Address Operation	No	Yes
Interrupt Request by Target + Device Select Code	Yes	No
IBI Payload	No	Yes
Write Data, T-bit sequence	No	Yes
Read Data, T-bit sequence	No	Yes
PEC, T-bit sequence	No	Yes

4.1.4.13 Bus Clear

The PMIC device supports the following described Bus Clear feature in I²C mode only. Any attempt by host to perform I²C Bus clear on a target device in I3C mode may result in an active drive bus contention on the SDA data line.

There may be abnormal circumstances when the host abruptly stops clocking SCL while the target device is in the middle of outputting data for read operation. For these type of events, the SDA data line may appear as stuck low as the device is expected to receive more clock pulses from the host. Eventually when the host has control of the SCL clock, the host may optionally clear the device that is stuck low on the SDA data line by sending continuous 18 clock pulses without driving the SDA data line followed by STOP operation. The device floats the SDA line within 18 clock pulses and returns to the Idle state. The device is ready for normal new transaction with Start condition.

4.1.4.14 Bus Reset

To prevent a malfunctioning device from locking up the I²C bus or I3C Basic bus, a bus reset mechanism is defined. It uses a timeout mechanism on SCL as shown in Figure 27 to force a device bus reset. All devices on a I²C or I3C Basic bus reset simultaneously. The Bus reset operation works the same way regardless of whether device is operating in I²C or I3C Basic mode.

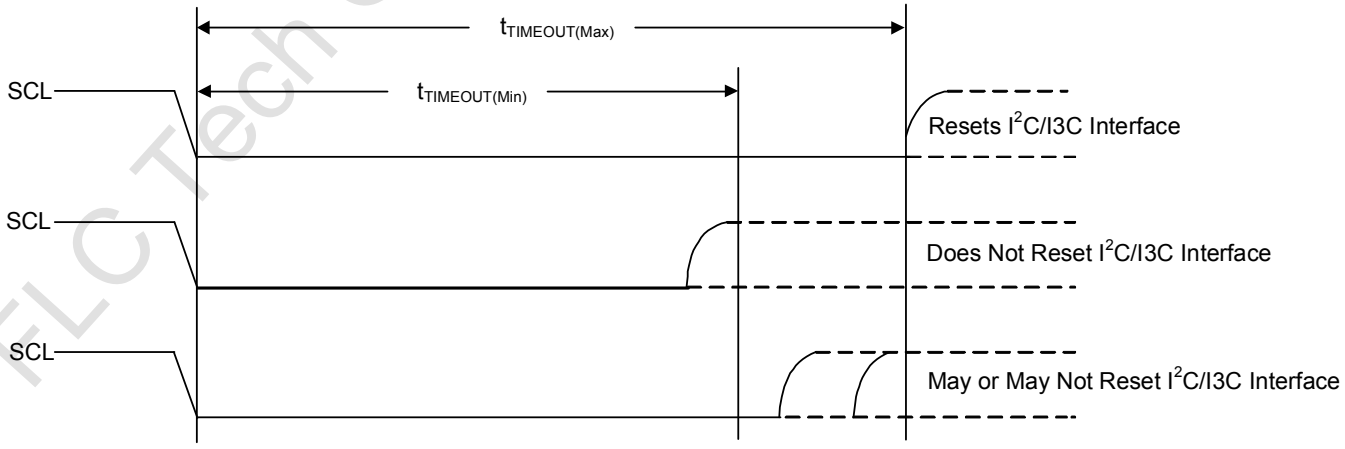
To guarantee that the device resets the I²C bus or I3C Basic bus, the SCL clock input Low time has to be greater than or equal to $t_{TIMEOUT(Max)}$. The PMIC device does not reset I²C bus or I3C Basic bus if the SCL clock input Low time is less than $t_{TIMEOUT(Min)}$.

If the SCL clock input Low time is between $t_{TIMEOUT(Min)}$ and $t_{TIMEOUT(Max)}$, it does not guarantee that the PMIC device resets the I²C bus or I3C Basic bus.

When Reset, the PMIC device takes the following actions:

1. Interface and any pending command or transactions are cleared.
2. All internal register values are preserved unless noted otherwise in item # 3 below.
3. Device returns to I²C mode of operation; R34[3:1] resets to '111'; "R34[7:5] resets to '000'; R32[6] to '0'; R0A[3:2] to '00'.
4. Device does not re-sample the PID pin.
5. Device floats the SDA pin such that it gets pulled High by an external/other device pull-up.
6. Device treats Bus reset as a STOP operation.

Figure 27. I²C or I3C Basic Bus Reset - PMIC Device



4.1.4.15 Command Truth Table

The command truth table as shown in Table 67 only applies in I3C Basic mode with PEC enabled. In I²C mode and I3C Basic mode with PEC disabled, the command truth table does not apply.

Table 67. For I3C Basic Mode Only w/ PEC Enabled - Command Truth Table

Command	Command Name	CMD Code	RW	Address
		2nd Byte Bits[7:5]	2nd Byte Bit[4]	1st Byte Bits[7:0]
Write 1 Byte to Register	W1R	000	0	V
Read 1 Byte from Register	R1R		1	V
Write 2 Byte to Register	W2R	001	0	V
Read 2 Byte from Register	R2R		1	V
Write 4 Byte to Register	W4R	010	0	V
Read 4 Byte from Register	R4R		1	V
Write 16 Byte to Register	W16R	011	0	V
Read 16 Byte from Register	R16R		1	V
Reserved	RSVD	100 to 111	RSVD	RSVD

4.2 Register Attribute Definition

All registers have Base Attributes as defined in Table 68.

Table 68. Register Base Attributes

Attribute	Abbreviation	Description
Read Only	RO	This bit can be read by Host. Write has no effect.
Read/Write	RW	This bit can be read or written by Host.
Write Only	WO	This bit can only be written by Host. Read from this bit returns ‘0’.
Reserved	RV or reserved	This bit is reserved for future expansion and its value must not be modified by software. The bit will return ‘0’ when read. When writing this bit, software must preserve the value read unless otherwise indicated.

Table 69. Register Base Modifier

Attribute	Abbreviation	Description
Write ‘1’ Only	W1O	This bit can only be set (i.e. write ‘1’) but not reset (i.e. write ‘0’) via I²C/I3C Bus.
Protected	P	This bit is protected by the password registers. This bit cannot be written to unless the password code has been written into the password registers.
Persistent	E	This bit is persistent during power cycle.

4.3 Register Map Breakdown

Table 70. Register Map Breakdown

Register Range	Region	Comments
0x00 ~ 0x3F	Host Region	Host Accessible Registers
0x40 ~ 0x6F	DIMM Vendor Region	DIMM Vendor Registers - Non Volatile Memory Allows DIMM vendors to program the PMIC for a given DRAM/DIMM vendor designs. These are password protected registers and the password is selected by DIMM vendor. Under normal operation, these registers are not used by any host. These registers require password for read access. Access to these registers without correct password will return all data as '0'. These registers require complete power cycle before it takes in effect. Changing these registers under normal operation is considered an illegal operation.
0x70 ~ 0xFF	Vendor Specific Region	Vendor Specific Registers - Non Volatile Memory These are vendor specific password protected registers. Under normal operation these registers are not used by any host. These registers require password for read access. Access to these registers without correct password will return all data as '0'.

4.4 Register Memory Protection

The PMIC DIMM vendors registers (0x40 - 0x6F) are password protected registers. Both Read and Write access to DIMM vendor registers are blocked unless it is unlocked by providing the correct password. The default password for DIMM vendor registers is 0x9473. The PMIC offers DIMM vendors to select their own password for DIMM vendor registers.

4.4.1 Steps to Access DIMM Vendor Region Registers

The steps to access the DIMM vendor registers are as following:

1. Write to Register R37 = 8 bit password LSB code.
2. Write to Register R38 = 8 bit password MSB code.
3. Write to Register R39 = 0x40.
4. Perform Read operations to DIMM vendor registers as desired.
5. Write to Register R39 = 0x00.

4.4.2 Steps to Change DIMM Vendor Region Password

By default, the DIMM vendor region register password is 0x9473. The steps to change the password from default password are as following (VIN_MGMT = 3.3V, VIN_BULK = 12V or no less than 5V):

1. Write to Register R37 = 0x73.
2. Write to Register R38 = 0x94.
3. Write to Register R39 = 0x40.
4. Write to Register R37 = New 8 bit password LSB code as desired by the DIMM vendor.
5. Write to Register R38 = New 8 bit password MSB code as desired by the DIMM vendor.
6. Write to Register R39 = 0x80.
7. Wait 200 ms.

8. Write to Register R39 = 0x00.
9. Power cycle the PMIC. (Remove VIN_BULK and VIN_MGMT supply from the PMIC. The new password is in effect after the power cycle.

To change the password again from this point on, repeat steps 1 to 8 but note that in steps 1 and 2 current password is required.

4.4.3 Steps to Burn or Program DIMM Vendor Region Registers

The steps to burn or to program the DIMM vendor registers are as following (VIN_MGMT = 3.3V, VIN_BULK = 12V or no less than 5V):

1. Write to Register R37 = 8 bit password LSB code.
2. Write to Register R38 = 8 bit password MSB code.
3. Write to Register R39 = 0x40.
4. Programming DIMM vendor registers are done at block level. Block 40 addresses: 0x40 - 0x4F; Block 50 addresses: 0x50 - 0x5F; Block 60 addresses: 0x60 - 0x6F. Perform write operation to each block as desired.
5. Burn each block one at a time: Block 40 addresses: Write Register R39 = 0x81. Block 50 addresses: Write register Register R39 = 0x82. Block 60 addresses: Write Register R39 = 0x85.
6. Wait time 200 ms.
7. To check if programming is complete: Perform read from Register R39. The code 0x5A indicates it is complete. It takes 200 ms per page to program.
8. To verify if programming is done correctly: Perform read operation from appropriate block addresses.
9. Write to Register R39 = 0x00.

4.4.4 Host Region Register Map

Table 71. Register Color Coding Scheme

Region	Register Range	Restriction
Host Region + DIMM Vendor Region + Vendor specific Region	R15 ~ R2F R32[7,5:0] R35 R40 ~ R6F R70 ~ RFF	Register Modification is NOT allowed in Write Protect Mode.
Host Region	R20 ~ R2D	Registers are copied from DIMM Vendor Region Setting at power on.

Table 72. Host Region - Register Map (Sheet 1 of 6)

Register	Attribute	Description
0x00 ~ 0x03	Reserved	R00[7:0] to R03[7:0] - Reserved
R04	ROE	R04[7] Global Error Count R04[6:4] Global Error History Log R04[3:0] Reserved
R05	ROE	R05[7] Reserved R05[6:3] Power On Reset - SWA, SWB, SWC & SWD Power Not Good R05[2:0] Power On Reset - High Level Status Code

Table 72. Host Region - Register Map (Sheet 2 of 6)

Register	Attribute	Description
R06	ROE	R06[7:4] Power On Reset - SWA, SWB, SWC & SWD Under Voltage Lockout R06[3:0] Power On Reset - SWA, SWB, SWC & SWD Over Voltage
0x07	ROE	R07[7:0] Reserved
R08	RO	R08[7] VIN_BULK Input Power Good Status R08[6] Critical Temperature Shutdown Status R08[5:2] SWA, SWB, SWC, SWD Output Power Good Status R08[1] VIN_MGMT Input Over Voltage Status R08[0] VIN_BULK Input Over Voltage Status
R09	RO	R09[7] PMIC High Temperature Warning Status R09[6] VBias Power Good Status R09[5] VLDO_1.8V Output Power Good Status R09[4] VIN_MGMT to VIN_BULK Input Supply Switchover Status R09[3:0] SWA, SWB, SWC & SWD High Output Current Consumption Warning Status
R0A	RO	R0A[7:4] SWA, SWB, SWC, SWD Output Over Voltage Status R0A[3] PEC Error Status R0A[2] Parity Error Status R0A[1] IBI Status R0A[0] Reserved
R0B	RO	R0B[7:4] SWA, SWB, SWC & SWD Output Current Limiter Warning Status R0B[3:0] SWA, SWB, SWC & SWD Output Under Voltage Lockout Status
R0C	RO	R0C[7:0] SWA Output Current or Power or Total Output Power Measurement
R0D	RO	R0D[7:6] Reserved R0D[5:0] SWB Output Current or Power Measurement
R0E	RO	R0E[7:6] Reserved R0E[5:0] SWC Output Current or Power Measurement
R0F	RO	R0F[7:6] Reserved R0F[5:0] SWD Output Current or Power Measurement
R10	W1O	R10[7] Clear VIN_BULK Input Power Good Status R10[6] Reserved R10[5:2] Clear SWA, SWB, SWC & SWD Output Power Good Status R10[1] Clear VIN_MGMT Input Over Voltage Status R10[0] Clear VIN_BULK Input Over Voltage Status
R11	W1O	R11[7] Clear PMIC High Temperature Warning Status R11[6] Clear VBIAS Power Good Status R11[5] Clear VLDO_1.8V Output Power Good Status R11[4] Clear VIN_MGMT to VIN_BULK Input Supply Switchover Status R11[3:0] Clear SWA, SWB, SWC & SWD High Output Current Consumption Warning Status

Table 72. Host Region - Register Map (Sheet 3 of 6)

Register	Attribute	Description
R12	W1O	R12[7:4] Clear SWA, SWB, SWC, SWD Output Over Voltage Status R12[3] Clear PEC Error R12[2] Clear Parity Error R12[1:0] Reserved
R13	W1O	R13[7:4] Clear SWA, SWB, SWC & SWD Output Current Limiter Warning Status R13[3:0] Clear SWA, SWB, SWC & SWD Output Under Voltage Lockout Status
R14	W1O	R14[7:5] Reserved R14[4] Clear VIN_MGMT Power Good Status in Switchover Mode R14[3] Clear VBias Output or VIN_BULK Input Under VoltageLockout Status R14[2] Clear VLDO_1.0V Output Power Good Status R14[1] Reserved R14[0] Clear Global Status
R15	RW	R15[7] Mask VIN_BULK Input Power Good Status R15[6] Reserved R15[5:2] Mask SWA, SWB,SWC & SWD Output Power Good Status R15[1] Mask VIN_MGMT Input Over Voltage Status R15[0] Mask VIN_BULK Input Over Voltage Status
R16	RW	R16[7] Mask PMIC High Temperature Warning Status R16[6] Mask VBias Power Good Status R16[5] Mask VLDO_1.8V Output Power Good Status R16[4] Mask VIN_MGMT to VIN_BULK Input Supply Switchover Status R16[3:0] Mask SWA, SWB, SWC & SWD High Output Current Consumption Warning Status
R17	RW	R17[7:4] Mask SWA, SWB, SWC, SWD Output Over Voltage R17[3] Mask PEC Error Status R17[2] Mask Parity Error Status R17[1:0] Reserved
R18	RW	R18[7:4] Mask SWA, SWB, SWC & SWD Output Current Limiter Warning Status R18[3:0] Mask SWA, SWB, SWC & SWD Output Under Voltage Lockout Status
R19	RW	R19[7:5] Reserved R19[4] Mask VIN_MGMT Power Good Status Switchover Mode R19[3] Mask Vbias Output or VIN_BULK Input Under Voltage Lockout Status R19[2] Mask VLDO_1.0V Output Power Good Status R19[1:0] Reserved
R1A	RW	R1A[7:5] VIN_BULK Input Power Good Threshold Voltage R1A[4] Reserved R1A[3] VBIAS Power Good Threshold Voltage R1A[2] VLDO_1.8V Power Good Threshold Voltage R1A[1] Output Power Measurement Select R1A[0] VLDO_1.0V Power Good Threshold Voltage

Table 72. Host Region - Register Map (Sheet 4 of 6)

Register	Attribute	Description
R1B	RW	R1B[7] VIN_BULK Input Over Voltage Threshold R1B[6] Current or Power Meter Select R1B[5] VIN_MGMT Input Over Voltage Threshold R1B[4] Global Mask Control for CAMP Output Pin R1B[3] GSI_n Pin Enable R1B[2:0] PMIC High Temperature Warning Threshold
R1C	RW	R1C[7:2] SWA Output High Current Threshold R1C[1:0] Reserved
R1D	RW	R1D[7:2] SWB Output High Current Threshold R1D[1:0] Reserved
R1E	RW	R1E[7:2] SWC Output High Current Threshold R1E[1:0] Reserved
R1F	RW	R1F[7:2] SWD Output High Current Threshold R1F[1:0] Reserved
R20	RW	R20[7:6] SWA Output Current Limiter Warning Threshold R20[5:4] SWB Output Current Limiter Warning Threshold R20[3:2] SWC Output Current Limiter Warning Threshold R20[1:0] SWD Output Current Limiter Warning Threshold
R21	RW	R21[7:1] SWA Voltage Setting R21[0] SWA Power Good Low Side Threshold
R22	RW	R22[7:6] SWA Power Good High Side Threshold R22[5:4] SWA Over Voltage Threshold R22[3:2] SWA Under Voltage Lockout Threshold R22[1:0] SWA Soft Stop Time
R23	RW	R23[7:1] SWB Voltage Setting R23[0] SWB Power Good Low Side Threshold
R24	RW	R24[7:6] SWB Power Good High Side Threshold R24[5:4] SWB Over Voltage Threshold R24[3:2] SWB Under Voltage Lockout Threshold R24[1:0] SWB Soft Stop Time
R25	RW	R25[7:1] SWC Voltage Setting R25[0] SWC Power Good Low Side Threshold
R26	RW	R26[7:6] SWC Power Good High Side Threshold R26[5:4] SWC Over Voltage Threshold R26[3:2] SWC Under Voltage Lockout Threshold R26[1:0] SWC Soft Stop Time
R27	RW	R27[7:1] SWD Voltage Setting R27[0] SWD Power Good Low Side Threshold

Table 72. Host Region - Register Map (Sheet 5 of 6)

Register	Attribute	Description
R28	RW	R28[7:6] SWD Power Good High Side Threshold R28[5:4] SWD Over Voltage Threshold R28[3:2] SWD Under Voltage Lockout Threshold R28[1:0] SWD Soft Stop Time
R29	RW	R29[7:6] SWA Mode Select R29[5:4] SWA Switching Frequency R29[3:2] SWB Mode Select R29[1:0] SWB Switching Frequency
R2A	RW	R2A[7:6] SWC Mode Select R2A[5:4] SWC Switching Frequency R2A[3:2] SWD Mode Select R2A[1:0] SWD Switching Frequency
R2B	RW	R2B[7:6] VLDO_1.8V LDO Setting R2B[5:3] Voltage Range Selection for SWA, SWB and SWC R2B[2:1] VLDO_1.0V LDO Setting R2B[0] Voltage Range Selection for SWD
R2C	RW	R2C[7:5] SWA Soft Start Time R2C[4] Reserved R2C[3:1] SWB Soft Start Time R2C[0] Reserved
R2D	RW	R2D[7:5] SWC Soft Start Time R2D[4] Reserved R2D[3:1] SWD Soft Start Time R2D[0] Reserved
R2E	RW	R2E[7:3] Reserved R2E[2:0] PMIC Shutdown temperature threshold
R2F	RW	R2F[7] VIN_MGMT Input Supply Switchover Threshold Voltage R2F[6:3] SWA, SWB, SWC & SWD Enable R2F[2] Write Protect Function Control R2F[1:0] Mask Bits Register Control
R30	RW	R30[7] ADC Enable R30[6:3] ADC Select R30[2] Reserved R30[1:0] ADC Register Update Frequency
R31	RO	R31[7:0] ADC Read Out
R32	RW, RO	R32[7] VR Enable R32[6] Management Interface Selection R32[5] Execute VR Enable Control R32[4:3] Execute CAMP Fail_n Function Control R32[3] PMIC CAMP Power Good Output Signal Control R32[2:0] Reserved

Table 72. Host Region - Register Map (Sheet 6 of 6)

Register	Attribute	Description
R33	RO	R33[7:5] Temperature Measurement R33[4] VIN_MGMT Power Good Status in Switchover Mode Only R33[3] VBias Output or VIN_BULK Input Under Voltage Lockout Status R33[2] VLDO_1.0V Output Power Good Status R33[1:0] Reserved
R34	RO	R34[7] PEC Enable R34[6] IBI Enable R34[5] Parity Disabled R34[4] Reserved R34[3:1] HID_CODE R34[0] Reserved
R35	RW	R35[7] Error Injection Enable R35[6:4] Output Rail Selection R35[3] Over and Under Voltage Select R35[2:0] Misc. Error Injection Type
0x36	Reserved	R36[7:0] Reserved
R37	WO	R37[7:0] Password Lower Byte 0
R38	WO	R38[7:0] Password Upper Byte 1
R39	RW	R39[7:0] Command Codes
R3A	RW	R3A[7] Reserved R3A[6] Default Read Address Pointer Enable R3A[5:4] Default Read Address Pointer Selection R3A[3:2] Burst Length for Default Read Address Pointer Mode in PEC Enabled Mode R3A[1:0] Reserved
R3B	ROE	R3B[7:6] Reserved R3B[5:4] Major Revision ID R3B[3:1] Minor Revision ID R3B[0] PMIC Current Capability
R3C	ROE	R3C[7:0] VENDOR_ID_BYTE0
R3D	ROE	R3D[7:0] VENDOR_ID_BYTE1
0x3E ~ 0x3F	Reserved	R3E[7:0] to R3F[7:0] Reserved

4.4.5 DIMM Vendor Region Register Map

Table 73. DIMM Vendor Region - Register Map (Sheet 1 of 3)

Register	Attribute	Description
R40	RWPE	R40[7:0] Power On Sequence Config 0
R41,	RWPE	R41[7:0] Power On Sequence Config 1
R42,	RWPE	R42[7:0] Power On Sequence Config 2

Table 73. DIMM Vendor Region - Register Map (Sheet 2 of 3)

Register	Attribute	Description
R43,	RWPE	R43[7:0] Power On Sequence Config 3
0x44	RV	R44[7:0] Reserved
R45	RWPE	R45[7:1] SWA Voltage Setting R45[0] SWA Power Good Low Side Threshold
R46	RWPE	R46[7:6] SWA Power Good High Side Threshold R46[5:4] SWA Over Voltage Threshold R46[3:2] SWA Under Voltage Lockout Threshold R46[1:0] SWA Soft Stop Time
R47	RWPE	R47[7:1] SWB Voltage Setting R47[0] SWB Power Good Low Side Threshold
R48	RWPE	R48[7:6] SWB Power Good High Side Threshold R48[5:4] SWB Over Voltage Threshold R48[3:2] SWB Under Voltage Lockout Threshold R48[1:0] SWB Soft Stop Time
R49	RWPE	R49[7:1] SWC Voltage Setting R49[0] SWC Power Good Low Side Threshold
R4A	RWPE	R4A[7:6] SWC Power Good High Side Threshold R4A[5:4] SWC Over Voltage Threshold R4A[3:2] SWC Under Voltage Lockout Threshold R4A[1:0] SWC Soft Stop Time
R4B	RWPE	R4B[7:1] SWD Voltage Setting R4B[0] SWD Power Good Low Side Threshold
R4C	RWPE	R4C[7:6] SWD Power Good High Side Threshold R4C[5:4] SWD Over Voltage Threshold R4C[3:2] SWD Under Voltage Lockout Threshold R4C[1:0] SWD Soft Stop Time
R4D	RWPE	R4D[7:6] SWA Mode Select R4D[5:4] SWA Switching Frequency R4D[3:2] SWB Mode Select R4D[1:0] SWB Switching Frequency
R4E	RWPE	R4E[7:6] SWC Mode Select R4E[5:4] SWC Switching Frequency R4E[3:2] SWD Mode Select R4E[1:0] SWD Switching Frequency
R4F	RWPE	R4F[7] Output Regulator Disable Control R4F[6:5] Reserved R4F[4] SWA Remote Sensing Scheme R4F[3] Reserved R4F[2] SWC Remote Sensing Scheme R4F[1] SWD Remote Sensing Scheme R4F[0] SWA, SWB Single or Dual Phase Regulator Select

Table 73. DIMM Vendor Region - Register Map (Sheet 3 of 3)

Register	Attribute	Description
R50	RWPE	R50[7:6] SWA Current Limit Warning Threshold R50[5:4] SWB Current Limit Warning Threshold R50[3:2] SWC Current Limit Warning Threshold R50[1:0] SWD Current Limit Warning Threshold
R51	RWPE	R51[7:6] VLDO_1.8V LDO Setting R51[5:3] Voltage Range Selection for SWA, SWB and SWC R51[2:1] VLDO_1.0V LDO Setting R51[0] Voltage Range Selection for SWD
0x52 ~ 0x57	RV	R52[7:0] to R57[7:0] Reserved
R58	RWPE	R58[7:0] Power Off Sequence Config 0
R59,	RWPE	R59[7:0] Power Off Sequence Config 1
R5A,	RWPE	R5A[7:0] Power Off Sequence Config 2
R5B,	RWPE	R5B[7:0] Power Off Sequence Config 3
R5C	RV	R5C[7:0] Reserved
R5D	RWPE	R5D[7:5] SWA Soft Start Time R5D[4] Reserved R5D[3:1] SWB Soft Start Time R5D[0] Reserved
R5E	RWPE	R5E[7:5] SWC Soft Start Time R5E[4] Reserved R5E[3:1] SWD Soft Start Time R5E[0] Reserved
0x5F ~ 0x6F	RV	R5F[7:0] to R6F[7:0] Reserved

4.5 Register Reset Condition

Table 74. Register Reset Condition

Reset Condition	Reset Register
POR (VBIAS < 2 V)	All registers
VIN_BULK UV and VIN_MGMT UV	All registers
VLDO_1.8V invalid or VLDO_1.0V invalid (<V_{UV_LDOx})	All registers

4.6 Host Region Register

The default values of Host Region Registers are marked in gray, and are the same as JEDEC spec. The actual values of Registers R20 to R2D depend on the related DIMM Vendor Region registers contents when the input power rails are ready, and after that the host can also change some Host Region register values per needs.

4.6.1 Status Registers

The PMIC offers status registers that are grouped into four different categories.

1. Global History of Error Log Register (R04[7:4])
2. Error Log Registers (R05[6:0], R06[7:0], R07[7:0]; R07[7:0] is currently defined as Reserved)
3. Real time Status Registers (R08[7:0], R09[7:0], R0A[7:1], R0B[7:0], R33[4:2])
4. Periodic Status Registers (R0C[7:0], R0D[5:0], R0E[5:0], R0F[5:0], R33[7:5])

Global History of Error Log Registers (R04[7:4]) - This register records the PMIC state at each abnormal power down cycle. This register reports the cumulative error of each abnormal power down sequence. The PMIC writes this register on its own when it internally generates VR Disable command on its own due to failure. The host can erase this register in MTP memory and clear the status register by writing the code 0x74 in Register R39.

Error Log Registers (R05[6:0], R06[7:0] to R07[7:0]) - These registers record the PMIC state at each power down sequence. The PMIC may report abnormal power down sequence or normal power down sequence. The PMIC writes this register on its own when it internally generates VR Disable command on its own due to failure. These registers are updated at power down cycle, if update is needed by the PMIC on its own. The host can clear the status register by writing the code 0x74 in Register R39.

Real Time Status Registers (R08[7:0], R09[7:0], R0A[7:1], to R0B[7:0], R33[4:2]): These registers are updated to '1' any time based on any event that occurs. The status registers will remain at '1' even if the failing condition is no longer present until the Clear Register command is received by the PMIC. The status Registers R08[7], R09[5] and R33[2] is only valid once valid VIN_BULK and VIN_MGMT input supply is valid at the PMIC input pin. The remaining status registers are valid after VR Enable command is registered.

Periodic Status Registers (R0C[7:0], R0D[5:0], R0E[5:0], R0F[5:0], R33[7:5]) - These registers are updated periodically. These registers are only valid after VR Enable command is registers.

All Read Only (RO) registers except for Registers R0C[7:0], R0D[5:0], R0E[5:0] and R0F[5:0] are one time latched registers. In other words, once PMIC sets those register flag, the host must explicitly clear those registers appropriately. The PMIC does not automatically update the registers on its own even if the event that triggered the status is no longer present. The Registers R0C[7:0], R0D[5:0], R0E[5:0], R0F[5:0] are dynamically updated by the PMIC at certain frequency and they represent the status at that point.

Table 75. R04

Address: 04H
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7	GLOBAL_ ERROR_ COUNT	ROE	Global Error Count since the last Erase operation. **GLOBAL_ERROR_COUNT** / **ERROR Status** 0 / No Error or Only 1 Error since the last Erase operation 1 / >1 Error Count since the last Erase operation PMIC counts the error since the last Erase operation, and if there are more than one error occurring, it sets this bit to '1'.
b6	GLOBAL_ERR_ LOG_BULK_ OVUV	ROE	Global Error Log History for Buck Regulator Output Over Voltage or Under Voltage. **GLOBAL_ERR_LOG_BULK_OVUV** / **ERROR Status** 0 / No error occurred 1 / Error occurred PMIC sets this bit when the error occurs.
b5	GLOBAL_ERR_ LOG_VIN_ BULK_OV	ROE	Global Error Log History for VIN_BULK Over Voltage. **GLOBAL_ERR_LOG_VIN_BULK_OV** / **ERROR Status** 0 / No error occurred 1 / Error occurred PMIC sets this bit when the error occurs.
b4	GLOBAL_ERR_ LOG_OTP	ROE	Global Error Critical Temperature. **GLOBAL_ERR_LOG_OTP** / **ERROR Status** 0 / No error occurred 1 / Error occurred PMIC sets this bit when the error occurs.
b3 ~ b0	Reserved	RV	Reserved

The PMIC always attempts to write this register into its non-volatile memory. However, it may not be guaranteed that depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 5.0V for VIN_BULK voltage and up to 200ms duration from the CAMP signal de-asserted to guarantee the Write operation into non-volatile memory.

Host must explicitly perform Erase operation to erase this entire register R04[7:0] via R39. PMIC needs minimum of 200ms for Erase operation.

Table 76. R05

Address: 05H
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7	Reserved	RV	Reserved
b6	SWA_POWER_GOOD	ROE	SWA condition from the previous power cycle. **SWA_POWER_GOOD** / **SWA Status** 0 / Normal 1 / Failed This register bit is set only if PMIC generates internal VR Disable command due to fault condition.
b5	SWB_POWER_GOOD	ROE	SWB condition from the previous power cycle. Only applicable if R4F[0]='0'. **SWB_POWER_GOOD** / **SWB Status** 0 / Normal 1 / Failed This register bit is set only if PMIC generates internal VR Disable command due to fault condition.
b4	SWC_POWER_GOOD	ROE	SWC condition from the previous power cycle. **SWC_POWER_GOOD** / **SWC Status** 0 / Normal 1 / Failed This register bit is set only if PMIC generates internal VR Disable command due to fault condition.
b3	SWD_POWER_GOOD	ROE	SWD condition from the previous power cycle. **SWD_POWER_GOOD** / **SWD Status** 0 / Normal 1 / Failed This register bit is set only if PMIC generates internal VR Disable command due to fault condition.
b2 ~ b0	PMIC_ERROR_LOG	ROE	High level status bits to indicate PMIC condition from the last known power cycle or system reset. **Status** / **Status** 000 / Normal Power On Reset — 100 / VIN_BULK Input OV 001 / Reserved — 101 / Reserved 010 / Buck Regulator Output OV or UV — 110 / Reserved 011 / Critical Temperature — 111 / Reserved The code 3'b010 is a logical OR function of Register R06[7:0] bits.

The PMIC always attempts to write this register into its non-volatile memory. However, it may not be guaranteed that depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 5.0V for VIN_BULK voltage and 200ms duration from the CAMP signal to guarantee the write operation into non-volatile memory.

This entire register status reflects the previous power down of PMIC and is updated by PMIC on its own at each power down cycle if the update is needed. Because this register is updated only if there is an error, there is no NVM lifetime impact. This register is cleared when Host issues an Erase command to Register R39. PMIC needs minimum of 200ms for the Erase operation.

Table 77. R06 (Sheet 1 of 2)

Address: 06H
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7	SWA_UVLO	ROE	SWA under voltage lockout status. **SWA_UVLO** / **SWA Status** 0 – Normal Power On 1 – SWA Under Voltage Lockout
b6	SWB_UVLO	ROE	SWB under voltage lockout status. Only applicable if R4F[0] = '0'. **SWB_UVLO** / **SWB Status** 0 – Normal Power On 1 – SWB Under Voltage Lockout
b5	SWC_UVLO	ROE	SWC under voltage lockout status. **SWC_UVLO** / **SWC Status** 0 – Normal Power On 1 – SWC Under Voltage Lockout
b4	SWD_UVLO	ROE	SWD under voltage lockout status. **SWD_UVLO** / **SWD Status** 0 – Normal Power On 1 – SWD Under Voltage Lockout
b3	SWA_OV	ROE	SWA over voltage status. **SWA_OV** / **SWA Status** 0 – Normal Power On 1 – SWA Over Voltage
b2	SWB_OV	ROE	SWB over voltage status. Only applicable if R4F[0] = '0'. **SWB_OV** / **SWB Status** 0 – Normal Power On 1 – SWB Over Voltage

Table 77. R06 (Sheet 2 of 2)

Address: 06H
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b1	SWC_OV	ROE	SWC over voltage status. **SWC_OV** / **SWC Status** 0 / Normal Power On 1 / SWC Over Voltage
b0	SWD_OV	ROE	SWD over voltage status. **SWD_OV** / **SWD Status** 0 / Normal Power On 1 / SWD Over Voltage

The PMIC always attempts to write this register into its non-volatile memory. However, it may not be guaranteed that depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 5.0 V for VIN_BULK voltage and up to 200ms duration from the CAMP signal de-asserted to guarantee the write operation into non-volatile memory.

This entire register status reflects the previous power down of PMIC and is updated by the PMIC at each power down cycle if the update is needed. Because this register is updated only if there is an error, there is no NVM lifetime impact. This register is cleared when Host issues an Erase command to Register R39. PMIC needs minimum of 200ms for the Erase operation.

Table 78. R08 (Sheet 1 of 2)

Address: 08H
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7	VIN_BULK_PG_STATUS	RO	VIN_BULK input power good status. **VIN_BULK_PG_STATUS** / **VIN_BULK Status** 0 / Power Good 1 / Power Not Good; VIN_BULK < VIN_BULK_PGL_th (R1A[7:5])
b6	OT_SD_STATUS	RO	Critical Temperature Shutdown status. **OT_SD_STATUS** / **PMIC Temperature Status** 0 / No Critical Temperature Shutdown 1 / Critical Temperature shutdown; PMIC temperature > OTP_th (R2E[2:0])

Table 78. R08 (Sheet 2 of 2)

Address: 08H
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b5	SWA_PG_STATUS	RO	SWA output power good status. **SWA_PG_STATUS** / **SWA Status** 0 / Power Good 1 / Power Not Good; SWA < SWA_PGL_th (R21[0]) or SWA > SWA_PGH_th (R22[7:6])
b4	SWB_PG_STATUS	RO	SWB output power good status. Only applicable if R4F[0] = '0'. **SWB_PG_STATUS** / **SWB Status** 0 / Power Good 1 / Power Not Good; SWB < SWB_PGL_th (R23[0]) or SWB > SWB_PGH_th (R24[7:6])
b3	SWC_PG_STATUS	RO	SWC output power good status. **SWC_PG_STATUS** / **SWC Status** 0 / Power Good 1 / Power Not Good SWC < SWC_PGL_th (R25[0]) or SWC > SWC_PGH_th (R26[7:6])
b2	SWD_PG_STATUS	RO	SWD output power good status. **SWD_PG_STATUS** / **SWD Status** 0 / Power Good 1 / Power Not Good; SWD < SWD_PGL_th (R27[0]) or SWD > SWD_PGH_th (R28[7:6])
b1	VIN_MGMT_OV_STATUS	RO	VIN_MGMT input over voltage status. **VIN_MGMT_OV_STATUS** / **VIN_MGMT Status** 0 / No Over Voltage 1 / Over Voltage; VIN_MGMT > VIN_MGMT_OV_th (R1B[5])
b0	VIN_BULK_OV_STATUS	RO	VIN_BULK input over voltage status. **VIN_BULK_OV_STATUS** / **VIN_BULK Status** 0 / No Over Voltage 1 / Over Voltage; VIN_BULK > VIN_BULK_OV_th (R1B[7])

Table 79. R09 (Sheet 1 of 2)

Address: 09H
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7	OTW_STATUS	RO	PMIC High Temperature Warning Status. **OTW_STATUS** / **PMIC Temperature Status** 0 – Temperature Below the Warning Threshold 1 – Temperature exceeds the Warning Threshold; PMIC temperature > OTWARN_th (R1B[2:0])
b6	VBIAS_PG_ STATUS	RO	VBIAS input power good status. **VBIAS_PG_STATUS** / **VBIAS Status** 0 – Power Good 1 – Power Not Good; VBIAS < VBIAS_PG_th (R1A[3])
b5	LDO1P8_PG_ STATUS	RO	VLDO_1.8V LDO output power good status. **LDO1P8_PG_STATUS** / **LDO1P8 Status** 0 – Power Good 1 – Power Not Good; LDO1P8 < LDO1P8_PG_th (R1A[2])
b4	SWOVER_ STATUS	RO	VIN_MGMT to VIN_BULK input supply automatic switchover status. **SWOVER_STATUS** / **Switchover Status** 0 – VIN_MGMT Input Supply is Present (Using VIN_MGMT Input Supply) 1 – VIN_MGMT Input Supply is Removed; VIN_MGMT < SWOVER_th (R2F[7]) (Using VIN_BULK Input Supply)
b3	SWA_CONSUM _WARNING _STATUS	RO	SWA High Output Current Consumption Warning Status. **SWA_CONSUM_WARNING_ STATUS** / **SWA Current Status** 0 – No High Current Consumption Warning 1 – High Current Consumption Warning; SWA current > SWA_CONSUM_WARNING_th (R1C[7:2])

Table 79. R09 (Sheet 2 of 2)

Address: 09H
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b2	SWB_CONSUM_WARNING_STATUS	RO	SWB High Output Current Consumption Warning Status. If R4F[0] = '1', the setting in R1D[7:2] must be identical to R1C[7:2]. **SWB_CONSUM_WARNING_STATUS** / **SWB Current Status** 0 / No High Current Consumption Warning 1 / High Current Consumption Warning; SWB current > SWB_CONSUM_WARNING_th (R1D[7:2])
b1	SWC_CONSUM_WARNING_STATUS	RO	SWC High Output Current Consumption Warning Status. **SWC_CONSUM_WARNING_STATUS** / **SWC Current Status** 0 / No High Current Consumption Warning 1 / High Current Consumption Warning; SWC current > SWC_CONSUM_WARNING_th (R1E[7:2])
b0	SWD_CONSUM_WARNING_STATUS	RO	SWD High Output Current Consumption Warning Status. **SWD_CONSUM_WARNING_STATUS** / **SWD Current Status** 0 / No High Current Consumption Warning 1 / High Current Consumption Warning; SWD current > SWD_CONSUM_WARNING_th (R1F[7:2])

Table 80. R0A (Sheet 1 of 3)

Address: 0AH
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7	SWA_OV_STATUS	RO	SWA output over voltage status. **SWA_OV_STATUS** / **SWA Status** 0 / No Over Voltage 1 / Over Voltage; SWA > SWA_OV_th (R22[5:4])

Table 80. R0A (Sheet 2 of 3)

Address: 0AH
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b6	SWB_OV_STATUS	RO	SWB output over voltage status. Only applicable if R4F[0] = '0'. This register is set when SWB output voltage goes above the threshold setting in R24[5:4]. If R4F[0] = '1', the setting in R24[5:4] must be identical as R22 [5:4]. **SWB_OV_STATUS** / **SWB Status** 0 / No Over Voltage 1 / Over Voltage; SWB > SWB_OV_th (R24[5:4])
b5	SWC_OV_STATUS	RO	SWC output over voltage status. **SWC_OV_STATUS** / **SWC Status** 0 / No Over Voltage 1 / Over Voltage; SWC > SWC_OV_th (R26[5:4])
b4	SWD_OV_STATUS	RO	SWD output over voltage status. **SWD_OV_STATUS** / **SWD Status** 0 / No Over Voltage 1 / Over Voltage; SWD > SWD_OV_th (R28[5:4])
b3	PEC_ERROR_STATUS	RO	Packet Error Code Status. **PEC_ERROR_STATUS** / **Packet Error Code Status** 0 / No PEC Error 1 / PEC Error Applicable in I3C Basic Mode only and if enabled in R34[7]. This register is updated when the PMIC device goes through bus reset.
b2	PARITY_ERR_STATUS	RO	T Bit Parity Error Status. **PARITY_ERR_STATUS** / **T Bit Parity Error Status** 0 / No PEC Error 1 / Parity Error Applicable in I3C Basic Mode only and if enabled in R34[5]. Also applicable in I^2C mode for supported CCC. This register is updated when the PMIC device goes through bus reset.

Table 80. R0A (Sheet 3 of 3)

Address: 0AH
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b1	IBI_STATUS	RO	In-Band Interrupt (IBI) Status. IBI_STATUS: 0 = No Pending IBI; 1 = Pending IBI This register can be used as Global Status in addition to IBI status.
b0	Reserved	RV	Reserved

Table 81. R0B (Sheet 1 of 2)

Address: 0BH
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7	SWA_OCW_STATUS	RO	SWA output current limiter warning status. SWA_OCW_STATUS: 0 = No Current Limiter Event; 1 = Current Limiter Event; SWA current > SWA_OCW_th (R20[7:6])
b6	SWB_OCW_STATUS	RO	SWB output current limiter warning status. This register is applicable regardless of the setting R4F[0]. This register is set when SWB output current goes above the threshold setting in R20[5:4]. If R4F[0] = '1', the setting in R20[5:4] must be identical as R20[7:6]. SWB_OCW_STATUS: 0 = No Current Limiter Event; 1 = Current Limiter Event; SWB current > SWB_OCW_th (R20[5:4])
b5	SWC_OCW_STATUS	RO	SWC output current limiter warning status. SWC_OCW_STATUS: 0 = No Current Limiter Event; 1 = Current Limiter Event; SWC current > SWC_OCW_th (R20[3:2])
b4	SWD_OCW_STATUS	RO	SWD output current limiter warning status. SWD_OCW_STATUS: 0 = No Current Limiter Event; 1 = Current Limiter Event; SWD current > SWD_OCW_th (R20[1:0])

Table 81. R0B (Sheet 2 of 2)

Address: 0BH
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b3	SWA_UVLO_STATUS	RO	SWA output under voltage lockout status. **SWA_UVLO_STATUS** / **SWA Status** 0 / No Under Voltage Lockout 1 / Under Voltage Lockout; SWA < SWA_UV_th (R22[3:2])
b2	SWB_UVLO_STATUS	RO	SWB output under voltage lockout status. Only applicable if R4F[0] = '0'. If R4F[0] = '1', the setting in R24[3:2] must be identical as R22[3:2]. **SWB_UVLO_STATUS** / **SWB Status** 0 / No Under Voltage Lockout 1 / Under Voltage Lockout; SWB < SWB_UV_th (R24[3:2])
b1	SWC_UVLO_STATUS	RO	SWC output under voltage lockout status. **SWC_UVLO_STATUS** / **SWC Status** 0 / No Under Voltage Lockout 1 / Under Voltage Lockout; SWC < SWC_UV_th (R26[3:2])
b0	SWD_UVLO_STATUS	RO	SWD output under voltage lockout status. **SWD_UVLO_STATUS** / **SWD Status** 0 / No Under Voltage Lockout 1 / Under Voltage Lockout; SWD < SWD_UV_th (R28[3:2])

Table 82. R0C

Address: 0CH
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7 ~ b0	SWA_CURRENT_POWER_MEASUREMENT	RO	SWA output current/power measurement. If R1B[6]='0', the PMIC reports current measurement. If R1B[6]='1', the PMIC reports power measurement. If R4F[0]='1', the host adds the current or power reported in R0C[7:0] and R0D[5:0] for total current or power consumption of SWAB.

R1A[1]=0, SWA Current/Power Measurement

SWA_CURRENT_POWER_MEASUREMENT	SWA Current/Power Value	SWA_CURRENT_POWER_MEASUREMENT	SWA Current/Power Value
0000 0000	Undefined	0010 0000	4.0A or 4000mW
0000 0001	0.125A or 125mW	0010 0001	4.125A or 4125mW
0000 0010	0.25A or 250mW	0010 0010	4.25A or 4250mW
0000 0011	0.375A or 375mW	0010 0011	4.375A or 4375mW
0000 0100	0.5A or 500mW	0010 0100	4.5A or 4500mW
0000 0101	0.625A or 625mW	0010 0101	4.625A or 4625mW
0000 0110	0.75A or 750mW	0010 0110	4.75A or 4750mW
0000 0111	0.875A or 875mW	0010 0111	4.875A or 4875mW
0000 1000	1.0A or 1000mW	0010 1000	5.0A or 5000mW
0000 1001	1.125A or 1125mW	0010 1001	5.125A or 5125mW
0000 1010	1.25A or 1250mW	0010 1010	5.25A or 5250mW
0000 1011	1.375A or 1375mW	0010 1011	5.375A or 5375mW
0000 1100	1.5A or 1500mW	0010 1100	5.5A or 5500mW
0000 1101	1.625A or 1625mW	0010 1101	5.625A or 5625mW
0000 1110	1.75A or 1750mW	0010 1110	5.75A or 5750mW
0000 1111	1.875A or 1875mW	0010 1111	5.875A or 5875mW
0001 0000	2.0A or 2000mW	0011 0000	6.0A or 6000mW
0001 0001	2.125A or 2125mW	0011 0001	6.125A or 6125mW
0001 0010	2.25A or 2250mW	0011 0010	6.25A or 6250mW
0001 0011	2.375A or 2375mW	0011 0011	6.375A or 6375mW
0001 0100	2.5A or 2500mW	0011 0100	6.5A or 6500mW
0001 0101	2.625A or 2625mW	0011 0101	6.625A or 6625mW
0001 0110	2.75A or 2750mW	0011 0110	6.75A or 6750mW
0001 0111	2.875A or 2875mW	0011 0111	6.875A or 6875mW
0001 1000	3.0A or 3000mW	0011 1000	7.0A or 7000mW
0001 1001	3.125A or 3125mW	0011 1001	7.125A or 7125mW
0001 1010	3.25A or 3250mW	0011 1010	7.25A or 7250mW
0001 1011	3.375A or 3375mW	0011 1011	7.375A or 7375mW
0001 1100	3.5A or 3500mW	0011 1100	7.5A or 7500mW
0001 1101	3.625A or 3625mW	0011 1101	7.625A or 7625mW
0001 1110	3.75A or 3750mW	0011 1110	7.75A or 7750mW
0001 1111	3.875A or 3875mW	0011 1111	≥7.875A or 7875mW

R1A[1]=1, Sum of power measurement for SWA/B/C/D.
(R1B[6] must be configured as '1'.)

0000 0000 = Undefined
0000 0001 = 125mW
0000 0010 = 250mW
0000 0011 = 375mW
0000 0100 = 500mW
...
1111 1100 = 31500mW
1111 1101 = 31625mW
1111 1110 = 31750mW
1111 1111 ≥ 31875mW

Sum of power measurement for SWA/B/C/D = R0C[7:0] * 125 mW. (R0C[7:0]='0': Undefined)

PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers the VR Disable command on its own, PMIC does not report current or power measurement. For all other events that causes PMIC's power good status as Not Good, PMIC continues to provide current or power measurement.

Table 83. R0D

Address: 0DH
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7 ~ b6	Reserved	RV	Reserved
b5 ~ b0	SWB_CURRENT_POWER_MEASUREMENT	RO	SWB output current/power measurement. If R1B[6]='0', PMIC reports current measurement. If R1B[6]='1', PMIC reports power measurement. If R4F[0]='1', Host adds the current or power reported in R0C[7:0] and R0D[5:0] for total current or power consumption of SWAB.

SWB_CURRENT_POWER_MEASUREMENT	SWB Current/Power Value	SWB_CURRENT_POWER_MEASUREMENT	SWB Current/Power Value
000000	Undefined	100000	4.0A or 4000mW
000001	0.125A or 125mW	100001	4.125A or 4125mW
000010	0.25A or 250mW	100010	4.25A or 4250mW
000011	0.375A or 375mW	100011	4.375A or 4375mW
000100	0.5A or 500mW	100100	4.5A or 4500mW
000101	0.625A or 625mW	100101	4.625A or 4625mW
000110	0.75A or 750mW	100110	4.75A or 4750mW
000111	0.875A or 875mW	100111	4.875A or 4875mW
001000	1.0A or 1000mW	101000	5.0A or 5000mW
001001	1.125A or 1125mW	101001	5.125A or 5125mW
001010	1.25A or 1250mW	101010	5.25A or 5250mW
001011	1.375A or 1375mW	101011	5.375A or 5375mW
001100	1.5A or 1500mW	101100	5.5A or 5500mW
001101	1.625A or 1625mW	101101	5.625A or 5625mW
001110	1.75A or 1750mW	101110	5.75A or 5750mW
001111	1.875A or 1875mW	101111	5.875A or 5875mW
010000	2.0A or 2000mW	110000	6.0A or 6000mW
010001	2.125A or 2125mW	110001	6.125A or 6125mW
010010	2.25A or 2250mW	110010	6.25A or 6250mW
010011	2.375A or 2375mW	110011	6.375A or 6375mW
010100	2.5A or 2500mW	110100	6.5A or 6500mW
010101	2.625A or 2625mW	110101	6.625A or 6625mW
010110	2.75A or 2750mW	110110	6.75A or 6750mW
010111	2.875A or 2875mW	110111	6.875A or 6875mW
011000	3.0A or 3000mW	111000	7.0A or 7000mW
011001	3.125A or 3125mW	111001	7.125A or 7125mW
011010	3.25A or 3250mW	111010	7.25A or 7250mW
011011	3.375A or 3375mW	111011	7.375A or 7375mW
011100	3.5A or 3500mW	111100	7.5A or 7500mW
011101	3.625A or 3625mW	111101	7.625A or 7625mW
011110	3.75A or 3750mW	111110	7.75A or 7750mW
011111	3.875A or 3875mW	111111	≥7.875A or 7875mW

PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers the VR Disable command on its own, PMIC does not report current or power measurement. For all other events that causes PMIC's power good status as Not Good, PMIC continues to provide current or power measurement.

Table 84. R0E

Address: 0EH
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7 ~ b6	Reserved	RV	Reserved
b5 ~ b0	**SWC_CURRENT_POWER_MEASUREMENT**	**RO**	SWC output current/power measurement. If R1B[6] = '0', PMIC reports current measurement. If R1B[6] = '1', PMIC reports power measurement.

SWC_CURRENT_POWER_MEASUREMENT	SWC Current/Power Value	SWC_CURRENT_POWER_MEASUREMENT	SWC Current/Power Value
000000	Undefined	100000	4.0A or 4000mW
000001	0.125A or 125mW	100001	4.125A or 4125mW
000010	0.25A or 250mW	100010	4.25A or 4250mW
000011	0.375A or 375mW	100011	4.375A or 4375mW
000100	0.5A or 500mW	100100	4.5A or 4500mW
000101	0.625A or 625mW	100101	4.625A or 4625mW
000110	0.75A or 750mW	100110	4.75A or 4750mW
000111	0.875A or 875mW	100111	4.875A or 4875mW
001000	1.0A or 1000mW	101000	5.0A or 5000mW
001001	1.125A or 1125mW	101001	5.125A or 5125mW
001010	1.25A or 1250mW	101010	5.25A or 5250mW
001011	1.375A or 1375mW	101011	5.375A or 5375mW
001100	1.5A or 1500mW	101100	5.5A or 5500mW
001101	1.625A or 1625mW	101101	5.625A or 5625mW
001110	1.75A or 1750mW	101110	5.75A or 5750mW
001111	1.875A or 1875mW	101111	5.875A or 5875mW
010000	2.0A or 2000mW	110000	6.0A or 6000mW
010001	2.125A or 2125mW	110001	6.125A or 6125mW
010010	2.25A or 2250mW	110010	6.25A or 6250mW
010011	2.375A or 2375mW	110011	6.375A or 6375mW
010100	2.5A or 2500mW	110100	6.5A or 6500mW
010101	2.625A or 2625mW	110101	6.625A or 6625mW
010110	2.75A or 2750mW	110110	6.75A or 6750mW
010111	2.875A or 2875mW	110111	6.875A or 6875mW
011000	3.0A or 3000mW	111000	7.0A or 7000mW
011001	3.125A or 3125mW	111001	7.125A or 7125mW
011010	3.25A or 3250mW	111010	7.25A or 7250mW
011011	3.375A or 3375mW	111011	7.375A or 7375mW
011100	3.5A or 3500mW	111100	7.5A or 7500mW
011101	3.625A or 3625mW	111101	7.625A or 7625mW
011110	3.75A or 3750mW	111110	7.75A or 7750mW
011111	3.875A or 3875mW	111111	≥7.875A or 7875mW

PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers the VR Disable command on its own, PMIC does not report current or power measurement. For all other events that causes PMIC's power good status as Not Good, PMIC continues to provide current or power measurement.

Table 85. R0F

Address: 0FH
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7 ~ b6	Reserved	RV	Reserved
b5 ~ b0	SWC_CURRENT_POWER_MEASUREMENT	RO	SWD output current/power measurement. If R1B[6]='0', the PMIC reports current measurement. If R1B[6]='1', the PMIC reports power measurement.

SWD_CURRENT_POWER_MEASUREMENT	SWD Current/Power Value	SWD_CURRENT_POWER_MEASUREMENT	SWD Current/Power Value
000000	Undefined	100000	4.0A or 4000mW
000001	0.125A or 125mW	100001	4.125A or 4125mW
000010	0.25A or 250mW	100010	4.25A or 4250mW
000011	0.375A or 375mW	100011	4.375A or 4375mW
000100	0.5A or 500mW	100100	4.5A or 4500mW
000101	0.625A or 625mW	100101	4.625A or 4625mW
000110	0.75A or 750mW	100110	4.75A or 4750mW
000111	0.875A or 875mW	100111	4.875A or 4875mW
001000	1.0A or 1000mW	101000	5.0A or 5000mW
001001	1.125A or 1125mW	101001	5.125A or 5125mW
001010	1.25A or 1250mW	101010	5.25A or 5250mW
001011	1.375A or 1375mW	101011	5.375A or 5375mW
001100	1.5A or 1500mW	101100	5.5A or 5500mW
001101	1.625A or 1625mW	101101	5.625A or 5625mW
001110	1.75A or 1750mW	101110	5.75A or 5750mW
001111	1.875A or 1875mW	101111	5.875A or 5875mW
010000	2.0A or 2000mW	110000	6.0A or 6000mW
010001	2.125A or 2125mW	110001	6.125A or 6125mW
010010	2.25A or 2250mW	110010	6.25A or 6250mW
010011	2.375A or 2375mW	110011	6.375A or 6375mW
010100	2.5A or 2500mW	110100	6.5A or 6500mW
010101	2.625A or 2625mW	110101	6.625A or 6625mW
010110	2.75A or 2750mW	110110	6.75A or 6750mW
010111	2.875A or 2875mW	110111	6.875A or 6875mW
011000	3.0A or 3000mW	111000	7.0A or 7000mW
011001	3.125A or 3125mW	111001	7.125A or 7125mW
011010	3.25A or 3250mW	111010	7.25A or 7250mW
011011	3.375A or 3375mW	111011	7.375A or 7375mW
011100	3.5A or 3500mW	111100	7.5A or 7500mW
011101	3.625A or 3625mW	111101	7.625A or 7625mW
011110	3.75A or 3750mW	111110	7.75A or 7750mW
011111	3.875A or 3875mW	111111	≥7.875A or 7875mW

PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers the VR Disable command on its own, PMIC does not report current or power measurement. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

4.6.2 Clear Registers

For all other events that causes PMIC's power good status as Not Good for each Real Time Status Registers (R08[7:0], R09[7:0], R0A[7:1], R0B[7:0] and R33[4:2]), the PMIC offers a way to clear the status of each event. The clear registers are R10[7,5:0], R11[7:0], R12[7:2], R13[7:0] and R14[4:2,0] respectively. All clear registers are Write '1' only registers. When '1' is written to any of the clear registers, the PMIC updates the status registers to default state and removes the interrupt condition on GSI_n and CAMP output signal assuming that event is no longer present. If the failing condition is still present, the status register will still remain at '1'. Note that GSI_n and CAMP interrupt is only applicable if that event is not masked. GSI_n output signal can be disabled.

The PMIC offers a Global Clear command by writing '1' to Register R14[0]. This command works same way as individual clear command. This command can alternatively be used by the host if more than one clear command is required to different registers.

Table 86. R10

Address: 10H **Default: 00000000B**			
Data Bit	**Data Name**	**Attribute**	**Function Description[1]**
b7	CLR_VIN_BULK_PG	W1O	Clear VIN_BULK input power good status. 1 = Clear R08[7].[2]
b6	Reserved	RV	Reserved
b5	CLR_SWA_PG_STATUS	W1O	Clear SWA output power good status. 1 = Clear R08[5].[2]
b4	CLR_SWB_PG_STATUS	W1O	Clear SWB output power good status. Only applicable if R4F[0]='0'. 1 = Clear R08[4].[2]
b3	CLR_SWC_PG_STATUS	W1O	Clear SWC output power good status. 1 = Clear R08[3].[2]
b2	CLR_SWD_PG_STATUS	W1O	Clear SWD output power good status. 1 = Clear R08[2].[2]
b1	CLR_VIN_MGMT_OV	W1O	Clear VIN_MGMT input supply over voltage status. 1 = Clear R08[1].[2]
b0	CLR_VIN_BULK_OV	W1O	Clear VIN_BULK input supply over voltage status. Set 1 to clear R08[0].

1. R10[7:0] are self clearing bits.
2. See Table 7 and Table 8 for GSI_n and CAMP output signal status change.

Table 87. R11

Address: 11H Default: 00000000B			
Data Bit	**Data Name**	**Attribute**	**Function Description[1]**
b7	CLR_OTW_STATUS	W1O	Clear PMIC High Temperature Warning Status. 1 = Clear R09[7].[2]
b6	CLR_VBIAS_PG_STATUS	W1O	Clear VBIAS power good status. 1 = Clear R09[6].[2]
b5	CLR_LDO1P8_PG_STATUS	W1O	Clear VLDO_1.8V LDO output power good status. 1 = Clear R08[5].[2]
b4	CLR_SWOVER_STATUS	W1O	Clear VIN_MGMT to VIN_BULK Input Supply Switchover Status. 1 = Clear R09[4].[2]
b3	CLR_SWA_CONSUM	W1O	Clear SWA High Output Current Consumption Warning Status. 1 = Clear R09[3].[2]
b2	CLR_SWB_CONSUM	W1O	Clear SWB High Output Current Consumption Warning Status. This register is applicable regardless of the setting in R4F[0]. 1 = Clear R09[2].[2]
b1	CLR_SWC_CONSUM	W1O	Clear SWC High Output Current Consumption Warning Status. 1 = Clear R09[1].[2]
b0	CLR_SWD_CONSUM	W1O	Clear SWD High Output Current Consumption Warning Status. 1 = Clear R09[0].[2]

1. R11[7:0] are self clearing bits.
2. See Table 7 and Table 8 for GSI_n and CAMP output signal status change.

Table 88. R12

Address: 12H Default: 00000000B			
Data Bit	**Data Name**	**Attribute**	**Function Description[1]**
b7	CLR_SWA_OV_STATUS	W1O	Clear SWA output over voltage status. 1 = Clear R0A[7].[2]
b6	CLR_SWB_OV_STATUS	W1O	Clear SWB output over voltage status. Only applicable if R4F[0]='0'. 1 = Clear R0A[6].[2]
b5	CLR_SWC_OV_STATUS	W1O	Clear SWC output over voltage status. 1 = Clear R0A[5].[2]
b4	CLR_SWD_OV_STATUS	W1O	Clear SWD output over voltage status. 1 = Clear R0A[4].[2]
b3	CLR_PEC_ERROR	W1O	Clear Packet Error Code Status. 1 = Clear R0A[3].[2]
b2	CLR_PARITY_ERROR	W1O	Clear T Bit Parity Error Status. 1 = Clear R0A[2].[2]
b1 ~ b0	Reserved	RV	Reserved.

1. R12[7:0] are self clearing bits.
2. See Table 7 and Table 8 for GSI_n and CAMP output signal status change.

Table 89. R13

Address: 13H **Default: 00000000B**			
Data Bit	**Data Name**	**Attribute**	**Function Description[1]**
b7	CLR_SWA_OCW_STATUS	W1O	Clear SWA output current limiter warning status. 1 = Clear R0B[7].[2]
b6	CLR_SWB_OCW_STATUS	W1O	Clear SWB output current limiter warning status. This register is applicable regardless of the setting in R4F[0]. 1 = Clear R0B[6].[2]
b5	CLR_SWC_OCW_STATUS	W1O	Clear SWC output current limiter warning status. 1 = Clear R0B[5].[2]
b4	CLR_SWD_OCW_STATUS	W1O	Clear SWD output current limiter warning status. 1 = Clear R0B[4].[2]
b3	CLR_SWA_UVLO_STATUS	W1O	Clear SWA under voltage lockout status. 1 = Clear R0B[3].[2]
b2	CLR_SWB_UVLO_STATUS	W1O	Clear SWB under voltage lockout status. Only applicable if R4F[0]='0'. 1 = Clear R0B[2].[2]
b1	CLR_SWC_UVLO_STATUS	W1O	Clear SWC under voltage lockout status. 1 = Clear R0B[1].[2]
b0	CLR_SWD_UVLO_STATUS	W1O	Clear SWD under voltage lockout status. 1 = Clear R0B[0].[2]

1. R13[7:0] are self clearing bits.
2. See Table 7 and Table 8 for GSI_n and CAMP output signal status change.

Table 90. R14

Address: 14H **Default: 00000000B**			
Data Bit	**Data Name**	**Attribute**	**Function Description[1]**
b7 ~ b5	Reserved	RV	Reserved.
b4	CLR_VIN_MGMT_PG_SWOVER_MODE	W1O	Clear valid VIN_MGMT power good status in switchover mode. 1 = Clear R33[4].[2]
b3	CLR_VBIAS_VIN_BULK_UVLO_STATUS	W1O	Clear VBIAS output or VIN_BULK input under-voltage lockout status. 1 = Clear R33[3].[2]
b2	CLR_LDO1P1_PG_STATUS	W1O	Clear VLDO_1.0V LDO output power good status. 1 = Clear R33[2].[2]
b1	Reserved	RV	Reserved.
b0	GLOBAL_CLEAR_STATUS	W1O	Clear all status bits. Self clearing bit. 1 = Clear all status bits in R10[7,5:0], R11, R12[7:2], R13, R14[4:2].[2]

1. R13[7:0] are self clearing bits.
2. See Table 7 and Table 8 for GSI_n and CAMP output signal status change.

4.6.3 Mask Registers

For each Real Time Status Registers (R08[7:0], R09[7:0], R0A[7:1], R0B[7:0], R33[4:2]), the PMIC offers a way to mask the status of each event interrupt. The mask registers are R15[7,5:0], R16[7:0], R17[7:2], R18[7:0] and R19[4:2] respectively. The mask registers only masks the event interrupt on GSI_n and CAMP signal.

There is also a global mask bits register control R2F[1:0] to control the GSI_n and CAMP output signal. When all mask registers are R15[7,5:0], R16[7:0], R17[7:2] and R18[7:0] configured as '0', the setting in R2F[1:0] does not matter. The setting in R2F[1:0] only matters when one or more mask registers R15[7,5:0], R16[7:0], R17[7:2], R18[7:0] are configured to '1'.

For any failure events that causes the PMIC to generate VR Disable command on its own, the mask register bits (R15[0], R17[7:4], R18[3:0], R19[3], R2F[1:0]) do not apply and PMIC will assert CAMP output signal regardless of the setting in mask registers. The PMIC still updates the status registers appropriately when any event occurs. When masked, the host is expected to read the status registers periodically to learn if any of the event has occurred or not. The host can mask or un-mask each event individually. The host can mask or un-mask at any time in Non-Write Protect mode. In Write Protect mode of operation, the mask registers are locked.

Table 91. R15 (Sheet 1 of 2)

Address: 15H Default: 10111100B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7	MSK_VIN_BULK_PG	RW	Mask VIN_BULK input power good status event. 0 – Do Not Mask VIN_BULK input power good status event. 1 – Mask VIN_BULK input power good status event.[1] 1. Not assert GSI_n or assert CAMP output signal.
b6	Reserved	RV	Reserved.
b5	MSK_SWA_PG_STATUS	RW	Mask SWA output power good status event. 0 – Do Not Mask SWA output power good status event. 1 – Mask SWA output power good status event.[1] 1. Not assert GSI_n or assert CAMP output signal.
b4	MSK_SWB_PG_STATUS	RW	Mask SWB output power good status event. Applicable only if R4F[0]='0'. 0 – Do Not Mask SWB output power good status event. 1 – Mask SWB output power good status event.[1] 1. Not assert GSI_n or assert CAMP output signal.
b3	MSK_SWC_PG_STATUS	RW	Mask SWC output power good status event. 0 – Do Not Mask SWC output power good status event. 1 – Mask SWC output power good status event.[1] 1. Not assert GSI_n or assert CAMP output signal.

Table 91. R15 (Sheet 2 of 2)

Address: 15H Default: 10111100B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b2	MSK_SWD_PG_STATUS	RW	Mask SWD output power good status event. 0 – Do Not Mask SWD output power good status event. 1 – Mask SWD output power good status event.[1] 1. Not assert GSI_n or assert CAMP output signal.
b1	MSK_VIN_MGMT_OV	RW	Mask VIN_MGMT input supply over voltage status event. 0 – Do Not Mask VIN_MGMT input supply over voltage status event. 1 – Mask VIN_MGMT input supply over voltage status even.[1] 1. Not assert GSI_n output signal.
b0	MSK_VIN_BULK_OV	RW	Mask VIN_BULK input supply over voltage status event. 0 – Do Not Mask VIN_BULK input supply over voltage status event. 1 – Mask VIN_BULK input supply over voltage status even.[1] 1. Not assert GSI_n output signal.

Table 92. R16 (Sheet 1 of 2)

Address: 16H Default: 00100000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7	MSK_OTW_STATUS	RW	Mask PMIC high temperature warning status event. 0 – Do Not Mask PMIC high temperature warning status event. 1 – Mask PMIC high temperature warning status event.[1] 1. Not assert GSI_n output signal.
b6	MSK_VBIAS_PG_ STATUS	RW	Mask VBIAS power good status event. 0 – Do Not Mask VBIAS power good status event;. 1 – Mask VBIAS power good status event.[1] 1. Not assert GSI_n or assert CAMP output signal.
b5	MSK_LDO1P8_PG_ STATUS	RW	Mask VLDO_1.8V LDO output power good status event. 0 – Do Not Mask 1.8V output power good status event. 1 – Mask 1.8V output power good status event.[1] 1. Not assert GSI_n or assert CAMP output signal.

Table 92. R16 (Sheet 2 of 2)

Address: 16H Default: 00100000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b4	MSK_SWOVER_STATUS	RW	Mask VIN_MGMT to VIN_BULK input supply switchover status event. 0: Do Not Mask VIN_MGMT to VIN_BULK input supply switchover status Event. 1: Mask VIN_MGMT to VIN_BULK input supply switchover status Event.[1] 1. Not assert GSI_n output signal.
b3	MSK_SWA_CONSUM	RW	Mask SWA high output current consumption warning status event. 0: Do Not Mask SWA output current consumption warning status event. 1: Mask SWA output current consumption warning status event.[1] 1. Not assert GSI_n output signal.
b2	MSK_SWB_CONSUM	RW	Mask SWB high output current consumption warning status event. This register is regardless of the setting in R4F[0]. 0: Do Not Mask SWB output current consumption warning status event. 1: Mask SW**A** output current consumption warning status event.[1] 1. Not assert GSI_n output signal.
b1	MSK_SWC_CONSUM	RW	Mask SWC high output current consumption warning status event. 0: Do Not Mask SWC output current consumption warning status event. 1: Mask SWC output current consumption warning status event.[1] 1. Not assert GSI_n output signal.
b0	MSK_SWD_CONSUM	RW	Mask SWD high output current consumption warning status event. 0: Do Not Mask SWD output current consumption warning status event. 1: Mask SWD output current consumption warning status event.[1] 1. Not assert GSI_n output signal.

Table 93. R17

Address: 17H Default: 00000000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7	MSK_SWA_OV_STATUS	RW	Mask SWA output over voltage status event. 0 – Do Not Mask SWA output over voltage status event. 1 – Mask SWA output over voltage status event.[1] 1. Not assert GSI_n output signal.
b6	MSK_SWB_OV_STATUS	RW	Mask SWB output over voltage status event. Only applicable if R4F[0]='0'. 0 – Do Not Mask SWB output over voltage status event. 1 – Mask SWB output over voltage status event.[1] 1. Not assert GSI_n output signal.
b5	MSK_SWC_OV_STATUS	RW	Mask SWC output over voltage status event. 0 – Do Not Mask SWC output over voltage status event. 1 – Mask SWC output over voltage status event.[1] 1. Not assert GSI_n output signal.
b4	MSK_SWD_OV_STATUS	RW	Mask SWD output over voltage status event. 0 – Do Not Mask SWD output over voltage status event. 1 – Mask SWD output over voltage status event.[1] 1. Not assert GSI_n output signal.
b3	MSK_PEC_ERROR	RW	Mask Packet Error Code Status event. Only applicable when PMIC is in I3C Basic Mode. This Mask register only masks the GSI_n output. Does not apply to IBI. 0 – Do Not Mask PEC error status event. 1 – Mask PEC error status.
b2	MSK_PARITY_ERROR	RW	Mask T Bit Parity Error Status event. Only applicable when PMIC is in I3C Basic Mode. This Mask register only masks the GSI_n output. Does not apply to IBI. 0 – Do Not Mask Parity error status event. 1 – Mask Parity error status.
b1 ~ b0	Reserved	RV	Reserved.

Table 94. R18 (Sheet 1 of 2)

Address: 18H Default: 00000000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7	MSK_SWA_OCW_STATUS	RW	Mask SWA output current limiter warning status event. 0 – Do Not Mask SWA output current limiter warning status event. 1 – Mask SWA output current limiter warning status event.[1] 1. Not assert GSI_n output signal.
b6	MSK_SWB_OCW_STATUS	RW	Mask SWB output current limiter warning status event. This register is regardless of the setting in R4F[0]. 0 – Do Not Mask SWB output current limiter warning status event. 1 – Mask SWB output current limiter warning status event.[1] 1. Not assert GSI_n output signal.
b5	MSK_SWC_OCW_STATUS	RW	Mask SWC output current limiter warning status event. 0 – Do Not Mask SWC output current limiter warning status event. 1 – Mask SWC output current limiter warning status event.[1] 1. Not assert GSI_n output signal.
b4	MSK_SWD_OCW_STATUS	RW	Mask SWD output current limiter warning status event. 0 – Do Not Mask SWD output current limiter warning status event. 1 – Mask SWD output current limiter warning status event.[1] 1. Not assert GSI_n output signal.
b3	MSK_SWA_UVLO_STATUS	RW	Mask SWA under voltage lockout status event. 0 – Do Not Mask SWA output under voltage lockout status event. 1 – Mask SWA output under voltage lockout status event.[1] 1. Not assert GSI_n output signal.
b2	MSK_SWB_UVLO_STATUS	RW	Mask SWA under voltage lockout status event. 0 – Do Not Mask SWB output under voltage lockout status event. 1 – Mask SWB output under voltage lockout status event.[1] 1. Not assert GSI_n output signal.
b1	MSK_SWC_UVLO_STATUS	RV	Mask SWC under voltage lockout status event. 0 – Do Not Mask SWC output under voltage lockout status event. 1 – Mask SWC output under voltage lockout status event.[1] 1. Not assert GSI_n output signal.

Table 94. R18 (Sheet 2 of 2)

Address: 18H Default: 00000000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b0	MSK_SWD_UVLO_STATUS	RV	Mask SWD under voltage lockout status event. 0 – Do Not Mask SWD output under voltage lockout status event. 1 – Mask SWD output under voltage lockout status event.[1] 1. Not assert GSI_n output signal.

Table 95. R19

Address: 19H Default: 00000100B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b5	Reserved	RV	Reserved.
b4	MSK_VIN_MGMT_PG_SWOVER_MODE	RW	Mask VIN_MGMT input supply Power Good status in Switchover Mode only. 0 – Do Not Mask VIN_MGMT input power supply power good status event in switchover mode. 1 – Mask VIN_MGMT input power supply power good status event in switchover mode.[1] 1. Not assert GSI_n output signal.
b3	MSK_VBIAS_UVLO_STATUS	RW	Mask VBIAS output or VIN_BULK input Under-Voltage Lockout event. 0 – Do Not Mask VBIAS output or VIN_BULK input under voltage lockout event. 1 – Mask VBIAS output or VIN_BULK input under voltage lockout event.[1] 1. Not assert GSI_n output signal.
b2	MSK_LDO1P1_PG_STATUS	RW	Mask VLDO_1.0V LDO output power good status event. 0 – Do Not Mask VOUT_1.0V output power good status event. 1 – Mask VOUT_1.0V output power good status event.[1] 1. Not assert GSI_n or assert CAMP output signal.
b1 ~ b0	Reserved	RV	Reserved.

4.6.4 Threshold & Configuration Registers

Table 96. R1A

<table>
<tr><td colspan="4">Address: 1AH
Default: 11000000B</td></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b7 ~ b5</td><td>VIN_BULK_PGL_SET</td><td>RW</td><td>VIN_BULK Input Threshold Voltage for Input Power Good Status for falling input supply.
<table>
<tr><th>VIN_BULK_PGL_SET</th><th>VIN_BULK_PGL_th</th><th>VIN_BULK_PGL_SET</th><th>VIN_BULK_PGL_th</th></tr>
<tr><td>000</td><td>Reserved</td><td>100</td><td>6.5V</td></tr>
<tr><td>001</td><td>9.5V</td><td>101</td><td>5.5V</td></tr>
<tr><td>010</td><td>8.5V</td><td>110</td><td>4.25V</td></tr>
<tr><td>011</td><td>7.5V</td><td>111</td><td>Reserved</td></tr>
</table>
If VIN_BULK input falls below 4.25 V, the PMIC may not guarantee the operation.
If VIN_BULK voltage continues to fall below 4.1 V, the PMIC will trigger an internal VR disable and go through the preset power down sequence. This sequence is programmed in according to Config 0 to Config 3 registers.</td></tr>
<tr><td>b4</td><td>Reserved</td><td>RV</td><td>Reserved.</td></tr>
<tr><td>b3</td><td>VBIAS_PG_SET</td><td>RW</td><td>VBIAS LDO Output Threshold Voltage for Power Good Status.
<table>
<tr><th>VBIAS_PG_SET</th><th>VBIAS_PG_th</th></tr>
<tr><td>0</td><td>2.6 V</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>b2</td><td>LDO1P8_PG_SET</td><td>RW</td><td>VLDO_1.8 V LDO Output Threshold Voltage for Power Good Status.
<table>
<tr><th>LDO1P8_PG_SET</th><th>LDO1P8_PG_th</th></tr>
<tr><td>0</td><td>1.6 V</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>b1</td><td>PWR_MEAS_FORMAT</td><td>RW</td><td>PMIC Switch Regulator Output Power Select - Individual or All switching rails. Only applicable if R1B[6]=’1’.
<table>
<tr><th>PWR_MEAS_FORMAT</th><th>R0C[7:0] Power Measurement Report</th></tr>
<tr><td>0</td><td>Report individual power for rail using R0C, R0D, R0E and R0F</td></tr>
<tr><td>1</td><td>Report total power of each rail using R0C</td></tr>
</table></td></tr>
<tr><td>b0</td><td>LDO1P0_PG_SET</td><td>RW</td><td>VLDO_1.0V LDO Output Threshold Voltage for Power Good Status.
<table>
<tr><th>LDO1P0_PG_SET</th><th>LDO1P0_PG_th</th></tr>
<tr><td>0</td><td>-10% from the setting in R51[2:1]</td></tr>
<tr><td>1</td><td>-15% from the setting in R51[2:1]</td></tr>
</table></td></tr>
</table>

Table 97. R1B

Address: 1BH
Default: 00000101B

Data Bit	Data Name	Attribute	Function Description
b7	VIN_BULK_OV_SET	RW	VIN_BULK Input Over Voltage Threshold Setting For GSI_n Assertion. **VIN_BULK_OV_SET** / **VIN_BULK_OV_th** 0 / 14.5 V 1 / 16.0 V
b6	CUR_PWR_METER	RW	PMIC output regulator measurement - Current or Power Meter. **CUR_PWR_METER** / **ADC Measurement Report in R0C, R0D, R0E & R0F** 0 / Report Current Measurement in registers 1 / Report Power Measurement in registers
b5	VIN_MGMT_OV_SET	RW	VIN_MGMT Input Over Voltage Threshold Setting For GSI_n Assertion. **VIN_MGMT_OV_SET** / **VIN_MGMT_OV_th** 0 / 3.8 V 1 / 3.7 V
b4	MSK_GLOBAL_PG_STATUS	RW	Global mask CAMP output pin for all appropriate register bits in R15[7,5:0], R16, R17[7:4], R18, and R19[4:2]. Mask register control R2F[1:0] still applies when this bit is set to '1'. **MSK_GLOBAL_PG_STATUS** / **CAMP Output** 0 / Not Masked 1 / Masked
b3	GSI_N_ENABLE	RW	Enable GSI_n pin. This register can be used as Global Mask Function for GSI_n pin. If disabled, this masks GSI_n output signal for all register bits in R15[7,5:0], R16, R17[7:4], R18, and R19[4:2]. **GSI_N_ENALBE** / **GSI_n pin Status** 0 / Disabled 1 / Enabled
b2 ~ b0	OTWARN_SET	RW	PMIC High Temperature warning threshold setting. **OTWARN_SET** / **OTWRAN_th** / **OTWARN_SET** / **OTWARN_th** 000 / Reserved / 100 / PMIC temperature ≥ 115°C 001 / PMIC temperature ≥ 85°C / 101 / PMIC temperature ≥ 125°C 010 / PMIC temperature ≥ 95°C / 110 / PMIC temperature ≥ 135°C 011 / PMIC temperature ≥ 105°C / 111 / Reserved The tolerance of the temperature warning threshold is ±5°C from the selected setting.

Table 98. R1C

Address: 1CH
Default: 01100000B

Data Bit	Data Name	Attribute	Function Description
b7 ~ b2	SWA_CONSUM_WARNING_SET	RW	SWA output high current consumption warning threshold..
b1 ~ b0	Reserved	RV	Reserved

SWA_CONSUM_WARNING_SET	SWA_CONSUM_WARNING_th	SWA_CONSUM_WARNING_SET	SWA_CONSUM_WARNING_th
000000	Undefined	100000	>4.0A
000001	>0.125A	100001	>4.125A
000010	>0.25A	100010	>4.25A
000011	>0.375A	100011	>4.375A
000100	>0.5A	100100	>4.5A
000101	>0.625A	100101	>4.625A
000110	>0.75A	100110	>4.75A
000111	>0.875A	100111	>4.875A
001000	>1.0A	101000	>5.0A
001001	>1.125A	101001	>5.125A
001010	>1.25A	101010	>5.25A
001011	>1.375A	101011	>5.375A
001100	>1.5A	101100	>5.5A
001101	>1.625A	101101	>5.625A
001110	>1.75A	101110	>5.75A
001111	>1.875A	101111	>5.875A
010000	>2.0A	110000	>6.0A
010001	>2.125A	110001	>6.125A
010010	>2.25A	110010	>6.25A
010011	>2.375A	110011	>6.375A
010100	>2.5A	110100	>6.5A
010101	>2.625A	110101	>6.625A
010110	>2.75A	110110	>6.75A
010111	>2.875A	110111	>6.875A
011000	>3.0A	111000	>7.0A
011001	>3.125A	111001	>7.125A
011010	>3.25A	111010	>7.25A
011011	>3.375A	111011	>7.375A
011100	>3.5A	111100	>7.5A
011101	>3.625A	111101	>7.625A
011110	>3.75A	111110	>7.75A
011111	>3.875A	111111	>7.875A

Table 99. R1D

Address: 1DH
Default: 01100000B

Data Bit	Data Name	Attribute	Function Description
b7 ~ b2	SWB_CONSUM_WARNING_SET	RW	SWB output high current consumption warning threshold. For dual phase operation, this register should be configured identically as R1C[7:2].
b1 ~ b0	Reserved	RV	Reserved

SWB_CONSUM_WARNING_SET	SWB_CONSUM_WARNING_th	SWB_CONSUM_WARNING_SET	SWB_CONSUM_WARNING_th
000000	Undefined	100000	>4.0A
000001	>0.125A	100001	>4.125A
000010	>0.25A	100010	>4.25A
000011	>0.375A	100011	>4.375A
000100	>0.5A	100100	>4.5A
000101	>0.625A	100101	>4.625A
000110	>0.75A	100110	>4.75A
000111	>0.875A	100111	>4.875A
001000	>1.0A	101000	>5.0A
001001	>1.125A	101001	>5.125A
001010	>1.25A	101010	>5.25A
001011	>1.375A	101011	>5.375A
001100	>1.5A	101100	>5.5A
001101	>1.625A	101101	>5.625A
001110	>1.75A	101110	>5.75A
001111	>1.875A	101111	>5.875A
010000	>2.0A	110000	>6.0A
010001	>2.125A	110001	>6.125A
010010	>2.25A	110010	>6.25A
010011	>2.375A	110011	>6.375A
010100	>2.5A	110100	>6.5A
010101	>2.625A	110101	>6.625A
010110	>2.75A	110110	>6.75A
010111	>2.875A	110111	>6.875A
011000	>3.0A	111000	>7.0A
011001	>3.125A	111001	>7.125A
011010	>3.25A	111010	>7.25A
011011	>3.375A	111011	>7.375A
011100	>3.5A	111100	>7.5A
011101	>3.625A	111101	>7.625A
011110	>3.75A	111110	>7.75A
011111	>3.875A	111111	>7.875A

Table 100. R1E

Address: 1EH
Default: 01100000B

<table>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b7 ~ b2</td><td>SWC_CONSUM_WARNING_SET</td><td>RW</td><td>SWC output high current consumption warning threshold.
<table>
<tr><th>SWC_CONSUM_WARNING_SET</th><th>SWC_CONSUM_WARNING_th</th><th>SWC_CONSUM_WARNING_SET</th><th>SWC_CONSUM_WARNING_th</th></tr>
<tr><td>000000</td><td>Undefined</td><td>100000</td><td>>4.0A</td></tr>
<tr><td>000001</td><td>>0.125A</td><td>100001</td><td>>4.125A</td></tr>
<tr><td>000010</td><td>>0.25A</td><td>100010</td><td>>4.25A</td></tr>
<tr><td>000011</td><td>>0.375A</td><td>100011</td><td>>4.375A</td></tr>
<tr><td>000100</td><td>>0.5A</td><td>100100</td><td>>4.5A</td></tr>
<tr><td>000101</td><td>>0.625A</td><td>100101</td><td>>4.625A</td></tr>
<tr><td>000110</td><td>>0.75A</td><td>100110</td><td>>4.75A</td></tr>
<tr><td>000111</td><td>>0.875A</td><td>100111</td><td>>4.875A</td></tr>
<tr><td>001000</td><td>>1.0A</td><td>101000</td><td>>5.0A</td></tr>
<tr><td>001001</td><td>>1.125A</td><td>101001</td><td>>5.125A</td></tr>
<tr><td>001010</td><td>>1.25A</td><td>101010</td><td>>5.25A</td></tr>
<tr><td>001011</td><td>>1.375A</td><td>101011</td><td>>5.375A</td></tr>
<tr><td>001100</td><td>>1.5A</td><td>101100</td><td>>5.5A</td></tr>
<tr><td>001101</td><td>>1.625A</td><td>101101</td><td>>5.625A</td></tr>
<tr><td>001110</td><td>>1.75A</td><td>101110</td><td>>5.75A</td></tr>
<tr><td>001111</td><td>>1.875A</td><td>101111</td><td>>5.875A</td></tr>
<tr><td>010000</td><td>>2.0A</td><td>110000</td><td>>6.0A</td></tr>
<tr><td>010001</td><td>>2.125A</td><td>110001</td><td>>6.125A</td></tr>
<tr><td>010010</td><td>>2.25A</td><td>110010</td><td>>6.25A</td></tr>
<tr><td>010011</td><td>>2.375A</td><td>110011</td><td>>6.375A</td></tr>
<tr><td>010100</td><td>>2.5A</td><td>110100</td><td>>6.5A</td></tr>
<tr><td>010101</td><td>>2.625A</td><td>110101</td><td>>6.625A</td></tr>
<tr><td>010110</td><td>>2.75A</td><td>110110</td><td>>6.75A</td></tr>
<tr><td>010111</td><td>>2.875A</td><td>110111</td><td>>6.875A</td></tr>
<tr><td>011000</td><td>>3.0A</td><td>111000</td><td>>7.0A</td></tr>
<tr><td>011001</td><td>>3.125A</td><td>111001</td><td>>7.125A</td></tr>
<tr><td>011010</td><td>>3.25A</td><td>111010</td><td>>7.25A</td></tr>
<tr><td>011011</td><td>>3.375A</td><td>111011</td><td>>7.375A</td></tr>
<tr><td>011100</td><td>>3.5A</td><td>111100</td><td>>7.5A</td></tr>
<tr><td>011101</td><td>>3.625A</td><td>111101</td><td>>7.625A</td></tr>
<tr><td>011110</td><td>>3.75A</td><td>111110</td><td>>7.75A</td></tr>
<tr><td>011111</td><td>>3.875A</td><td>111111</td><td>>7.875A</td></tr>
</table></td></tr>
<tr><td>b1 ~ b0</td><td>Reserved</td><td>RV</td><td>Reserved</td></tr>
</table>

Table 101. R1F

Address: 1FH
Default: 01100000B

Data Bit	Data Name	Attribute	Function Description
b7 ~ b2	SWD_CONSUM_WARNING_SET	RW	SWD output high current consumption warning threshold.
b1 ~ b0	Reserved	RV	Reserved

SWD_CONSUM_WARNING_SET	SWD_CONSUM_WARNING_th	SWD_CONSUM_WARNING_SET	SWD_CONSUM_WARNING_th
000000	Undefined	100000	>4.0A
000001	>0.125A	100001	>4.125A
000010	>0.25A	100010	>4.25A
000011	>0.375A	100011	>4.375A
000100	>0.5A	100100	>4.5A
000101	>0.625A	100101	>4.625A
000110	>0.75A	100110	>4.75A
000111	>0.875A	100111	>4.875A
001000	>1.0A	101000	>5.0A
001001	>1.125A	101001	>5.125A
001010	>1.25A	101010	>5.25A
001011	>1.375A	101011	>5.375A
001100	>1.5A	101100	>5.5A
001101	>1.625A	101101	>5.625A
001110	>1.75A	101110	>5.75A
001111	>1.875A	101111	>5.875A
010000	>2.0A	110000	>6.0A
010001	>2.125A	110001	>6.125A
010010	>2.25A	110010	>6.25A
010011	>2.375A	110011	>6.375A
010100	>2.5A	110100	>6.5A
010101	>2.625A	110101	>6.625A
010110	>2.75A	110110	>6.75A
010111	>2.875A	110111	>6.875A
011000	>3.0A	111000	>7.0A
011001	>3.125A	111001	>7.125A
011010	>3.25A	111010	>7.25A
011011	>3.375A	111011	>7.375A
011100	>3.5A	111100	>7.5A
011101	>3.625A	111101	>7.625A
011110	>3.75A	111110	>7.75A
011111	>3.875A	111111	>7.875A

Table 102. R20[1] (Sheet 1 of 2)

<table>
<tr><td colspan="4">Address: 20H
Default: 00000000B</td></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b7 ~ b6</td><td>SWA_OCW_SET</td><td>RW</td><td>SWA Output Current Limiter Warning Threshold Setting. (COT Valley current limit)
Low Current PMIC Encoding Definition (PMIC5010):
<table>
<tr><th>SWA_OCW_SET</th><th>SWA_OCW_th</th></tr>
<tr><td>00</td><td>2.0 A</td></tr>
<tr><td>01</td><td>2.5 A</td></tr>
<tr><td>10</td><td>3.0 A</td></tr>
<tr><td>11</td><td>3.5 A</td></tr>
</table>
High Current PMIC Encoding Definition (PMIC5000):
<table>
<tr><th>SWA_OCW_SET</th><th>SWA_OCW_th</th></tr>
<tr><td>00</td><td>4.0 A</td></tr>
<tr><td>01</td><td>4.5 A</td></tr>
<tr><td>10</td><td>5.0 A</td></tr>
<tr><td>11</td><td>5.5 A</td></tr>
</table></td></tr>
<tr><td>b5 ~ b4</td><td>SWB_OCW_SET</td><td>RW</td><td>SWB Output Current Limiter Warning Threshold Setting (COT Valley current limit).
This register is applicable regardless of the setting in R4F[0]. If R4F[0]=’1’, this register must be configured identically as R20[7:6]
Low Current PMIC Encoding Definition (PMIC5010).
<table>
<tr><th>SWB_OCW_SET</th><th>SWB_OCW_th</th></tr>
<tr><td>00</td><td>2.0 A</td></tr>
<tr><td>01</td><td>2.5 A</td></tr>
<tr><td>10</td><td>3.0 A</td></tr>
<tr><td>11</td><td>3.5 A</td></tr>
</table>
High Current PMIC Encoding Definition (PMIC5000):
<table>
<tr><th>SWB_OCW_SET</th><th>SWB_OCW_th</th></tr>
<tr><td>00</td><td>4.0 A</td></tr>
<tr><td>01</td><td>4.5 A</td></tr>
<tr><td>10</td><td>5.0 A</td></tr>
<tr><td>11</td><td>5.5 A</td></tr>
</table></td></tr>
</table>

Table 102. R20[1] (Sheet 2 of 2)

<table>
<tr><td colspan="4">Address: 20H
Default: 00000000B</td></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b3 ~ b2</td><td>SWC_OCW_SET</td><td>RW</td><td>SWC Output Current Limiter Warning Threshold Setting. (COT Valley current limit)
Low Current PMIC Encoding Definition (PMIC5010):
<table>
<tr><th>SWC_OCW_SET</th><th>SWC_OCW_th</th></tr>
<tr><td>00</td><td>2.0 A</td></tr>
<tr><td>01</td><td>2.5 A</td></tr>
<tr><td>10</td><td>3.0 A</td></tr>
<tr><td>11</td><td>3.5 A</td></tr>
</table>
High Current PMIC Encoding Definition (PMIC5000):
<table>
<tr><th>SWC_OCW_SET</th><th>SWC_OCW_th</th></tr>
<tr><td>00</td><td>4.0 A</td></tr>
<tr><td>01</td><td>4.5 A</td></tr>
<tr><td>10</td><td>5.0 A</td></tr>
<tr><td>11</td><td>5.5 A</td></tr>
</table></td></tr>
<tr><td>b1 ~ b0</td><td>SWD_OCW_SET</td><td>RW</td><td>SWD Output Current Limiter Warning Threshold Setting. (COT Valley current limit)
Low Current PMIC Encoding Definition (PMIC5010):
<table>
<tr><th>SWD_OCW_SET</th><th>SWD_OCW_th</th></tr>
<tr><td>00</td><td>2.0 A</td></tr>
<tr><td>01</td><td>2.5 A</td></tr>
<tr><td>10</td><td>3.0 A</td></tr>
<tr><td>11</td><td>3.5 A</td></tr>
</table>
High Current PMIC Encoding Definition (PMIC5000):
<table>
<tr><th>SWD_OCW_SET</th><th>SWD_OCW_th</th></tr>
<tr><td>00</td><td>4.0 A</td></tr>
<tr><td>01</td><td>4.5 A</td></tr>
<tr><td>10</td><td>5.0 A</td></tr>
<tr><td>11</td><td>5.5 A</td></tr>
</table></td></tr>
</table>

1. At first power on, this register is automatically configured to be identical to R50 by the PMIC on its own.

Table 103. R21[1]

Address: 21H Default: 01111000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b1	SWA_VSET	RW	SWA Output Regulator Voltage setting. If R2B[5]=1'b0: SWA Voltage=R21[7:1] * 5mV + 800mV. (Default: R21[7:1]=7'b0111100, SWA=1100mV) If R2B[5]=1'b1: SWA Voltage=R21[7:1] * 5mV + 600mV. (Default: R21[7:1]=7'b0111100, SWA=900mV) PMIC guarantees the efficiency spec and all electrical characteristics spec within a range of 1050mV to 1160mV. After VR is enabled, the host may update this register to any new setting that it may desire. However, to prevent triggering false error, the PMIC internally will increase the SWA output voltage setting by 5 mV at a time. The time that it takes for the PMIC to adjust the output voltage is 5 µs for each 5 mV increment. The host must wait sufficient time for the PMIC to adjust to the final value. As an example, if the host adjusts the output voltage by 50 mV from the original voltage, the host must wait minimum of 50 µs before the PMIC can guarantee the new output voltage.
b0	SWA_PGL_SET	RW	SWA Output Threshold Low Side Voltage For Power Good Status. **SWA_PGL_SET** / **SWA_PGL_th** 0 / -5% from the setting in R21[7:1] 1 / -7.5% from the setting in R21[7:1]

1. At first power on, this register is automatically configured to be identical to R45 by the PMIC on its own. If required, Host must update the settings in register R21[0], R22 and R20[7:6] first prior to updating the settings in the register R21[7:1].

Table 104. R22[1] (Sheet 1 of 2)

Address: 22H Default: 01100000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b6	SWA_PGH_SET	RW	SWA Output Threshold High Side Voltage For Power Good Status. **SWA_PGH_SET** / **SWA_PGH_th** 00 / +5% from the setting in R21[7:1] 01 / +7.5% from the setting in R21[7:1] 10 / +10% from the setting in R21[7:1] 11 / Reserved

Table 104. R22[1] (Sheet 2 of 2)

<table>
<tr><td colspan="4">Address: 22H
Default: 01100000B</td></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b5 ~ b4</td><td>SWA_OV_SET</td><td>RW</td><td>SWA Output Regulator Threshold for Over-Voltage Status.
This setting must be higher than Power Good High Side Voltage threshold in R22[7:6].
<table>
<tr><th>SWA_OV_SET</th><th>SWA_OV_th</th></tr>
<tr><td>00</td><td>+7.5% from the setting in R21[7:1]</td></tr>
<tr><td>01</td><td>+10.0% from the setting in R21[7:1]</td></tr>
<tr><td>10</td><td>+12.5% from the setting in R21[7:1]</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>b3 ~ b2</td><td>SWA_UV_SET</td><td>RW</td><td>SWA Output Regulator Threshold for Under-Voltage Lockout Status.
<table>
<tr><th>SWA_UV_SET</th><th>SWA_UV_th</th></tr>
<tr><td>00</td><td>-10% from the setting in R21[7:1]</td></tr>
<tr><td>01</td><td>-12.5% from the setting in R21[7:1]</td></tr>
<tr><td>10</td><td>Reserved</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>b1 ~ b0</td><td>SWA_SSTOP_TIME</td><td>RW</td><td>SWA Output Regulator Soft Stop Time after VR Disable. This is the time it takes for buck regulator to go from steady state voltage to 0 V.
<table>
<tr><th>SWA_SSTOP_TIME</th><th>SSTOP_TIME</th></tr>
<tr><td>00</td><td>0.5 ms</td></tr>
<tr><td>01</td><td>1 ms</td></tr>
<tr><td>10</td><td>2 ms</td></tr>
<tr><td>11</td><td>4 ms</td></tr>
</table></td></tr>
</table>

1. At first power on, this register is automatically configured to be identical to R46 by the PMIC on its own. If required, Host must update the settings in register R21[0], R22 and R20[7:6] first prior to updating the settings in the register R21[7:1].

Table 105. R23[1]

Address: 23H Default: 01111000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b1	SWB_VSET	RW	SWB Output Regulator Voltage setting. Only applicable if R4F[0]='0'. If R2B[4]=1'b0: SWB Voltage=R23[7:1] * 5mV + 800mV. (Default: R23[7:1]=7'b0111100, SWB=1100mV) If R2B[4]=1'b1: SWB Voltage=R23[7:1] * 5mV + 600mV. (Default: R23[7:1]=7'b0111100, SWB=900mV) PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1050mV to 1160mV After VR is enabled, the host may update this register to any new setting that it may desire. However, to prevent triggering false error, the PMIC internally will increase the SWB output voltage setting by 10mV at a time. The time it takes for the PMIC to adjust the output voltage is 5µs for each 5mV increment. The host must wait sufficient time for the PMIC to adjust to the final value. As an example, if the host adjusts the output voltage by 50mV from the original voltage, the host must wait minimum of 50µs before the PMIC can guarantee the new output voltage.
b0	SWB_PGL_SET	RW	SWB Output Threshold Low Side Voltage For Power Good Status. Only applicable if R4F[0]='0'.. **SWB_PGL_SET** / **SWB_PGL_th** 0 / -5% from the setting in R23[7:1] 1 / -7.5% from the setting in R23[7:1]

1. At first power on, this register is automatically configured to be identical to R47 by the PMIC on its own. If required, the host must update the settings in register R23[0], R24 and R20[5:4] first prior to updating the settings in the register R23[7:1].

Table 106. R24[1] (Sheet 1 of 2)

Address: 24H Default: 01100000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b6	SWB_PGH_SET	RW	SWB Output Threshold High Side Voltage For Power Good Status. Only applicable if R4F[0]='0'. **SWB_PGH_SET** / **SWB_PGH_th** 00 / +5% from the setting in R23[7:1] 01 / +7.5% from the setting in R23[7:1] 10 / +10% from the setting in R23[7:1] 11 / Reserved

Table 106. R24[1] (Sheet 2 of 2)

Address: 24H Default: 01100000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b5 ~ b4	SWB_OV_SET	RW	SWB Output Over Voltage Threshold. Only applicable if R4F[0]='0'. This setting must be higher than Power Good High Side Voltage threshold in R24[7:6]. **SWB_OV_SET** / **SWB_OV_th** 00 / +7.5% from the setting in R23[7:1] 01 / +10% from the setting in R23[7:1] 10 / +12.5% from the setting in R23[7:1] 11 / Reserved
b3 ~ b2	SWB_UV_SET	RW	SWB Output Regulator Threshold for Under-Voltage Lockout Status. Only applicable if R4F[0]='0'. **SWB_UV_SET** / **SWB_UV_th** 00 / -10% from the setting in R23[7:1] 01 / -12.5% from the setting in R23[7:1] 10 / Reserved 11 / Reserved
b1 ~ b0	SWB_SSTOP_TIME	RW	SWB Output Regulator Soft Stop Time after VR Disable. This is the time it takes for buck regulator to go from steady state voltage to 0 V. Only applicable if R4F[0]='0. **SWB_SSTOP_TIME** / **SSTOP_TIME** 00 / 0.5 ms 01 / 1 ms 10 / 2 ms 11 / 4 ms

1. At first power on, this register is automatically configured to be identical to R48 by the PMIC on its own. If required, the host must update the settings in register R23[0], R24 and R20[5:4] first prior to updating the settings in the register R23[7:1].

Table 107. R25[1]

Address: 25H Default: 01111000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b1	SWC_VSET	RW	SWC Output Regulator Voltage setting. If R2B[3]=1'b0: SWC Voltage=R25[7:1] * 5mV + 800mV. (Default: R25[7:1]=7'b0111100, SWC=1100mV) If R2B[3]=1'b1: SWC Voltage=R25[7:1] * 5mV + 600mV. (Default: R25[7:1]=7'b0111100, SWC=900mV) PMIC guarantees the efficiency spec and all electrical characteristics spec within a range of 1050mV to 1160mV. After VR is enabled, the host may update this register to any new setting that it may desire. However, to prevent triggering false error, the PMIC internally will increase the SWC output voltage setting by 5mV at a time. The time it takes for the PMIC to adjust the output voltage is 5µs for each 5mV increment. The host must wait sufficient time for the PMIC to adjust to the final value. As an example, if the host adjusts the output voltage by 50mV from the original voltage, the host must wait minimum of 50µs before the PMIC can guarantee the new output voltage.
b0	SWC_PGL_SET	RW	SWC Output Threshold Low Side Voltage For Power Good Status. **SWC_PGL_SET** / **SWC_PGL_th** 0 / -5% from the setting in R25[7:1] 1 / -7.5% from the setting in R25[7:1]

1. At first power on, this register is automatically configured to be identical to R49 by the PMIC on its own. If required, the host must update the settings in register R25[0], R26 and R20[3:2] first prior to updating the settings in the register R25[7:1].

Table 108. R26[1]

<table>
<tr><th colspan="4">Address: 26H
Default: 01100000B</th></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b7 ~ b6</td><td>SWC_PGH_SET</td><td>RW</td><td>SWC Output Threshold High Side Voltage For Power Good Status.
<table>
<tr><th>SWC_PGH_SET</th><th>SWC_PGH_th</th></tr>
<tr><td>00</td><td>+5% from the setting in R25[7:1]</td></tr>
<tr><td>01</td><td>+7.5% from the setting in R25[7:1]</td></tr>
<tr><td>10</td><td>+10% from the setting in R25[7:1]</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>b5 ~ b4</td><td>SWC_OV_SET</td><td>RW</td><td>SWC Output Regulator Threshold for Over-Voltage Status.
This setting must be higher than Power Good High Side Voltage threshold in R26[7:6].
<table>
<tr><th>SWC_OV_SET</th><th>SWC_OV_th</th></tr>
<tr><td>00</td><td>+7.5% from the setting in R25[7:1]</td></tr>
<tr><td>01</td><td>+10% from the setting in R25[7:1]</td></tr>
<tr><td>10</td><td>+12.5% from the setting in R25[7:1]</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>b3 ~ b2</td><td>SWC_UV_SET</td><td>RW</td><td>SWC Output Regulator Threshold for Under-Voltage Lockout Status.
<table>
<tr><th>SWC_UV_SET</th><th>SWC_UV_th</th></tr>
<tr><td>00</td><td>-10% from the setting in R25[7:1]</td></tr>
<tr><td>01</td><td>-12.5% from the setting in R25[7:1]</td></tr>
<tr><td>10</td><td>Reserved</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>b1 ~ b0</td><td>SWC_SSTOP_TIME</td><td>RW</td><td>SWC Output Regulator Soft Stop Time after VR Disable. This is the time it takes for buck regulator to go from steady state voltage to 0V.
<table>
<tr><th>SWC_SSTOP_TIME</th><th>SSTOP_TIME</th></tr>
<tr><td>00</td><td>0.5 ms</td></tr>
<tr><td>01</td><td>1 ms</td></tr>
<tr><td>10</td><td>2 ms</td></tr>
<tr><td>11</td><td>4 ms</td></tr>
</table></td></tr>
</table>

1. At first power on, this register is automatically configured to be identical to R4A by the PMIC on its own. If required, the host must update the settings in register R25[0], R26 and R20[3:2] first prior to updating the settings in the register R25[7:1].

Table 109. R27[1]

Address: 27H Default: 01111000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b1	SWD_VSET	RW	SWD Output Regulator Voltage setting. If R2B[0]=1'b0: SWD Voltage=R27[7:1] * 5mV + 1500mV. (Default: R27[7:1]=7'b0111100, SWD=1800mV) If R2B[0]=1'b1: SWD Voltage=R27[7:1] * 5mV + 2200mV. (Default: R27[7:1]=7'b0111100, SWD=2500mV) PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1750mV to 1850mV. After VR is enabled, the host may update this register to any new setting that it may desire. However, to prevent triggering false error, the PMIC internally will increase the SWD output voltage setting by 5 mV at a time. The time it takes for the PMIC to adjust the output voltage is 5 µs for each 5 mV increment. The host must wait sufficient time for the PMIC to adjust to the final value. As an example, if the host adjusts the output voltage by 50 mV from the original voltage, the host must wait minimum of 50 µs before the PMIC can guarantee the new output voltage.
b0	SWD_PGL_SET	RW	SWD Output Threshold Low Side Voltage For Power Good Status. **SWD_PGL_SET** / **SWD_PGL_th** 0 / -5% from the setting in R27[7:1] 1 / -7.5% from the setting in R27[7:1]

1. At first power on, this register is automatically configured to be identical to R4B by the PMIC on its own. If required, the host must update the settings in register R27[0], R28 and R20[1:0]first prior to updating the settings in the register R27[7:1].

Table 110. R28[1] (Sheet 1 of 2)

Address: 28H Default: 01100000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b6	SWD_PGH_SET	RW	SWD Output Threshold High Side Voltage For Power Good Status. **SWD_PGH_SET** / **SWD_PGH_th** 00 / +5% from the setting in R27[7:1] 01 / +7.5% from the setting in R27[7:1] 10 / +10% from the setting in R27[7:1] 11 / Reserved

Table 110. R28[1] (Sheet 2 of 2)

Address: 28H
Default: 01100000B

Data Bit	Data Name	Attribute	Function Description
b5 ~ b4	SWD_OV_SET	RW	SWD Output Regulator Threshold for Over-Voltage Status. This setting must be higher than Power Good High Side Voltage threshold in R28[7:6]. **SWD_OV_SET** / **SWD_OV_th** 00 / +7.5% from the setting in R27[7:1] 01 / +10% from the setting in R27[7:1] 10 / +12.5% from the setting in R27[7:1] 11 / Reserved
b3 ~ b2	SWD_UV_SET	RW	SWD Output Regulator Threshold for Under-Voltage Lockout Status. **SWD_UV_SET** / **SWD_UV_th** 00 / -10% from the setting in R27[7:1] 01 / -12.5% from the setting in R27[7:1] 10 / Reserved 11 / Reserved
b1 ~ b0	SWD_SSTOP_TIME	RW	SWD Output Regulator Soft Stop Time after VR Disable. This is the time it takes for buck regulator to go from steady state voltage to 0 V. **SWD_SSTOP_TIME** / **SSTOP_TIME** 00 / 1 ms 01 / 2 ms 10 / 4 ms 11 / 8 ms

1. At first power on, this register is automatically configured to be identical to R4C by the PMIC on its own. If required, the host must update the settings in register R27[0], R28 and R20[1:0]first prior to updating the settings in the register R27[7:1].

Table 111. R29[1]

<table>
<tr><th colspan="4">Address: 29H
Default: 10011001B</th></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b7 ~ b6</td><td>SWA_MODE_SELECT</td><td>RW</td><td>SWA output regulator mode selection.
<table>
<tr><th>SWA_MODE_SELECT</th><th>SWA Switching Mode</th></tr>
<tr><td>00</td><td>Reserved</td></tr>
<tr><td>01</td><td>Reserved</td></tr>
<tr><td>10</td><td>COT (Constant On Time);
DCM (Discontinuous Conduction Mode)</td></tr>
<tr><td>11</td><td>COT (Constant on Time);
FCCM (Forced Continuous Conduction Mode)</td></tr>
</table></td></tr>
<tr><td>b5 ~ b4</td><td>SWA_FREQ</td><td>RW</td><td>SWA output regulator switching frequency.
<table>
<tr><th>SWA_FREQ</th><th>Switching Frequency</th></tr>
<tr><td>00</td><td>500 kHz</td></tr>
<tr><td>01</td><td>750 kHz</td></tr>
<tr><td>10</td><td>1000 kHz</td></tr>
<tr><td>11</td><td>1250 kHz</td></tr>
</table></td></tr>
<tr><td>b3 ~ b2</td><td>SWB_MODE_SELECT</td><td>RW</td><td>SWB output regulator mode selection. Only applicable if R4F[0] = '0'.
<table>
<tr><th>SWB_MODE_SELECT</th><th>SWB Switching Mode</th></tr>
<tr><td>00</td><td>Reserved</td></tr>
<tr><td>01</td><td>Reserved</td></tr>
<tr><td>10</td><td>COT; DCM</td></tr>
<tr><td>11</td><td>COT; FCCM</td></tr>
</table></td></tr>
<tr><td>b1 ~ b0</td><td>SWB_FREQ</td><td>RW</td><td>SWB switching frequency setting. Only applicable if R4F[0] = '0'.
<table>
<tr><th>SWB_FREQ</th><th>Switching Frequency</th></tr>
<tr><td>00</td><td>500 kHz</td></tr>
<tr><td>01</td><td>750 kHz</td></tr>
<tr><td>10</td><td>1000 kHz</td></tr>
<tr><td>11</td><td>1250 kHz</td></tr>
</table></td></tr>
</table>

1. At first power on, this register is automatically configured to be identical to R4D by the PMIC on its own. If required, the host must adjust this register first before issuing VR Enable command by setting R32[7]='1'.

Table 112. R2A[1]

<table>
<tr><th colspan="4">Address: 2AH
Default: 10011001B</th></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b7 ~ b6</td><td>SWC_MODE_SELECT</td><td>RW</td><td>SWC output regulator mode selection.
<table>
<tr><th>SWC_MODE_SELECT</th><th>SWC Switching Mode</th></tr>
<tr><td>00</td><td>Reserved</td></tr>
<tr><td>01</td><td>Reserved</td></tr>
<tr><td>10</td><td>COT; DCM</td></tr>
<tr><td>11</td><td>COT; FCCM</td></tr>
</table></td></tr>
<tr><td>b5 ~ b4</td><td>SWC_FREQ</td><td>RW</td><td>SWC output regulator switching frequency.
<table>
<tr><th>SWC_FREQ</th><th>Switching Frequency</th></tr>
<tr><td>00</td><td>500 kHz</td></tr>
<tr><td>01</td><td>750 kHz</td></tr>
<tr><td>10</td><td>1000 kHz</td></tr>
<tr><td>11</td><td>1250 kHz</td></tr>
</table></td></tr>
<tr><td>b3 ~ b2</td><td>SWD_MODE_SELECT</td><td>RW</td><td>SWD output regulator mode selection.
<table>
<tr><th>SWD_MODE_SELECT</th><th>SWD Switching Mode</th></tr>
<tr><td>00</td><td>Reserved</td></tr>
<tr><td>01</td><td>Reserved</td></tr>
<tr><td>10</td><td>COT; DCM</td></tr>
<tr><td>11</td><td>COT; FCCM</td></tr>
</table></td></tr>
<tr><td>b1 ~ b0</td><td>SWD_FREQ</td><td>RW</td><td>SWD output regulator switching frequency.
<table>
<tr><th>SWD_FREQ</th><th>Switching Frequency</th></tr>
<tr><td>00</td><td>500 kHz</td></tr>
<tr><td>01</td><td>750 kHz</td></tr>
<tr><td>10</td><td>1000 kHz</td></tr>
<tr><td>11</td><td>1250 kHz</td></tr>
</table></td></tr>
</table>

1. At first power on, this register is automatically configured to be identical to R4E by the PMIC on its own. If required, the host must adjust this register first before issuing VR Enable command by setting R32[7]='1'.

Table 113. R2B[1] (Sheet 1 of 2)

<table>
<tr><td colspan="4">Address: 2BH
Default: 01000010B</td></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b7 ~ b6</td><td>LDO1P8_VSET</td><td>RW</td><td>VLDO_1.8V LDO Output Voltage Setting.
<table>
<tr><th>LDO1P8_VSET</th><th>VLDO 1.8V LDO Voltage</th></tr>
<tr><td>00</td><td>1.7 V</td></tr>
<tr><td>01</td><td>1.8 V</td></tr>
<tr><td>10</td><td>1.9 V</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table>
The VLDO_1.8V Power Good threshold in register R1A[2] is always fixed regardless of the setting in this register.</td></tr>
<tr><td>b5</td><td>SWA_RANGE</td><td>RW</td><td>SWA Output Voltage Range Selection. Apply to Register R21[7:1].
<table>
<tr><th>SWA_RANGE</th><th>SWA Output Voltage Range</th></tr>
<tr><td>0</td><td>Range: 800mV to 1435mV for SWA; 5mV step size</td></tr>
<tr><td>1</td><td>Range: 600mV to 1235mV for SWA; 5mV step size</td></tr>
</table></td></tr>
<tr><td>b4</td><td>SWB_RANGE</td><td>RW</td><td>SWB Output Voltage Range Selection. Apply to Register R23[7:1].
Only applicable if R4F[0]=’0’
<table>
<tr><th>SWB_RANGE</th><th>SWB Output Voltage Range</th></tr>
<tr><td>0</td><td>Range: 800mV to 1435mV for SWB; 5mV step size</td></tr>
<tr><td>1</td><td>Range: 600mV to 1235mV for SWB; 5mV step size</td></tr>
</table></td></tr>
<tr><td>b3</td><td>SWC_RANGE</td><td>RW</td><td>SWC Output Voltage Range Selection. Apply to Register R23[7:1].
<table>
<tr><th>SWC_RANGE</th><th>SWC Output Voltage Range</th></tr>
<tr><td>0</td><td>Range: 800mV to 1435mV for SWC; 5mV step size</td></tr>
<tr><td>1</td><td>Range: 600mV to 1235mV for SWC; 5mV step size</td></tr>
</table></td></tr>
<tr><td>b2 ~ b1</td><td>LDO1P0_VSET</td><td>RW</td><td>VLDO_1.0V LDO Output Voltage Setting.
<table>
<tr><th>LDO1P0_VSET</th><th>VLDO_1.0V LDO Voltage</th></tr>
<tr><td>00</td><td>0.9 V</td></tr>
<tr><td>01</td><td>1.0 V</td></tr>
<tr><td>10</td><td>1.1 V</td></tr>
<tr><td>11</td><td>1.2 V</td></tr>
</table>
If required, Host must adjust this register one step at a time (0.1V increment or decrement) to prevent false trigger of power good status and PWR_GOOD pin assertion. In other words, Host should not increment or decrement 0.2V or 0.3V from its current setting.</td></tr>
</table>

Table 113. R2B[1] (Sheet 2 of 2)

Address: 2BH Default: 01000010B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b0	SWD_RANGE	RW	SWD Output Voltage Range Selection. Apply to Register R27[7:1]. **SWD_RANGE** / **SWD Output Voltage Range** 0 / Range: 1500mV to 2135mV for SWD; 5mV step size 1 / Range: 2200mV to 2835mV for SWD; 5mV step size

1. At first power on, this register is automatically configured to be identical to R51 by the PMIC on its own. If required, the host must adjust this register first before issuing VR Enable command by setting R32[7]='1'. The host must also wait minimum of 5 µs after the adjustment before issuing VR Enable command.

Table 114. R2C[1]

Address: 2CH Default: 00100010B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b5	SWA_SSTRT_TIME	RW	SWA Output Regulator Soft Start Time After VR Enable. This is the time it takes for buck regulator to go from 0V to the steady state voltage. **SWA_SSTRT_TIME** / **SSTRT Time** / **SWA_SSTRT_TIME** / **SSTRT Time** 000 / 1 ms / 100 / 8 ms 001 / 2 ms / 101 / 10 ms 010 / 4 ms / 110 / 12 ms 011 / 6 ms / 111 / 14 ms
b4	Reserved	RV	Reserved
b3 ~ b1	SWB_SSTRT_TIME	RW	SWB Output Regulator Soft Start Time After VR Enable. This is the time it takes for buck regulator to go from 0V to the steady state voltage. Only applicable if R4F[0] = '0'. **SWB_SSTRT_TIME** / **SSTRT Time** / **SWB_SSTRT_TIME** / **SSTRT Time** 000 / 1 ms / 100 / 8 ms 001 / 2 ms / 101 / 10 ms 010 / 4 ms / 110 / 12 ms 011 / 6 ms / 111 / 14 ms
b0	Reserved	RV	Reserved

1. At first power on, this register is automatically configured to be identical to R5D by the PMIC on its own. If required, the host must adjust this register first before issuing VR Enable command by setting R32[7]='1'.

Table 115. R2D[1]

<table>
<tr><td colspan="4">Address: 2DH
Default: 00100010B</td></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b7 ~ b5</td><td>SWC_SSTRT_TIME</td><td>RW</td><td>SWC Output Regulator Soft Start Time After VR Enable. This is the time it takes for buck regulator to go from 0 V to the steady state voltage.
<table>
<tr><th>SWC_SSTRT_TIME</th><th>SSTRT Time</th><th>SWC_SSTRT_TIME</th><th>SSTRT Time</th></tr>
<tr><td>000</td><td>1 ms</td><td>100</td><td>8 ms</td></tr>
<tr><td>001</td><td>2 ms</td><td>101</td><td>10 ms</td></tr>
<tr><td>010</td><td>4 ms</td><td>110</td><td>12 ms</td></tr>
<tr><td>011</td><td>6 ms</td><td>111</td><td>14 ms</td></tr>
</table></td></tr>
<tr><td>b4</td><td>Reserved</td><td>RV</td><td>Reserved</td></tr>
<tr><td>b3 ~ b1</td><td>SWD_SSTRT_TIME</td><td>RW</td><td>SWD Output Regulator Soft Start Time After VR Enable. This is the time it takes for buck regulator to go from 0V to the steady state voltage.
<table>
<tr><th>SWD_SSTRT_TIME</th><th>SSTRT Time</th><th>SWD_SSTRT_TIME</th><th>SSTRT Time</th></tr>
<tr><td>000</td><td>1 ms</td><td>100</td><td>8 ms</td></tr>
<tr><td>001</td><td>2 ms</td><td>101</td><td>10 ms</td></tr>
<tr><td>010</td><td>4 ms</td><td>110</td><td>12 ms</td></tr>
<tr><td>011</td><td>6 ms</td><td>111</td><td>14 ms</td></tr>
</table></td></tr>
<tr><td>b0</td><td>Reserved</td><td>RV</td><td>Reserved</td></tr>
</table>

1. At first power on, this register is automatically configured to be identical to R5E by the PMIC on its own. If required, the host must adjust this register first before issuing VR Enable command by setting R32[7]='1'.

Table 116. R2E

Address: 2EH Default: 00000100B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b3	Reserved	RV	Reserved
b2 ~ b0	OTP_SET	RW	PMIC Shutdown Temperature Threshold. **OTP_SET** / **OTP_th** / **OTP_SET** / **OTP_th** 000 / PMIC Temperature ≥ 105°C / 100 / PMIC Temperature ≥ 145°C 001 / PMIC Temperature ≥ 115°C / 101 / Reserved 010 / PMIC Temperature ≥ 125°C / 110 / Reserved 011 / PMIC Temperature ≥ 135°C / 111 / Reserved

Table 117. R2F[1] (Sheet 1 of 2)

Address: 2FH Default: 00000010B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7	SWOVER_VSET	RW	VIN_MGMT Input Supply Switchover Voltage Threshold to VIN_BULK Input Supply. **SWOVER_VSET** / **SWOVER_th** 0 / 2.8 V 1 / 2.75V
b6	SWA_REG_CTRL	RW	Disable SWA Regulator Output. **SWA_REG_CTRL** / **SWA Output** 0 / Disable SWA Output Regulator 1 / Enable SWA Output Regulator
b5	SWB_REG_CTRL	RW	Disable SWB Regulator Output. Only applicable if R4F[0] = '0'. **SWB_REG_CTRL** / **SWB Output** 0 / Disable SWB Output Regulator 1 / Enable SWB Output Regulator
b4	SWC_REG_CTRL	RW	Disable SWC Regulator Output. **SWC_REG_CTRL** / **SWC Output** 0 / Disable SWC Output Regulator 1 / Enable SWC Output Regulator

Table 117. R2F[1] (Sheet 2 of 2)

<table>
<tr><td>b3</td><td>SWD_REG_CTRL</td><td>RW</td><td>Disable SWD Regulator Output.
<table><tr><th>SWD_REG_CTRL</th><th>SWD Output</th></tr><tr><td>0</td><td>Disable SWD Output Regulator</td></tr><tr><td>1</td><td>Enable SWD Output Regulator</td></tr></table></td></tr>
<tr><td>b2</td><td>WRITE_PROT_ CONTROL</td><td>RW</td><td>PMIC Write Protect Function Control.
<table><tr><th>WRITE_PROT_CONTROL</th><th>PMIC Mode Operation</th></tr><tr><td>0</td><td>CAMP input signal determines the Write Protect Function as noted in Section 3.7.1, "Register Write Protect Function".</td></tr><tr><td>1</td><td>Write Protect Function is disabled; all register write access is allowed independent of CAMP input signal as noted in Section 3.7.1, "Register Write Protect Function".</td></tr></table></td></tr>
<tr><td>b1 ~ b0</td><td>MSK_BIT_REG_ CTRL</td><td>RW</td><td>Mask Bits Register Control. Applies to Mask Registers R15[7:5,0], R16, R17[7:2], R18, R19[4:2] when any one or more Mask registers are set to ‘1’. If all Mask registers are configured as ‘0’, the setting in R2F[1:0] does not matter.
<table><tr><th>MSK_BIT_REG_CTRL</th><th>Mask Control</th></tr><tr><td>00</td><td>Mask GSI_n Signal Only (PWR_GOOD Signal will de-assert)</td></tr><tr><td>01</td><td>Mask PWR_GOOD Signal Only (GSI_n Signal will assert)</td></tr><tr><td>10</td><td>Mask GSI_n and PWR_GOOD Signals (neither PWR_GOOD de-assert or GSI_n signal will assert)</td></tr><tr><td>11</td><td>Reserved</td></tr></table></td></tr>
</table>

1. R2F[6:3] must be used only after power up sequence (after VR Enable command). At the first power up, PMIC automatically updates the status of these registers to '1' after VR Enable command. When VR Enable command is registered, the PMIC updates these registers based on Power On Sequence Configuration register (0 to 3) settings. If enabled, under Non-Write Protect mode of operation only, the PMIC's output regulators can be disabled by clearing these bits and they can be re-enabled again by setting these bits. The PMIC does not alter its Power Good output signal and it keeps it asserted High. If any regulator is not enabled in Power on Sequence Configuration 0 to 3, it cannot be enabled using this register. For example, if only SWA is enabled and SWB, SWC & SWD are not enabled in R40 to R43, then only SWA can be disabled and re-enabled again, but SWB, SWC and SWD cannot be enabled using R2F[6:3].

Table 118. R30

Address: 30H
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7	ADC_ENABLE	RW	Enable ADC (Analog to Digital Conversion). Set '0' to disable the ADC function completely. **ADC_ENABLE** / **ADC** 0 / Disabled 1 / Enabled It applies to voltage readout in Register R31, as well as current or power readout in Register R0C, R0D, R0E and R0F. However, it doesn't apply to thermal sensor/ temperature readout in Register R33[7:5], as well as, high temperature warning and critical temperature shutdown function.
b6 ~ b3	ADC_SELECT	RW	Input Selection for ADC Readout. Setting '0001' is only applicable if R4F[0]='0'. The host shall wait minimum of 9ms delay after the input selection for ADC readout and the actual readout from R31 to get the latest reading. **ADC_SELECT** / **ADC Input** / **ADC_SELECT** / **ADC Input** 0000 / SWA Output Voltage / 1000 / VLDO_1.8V Output Voltage 0001 / SWB Output Voltage / 1001 / VLDO_1.0V Output Voltage 0010 / SWC Output Voltage / 1010 / Reserved 0011 / SWD Output Voltage / 1011 / Reserved 0100 / Reserved / 1100 / Reserved 0101 / VIN_BULK Input voltage / 1101 / Reserved 0110 / VIN_MGMT Input voltage / 1110 / Reserved 0111 / VBIAS Output voltage / 1111 / Reserved
b2	Reserved	RV	Reserved
b1 ~ b0	ADC_UPDATE_FREQ	RW	ADC Current or Power Measurement Update Frequency. For average output current or power measurement in registers R0C, R0D, R0E and R0F. This register represents how often the registers are updated. **ADC_UPDATE_FREQ** / **Update Frequency** 00 / 1 ms 01 / 2 ms 10 / 4 ms 11 / 8 ms

Table 119. R31

Address: 31H **Default: 00000000B**			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b0	ADC_READ	RO	ADC Output voltage reading. For R30[6:3]='0000' or '0001' or '0010' or '0011' or '0110' or '1000' or '1001': (applies to SWA/B/C/D, VLDO_1.8V, VLDO_1.0V, VIN_MGMT) 0000 0000 = Undefined 0000 0001 = 15 mV 0000 0010 = 30 mV … 1111 1111 ≥ 3825 mV For R30[6:3]='0101': (applies to VIN_BULK Input Voltage) 0000 0000 = Undefined 0000 0001 = 70 mV 0000 0010 = 140 mV … 1111 1111 ≥ 17850 mV For R30[6:3]='0111': (applies to VBIAS Output Voltage) 0000 0000 = Undefined 0000 0001 = 25 mV 0000 0010 = 50 mV … 1111 1111 ≥ 6375 mV

Table 120. R32 (Sheet 1 of 2)

Address: 32H
Default: 00100000B

Data Bit	Data Name	Attribute	Function Description
b7	VR_ENABLE	RW	PMIC Enable. **VR_ENABLE** / **PMIC** 0 / Disabled 1 / Enabled Host sets this bit at first Power On. After this bit is set, PMIC executes Power On Sequence configuration 0 to 3 registers(R40 to R43). Host shall ensure that prior to issuing VR Enable command, there is no pending IBI interrupt (i.e R0A[1] = '1') status. After Host issues VR Enable command, PMIC may NACK any I²C or I3C Basic bus transaction by Host until $t_{PMIC\_PWR\_GOOD\_OUT}$ timing parameter is satisfied. Host shall not access any device specific registers or issue any CCCs until $t_{PMIC\_PWR\_GOOD\_OUT}$ parameter is satisfied. PMIC device may request an IBI during the Power Up sequence (i.e. during $t_{PMIC\_PWR\_GOOD\_OUT}$ time) if any event occurs. Once R32[7] is set to '1' via VR Enable command, the subsequent write to R32[5]='0' is ignored by the PMIC. If there is a simultaneous write to R32[7,5]='10', the PMIC prioritizes bit [5] and does not execute VR Enable command.
b6	INTERFACE_SEL	RO	PMIC Management Bus Interface Protocol Selection. **INTERFACE_SEL** / **Interface** 0 / I²C Protocol (Max. speed 1MHz) 1 / I3C Basic Protocol This register is automatically updated when SETAASA CCC or RSTDAA CCC is registered by the PMIC device or when the PMIC device goes through Bus reset regardless of whether PMIC is in Write Protect mode or Non-Write Protect mode of operation. This register can be read by Host through normal Read operation, but it cannot be written with normal write operation either in I²C mode or I3C Basic mode of operation.
b5	EXECUTE_VR_EN_CTRL	RW	PMIC VR Enable Command Execution Control over I²C/I3C Basic Bus. **EXECUTE_VR_EN_CTRL** / **VR Enable Command** 0 / Do not execute VR Enable Command; i.e. ignore bit[7] ='1' and keep it as '0'. 1 / Execute VR enable command
b4	EXECUTE_CAMP_FAIL_N	RW	PMIC CAMP Fail_n function (Transition from High to Low) Control. **EXECUTE_CAMP_FAIL_N** / **VR Disable Command** 0 / Execute VR disable command 1 / Do not execute VR disable command

Table 120. R32 (Sheet 2 of 2)

Address: 32H Default: 00100000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b3	CAMP_PG_OUT_CTRL	RW	PMIC CAMP PWR_GOOD Output Signal Control. **CAMP_PG_OUT_CTRL** / **CAMP Pin** 0 / PMIC controls PWR_GOOD output on its own based on internal status 1 / PWR_GOOD output float When setting to '11', PMIC always floats the PWR_GOOD output signal even when there is an internal VR Disable command due to fault condition.
b2 ~ b0	Reserved	RV	Reserved

Table 121. R33 (Sheet 1 of 2)

Address: 33H Default: 00000000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b5	TEMP_MEAS	RO	PMIC Temperature Measurement. **TEMP_MEAS** / **PMIC Temp.** / **TEMP_MEAS** / **PMIC Temp.** 000 / ≤ 80°C / 100 / 110°C < x ≤ 120°C 001 / 80°C < x ≤ 90°C / 101 / 120°C < x ≤ 130°C 010 / 90°C < x ≤ 100°C / 110 / 130°C < x ≤ 140°C 011 / 100°C < x ≤ 110°C / 111 / > 140°C
b4	VIN_MGMT_PG_ SWOVER_MODE	RO	VIN_MGMT Input Power Good Status Switchover Mode Only. **VIN_MGMT_PG_SWOVER_MODE** / **VIN_MGMT Status** 0 / Power Not Good 1 / Power Good
b3	VBIAS_VIN_BULK _ UVLO_STATUS	RO	VBIAS Or VIN_BULK Under Voltage Lockout Status. **VBIAS_VIN_BULK_UVLO_STATUS** / **VBIAS or VIN_BULK Status** 0 / No Under-Voltage Lockout 1 / Under-Voltage Lockout VBIAS < 2.55V or VIN_BULK < 4.0V

Table 121. R33 (Sheet 2 of 2)

Address: 33H
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b2	LDO1P1_PG_STATUS	RO	VLDO_1.0V Output Power Good Status. **LDO1P0_PG_STATUS** / **LDO1P0 Status** 0 / Power Good 1 / Power Not Good LDO1P**0** < LDO1P0_PG_th (R1A[0])
b1 ~ b0	Reserved	RV	Reserved

Table 122. R34[1]

Address: 34H
Default: 00001110B

Data Bit	Data Name	Attribute	Function Description
b7	PEC_EN	RO	Packet Error Code (PEC) enable. Applicable only if R32[6]='1'. **PEC_EN** / **PEC Function** 0 / Disable 1 / Enable
b6	IBI_EN	RO	In-Band Interrupt (IBI) enable. Applicable only if R32[6]='1'. **IBI_EN** / **IBI Function** 0 / Disabled 1 / Enabled
b5	PARITY_DISABLE	RO	T Bit Parity Code Disable. Applicable only if R32[6]='1'. **PARITY_DISABLE** / **T Bit Parity Code Function** 0 / Enabled 1 / Disabled
b4	Reserved	RV	Reserved
b3 ~ b1	HID_CODE	RO	PMIC's 3-bit HID Code. **HID_CODE** / **HID_CODE** 000 / 100 001 / 101 010 / 110 011 / 111
b0	Reserved	RV	Reserved

1. The Write (or Update) transaction to this register must be followed by the STOP operation to allow the PMIC device to update the setting

Table 123. R35 (Sheet 1 of 2)

Address: 35H
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7	ERROR_INJ_ENABLE	RW	Error Injection Enable. ERROR_INJ_ENABLE: 0 = Disabled; 1 = Enabled
b6 ~ b4	ERROR_INJ_RAIL_SEL	RW	Error Injection - Input Rail and Output Rail Selection. 000 = Undefined; 001 = SWA Output only; 010 = SWB Output only; 011 = SWC Output only; 100 = SWD Output only; 101 = VIN_BULK Input only; 110 = VIN_MGMT Input only; 111 = Do Not Use This register is applicable only if bit R35[2:0]='000'. Any value other than '000' in both R35[6:4] and R35[2:0] is considered as an illegal setting and the PMIC operation is not guaranteed. If Dual-phase regulator is selected, use SWA encoding to inject the error. Register bit [3] selects either Over-Voltage or Under-voltage condition for the setting selected in this register.
b3	ERROR_INJ_OVUV	RW	Over-Voltage or Under-Voltage Selection for R35[6:4].. ERROR_INJ_OVUV: 0 = Over Voltage; 1 = Under Voltage This register is applicable only if bit R35[6:4] is anything other than '000'. The Under Voltage selection is only applied to SWx output rails and VIN_BULK supply. It doesn't apply to VIN_MGMT input.

Table 123. R35 (Sheet 2 of 2)

<table>
<tr>
<td>b2~ b0</td>
<td>ERROR_INJ_MISC_ TYPE</td>
<td>RW</td>
<td>Miscellaneous error injection type.
<table>
<tr><th>ERROR_INJ_ MISC_TYPE</th><th>Error Injection Type</th><th>ERROR_INJ_ MISC_TYPE</th><th>Error Injection Type</th></tr>
<tr><td>000</td><td>Undefined</td><td>100</td><td>VLDO_1.8V LDO Power Good</td></tr>
<tr><td>001</td><td>VIN_MGMT to VIN_BULK Switchover</td><td>101</td><td>High Current Consumption Warning</td></tr>
<tr><td>010</td><td>Critical Temperature Shutdown</td><td>110</td><td>Reserved</td></tr>
<tr><td>011</td><td>High Temperature Warning Threshold</td><td>111</td><td>Current Limiter Warning</td></tr>
</table>
This register is applicable only if bit R35[6:3]='0000'. Any value other than ‘000’ in both R35[6:4] and R35[2:0] is considered as an illegal setting and the PMIC operation is not guaranteed.
The High Current Consumption Warning and Current Limiter Warning selections apply to all enabled SWx output regulators at the same time.</td>
</tr>
</table>

Table 124. R37

Address: 37H **Default:**			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b0	DIMM_PW_LOWER_BYTE	WO	DIMM Vendor Memory Region (0x40 - 0x6F) Password – Lower Byte[7:0] = Code.

Table 125. R38

Address: 38H **Default:**			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b0	DIMM_PW_UPPER_BYTE	WO	DIMM Vendor Memory Region (0x40 - 0x6F) Password – Upper Byte[7:0] = Code.

Table 126. R39

Address: 39H Default: 00000000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b0	DIMM_PW_CONTROL	RW	Host Region Codes: 0x74: Clear registers R04 to R07, Erase MTP memory for R04 to R07 Register. DIMM Vendor Region (0x40 to 0x6F) Write Codes: 0x00: Lock DIMM Vendor Region. 0x40: Unlock DIMM Vendor Region. Password needs to be present in R37 & R38 registers. 0x80: Burn DIMM Vendor Region Password. New password needs to be present in R37 & R38. 0x81: Burn DIMM Vendor Region - 0x40 to 0x4F 0x82: Burn DIMM Vendor Region - 0x50 to 0x5F 0x85: Burn DIMM Vendor Region - 0x60 to 0x6F DIMM Vendor Region (0x40 to 0x6F) Read Codes: 0x5A: Burning is complete in DIMM Vendor region.

Table 127. R3A[1] (Sheet 1 of 2)

<table>
<tr><td colspan="4">Address: 3AH
Default: 00000000B</td></tr>
<tr><td>Data Bit</td><td>Data Name</td><td>Attribute</td><td>Function Description</td></tr>
<tr><td>b7</td><td>Reserved</td><td>RV</td><td>Reserved</td></tr>
<tr><td>b6</td><td>DEFAULT_READ
_ADDR_POINTER
_ENABLE</td><td>RW</td><td>Enable Default Address Read Pointer when PMIC sees STOP operation.
<table>
<tr><th>DEFAULT_READ_ADDR_
POINTER_ENABLE</th><th>Default Address Read Pointer</th></tr>
<tr><td>0</td><td>Disable Default Address Pointer
(address pointer is set by Host)</td></tr>
<tr><td>1</td><td>Enable Default Address Pointer;
Address selected by register bits[5:4].</td></tr>
</table>
When setting to ‘0’, the register setting in R3A[5:4] is a Don’t Care.</td></tr>
<tr><td>b5 ~ b4</td><td>DEFAULT_READ
_STARTING
_ADDRESS</td><td>RW</td><td>Default Read Address Pointer Selection when PMIC sees STOP operation. Only applicable if R3A[6]=’1’.
<table>
<tr><th>DEFAULT_READ_STARTING_ADDRESS</th><th>Default Read Address</th></tr>
<tr><td>00</td><td>R08</td></tr>
<tr><td>01</td><td>R0C</td></tr>
<tr><td>10</td><td>Reserved</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table></td></tr>
</table>

Table 127. R3A[1] (Sheet 2 of 2)

Address: 3AH
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b3 ~ b2	BURST_LEN_FOR_READ_DEF_ADDR_POINTER	RW	Burst Length (# of Bytes) to be transferred for Read Default Address Pointer Mode. Only applicable if if R3A [6] = '1' and R34 [7] = '1'. **BURST_LEN_FOR_READ_DEF_ADDR_POINTER** / **Burst length** 00 / 2 Bytes 01 / 4 Bytes 10 / Reserved 11 / 16 Bytes
b1 ~ b0	Reserved	RV	Reserved

1. The Write (or Update) transaction to this register must be followed by the STOP operation to allow the PMIC device to update the setting.

Table 128. R3B[1] (Sheet 1 of 2)

Address: 3BH
Default: 00010110

Data Bit	Data Name	Attribute	Function Description
b7 ~ b6	PMIC_CURRENT_CAPABILITY_EXT	ROE	PMIC Current Capability Extension. The register R3B[7:6] and R3B[0] provide 3-bit encoding as following: **PMIC_CURRENT_CAPABILITY_EXT** / **Type** 000 / Small PMIC (Low Current) 001 / Big PMIC (High Current) 01x / Extreme PMIC (Highest Current) All other encodings / Reserved
b5 ~ b4	REVISION_ID_MAJOR	ROE	Major Revision Stepping. **REVISION_ID_MAJOR** / **Revision** 00 / Revision 1 01 / Revision 2 10 / Revision 3 11 / Revision 4

Table 128. R3B[1] (Sheet 2 of 2)

Address: 3BH
Default: 00010110

Data Bit	Data Name	Attribute	Function Description
b3 ~ b1	REVISION_ID_ MINOR	ROE	Major Revision Stepping. REVISION_ID_MINOR / Revision / REVISION_ID_MINOR / Revision 000 / Revision 0 / 100 / Reserved 001 / Revision 1 / 101 / Reserved 010 / Revision 2 / 110 / Reserved 011 / Revision 3 / 111 / Reserved
b0	PMIC_CURRENT_ CAPABILITY	ROE	PMIC Current Capability. Also see R3B[7:6] definition. PMIC_CURRENT_CAPABILITY / Type 0 / Small PMIC (Low Current) 1 / Big PMIC (High Current)

1. The Revision Value is for M88P5010C3.

Table 129. R3C

Address: 3CH
Default: 0x86

Data Bit	Data Name	Attribute	Function Description
b7 ~ b0	VENDOR_ID_BYTE0	ROE	Vendor Identification Register Byte 0: 0x86. This is a fixed register.

Table 130. R3D

Address: 3DH
Default: 0x32

Data Bit	Data Name	Attribute	Function Description
b7 ~ b0	VENDOR_ID_BYTE1	ROE	Vendor Identification Register Byte 1: 0x32. This is a fixed register.

4.7 DIMM Vendor Region Registers

The default values of DIMM Vendor Region Registers are marked in gray, and are the same as the JEDEC spec. Contact Montage for the actual burn values of the related PMIC device.

Table 131. R40[1]

<table>
<tr><td colspan="4">Address: 40H
Default: 00000001B</td></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b7</td><td>ONSEQ_0</td><td>RWPE</td><td>PMIC Power On Sequence Config 0.
<table>
<tr><th>ONSEQ_0</th><th>Time Slot 0</th></tr>
<tr><td>0</td><td>Do Not Execute Config 0</td></tr>
<tr><td>1</td><td>Enable Config 0</td></tr>
</table></td></tr>
<tr><td>b6</td><td>ONSEQ_0_SWA_EN</td><td>RWPE</td><td>Enable SWA Output Regulator in Power On Sequence 0.
<table>
<tr><th>ONSEQ_0_SWA_EN</th><th>SWA Output Regulator</th></tr>
<tr><td>0</td><td>Disable SWA Output Regulator</td></tr>
<tr><td>1</td><td>Enable SWA Output Regulator</td></tr>
</table></td></tr>
<tr><td>b5</td><td>ONSEQ_0_SWB_EN</td><td>RWPE</td><td>Enable SWB Output Regulator in Power On Sequence 0.
Only applicable if R4F[0]=’0’. This bit is a Don’t Care when R4F[0]=’1’.
<table>
<tr><th>ONSEQ_0_SWB_EN</th><th>SWB Output Regulator</th></tr>
<tr><td>0</td><td>Disable SWB Output Regulator</td></tr>
<tr><td>1</td><td>Enable SWB Output Regulator</td></tr>
</table></td></tr>
<tr><td>b4</td><td>ONSEQ_0_SWC_EN</td><td>RWPE</td><td>Enable SWC Output Regulator in Power On Sequence 0.
<table>
<tr><th>ONSEQ_0_SWC_EN</th><th>SWC Output Regulator</th></tr>
<tr><td>0</td><td>Disable SWC Output Regulator</td></tr>
<tr><td>1</td><td>Enable SWC Output Regulator</td></tr>
</table></td></tr>
<tr><td>b3</td><td>ONSEQ_0_SWD_EN</td><td>RWPE</td><td>Enable SWD Output Regulator in Power On Sequence 0.
<table>
<tr><th>ONSEQ_0_SWD_EN</th><th>SWD Output Regulator</th></tr>
<tr><td>0</td><td>Disable SWD Output Regulator</td></tr>
<tr><td>1</td><td>Enable SWD Output Regulator</td></tr>
</table></td></tr>
<tr><td>b2 ~ b0</td><td>ONSEQ_0_IDLE</td><td>RWPE</td><td>Idle Time After Power On Sequence Config 0.
<table>
<tr><th>ONSEQ_0_IDLE</th><th>Idle Time</th><th>ONSEQ_0_IDLE</th><th>Idle Time</th></tr>
<tr><td>000</td><td>0 ms</td><td>100</td><td>8 ms</td></tr>
<tr><td>001</td><td>2 ms</td><td>101</td><td>10 ms</td></tr>
<tr><td>010</td><td>4 ms</td><td>110</td><td>12 ms</td></tr>
<tr><td>011</td><td>6 ms</td><td>111</td><td>24 ms</td></tr>
</table>
The idle time is the additional time after the soft-start time expires. The PMIC waits sum of soft start time and idle time before it executes the next power on sequence configuration register. If more than one regulator is enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.</td></tr>
</table>

1. If more than one configuration register is used for power on sequence, the first register must start at R40 and it must go in sequential order to R43 to turn on all desired regulators. In other words, there must not be any gap of the register that is used for power on sequence.

Table 132. R41[1,2] (Sheet 1 of 2)

<table>
<tr><th colspan="4">Address: 41H
Default: 00000001B</th></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b7</td><td>ONSEQ_1</td><td>RWPE</td><td>PMIC Power On Sequence Config 1.
<table><tr><th>ONSEQ_1</th><th>Time Slot 2</th></tr><tr><td>0</td><td>Do Not Execute Config 1</td></tr><tr><td>1</td><td>Enable Config 1</td></tr></table></td></tr>
<tr><td>b6</td><td>ONSEQ_1_SWA_EN</td><td>RWPE</td><td>Enable SWA Output Regulator in Power On Sequence 1.
<table><tr><th>ONSEQ_1_SWA_ENABLE</th><th>SWA Output Regulator</th></tr><tr><td>0</td><td>Disable SWA Output Regulator</td></tr><tr><td>1</td><td>Enable SWA Output Regulator</td></tr></table></td></tr>
<tr><td>b5</td><td>ONSEQ_1_SWB_EN</td><td>RWPE</td><td>Enable SWB Output Regulator in Power On Sequence 1.
Only applicable if R4F[0]=’0’. This bit is a Don’t Care when R4F[0]=’1’.
<table><tr><th>ONSEQ_1_SWB_ENABLE</th><th>SWB Output Regulator</th></tr><tr><td>0</td><td>Disable SWB Output Regulator</td></tr><tr><td>1</td><td>Enable SWB Output Regulator</td></tr></table></td></tr>
<tr><td>b4</td><td>ONSEQ_1_SWC_EN</td><td>RWPE</td><td>Enable SWC Output Regulator in Power On Sequence 1.
<table><tr><th>ONSEQ_1_SWC_ENABLE</th><th>SWC Output Regulator</th></tr><tr><td>0</td><td>Disable SWC Output Regulator</td></tr><tr><td>1</td><td>Enable SWC Output Regulator</td></tr></table></td></tr>
<tr><td>b3</td><td>ONSEQ_1_SWD_EN</td><td>RWPE</td><td>Enable SWD Output Regulator in Power On Sequence 1.
<table><tr><th>ONSEQ_1_SWD_ENABLE</th><th>SWD Output Regulator</th></tr><tr><td>0</td><td>Disable SWD Output Regulator</td></tr><tr><td>1</td><td>Enable SWD Output Regulator</td></tr></table></td></tr>
</table>

Table 132. R41[1,2] (Sheet 2 of 2)

Address: 41H Default: 00000001B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b2 ~ b0	ONSEQ_1_IDLE	RWPE	Idle Time After Power On Sequence Config 0. **ONSEQ_1_IDLE / Idle Time / ONSEQ_1_IDLE / Idle Time** 000 / 0 ms / 100 / 8 ms 001 / 2 ms / 101 / 10 ms 010 / 4 ms / 110 / 12 ms 011 / 6 ms / 111 / 24 ms The idle time is the additional time after the soft-start time expires. The PMIC waits sum of soft start time and idle time before it executes the next power on sequence configuration register. If more than one regulator is enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.

1. If any regulators are enabled in R40[6:3], those regulators must be configured as '1' in this sequence.
2. If more than one configuration register is used for power on sequence, the first register must start at R40 and it must go in sequential order to R43 to turn on all desired regulators. In other words, there must not be any gap of the register that is used for power on sequence.

Table 133. R42[1,2] (Sheet 1 of 2)

Address: 42H Default: 00000001B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7	ONSEQ_2	RWPE	PMIC Power On Sequence Config 2. **ONSEQ_2 / Time Slot 2** 0 / Do Not Execute Config 2 1 / Enable Config 2
b6	ONSEQ_2_SWA_EN	RWPE	Enable SWA Output Regulator in Power On Sequence 2. **ONSEQ_2_SWA_ENABLE / SWA Output Regulator** 0 / Disable SWA Output Regulator 1 / Enable SWA Output Regulator
b5	ONSEQ_2_SWB_EN	RWPE	Enable SWB Output Regulator in Power On Sequence 2. Only applicable if R4F[0]='0'. This bit is a Don't Care when R4F[0]='1'. **ONSEQ_2_SWB_ENABLE / SWB Output Regulator** 0 / Disable SWB Output Regulator 1 / Enable SWB Output Regulator

Table 133. R42[1,2] (Sheet 2 of 2)

Address: 42H
Default: 00000001B

Data Bit	Data Name	Attribute	Function Description
b4	ONSEQ_2_SWC_EN	RWPE	Enable SWC Output Regulator in Power On Sequence 2. ONSEQ_2_SWC_ENABLE: 0 = Disable SWC Output Regulator; 1 = Enable SWC Output Regulator
b3	ONSEQ_2_SWD_EN	RWPE	Enable SWD Output Regulator in Power On Sequence 2. ONSEQ_2_SWD_ENABLE: 0 = Disable SWD Output Regulator; 1 = Enable SWD Output Regulator
b2 ~ b0	ONSEQ_2_IDLE	RWPE	Idle Time After Power On Sequence Config 2. ONSEQ_2_IDLE / Idle Time: 000 = 0 ms; 001 = 2 ms; 010 = 4 ms; 011 = 6 ms; 100 = 8 ms; 101 = 10 ms; 110 = 12 ms; 111 = 24 ms The idle time is the additional time after the soft-start time expires. The PMIC waits sum of soft start time and idle time before it executes the next power on sequence configuration register. If more than one regulator is enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.

1. If any regulators are enabled in R40[6:3] or R41[6:3], those regulators must be configured as '1' in this sequence.
2. If more than one configuration register is used for power on sequence, the first register must start at R40 and it must go in sequential order to R43 to turn on all desired regulators. In other words, there must not be any gap of the register that is used for power on sequence.

Table 134. R43[1,2]

Address: 43H
Default: 00000001B

Data Bit	Data Name	Attribute	Function Description
b7	ONSEQ_3	RWPE	PMIC Power On Sequence Config 3. ONSEQ_3: 0 = Do Not Execute Config 3; 1 = Enable Config 3
b6	ONSEQ_3_SWA_EN	RWPE	Enable SWA Output Regulator in Power On Sequence 3. ONSEQ_3_SWA_ENABLE: 0 = Disable SWA Output Regulator; 1 = Enable SWA Output Regulator

Table 134. R43[1,2]

<table>
<tr><td colspan="4">Address: 43H
Default: 00000001B</td></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b5</td><td>ONSEQ_3_SWB_EN</td><td>RWPE</td><td>Enable SWB Output Regulator in Power On Sequence 3.
Only applicable if R4F[0]=’0’. This bit is a Don’t Care when R4F[0]=’1’.
<table>
<tr><th>ONSEQ_3_SWB_ENABLE</th><th>SWB Output Regulator</th></tr>
<tr><td>0</td><td>Disable SWB Output Regulator</td></tr>
<tr><td>1</td><td>Enable SWB Output Regulator</td></tr>
</table></td></tr>
<tr><td>b4</td><td>ONSEQ_3_SWC_EN</td><td>RWPE</td><td>Enable SWC Output Regulator in Power On Sequence 3.
<table>
<tr><th>ONSEQ_3_SWC_ENABLE</th><th>SWC Output Regulator</th></tr>
<tr><td>0</td><td>Disable SWC Output Regulator</td></tr>
<tr><td>1</td><td>Enable SWC Output Regulator</td></tr>
</table></td></tr>
<tr><td>b3</td><td>ONSEQ_3_SWD_EN</td><td>RWPE</td><td>Enable SWD Output Regulator in Power On Sequence 3.
<table>
<tr><th>ONSEQ_3_SWD_ENABLE</th><th>SWD Output Regulator</th></tr>
<tr><td>0</td><td>Disable SWD Output Regulator</td></tr>
<tr><td>1</td><td>Enable SWD Output Regulator</td></tr>
</table></td></tr>
<tr><td>b2 ~ b0</td><td>ONSEQ_3_IDLE</td><td>RWPE</td><td>Idle Time After Power On Sequence Config 3.
<table>
<tr><th>ONSEQ_3_IDLE</th><th>Idle Time</th><th>ONSEQ_3_IDLE</th><th>Idle Time</th></tr>
<tr><td>000</td><td>0 ms</td><td>100</td><td>8 ms</td></tr>
<tr><td>001</td><td>2 ms</td><td>101</td><td>10 ms</td></tr>
<tr><td>010</td><td>4 ms</td><td>110</td><td>12 ms</td></tr>
<tr><td>011</td><td>6 ms</td><td>111</td><td>24 ms</td></tr>
</table>
The idle time is the additional time after the soft-start time expires. The PMIC waits sum of soft start time and idle time before it executes the next power on sequence configuration register. If more than one regulator is enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.</td></tr>
</table>

1. If any regulators are enabled in R40[6:3] or R41[6:3] or R42[6:3], those regulators must be configured as '1' in this sequence.
2. If more than one configuration register is used for power on sequence, the first register must start at R40 and it must go in sequential order to R43 to turn on all desired regulators. In other words, there must not be any gap of the register that is used for power on sequence.

Table 135. R45

Address: 45H Default: 01111000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b1	SWA_VSET	RWPE	SWA Output Regulator Voltage setting. If R51[5]=1'b0: SWA Voltage=R45[7:1] * 5mV + 800mV. (Default: R45[7:1]=7'b0111100, SWA=1100mV) If R51[5]=1'b1: SWA Voltage=R45[7:1] * 5mV + 600mV. (Default: R45[7:1]=7'b0111100, SWA=900mV). PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1050mV to 1160mV.
b0	SWA_PGL_SET	RWPE	SWA Output Threshold Low Side Voltage For Power Good Status. **SWA_PGL_SET** / **SWA_PGL_th** 0 – -5% from the setting in R45[7:1] 1 – -7.5% from the setting in R45[7:1]

Table 136. R46 (Sheet 1 of 2)

Address: 46H Default: 01100000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b6	SWA_PGH_SET	RWPE	SWA Output Threshold High Side Voltage For Power Good Status. **SWA_PGH_SET** / **SWA_PGH_th** 00 – +5% from the setting in R45[7:1] 01 – +7.5% from the setting in R45[7:1] 10 – +10% from the setting in R45[7:1] 11 – Reserved
b5 ~ b4	SWA_OV_SET	RWPE	SWA Output Regulator Threshold for Over Voltage Status. This setting must be higher than Power Good High Side Voltage threshold in R46[7:6]. **SWA_OV_SET** / **SWA_OV_th** 00 – +7.5% from the setting in R45[7:1] 01 – +10% from the setting in R45[7:1] 10 – +12.5% from the setting in R45[7:1] 11 – Reserved

Table 136. R46 (Sheet 2 of 2)

Address: 46H Default: 01100000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b3 ~ b2	SWA_UV_SET	RWPE	SWA Output Regulator Threshold for Under Voltage Lockout Status. **SWA_UV_SET** / **SWA_UV_th** 00 / -10% from the setting in R45[7:1] 01 / -12.5% from the setting in R45[7:1] 10 / Reserved 11 / Reserved
b1 ~ b0	SWA_SSTOP_TIME	RWPE	SWA Output Regulator Soft Stop Time After VR Disable. This is the time it takes for buck regulator to go from steady state voltage to 0 V. **SWA_SSTOP_TIME** / **SSTOP Time** 00 / 0.5 ms 01 / 1 ms 10 / 2 ms 11 / 4 ms

Table 137. R47

Address: 47H Default: 01111000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b1	SWB_VSET	RWPE	SWB Output Regulator Voltage setting. Only applicable if R4F[0]='0'. If R51[4]=1'b0: SWB Voltage=R47[7:1] * 5mV + 800mV. (Default: R47[7:1]=7'b0111100, SWB=1100mV) If R51[4]=1'b1: SWB Voltage=R47[7:1] * 5mV + 600mV. (Default: R47[7:1]=7'b0111100, SWB=900mV). PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1050mV to 1160mV.
b0	SWB_PGL_SET	RWPE	SWB Output Threshold Low Side Voltage For Power Good Status. Only applicable if R4F[0]='0'. **SWB_PGL_SET** / **SWB_PGL_th** 0 / -5% from the setting in R47[7:1] 1 / -7.5% from the setting in R47[7:1]

Table 138. R48

Address: 48H Default: 01100000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b6	SWB_PGH_SET	RWPE	SWB Output Threshold High Side Voltage For Power Good Status. Only applicable if R4F[0]='0'. **SWB_PGH_SET** / **SWB_PGH_th** 00 / +5% from the setting in R47[7:1] 01 / +7.5% from the setting in R47[7:1] 10 / +10% from the setting in R47[7:1] 11 / Reserved
b5 ~ b4	SWB_OV_SET	RWPE	SWB Output Regulator Threshold for Over Voltage Status. This setting must be higher than Power Good High Side Voltage threshold in R48[7:6]. Only applicable if R4F[0]='0'. **SWB_OV_SET** / **SWB_OV_th** 00 / +7.5% from the setting in R47[7:1] 01 / +10% from the setting in R47[7:1] 10 / +12.5% from the setting in R47[7:1] 11 / Reserved
b3 ~ b2	SWB_UV_SET	RWPE	SWB Output Regulator Threshold for Under Voltage Lockout Status. Only applicable if R4F[0]='0'. **SWB_UV_SET** / **SWB_UV_th** 00 / -10% from the setting in R47[7:1] 01 / -12.5% from the setting in R47[7:1] 10 / Reserved 11 / Reserved
b1 ~ b0	SWB_SSTOP_TIME	RWPE	SWB Output Regulator Soft Stop Time After VR Disable. This is the time it takes for buck regulator to go from steady state voltage to 0V. Only applicable if R4F[0]='0'. **SWA_SSTOP_TIME** / **SSTOP Time** 00 / 0.5 ms 01 / 1 ms 10 / 2 ms 11 / 4 ms

Table 139. R49

Address: 49H Default: 01111000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b1	SWC_VSET	RWPE	SWC Output Regulator Voltage setting. If R51[3]=1'b0: SWC Voltage=R49[7:1] * 5mV + 800mV. (Default: R49[7:1]=7'b0111100, SWC=1100mV) If R51[3]=1'b1: SWC Voltage=R49[7:1] * 5mV + 600mV. (Default: R49[7:1]=7'b0111100, SWC=900mV). PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1050mV to 1160mV.
b0	SWC_PGL_SET	RWPE	SWC Output Threshold Low Side Voltage For Power Good Status.

SWC_PGL_SET	SWC_PGL_th
0	-5% from the setting in R49[7:1]
1	-7.5% from the setting in R49[7:1]

Table 140. R4A (Sheet 1 of 2)

Address: 4AH Default: 01100000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b6	SWC_PGH_SET	RWPE	SWC Output Threshold High Side Voltage For Power Good Status.

SWC_PGH_SET	SWC_PGH_th
00	+5% from the setting in R49[7:1]
01	+7.5% from the setting in R49[7:1]
10	+10% from the setting in R49[7:1]
11	Reserved

b5 ~ b4	SWC_OV_SET	RWPE	SWC Output Regulator Threshold for Over Voltage Status. This setting must be higher than Power Good High Side Voltage threshold in R4A[7:6].

SWC_OV_SET	SWC_OV_th
00	+7.5% from the setting in R49[7:1]
01	+10% from the setting in R49[7:1]
10	+12.5% from the setting in R49[7:1]
11	Reserved

Table 140. R4A (Sheet 2 of 2)

Address: 4AH Default: 01100000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b3 ~ b2	SWC_UV_SET	RWPE	SWC Output Regulator Threshold for Under Voltage Lockout Status. **SWC_UV_SET** / **SWC_UV_th** 00 / -10% from the setting in R49[7:1] 01 / -12.5% from the setting in R49[7:1] 10 / Reserved 11 / Reserved
b1 ~ b0	SWC_SSTOP_TIME	RWPE	SWC Output Regulator Soft Stop Time After VR Disable. This is the time it takes for buck regulator to go from steady state voltage to 0 V. **SWC_SSTOP_TIME** / **SSTOP Time** 00 / 0.5 ms 01 / 1 ms 10 / 2 ms 11 / 4 ms

Table 141. R4B

Address: 4BH Default: 01111000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7 ~ b1	SWD_VSET	RWPE	SWD Output Regulator Voltage setting. If R51[0]=1'b0: SWD Voltage=R4B[7:1] * 5mV + 1500mV. (Default: R4B[7:1]=7'b0111100, SWD=1800mV) If R51[0]=1'b1: SWD Voltage=R4B[7:1] * 5mV + 2200mV. (Default: R4B[7:1]=7'b0111100, SWD=2500mV). PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1750mV to 1850mV.
b0	SWD_PGL_SET	RWPE	SWD Output Threshold Low Side Voltage For Power Good Status. **SWD_PGL_SET** / **SWD_PGL_th** 0 / -5% from the setting in R4B[7:1] 1 / -7.5% from the setting in R4B[7:1]

Table 142. R4C

Address: 4CH
Default: 01100000B

Data Bit	Data Name	Attribute	Function Description
b7 ~ b6	SWD_PGH_SET	RWPE	SWD Output Threshold High Side Voltage For Power Good Status. SWD_PGH_SET: 00 = +5% from the setting in R4B[7:1]; 01 = +7.5% from the setting in R4B[7:1]; 10 = +10% from the setting in R4B[7:1]; 11 = Reserved
b5 ~ b4	SWD_OV_SET	RWPE	SWD Output Regulator Threshold for Over Voltage Status. This setting must be higher than Power Good High Side Voltage threshold in R4C[7:6]. SWD_OV_SET: 00 = +7.5% from the setting in R4B[7:1]; 01 = +10% from the setting in R4B[7:1]; 10 = +12.5% from the setting in R4B[7:1]; 11 = Reserved
b3 ~ b2	SWD_UV_SET	RWPE	SWD Output Regulator Threshold for Under Voltage Lockout Status. SWD_UV_SET: 00 = -10% from the setting in R4B[7:1]; 01 = -12.5% from the setting in R4B[7:1]; 10 = Reserved; 11 = Reserved
b1 ~ b0	SWD_SSTOP_TIME	RWPE	SWD Output Regulator Soft Stop Time After VR Disable. This is the time it takes for buck regulator to go from steady state voltage to 0 V. SWD_SSTOP_TIME: 00 = 1 ms; 01 = 2 ms; 10 = 4 ms; 11 = 8 ms

Table 143. R4D

<table>
<tr><td colspan="4">Address: 4DH
Default: 10011001B</td></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b7 ~ b6</td><td>SWA_MODE_SELECT</td><td>RWPE</td><td>SWA output regulator mode selection.
<table>
<tr><th>SWA_MODE_SELECT</th><th>SWA Switching Mode</th></tr>
<tr><td>00</td><td>Reserved</td></tr>
<tr><td>01</td><td>Reserved</td></tr>
<tr><td>10</td><td>COT; DCM
(Constant on Time; Discontinuous Current Mode)</td></tr>
<tr><td>11</td><td>COT; Forced CCM</td></tr>
</table></td></tr>
<tr><td>b5 ~ b4</td><td>SWA_FREQ</td><td>RWPE</td><td>SWA output regulator switching frequency.
<table>
<tr><th>SWA_FREQ</th><th>Switching Frequency</th></tr>
<tr><td>00</td><td>500 kHz</td></tr>
<tr><td>01</td><td>750 kHz[1]</td></tr>
<tr><td>10</td><td>1000 kHz</td></tr>
<tr><td>11</td><td>1250 kHz</td></tr>
</table>
1. 750kHz setting is required to achieve good performance of efficiency and load transient response.</td></tr>
<tr><td>b3 ~ b2</td><td>SWB_MODE_SELECT</td><td>RWPE</td><td>SWB output regulator mode selection. Only applicable if R4F[0] = '0'.
<table>
<tr><th>SWB_MODE_SELECT</th><th>SWB Switching Mode</th></tr>
<tr><td>00</td><td>Reserved</td></tr>
<tr><td>01</td><td>Reserved</td></tr>
<tr><td>10</td><td>COT; DCM
(Constant on Time; Discontinuous Current Mode)</td></tr>
<tr><td>11</td><td>COT; Forced CCM</td></tr>
</table></td></tr>
<tr><td>b1 ~ b0</td><td>SWB_FREQ</td><td>RWPE</td><td>SWB output regulator switching frequency. Only applicable if R4F[0] = '0'.
<table>
<tr><th>SWB_FREQ</th><th>Switching Frequency</th></tr>
<tr><td>00</td><td>500 kHz</td></tr>
<tr><td>01</td><td>750 kHz[1]</td></tr>
<tr><td>10</td><td>1000 kHz</td></tr>
<tr><td>11</td><td>1250 kHz</td></tr>
</table>
1. 750kHz setting is required to achieve good performance of efficiency and load transient response.</td></tr>
</table>

Table 144. R4E

<table>
<tr><th colspan="4">Address: 4EH
Default: 10011001B</th></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b7 ~ b6</td><td>SWC_MODE_SELECT</td><td>RWPE</td><td>SWC output regulator mode selection.
<table>
<tr><th>SWC_MODE_SELECT</th><th>SWC Switching Mode</th></tr>
<tr><td>00</td><td>Reserved</td></tr>
<tr><td>01</td><td>Reserved</td></tr>
<tr><td>10</td><td>COT; DCM
(Constant on Time; Discontinuous Current Mode)</td></tr>
<tr><td>11</td><td>COT; Forced CCM</td></tr>
</table></td></tr>
<tr><td>b5 ~ b4</td><td>SWC_FREQ</td><td>RWPE</td><td>SWC output regulator switching frequency.
<table>
<tr><th>SWC_FREQ</th><th>Switching Frequency</th></tr>
<tr><td>00</td><td>500 kHz</td></tr>
<tr><td>01</td><td>750 kHz[1]</td></tr>
<tr><td>10</td><td>1000 kHz</td></tr>
<tr><td>11</td><td>1250 kHz</td></tr>
</table>
1. 750kHz setting is required to achieve good performance of efficiency and load transient response.</td></tr>
<tr><td>b3 ~ b2</td><td>SWD_MODE_SELECT</td><td>RWPE</td><td>SWD output regulator mode selection. Only applicable if R4F[0] = '0'.
<table>
<tr><th>SWD_MODE_SELECT</th><th>SWD Switching Mode</th></tr>
<tr><td>00</td><td>Reserved</td></tr>
<tr><td>01</td><td>Reserved</td></tr>
<tr><td>10</td><td>COT; DCM
(Constant on Time; Discontinuous Current Mode)</td></tr>
<tr><td>11</td><td>COT; Forced CCM</td></tr>
</table></td></tr>
<tr><td>b1 ~ b0</td><td>SWD_FREQ</td><td>RWPE</td><td>SWD output regulator switching frequency. Only applicable if R4F[0] = '0'.
<table>
<tr><th>SWD_FREQ</th><th>Switching Frequency</th></tr>
<tr><td>00</td><td>500 kHz</td></tr>
<tr><td>01</td><td>750 kHz[1]</td></tr>
<tr><td>10</td><td>1000 kHz</td></tr>
<tr><td>11</td><td>1250 kHz</td></tr>
</table>
1. 750kHz setting is required to achieve good performance of efficiency and load transient response.</td></tr>
</table>

Table 145. R4F

Address: 4FH
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7	SW_DISABLE_CTRL	RWPE	Output Regulators SWA, SWB, SWC and SWD Disable Control for OV and UV. Applicable to Output OV, Output UV and Output OC. For VIN_BULK input over voltage, this bit does not apply and the PMIC always disables all switching regulators. **SW_DISABLE_CTRL** / **Regulators** 0 / Disable all switching regulators of PMIC 1 / Disable only the effected switching output regulator. The rest of the PMIC's switching regulators remains operational. For standard DDR5 RDIMM and DDR5 LRDIMM, this bit must be always configured to '0'. For DDR5 NVDIMM or any other custom DIMM, this bit can be configured to either '0' or '1' as desired.
b6 ~ b5	Reserved	RV	Reserved
b4	SWA_REMOTE_SEN	RWPE	SWA Output Regulator Remote Sensing Scheme on DIMM. **SWA_REMOTE_SEN** / **SWA Remote Sensing** 0 / Single-Ended Remote Sensing on DIMM. 1 / Differential Remote Sensing on DIMM
b3	Reserved	RV	Reserved
b2	SWC_REMOTE_SEN	RWPE	SWC Output Regulator Remote Sensing Scheme on DIMM. **SWC_REMOTE_SEN** / **SWC Remote Sensing** 0 / Single-Ended Remote Sensing on DIMM. 1 / Differential Remote Sensing on DIMM
b1	SWD_REMOTE_SEN	RWPE	SWD Output Regulator Remote Sensing Scheme on DIMM. **SWD_REMOTE_SEN** / **SWD Remote Sensing** 0 / Single-Ended Remote Sensing on DIMM. (Use SWD_FB_N pin as PID input pin to determine PMIC's ID) 1 / Differential Remote Sensing on DIMM When setting to '0', up to three different PMICs can be placed on the DIMM module. When setting to '1', only one PMIC can be placed on the DIMM module.
b0	SWAB_PHASE_MODE	RWPE	SWA and SWB Phase Regulator Mode Selection. **SWAB_PHASE_MODE** / **SWA/B Regulator Mode** 0 / Single Phase Regulator Mode 1 / Dual Phase Regulator Mode

Table 146. R50 (Sheet 1 of 2)

Address: 50H
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description[1]
b7 ~ b6	SWA_OCW_SET	RWPE	SWA Output Current Limiter Warning Threshold Setting. (COT Valley current limit) Low Current PMIC Encoding Definition (PMIC5010): **SWA_OCW_SET** / **SWA_OCW_th** 00 / 2.0 A 01 / 2.5 A 10 / 3.0 A 11 / 3.5 A High Current PMIC Encoding Definition (PMIC5000): **SWA_OCW_SET** / **SWA_OCW_th** 00 / 4.0 A 01 / 4.5 A 10 / 5.0 A 11 / 5.5 A
b5 ~ b4	SWB_OCW_SET	RWPE	SWB Output Current Limiter Warning Threshold Setting. (COT Valley current limit) This register is applicable regardless of the setting in R4F[0]. If R4F[0] = '1', this register must be configured identically as bits R50[7:6]. Low Current PMIC Encoding Definition (PMIC5010). **SWB_OCW_SET** / **SWB_OCW_th** 00 / 2.0 A 01 / 2.5 A 10 / 3.0 A 11 / 3.5 A High Current PMIC Encoding Definition (PMIC5000): **SWB_OCW_SET** / **SWB_OCW_th** 00 / 4.0 A 01 / 4.5 A 10 / 5.0 A 11 / 5.5 A

Table 146. R50 (Sheet 2 of 2)

Address: 50H
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description[1]
b3 ~ b2	SWC_OCW_SET	RWPE	SWC Output Current Limiter Warning Threshold Setting. (COT Valley current limit) Low Current PMIC Encoding Definition (PMIC5010): **SWC_OCW_SET** / **SWC_OCW_th** 00 / 2.0 A 01 / 2.5 A 10 / 3.0 A 11 / 3.5 A High Current PMIC Encoding Definition (PMIC5000): **SWC_OCW_SET** / **SWC_OCW_th** 00 / 4.0 A 01 / 4.5 A 10 / 5.0 A 11 / 5.5 A
b1 ~ b0	SWD_OCW_SET	RWPE	SWD Output Current Limiter Warning Threshold Setting. (COT Valley current limit) Low Current PMIC Encoding Definition (PMIC5010): **SWD_OCW_SET** / **SWD_OCW_th** 00 / 2.0 A 01 / 2.5 A 10 / 3.0 A 11 / 3.5 A High Current PMIC Encoding Definition (PMIC5000): **SWD_OCW_SET** / **SWD_OCW_th** 00 / 4.0 A 01 / 4.5 A 10 / 5.0 A 11 / 5.5 A

1. Please set valley current limit to "11" code for full load current operation.

Table 147. R51

Address: 51H
Default: 01000010B

Data Bit	Data Name	Attribute	Function Description
b7 ~ b6	LDO1P8_VSET	RWPE	VLDO_1.8V LDO Output Voltage Setting. **LDO1P8_VSET** / **VLDO_1.8V LDO Voltage** 00 / 1.7 V 01 / 1.8 V 10 / 1.9 V 11 / Reserved The VLDO_1.8V Power Good threshold in register R1A[2] is always fixed regardless of the setting in this register.
b5	SWA_RANGE	RWPE	SWA Output Voltage Range Selection. Apply to Register R45[7:1] **SWA_RANGE** / **SWA Output Voltage Range** 0 / Range: 800 mV to 1435 mV for SWA; 5mV step size 1 / Range: 600 mV to 1235 mV for SWA; 5mV step size
b4	SWB_RANGE	RWPE	SWB Output Voltage Range Selection. Apply to Register R47[7:1] **SWB_RANGE** / **SWB Output Voltage Range** 0 / Range: 800 mV to 1435 mV for SWB; 5mV step size 1 / Range: 600 mV to 1235 mV for SWB; 5mV step size
b3	SWC_RANGE	RWPE	SWC Output Voltage Range Selection. Apply to Register R49[7:1]. Only applicable if R4F[0]=’0’. **SWC_RANGE** / **SWC Output Voltage Range** 0 / Range: 800 mV to 1435 mV for SWC; 5mV step size 1 / Range: 600 mV to 1235 mV for SWC; 5mV step size
b2 ~ b1	LDO1P0_VSET	RWPE	VLDO_1.0V LDO Output Voltage Setting. **LDO1P0_VSET** / **VLDO_1.0V LDO Voltage** 00 / 0.9 V 01 / 1.0 V 10 / 1.1 V 11 / 1.2 V
b0	SWD_RANGE	RWPE	SWD Output Voltage Range Selection. Apply to Register R4B[7:1] **SWD_RANGE** / **SWD Output Voltage Range** 0 / Range: 1500 mV to 2135 mV for SWD; 5mV step size 1 / Range: 2200 mV to 2835 mV for SWD; 5mV step size

Table 148. R58[1]

Address: 58H
Default: 00000000B

Data Bit	Data Name	Attribute	Function Description
b7	OFFSEQ_0	RWPE	PMIC Power Off Sequence 0. OFFSEQ_0 = 0: Do Not Execute Config 0 OFFSEQ_0 = 1: Execute Config 0
b6	OFFSEQ_0_SWA_DIS	RWPE	Disable SWA Output Regulator in Power On Sequence 0. OFFSEQ_0_SWA_DIS = 0: Do Not Disable SWA Output Regulator OFFSEQ_0_SWA_DIS = 1: Disable SWA Output Regulator
b5	OFFSEQ_0_SWB_DIS	RWPE	Disable SWB Output Regulator in Power On Sequence 0. Only applicable if R4F[0]='0'. This bit is a Don't Care when R4F[0]='1'. OFFSEQ_0_SWB_DIS = 0: Do Not Disable SWB Output Regulator OFFSEQ_0_SWB_DIS = 1: Disable SWB Output Regulator
b4	OFFSEQ_0_SWC_DIS	RWPE	Disable SWC Output Regulator in Power On Sequence 0. OFFSEQ_0_SWC_DIS = 0: Do Not Disable SWC Output Regulator OFFSEQ_0_SWC_DIS = 1: Disable SWC Output Regulator
b3	OFFSEQ_0_SWD_DIS	RWPE	Disable SWD Output Regulator in Power On Sequence 0. OFFSEQ_0_SWD_DIS = 0: Do Not Disable SWD Output Regulator OFFSEQ_0_SWD_DIS = 1: Disable SWD Output Regulator
b2 ~ b0	OFFSEQ_0_IDLE	RWPE	Idle Time After Power Off Sequence Config 0. 000: 0 ms; 001: 1 ms; 010: 2 ms; 011: 3 ms; 100: 4 ms; 101: 5 ms; 110: 6 ms; 111: 7 ms The idle time is the additional time after the soft-stop time expires. The PMIC waits sum of the soft stop time and the idle time before it executes the next Power Off sequence configuration register. If more than one regulator is enabled, the PMIC uses the largest value of the soft stop time among the regulators that are enabled in this configuration register.

1. If more than one configuration register is used for power off sequence, the first register must start at R58 and it must go in sequential order to R5B to turn off all desired regulators. In other words, there must not be any gap of the register that is used for the power off sequence.

Table 149. R59[1,2]

Address: 59H Default: 00000000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7	OFFSEQ_1	RWPE	PMIC Power Off Sequence 1. **OFFSEQ_1** / **Time Slot 1** 0 / Do Not Execute Config 1 1 / Execute Config 1
b6	OFFSEQ_1_SWA_DIS	RWPE	Disable SWA Output Regulator in Power On Sequence 1. **OFFSEQ_1_SWA_DIS** / **SWA Output Regulator** 0 / Do Not Disable SWA Output Regulator 1 / Disable SWA Output Regulator
b5	OFFSEQ_1_SWB_DIS	RWPE	Disable SWB Output Regulator in Power On Sequence 1. Only applicable if R4F[0]='0'. This bit is a Don't Care when R4F[0]='1'. **OFFSEQ_1_SWB_DIS** / **SWB Output Regulator** 0 / Do Not Disable SWB Output Regulator 1 / Disable SWB Output Regulator
b4	OFFSEQ_1_SWC_DIS	RWPE	Disable SWC Output Regulator in Power On Sequence 1. **OFFSEQ_1_SWC_DIS** / **SWC Output Regulator** 0 / Do Not Disable SWC Output Regulator 1 / Disable SWC Output Regulator
b3	OFFSEQ_1_SWD_DIS	RWPE	Disable SWD Output Regulator in Power On Sequence 1. **OFFSEQ_1_SWD_DIS** / **SWD Output Regulator** 0 / Do Not Disable SWD Output Regulator 1 / Disable SWD Output Regulator
b2 ~ b0	OFFSEQ_1_IDLE	RWPE	Idle Time After Power Off Sequence Config 1. **OFFSEQ_1_IDLE** / **Idle Time** / **OFFSEQ_1_IDLE** / **Idle Time** 000 / 0 ms / 100 / 4 ms 001 / 1 ms / 101 / 5 ms 010 / 2 ms / 110 / 6 ms 011 / 3 ms / 111 / 7 ms The idle time is the additional time after the soft-stop time expires. The PMIC waits sum of the soft stop time and the idle time before it executes the next Power Off sequence configuration register. If more than one regulator is enabled, the PMIC uses the largest value of the soft stop time among the regulators that are enabled in this configuration register.

1. If any regulators are enabled in R58[6:3], those regulators must be configured as '1' in this sequence.
2. If more than one configuration register is used for power off sequence, the first register must start at R58 and it must go in sequential order to R5B to turn off all desired regulators. In other words, there must not be any gap of the register that is used for the power off sequence.

Table 150. R5A[1,2]

Address: 5AH Default: 00000000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7	OFFSEQ_2	RWPE	PMIC Power Off Sequence 2. **OFFSEQ_2** / **Time Slot 2** 0 / Do Not Execute Config 2 1 / Execute Config 2
b6	OFFSEQ_2_SWA_DIS	RWPE	Disable SWA Output Regulator in Power On Sequence 2. **OFFSEQ_2_SWA_DIS** / **SWA Output Regulator** 0 / Do Not Disable SWA Output Regulator 1 / Disable SWA Output Regulator
b5	OFFSEQ_2_SWB_DIS	RWPE	Disable SWB Output Regulator in Power On Sequence 2. Only applicable if R4F[0]='0'. This bit is a Don't Care when R4F[0]='1'. **OFFSEQ_2_SWB_DIS** / **SWB Output Regulator** 0 / Do Not Disable SWB Output Regulator 1 / Disable SWB Output Regulator
b4	OFFSEQ_2_SWC_DIS	RWPE	Disable SWC Output Regulator in Power On Sequence 2. **OFFSEQ_2_SWC_DIS** / **SWC Output Regulator** 0 / Do Not Disable SWC Output Regulator 1 / Disable SWC Output Regulator
b3	OFFSEQ_2_SWD_DIS	RWPE	Disable SWD Output Regulator in Power On Sequence 2. **OFFSEQ_2_SWD_DIS** / **SWD Output Regulator** 0 / Do Not Disable SWD Output Regulator 1 / Disable SWD Output Regulator
b2 ~ b0	OFFSEQ_2_IDLE	RWPE	Idle Time After Power Off Sequence Config 2. **OFFSEQ_2_IDLE** / **Idle Time** / **OFFSEQ_2_IDLE** / **Idle Time** 000 / 0 ms / 100 / 4 ms 001 / 1 ms / 101 / 5 ms 010 / 2 ms / 110 / 6 ms 011 / 3 ms / 111 / 7 ms The idle time is the additional time after the soft-stop time expires. The PMIC waits sum of the soft stop time and the idle time before it executes the next Power Off sequence configuration register. If more than one regulator is enabled, the PMIC uses the largest value of the soft stop time among the regulators that are enabled in this configuration register.

1. If any regulators are enabled in R58[6:3] or R59[6:3], those regulators must be configured as '1' in this sequence.
2. If more than one configuration register is used for power off sequence, the first register must start at R58 and it must go in sequential order to R5B to turn off all desired regulators. In other words, there must not be any gap of the register that is used for the power off sequence.

Table 151. R5B[1,2]

Address: 5BH Default: 00000000B			
Data Bit	**Data Name**	**Attribute**	**Function Description**
b7	OFFSEQ_3	RWPE	PMIC Power Off Sequence 3. **OFFSEQ_3** / **Time Slot 3** 0 / Do Not Execute Config 3 1 / Execute Config 3
b6	OFFSEQ_3_SWA_DIS	RWPE	Disable SWA Output Regulator in Power On Sequence 3. **OFFSEQ_3_SWA_DIS** / **SWA Output Regulator** 0 / Do Not Disable SWA Output Regulator 1 / Disable SWA Output Regulator
b5	OFFSEQ_3_SWB_DIS	RWPE	Disable SWB Output Regulator in Power On Sequence 3. Only applicable if R4F[0]='0'. This bit is a Don't Care when R4F[0]='1'. **OFFSEQ_3_SWB_DIS** / **SWB Output Regulator** 0 / Do Not Disable SWB Output Regulator 1 / Disable SWB Output Regulator
b4	OFFSEQ_3_SWC_DIS	RWPE	Disable SWC Output Regulator in Power On Sequence 3. **OFFSEQ_3_SWC_DIS** / **SWC Output Regulator** 0 / Do Not Disable SWC Output Regulator 1 / Disable SWC Output Regulator
b3	OFFSEQ_3_SWD_DIS	RWPE	Disable SWD Output Regulator in Power On Sequence 3. **OFFSEQ_3_SWD_DIS** / **SWD Output Regulator** 0 / Do Not Disable SWD Output Regulator 1 / Disable SWD Output Regulator
b2 ~ b0	Reserved	RV	Reserved

1. If any regulators are enabled in R58[6:3] or R59[6:3] or R5A[6:3], those regulators must be configured as '1' in this sequence.
2. If more than one configuration register is used for power off sequence, the first register must start at R58 and it must go in sequential order to R5B to turn off all desired regulators. In other words, there must not be any gap of the register that is used for power off sequence.

Table 152. R5D

<table>
<tr><th colspan="4">Address: 5DH
Default: 00100010B</th></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b7 ~ b5</td><td>SWA_SSTRT_TIME</td><td>RWPE</td><td>SWA Output Regulator Soft Start Time After VR Enable. This is the time it takes for buck regulator to go from 0 V to the steady state voltage.
<table>
<tr><th>SWA_SSTRT_TIME</th><th>SSTRT Time</th><th>SWA_SSTRT_TIME</th><th>SSTRT Time</th></tr>
<tr><td>000</td><td>1 ms</td><td>100</td><td>8 ms</td></tr>
<tr><td>001</td><td>2 ms</td><td>101</td><td>10 ms</td></tr>
<tr><td>010</td><td>4 ms</td><td>110</td><td>12 ms</td></tr>
<tr><td>011</td><td>6 ms</td><td>111</td><td>14 ms</td></tr>
</table></td></tr>
<tr><td>b4</td><td>Reserved</td><td>RV</td><td>Reserved</td></tr>
<tr><td>b3 ~ b1</td><td>SWB_SSTRT_TIME</td><td>RWPE</td><td>SWB Output Regulator Soft Start Time After VR Enable. This is the time it takes for buck regulator to go from 0 V to the steady state voltage.
Only applicable if R4F[0] = '0'.
<table>
<tr><th>SWB_SSTRT_TIME</th><th>SSTRT Time</th><th>SWB_SSTRT_TIME</th><th>SSTRT Time</th></tr>
<tr><td>000</td><td>1 ms</td><td>100</td><td>8 ms</td></tr>
<tr><td>001</td><td>2 ms</td><td>101</td><td>10 ms</td></tr>
<tr><td>010</td><td>4 ms</td><td>110</td><td>12 ms</td></tr>
<tr><td>011</td><td>6 ms</td><td>111</td><td>14 ms</td></tr>
</table></td></tr>
<tr><td>b0</td><td>Reserved</td><td>RV</td><td>Reserved</td></tr>
</table>

Table 153. R5E (Sheet 1 of 2)

<table>
<tr><th colspan="4">Address: 5EH
Default: 00100010B</th></tr>
<tr><th>Data Bit</th><th>Data Name</th><th>Attribute</th><th>Function Description</th></tr>
<tr><td>b7 ~ b5</td><td>SWC_SSTRT_TIME</td><td>RWPE</td><td>SWC Output Regulator Soft Start Time After VR Enable. This is the time it takes for buck regulator to go from 0 V to the steady state voltage.
<table>
<tr><th>SWC_SSTRT_TIME</th><th>SSTRT Time</th><th>SWC_SSTRT_TIME</th><th>SSTRT Time</th></tr>
<tr><td>000</td><td>1 ms</td><td>100</td><td>8 ms</td></tr>
<tr><td>001</td><td>2 ms</td><td>101</td><td>10 ms</td></tr>
<tr><td>010</td><td>4 ms</td><td>110</td><td>12 ms</td></tr>
<tr><td>011</td><td>6 ms</td><td>111</td><td>14 ms</td></tr>
</table></td></tr>
<tr><td>b4</td><td>Reserved</td><td>RV</td><td>Reserved</td></tr>
</table>

Table 153. R5E (Sheet 2 of 2)

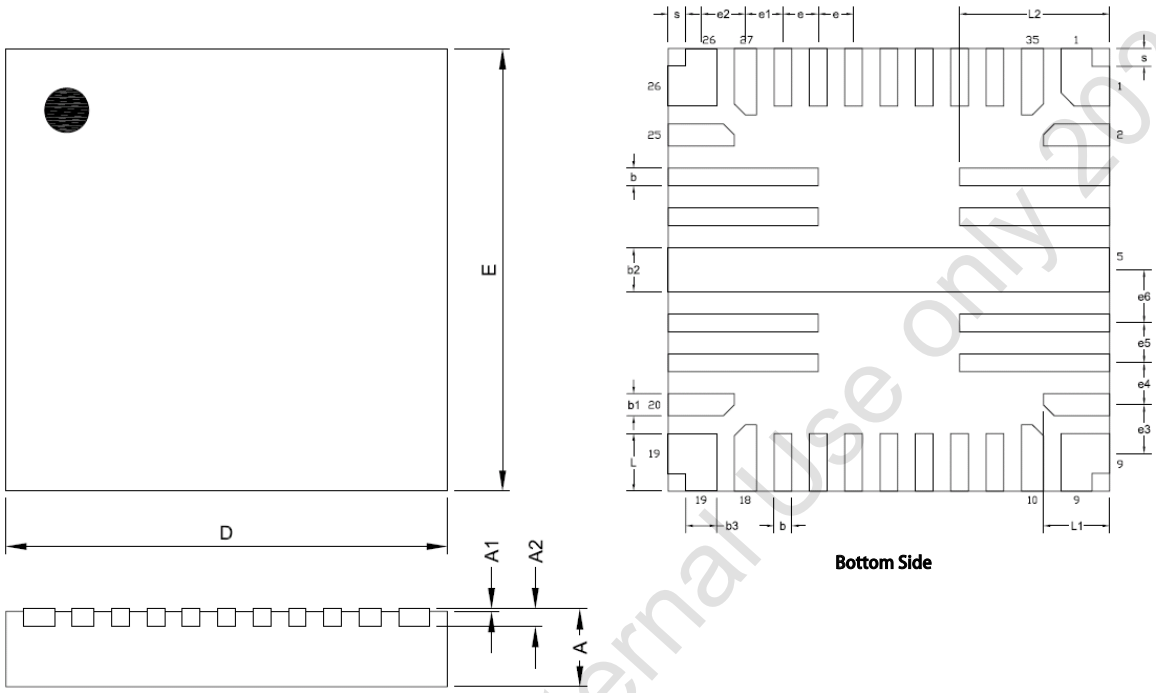
Address: 5EH
Default: 00100010B

Data Bit	Data Name	Attribute	Function Description
b3 ~ b1	SWD_SSTRT_TIME	RWPE	SWD Output Regulator Soft Start Time After VR Enable. This is the time it takes for buck regulator to go from 0V to the steady state voltage. Only applicable if R4F[0] = '0'.
b0	Reserved	RV	Reserved

SWD_SSTRT_TIME	SSTRT Time	SWD_SSTRT_TIME	SSTRT Time
000	1 ms	100	8 ms
001	2 ms	101	10 ms
010	4 ms	110	12 ms
011	6 ms	111	14 ms

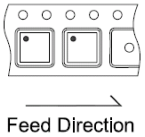
5 Mechanical Package Data

Figure 28. Package Outline



Symbol	Dimension in mm			Dimension in inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.80	0.85	0.90	0.0315	0.0335	0.0354
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 Ref.			0.0079 Ref.		
D	4.95	5.00	5.05	0.1949	0.1969	0.1988
E	4.95	5.00	5.05	0.1949	0.1969	0.1988
b (22x)	0.15	0.20	0.25	0.0059	0.0079	0.0098
b1 (8x)	0.20	0.25	0.30	0.0079	0.0098	0.0118
b2	0.45	0.50	0.55	0.0117	0.0197	0.0217
b3 (4x)	0.30	0.35	0.40	0.0118	0.0138	0.0157
e (12x)	0.400 BSC			0.0157 BSC		
e1 (4x)	0.425 BSC			0.0167 BSC		
e2 (4x)	0.500 BSC			0.0197 BSC		
e3 (4x)	0.550 BSC			0.0217 BSC		
e4 (4x)	0.475 BSC			0.0187 BSC		
e5 (4x)	0.450 BSC			0.0177 BSC		
e6 (4x)	0.600 BSC			0.0236 BSC		
L (18x)	0.60	0.65	0.70	0.0236	0.0256	0.0276
L1 (8x)	0.70	0.75	0.80	0.0276	0.0295	0.0315
L2 (8x)	1.65	1.70	1.75	0.0650	0.0669	0.0689
s (8x)	0.15	0.20	0.25	0.0059	0.0079	0.0098

Taping Specification



Package	Q'TY/Reel
FCQFN5X5 -35	3,000 ea