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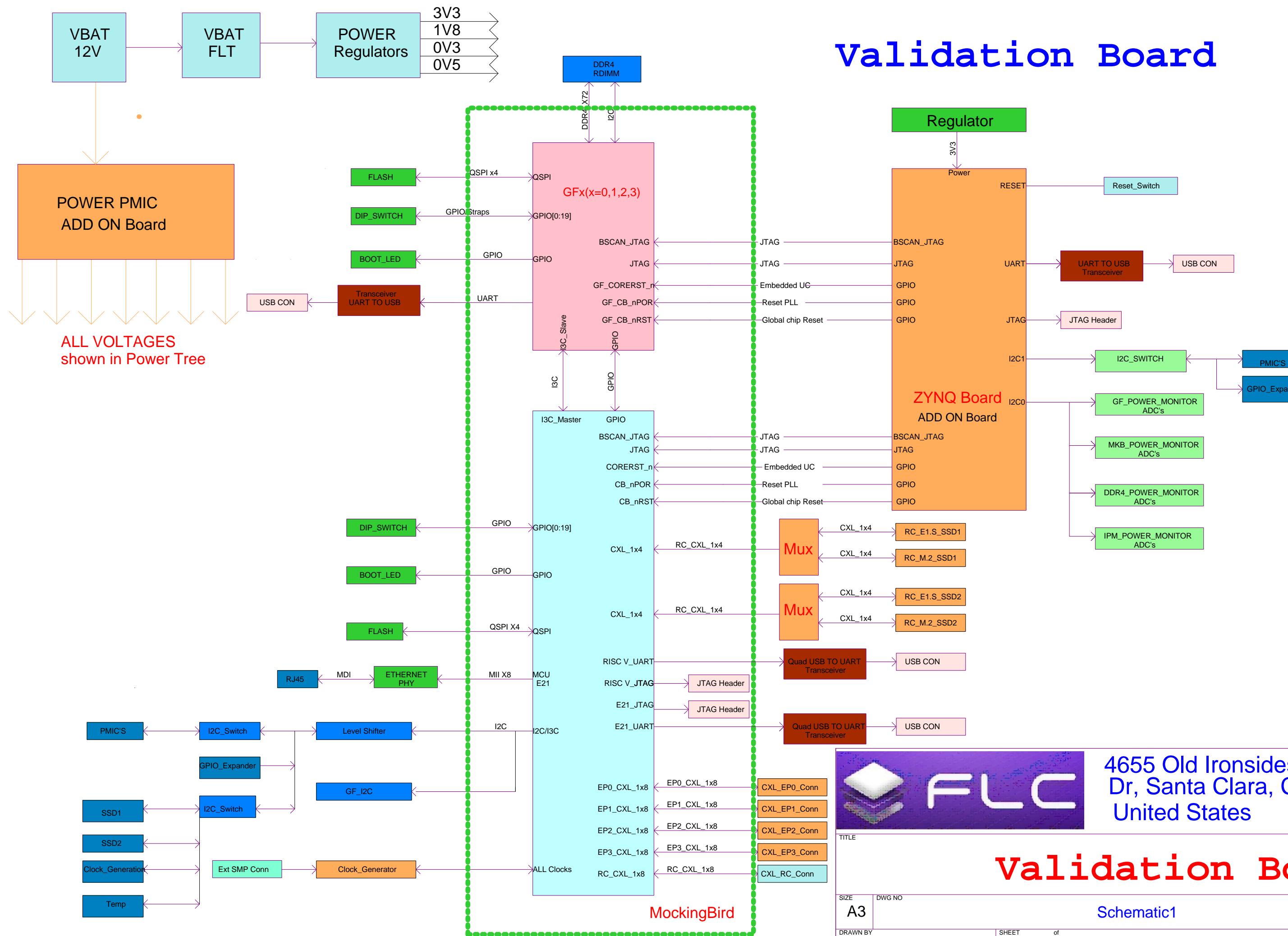
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				→ 62	GF0_RESET
				→ 63	GF1_RESET
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				→ 65	GF3_RESET



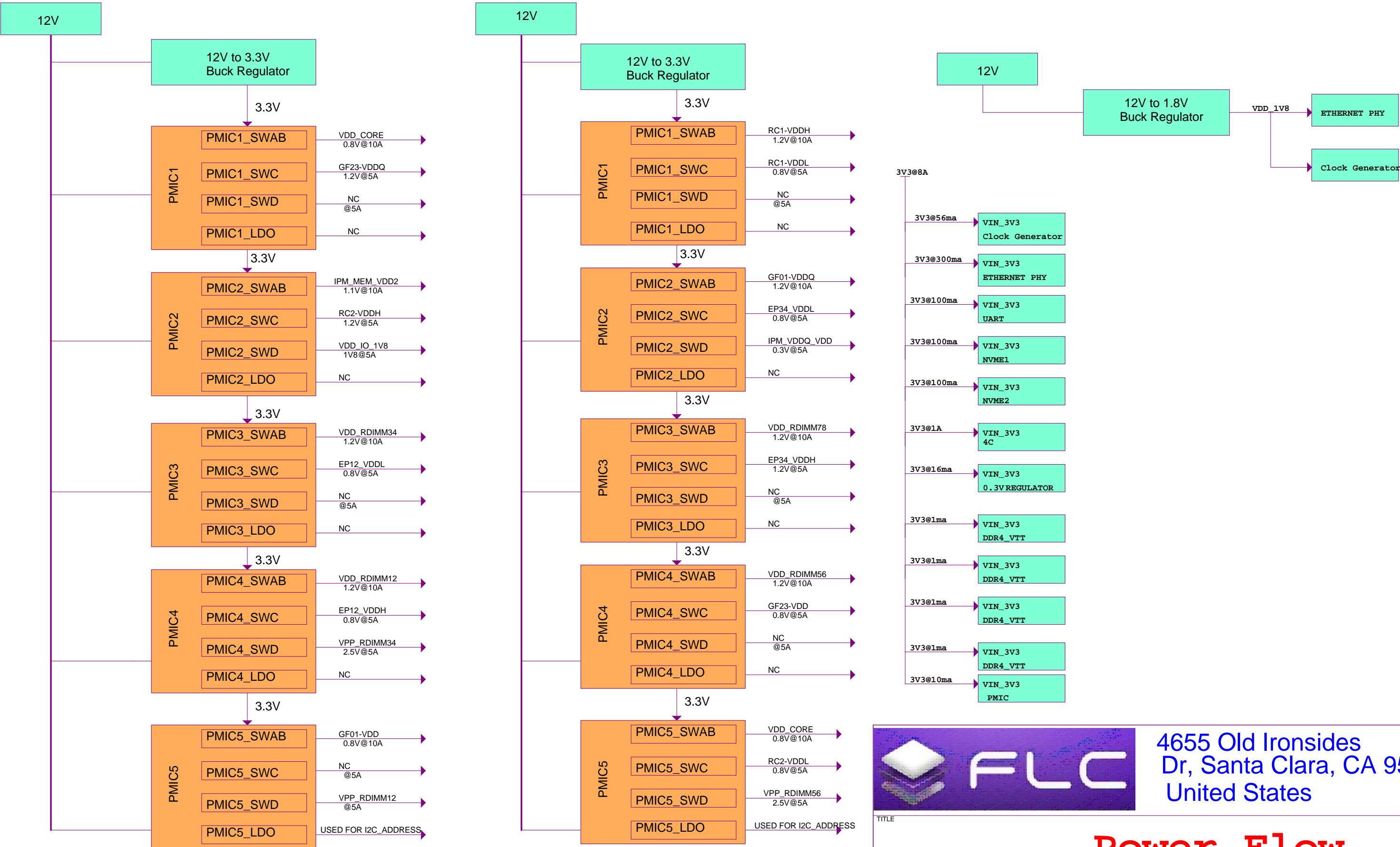
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Dr, Santa Clara, CA 95054,
United States

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Validation Board



Power_Flow



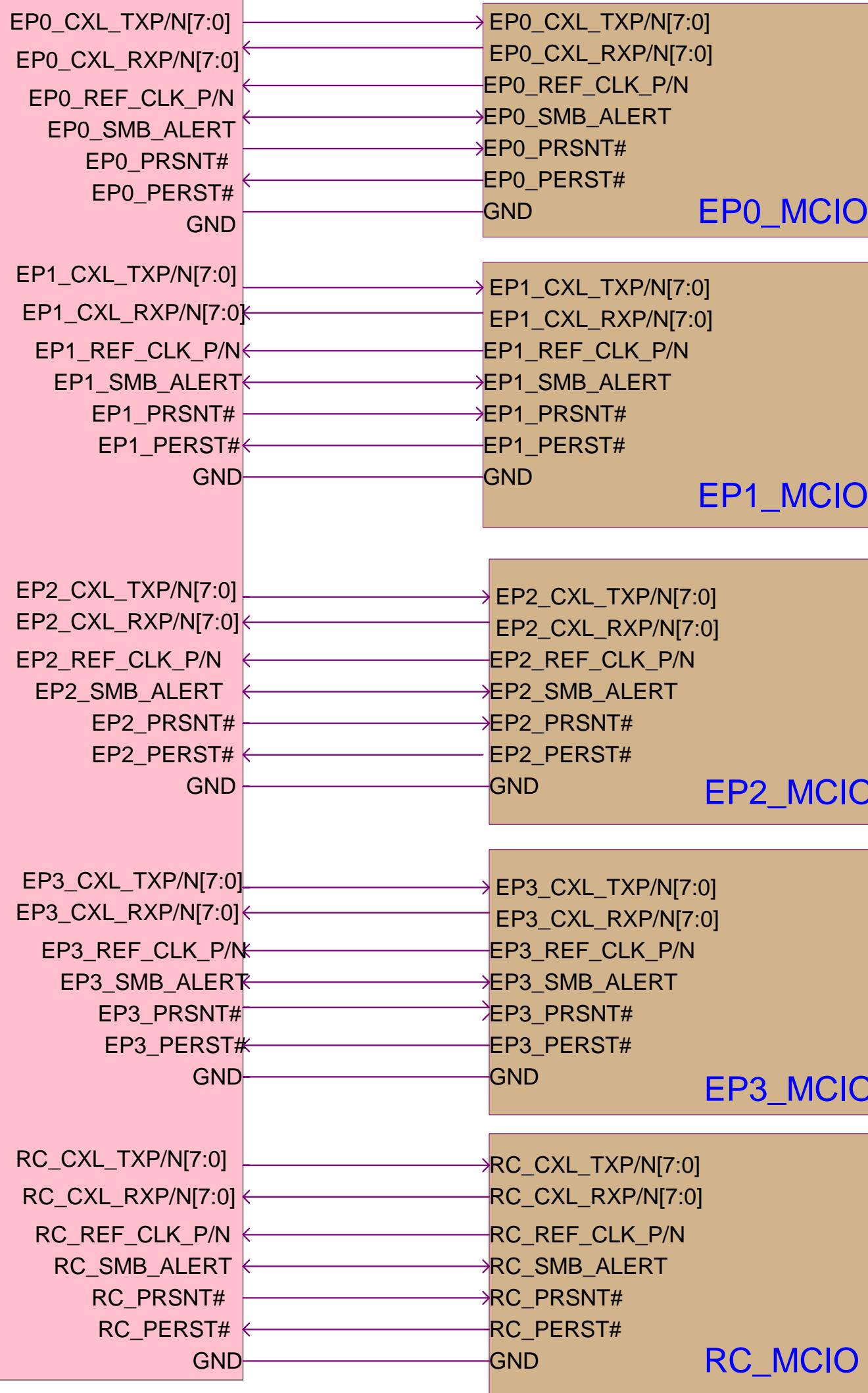
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Power_Flow

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MKB



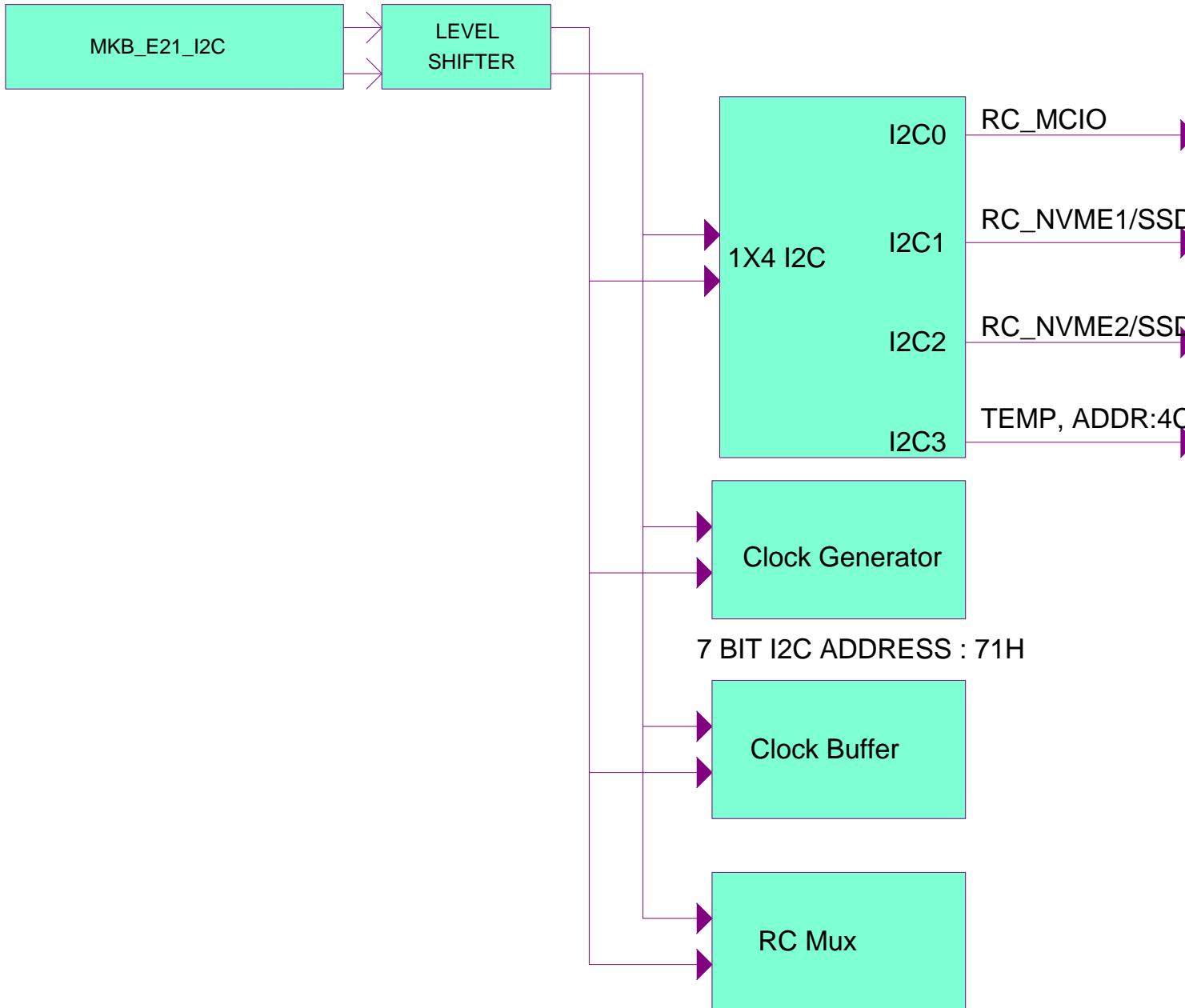
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Dr, Santa Clara, CA 95054,
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MKB_CXL

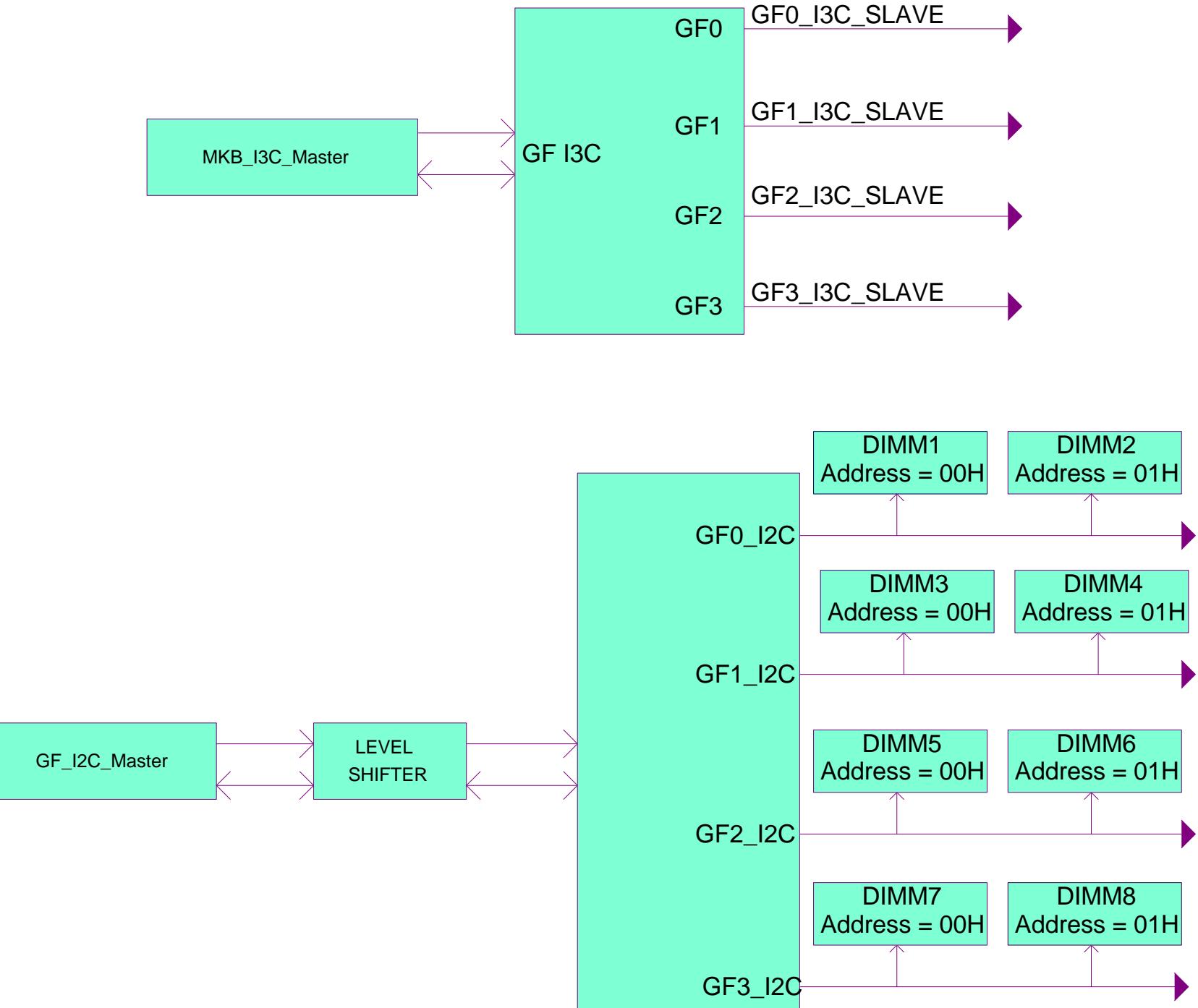
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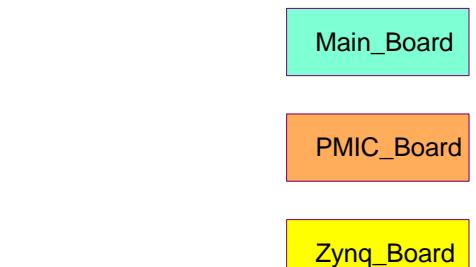
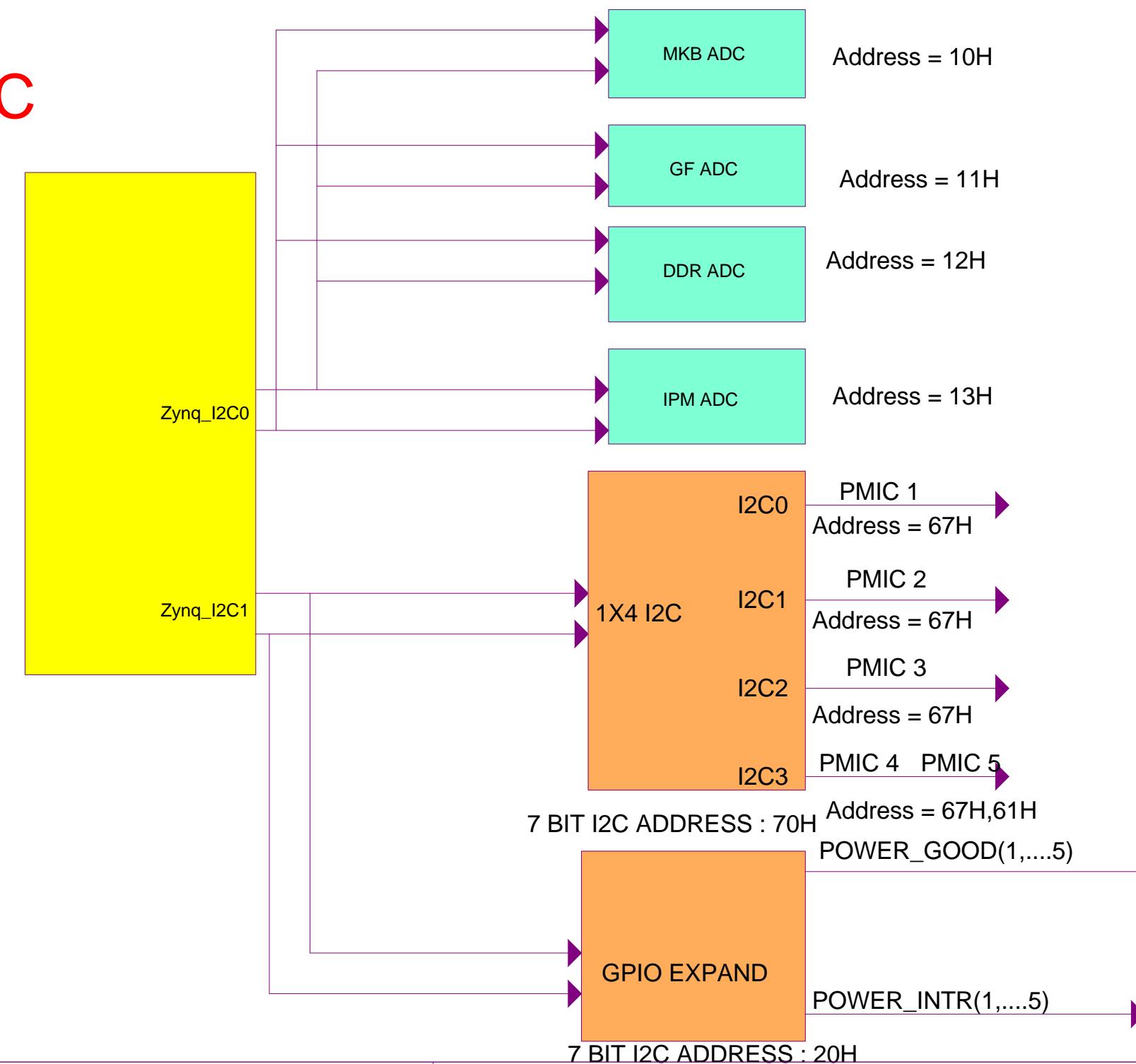
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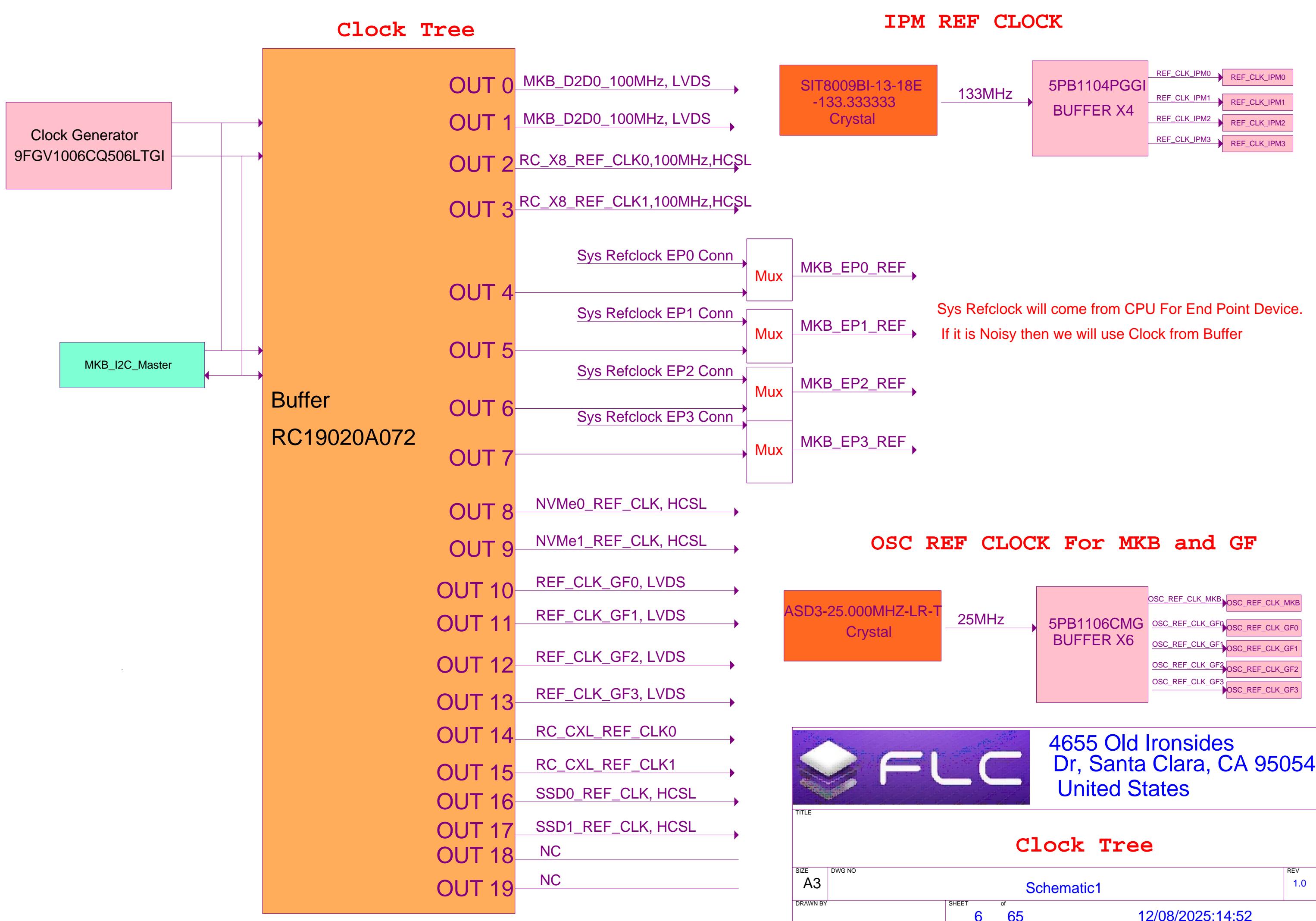


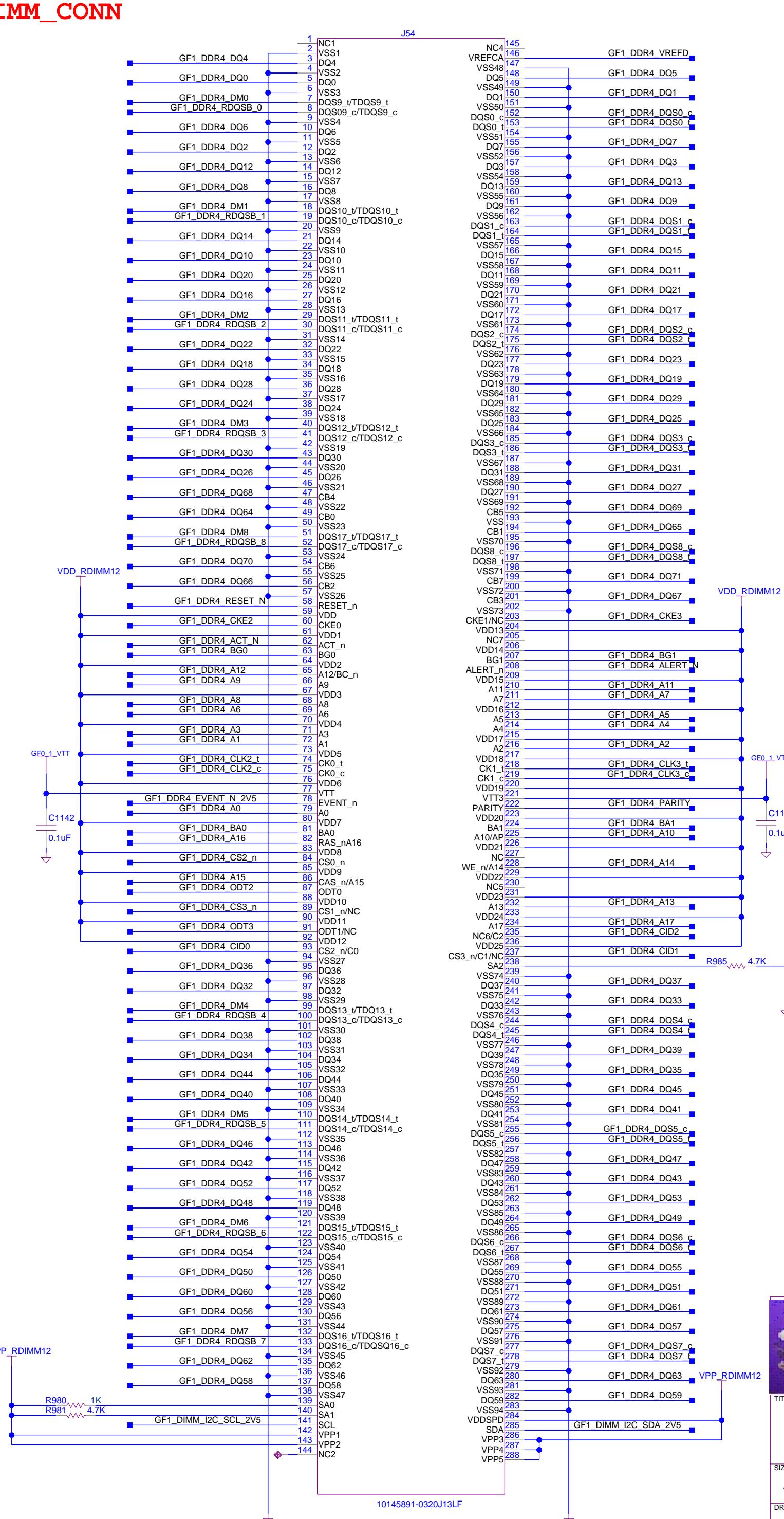
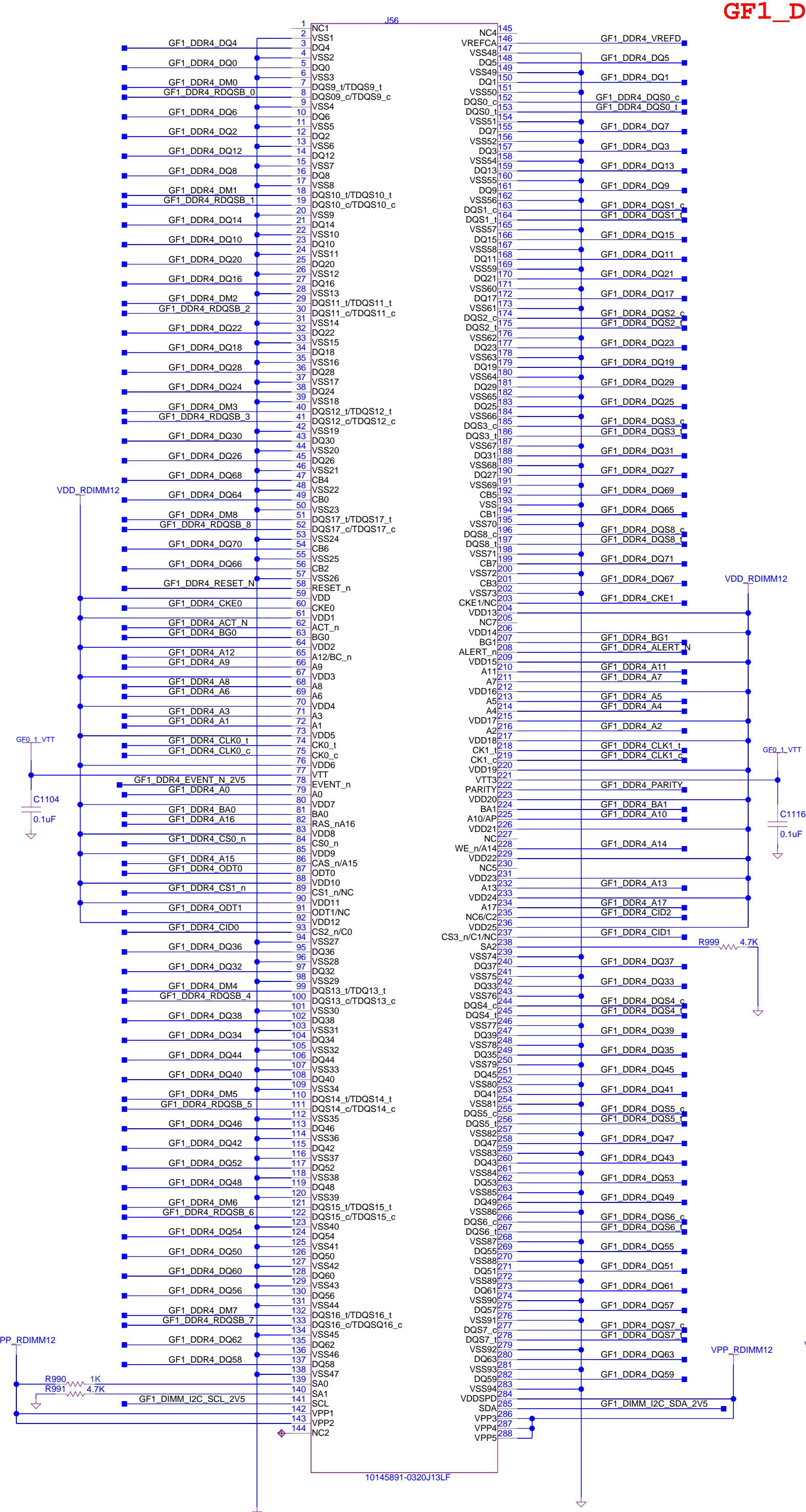
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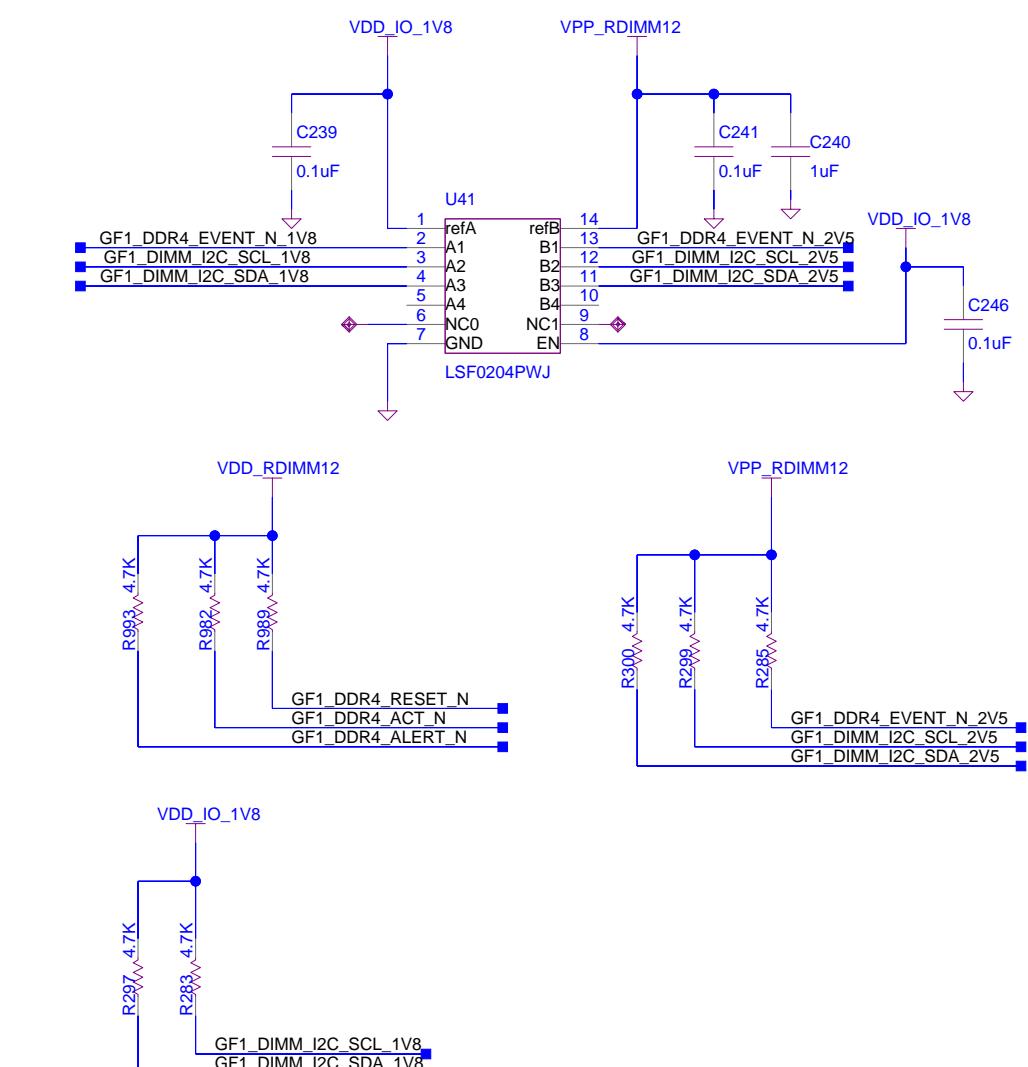
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LEVEL TRANSLATOR



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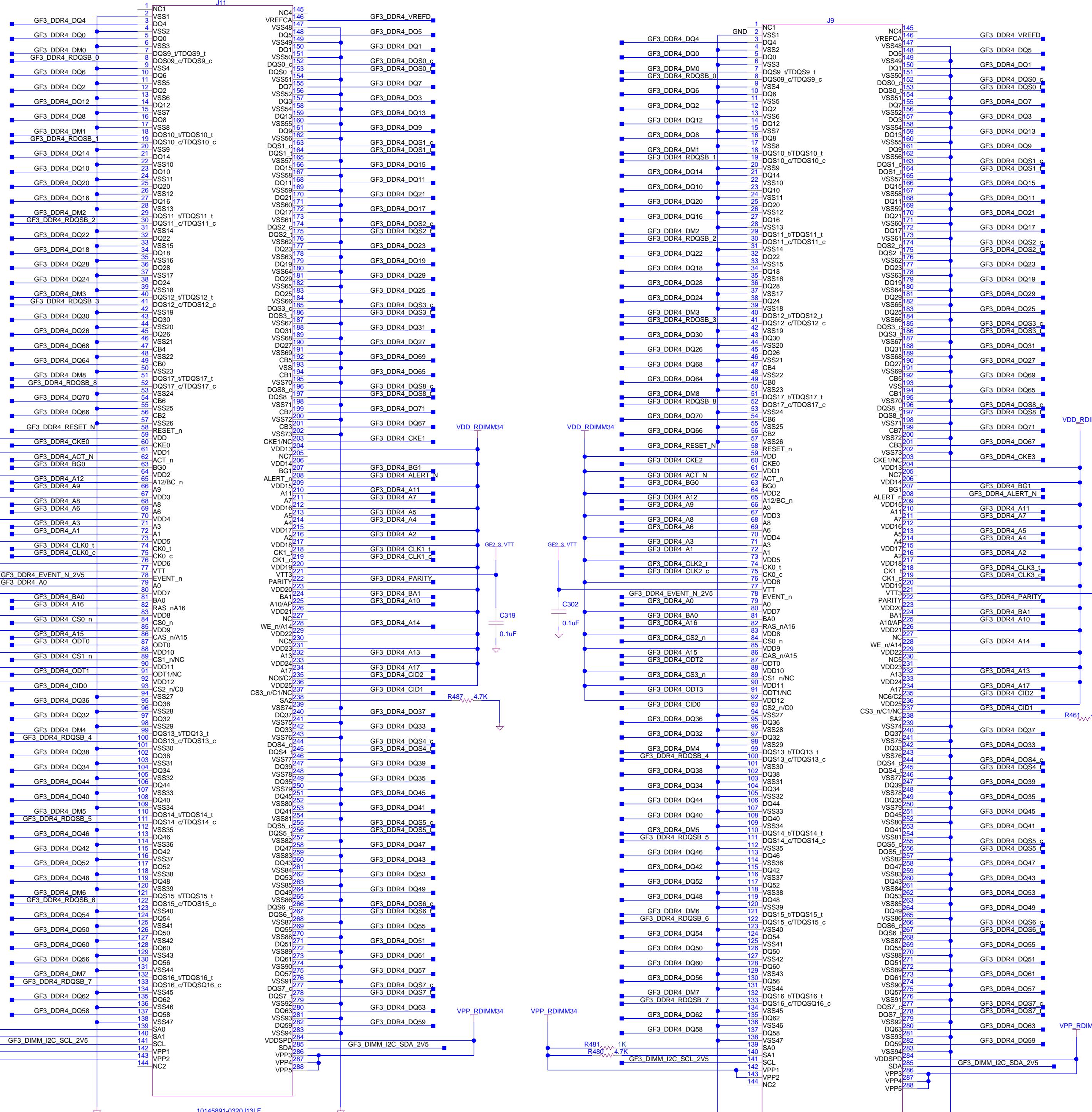


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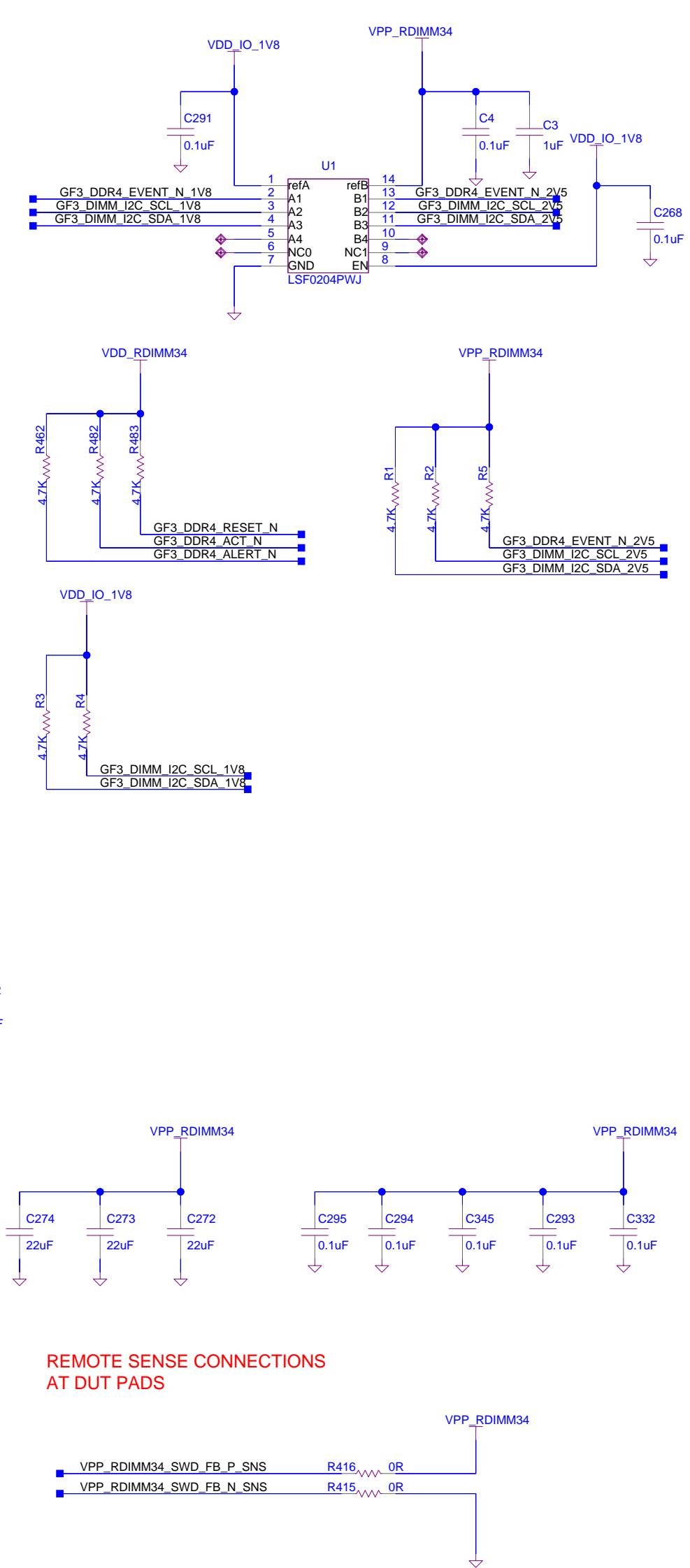
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Schematic

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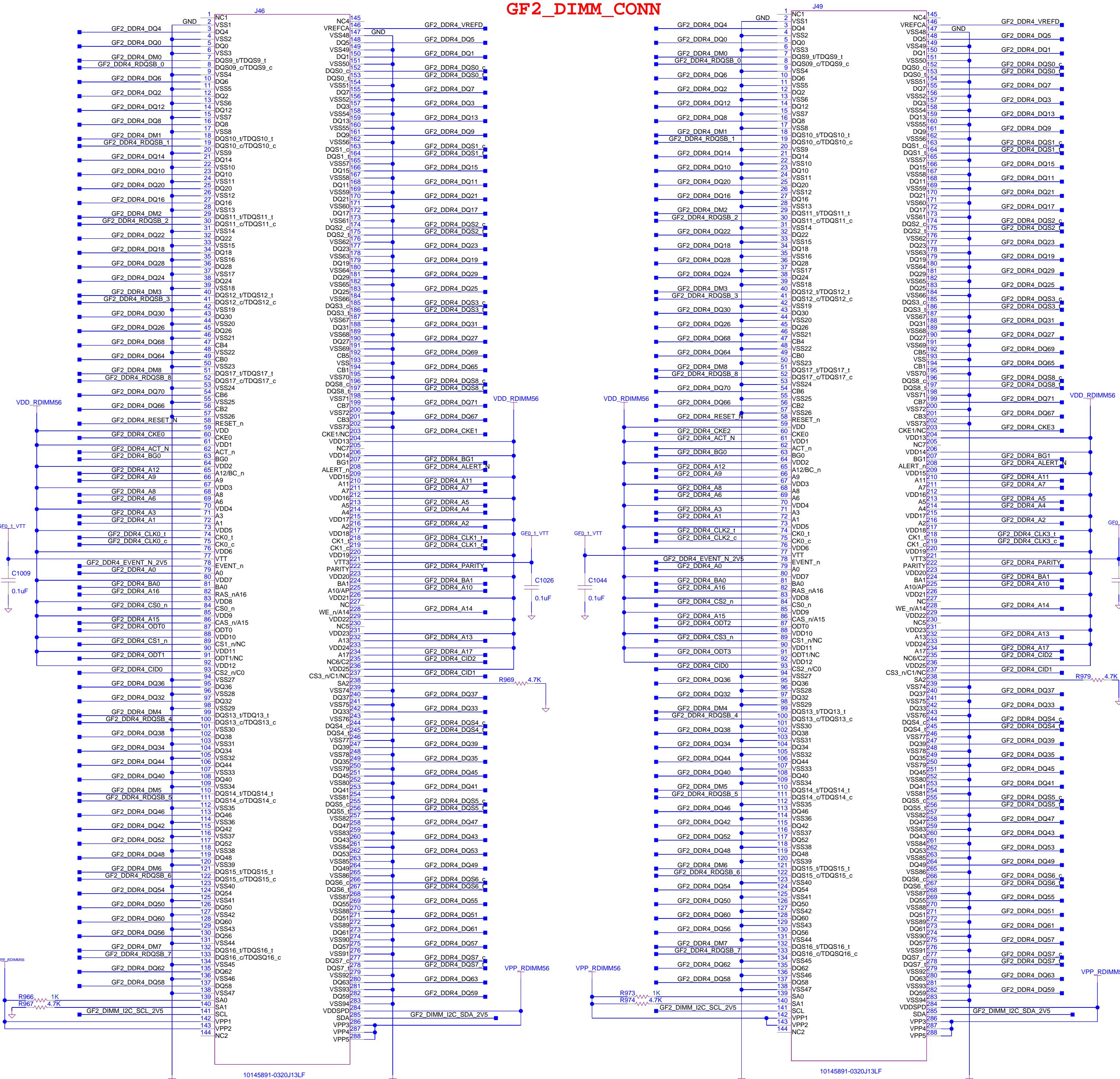


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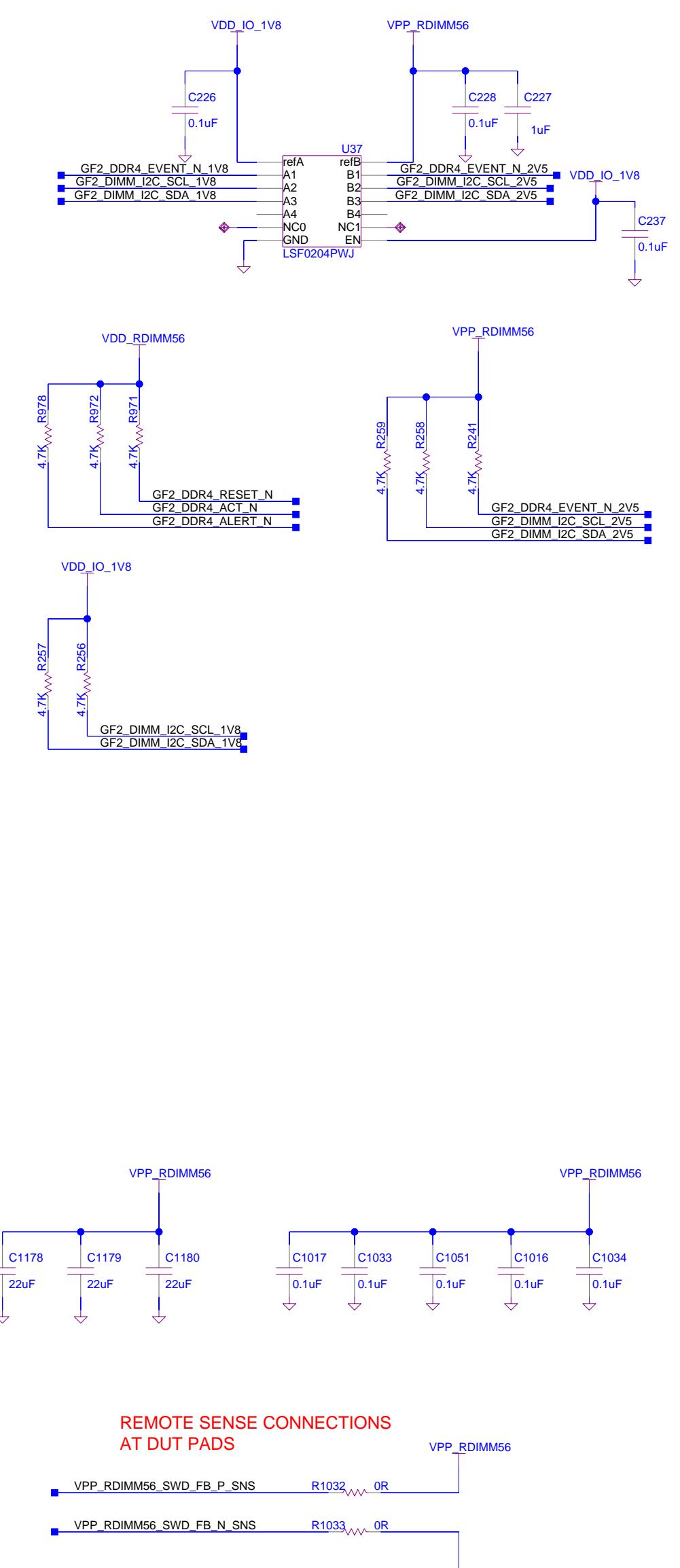


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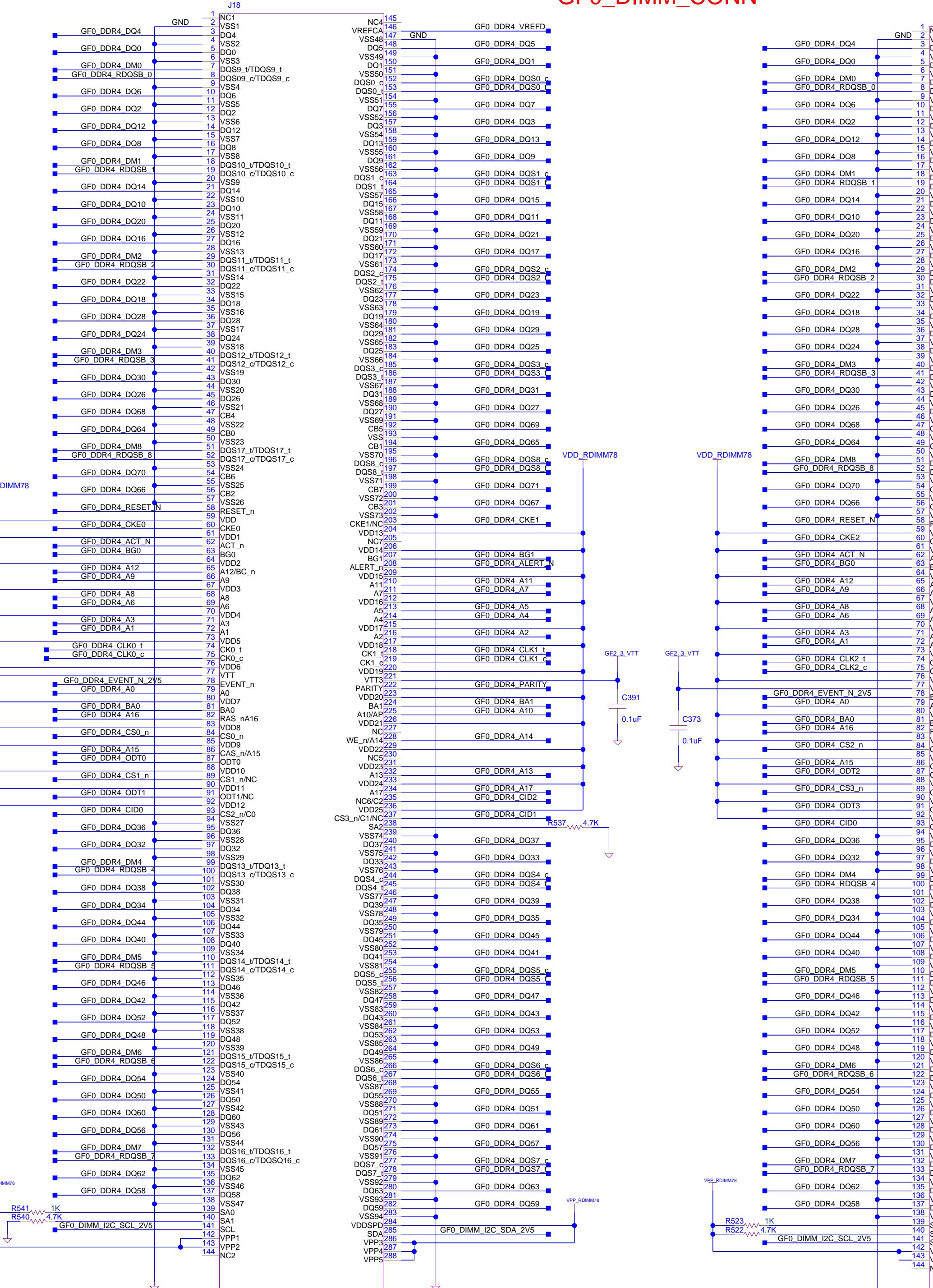
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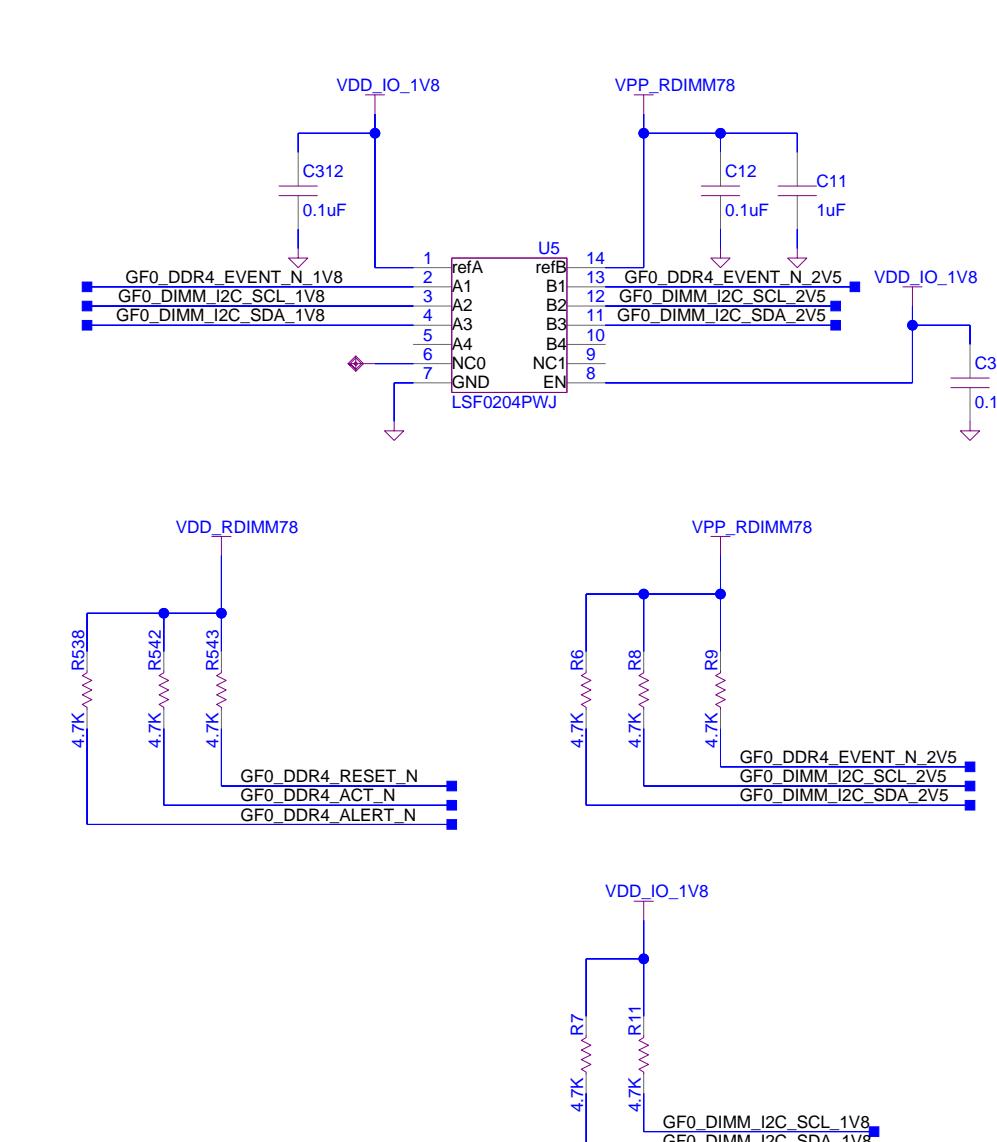
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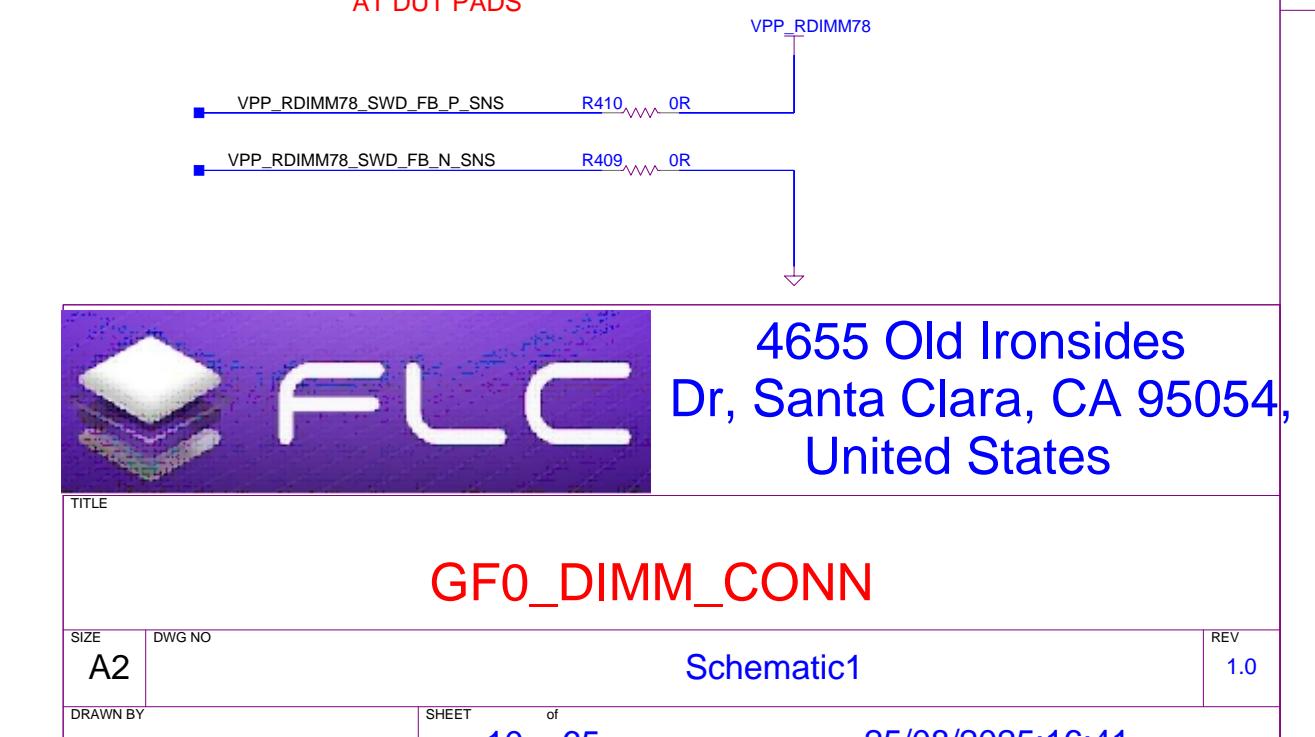
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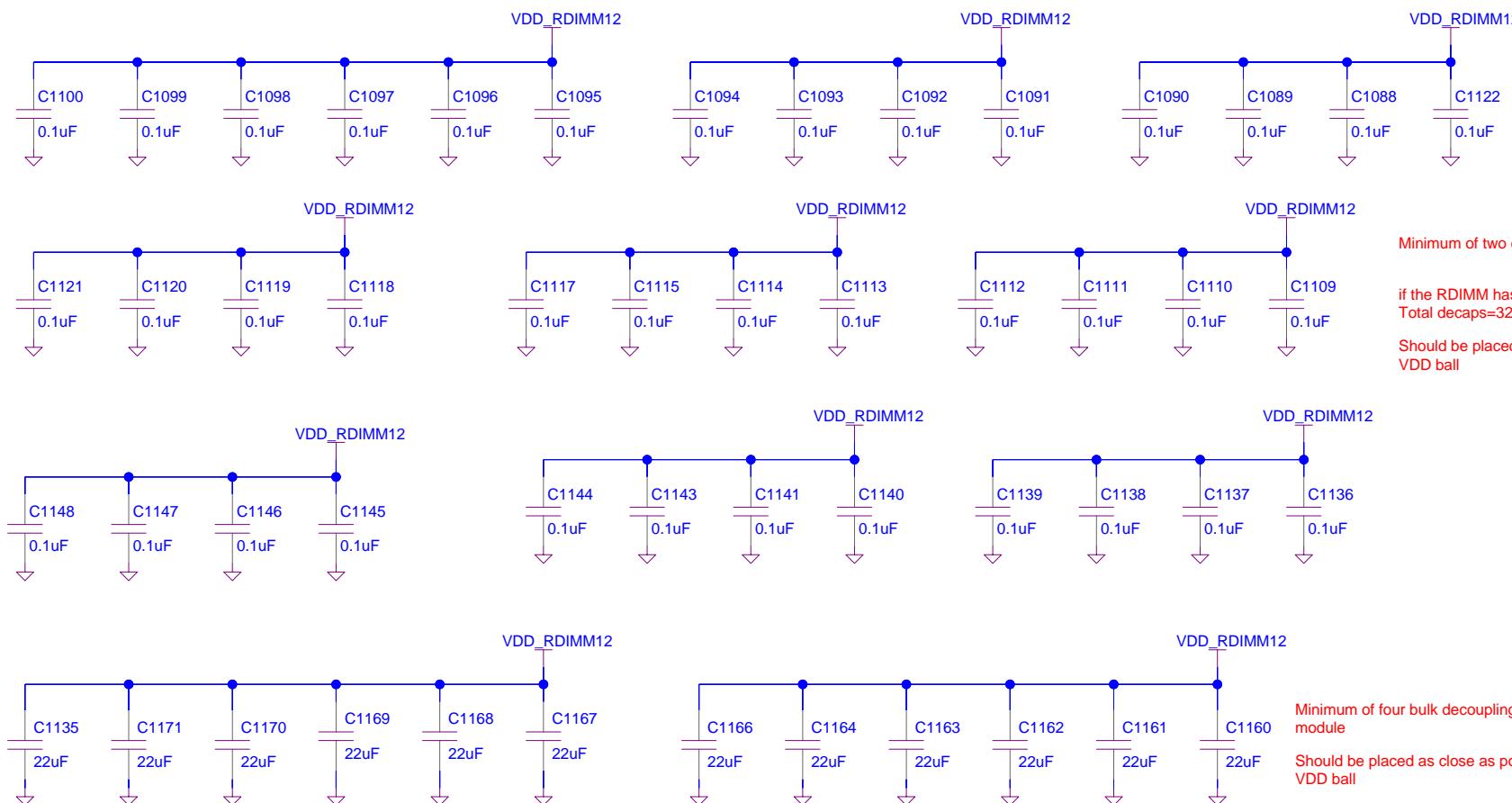
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REMOTE SENSE CONNECTIONS AT DUT PADS



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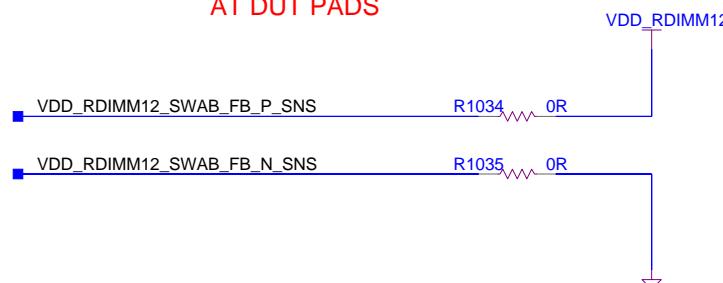


Minimum of two decoupling capacitors to VSS per SDRAM

if the RDIMM has 16 SDRAM devices, then:
Total decaps=32 decoupling capacitors

Should be placed as close as possible to the SDRAM VDD ball

REMOTE SENSE CONNECTIONS AT DUT PADS



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TITLE

DDR4_RDIMM_CAPS

SIZE

A4

DWG NO

Schematic1

REV

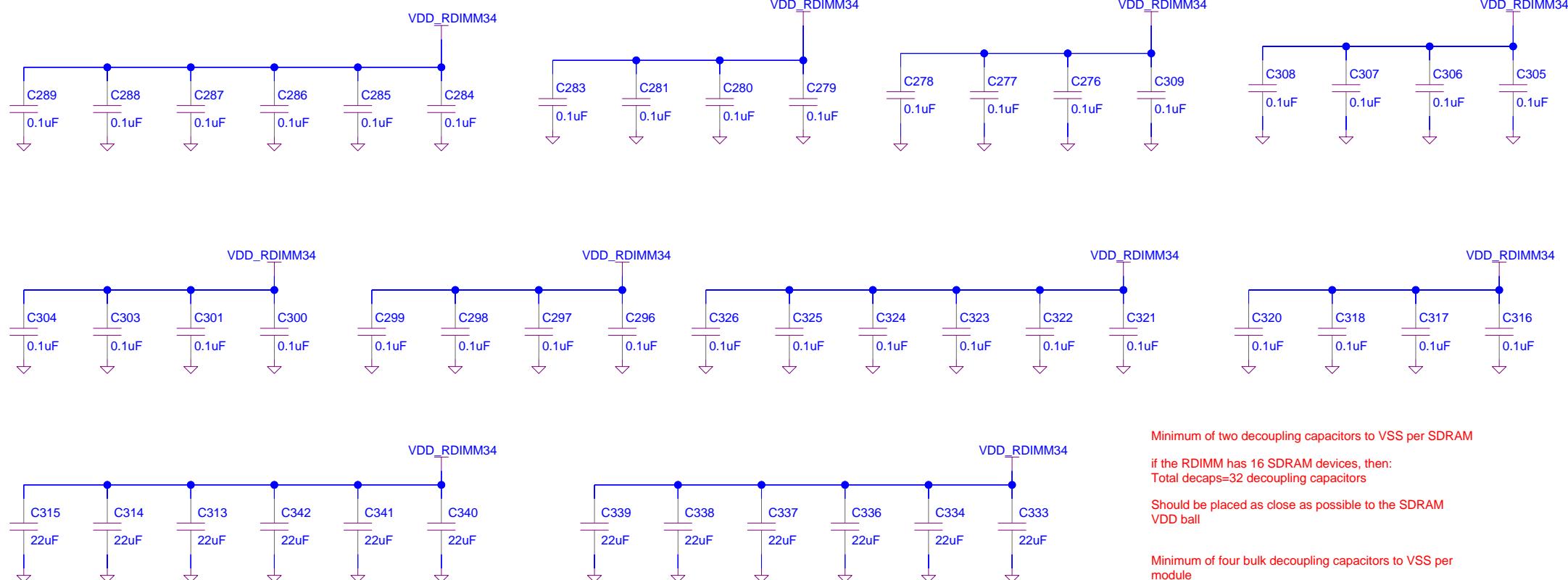
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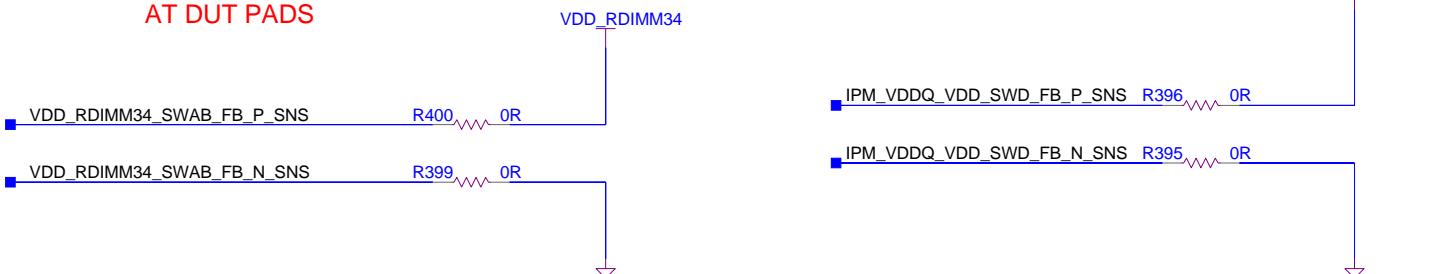
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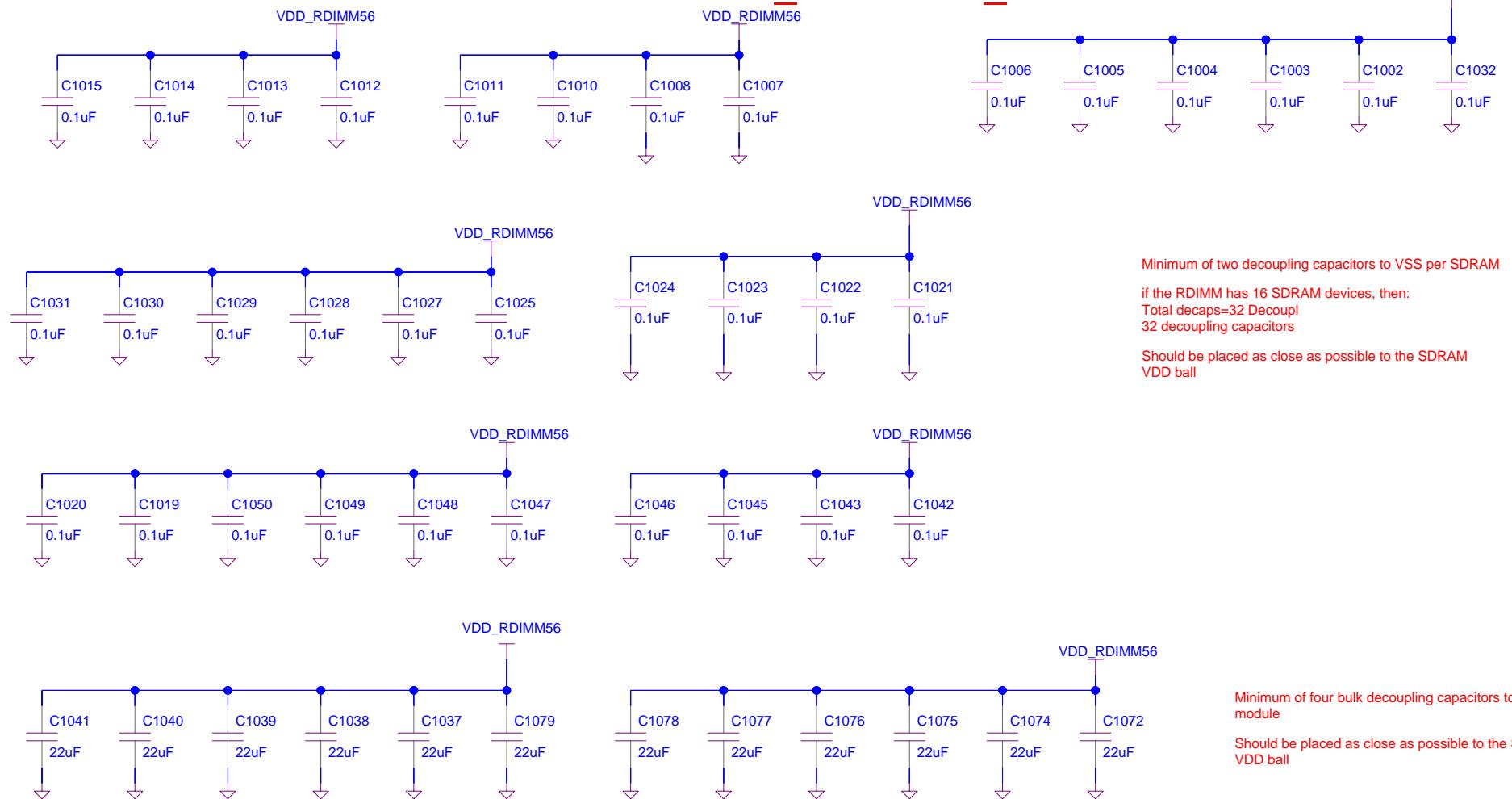
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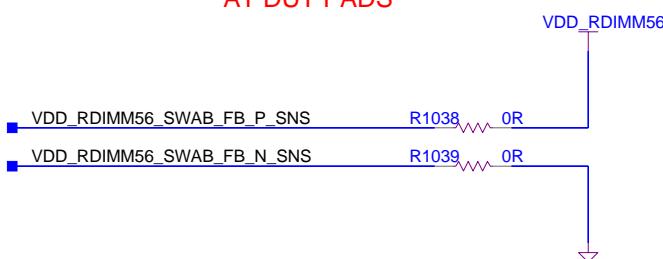
REMOTE SENSE CONNECTIONS AT DUT PADS



DDR4_RDIMM56_CAPS



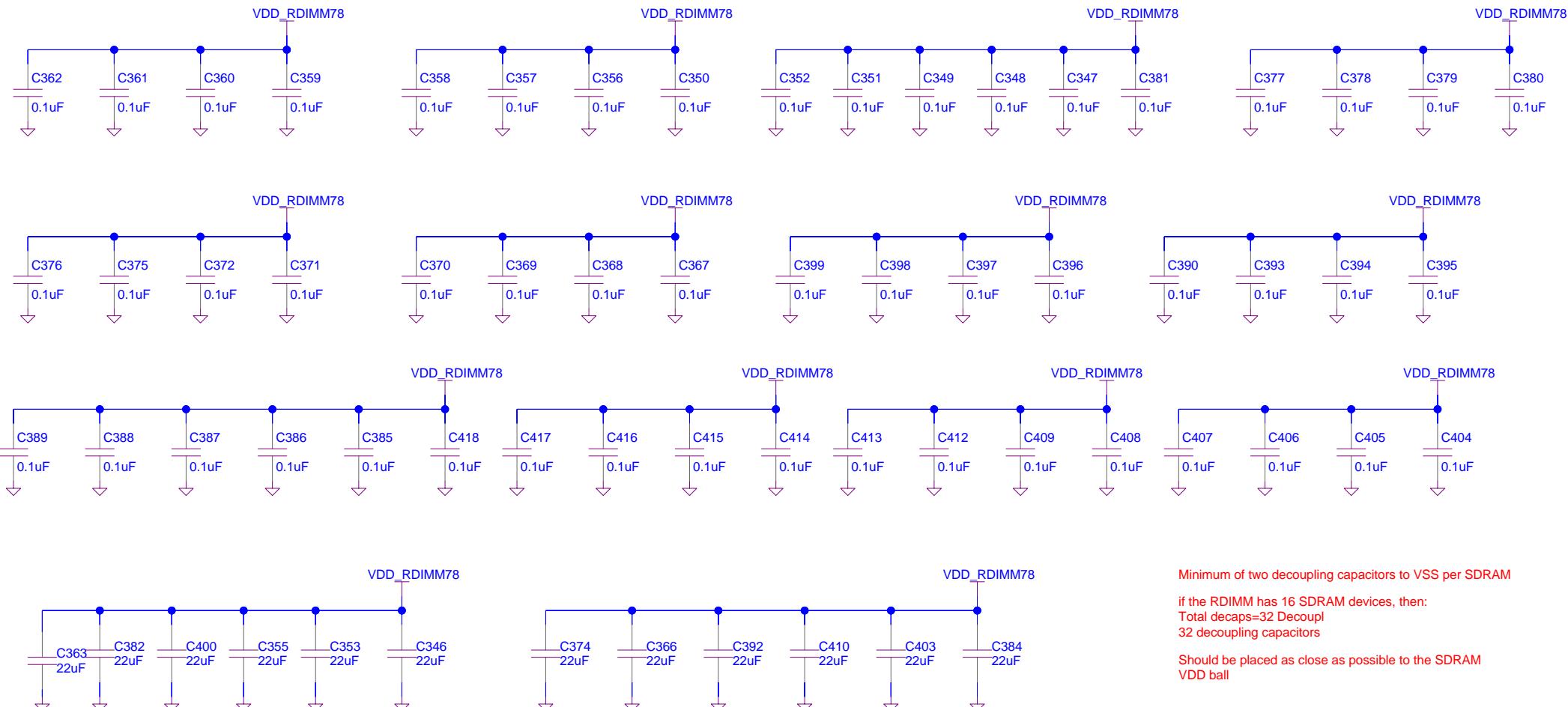
REMOTE SENSE CONNECTIONS AT DUT PADS



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TITLE	Schematic1	
SIZE	DWG NO	REV
A4		

DDR4_RDIMM78_CAPS



Minimum of two decoupling capacitors to VSS per SDRAM

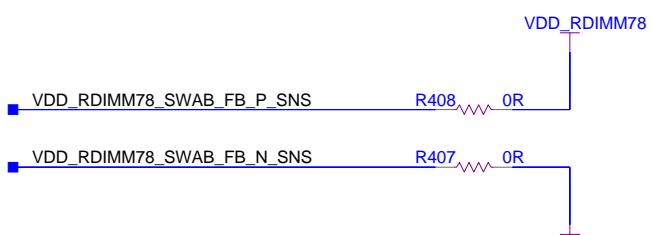
if the RDIMM has 16 SDRAM devices, then:

Total decaps=32 Decoupl
32 decoupling capacitors

Should be placed as close as possible to the SDRAM
VDD ball

Minimum of four bulk decoupling capacitors to VSS per
module

REMOTE SENSE CONNECTIONS AT DUT PADS



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TITLE

Schematic1

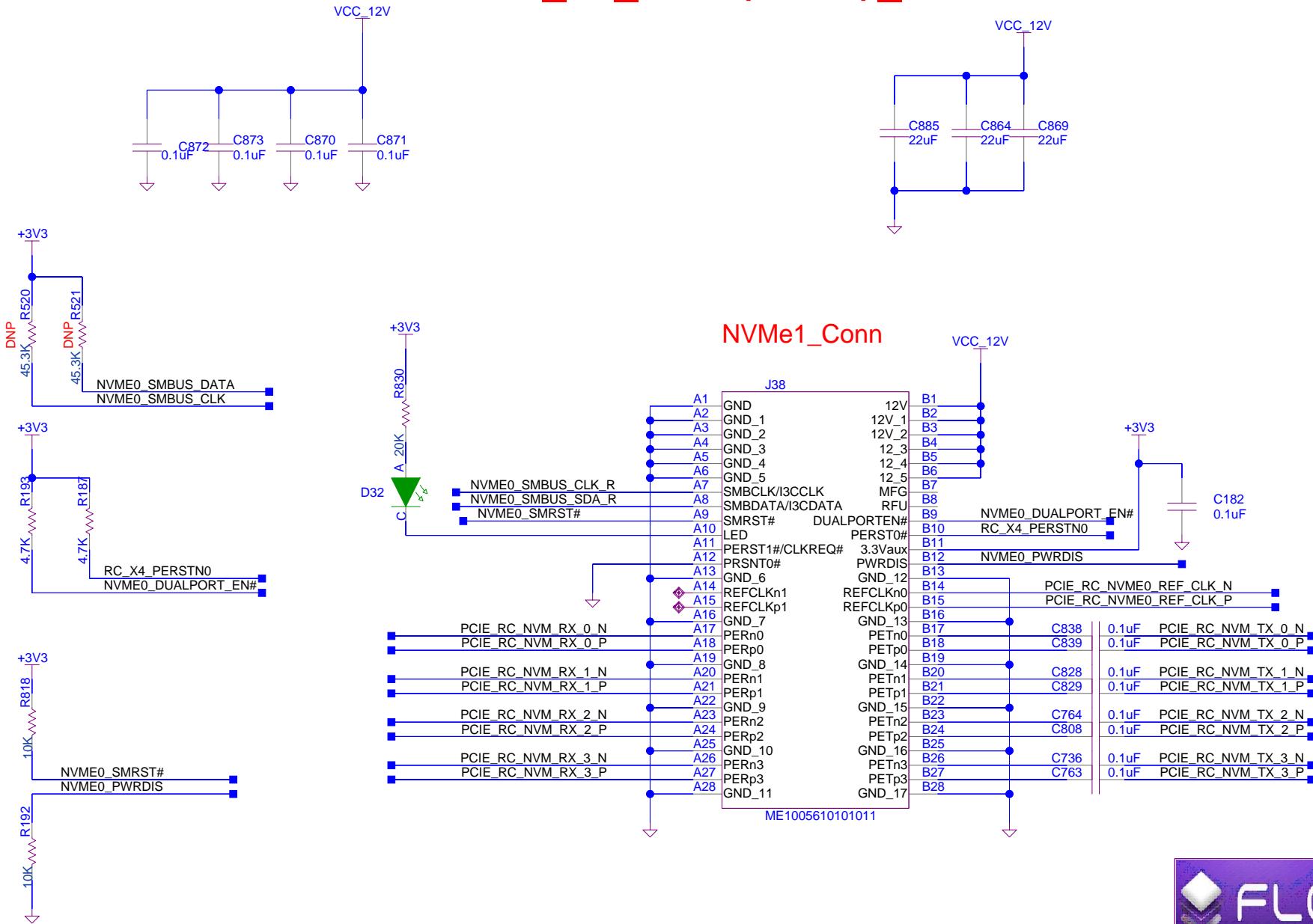
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DWG NO

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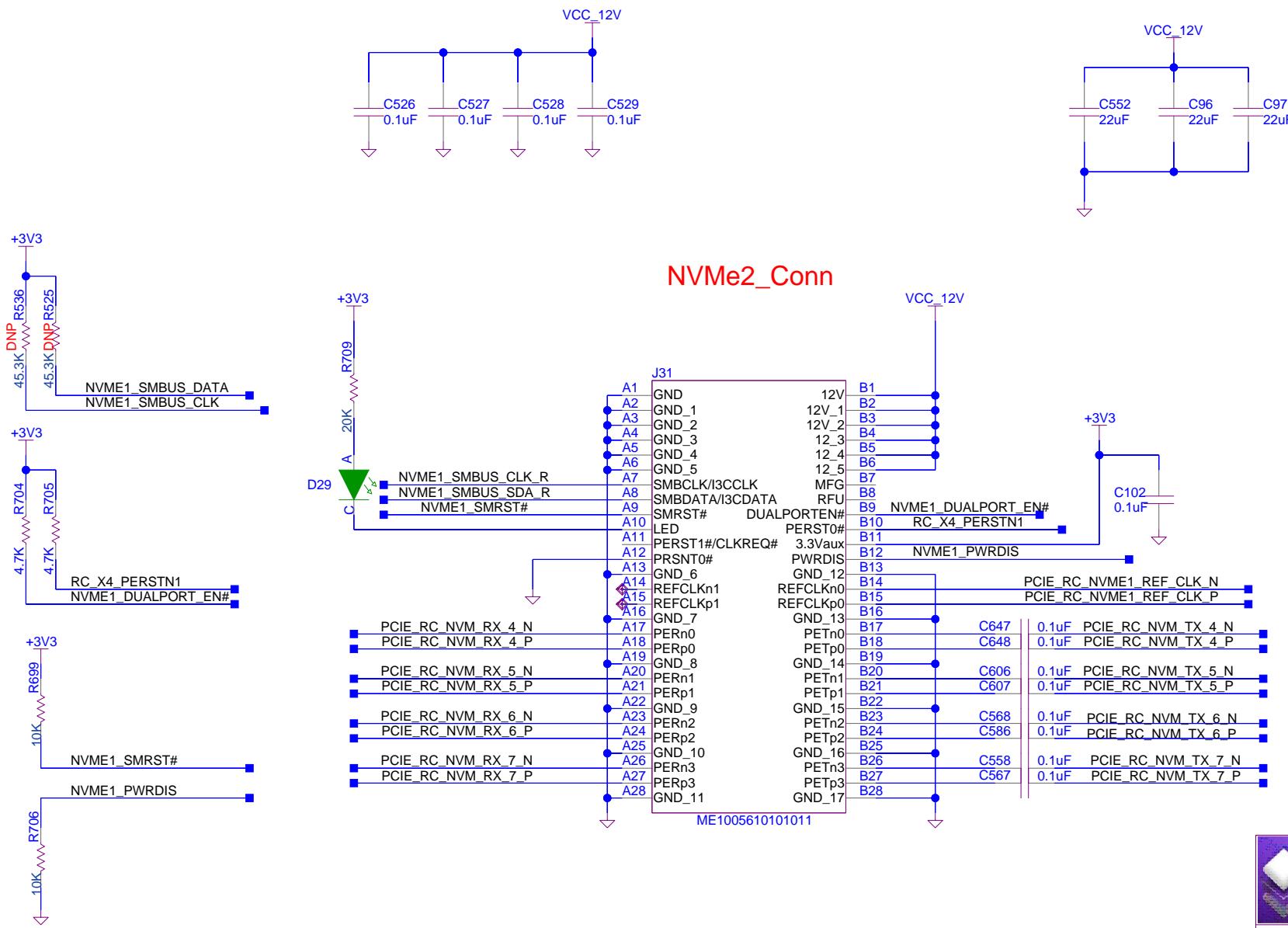
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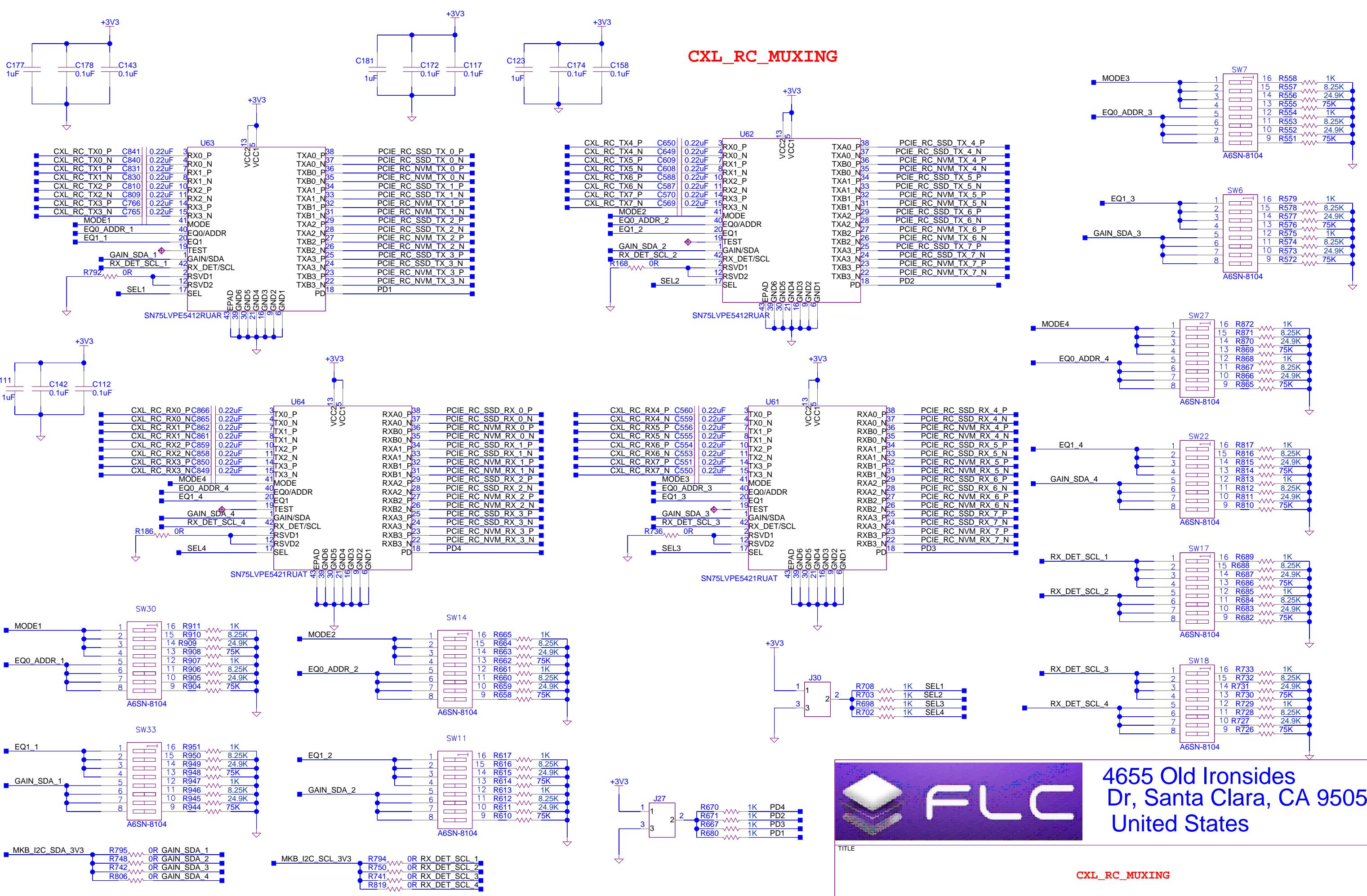
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MKB_RC_NVMe(E1.S)_CONN



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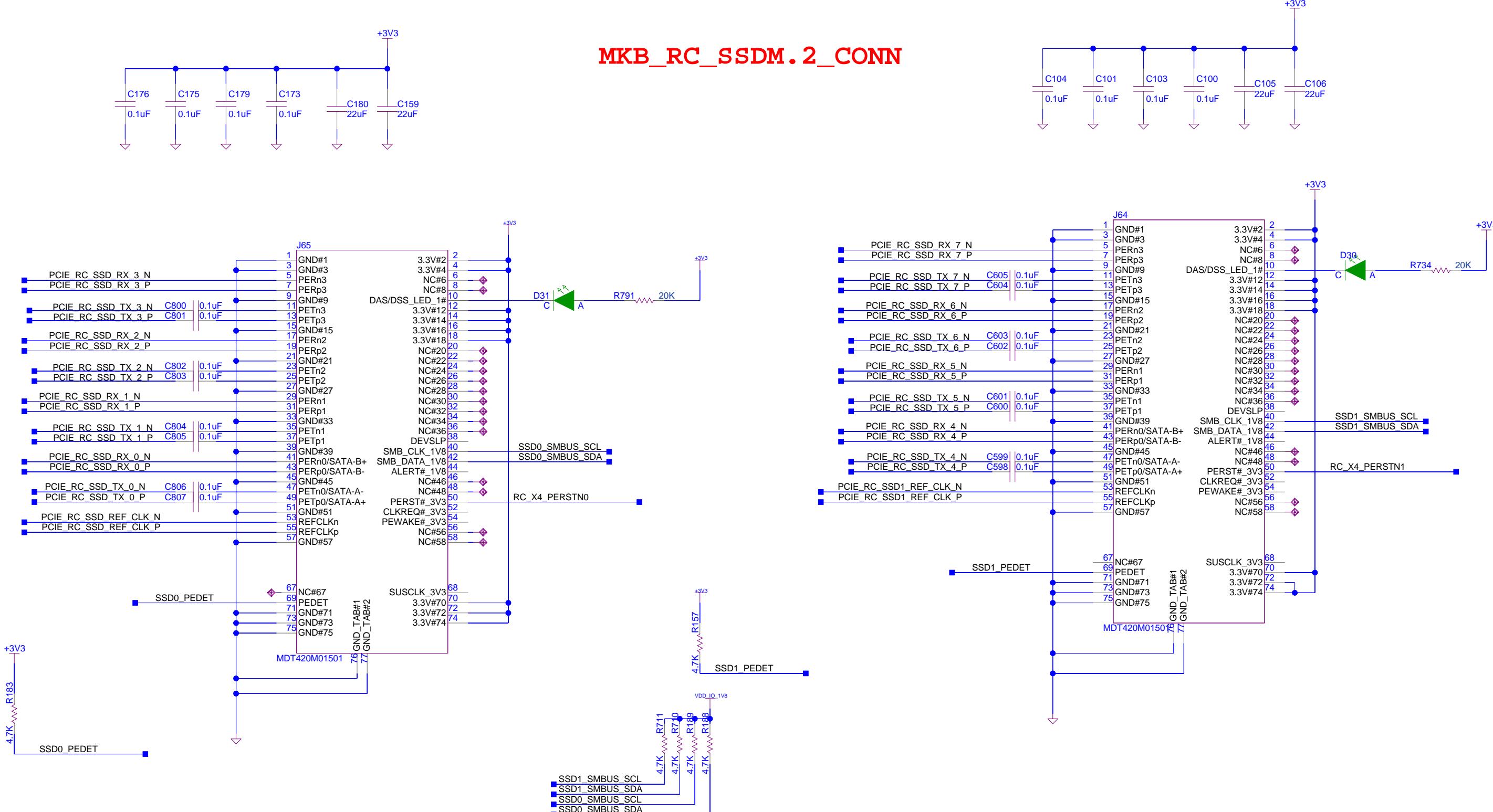


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CXL_RC_MUXING

Schematic1

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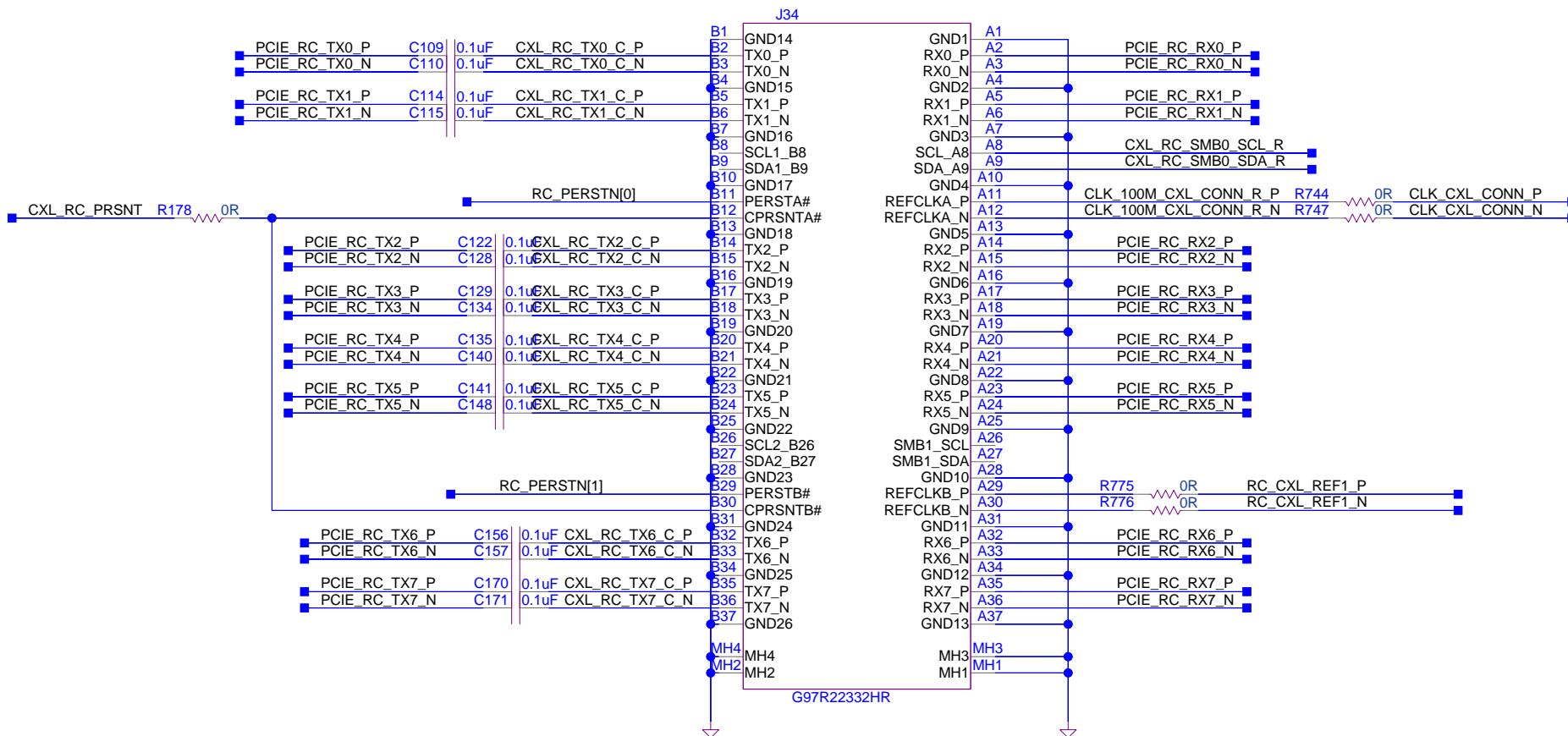


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MKB_RC_SSDM.2_CONN

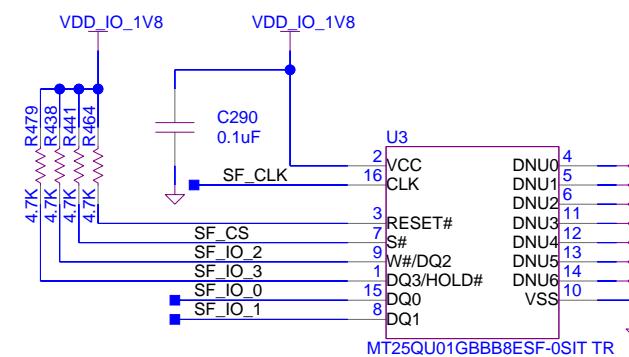
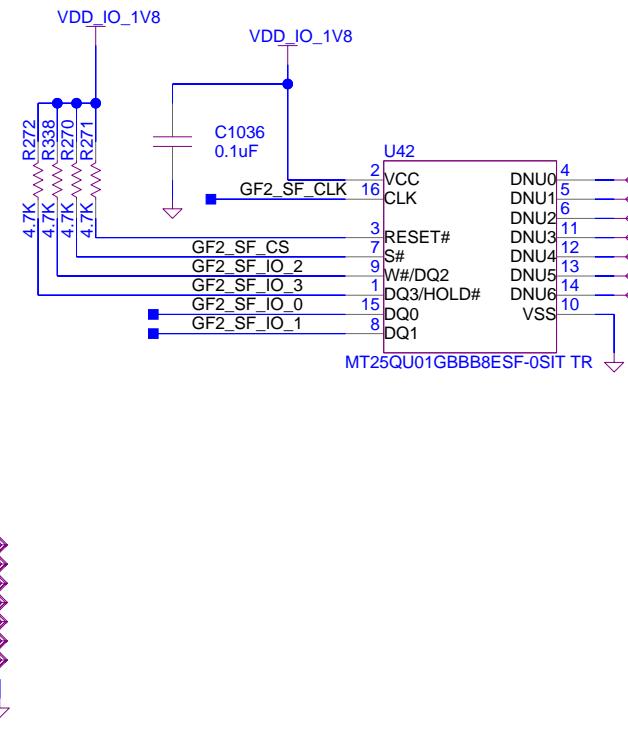
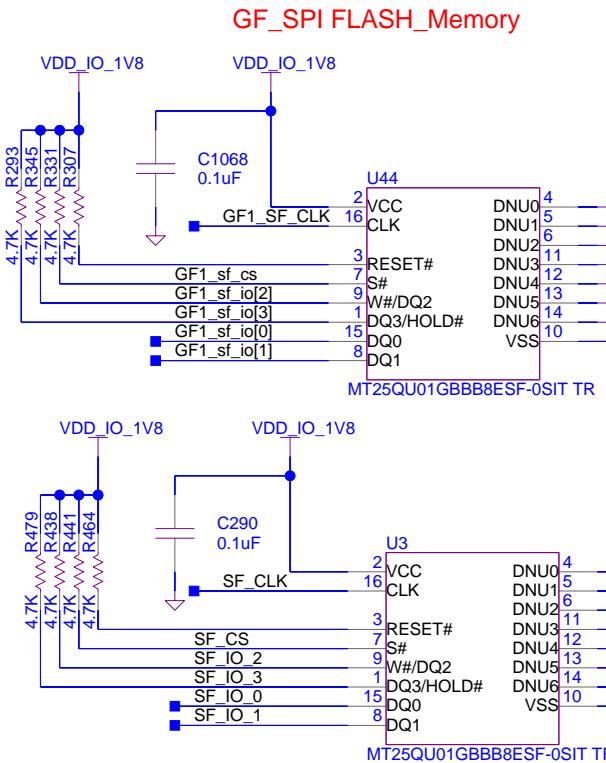
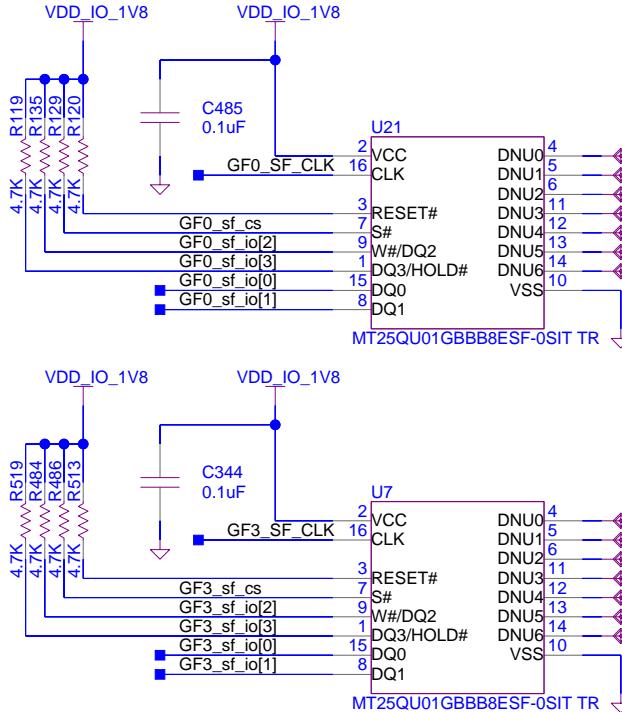
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RC_CXL_PCI_GEN5



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TITLE		
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TITLE

GF_SPI FLASH_Memory

SIZE

A4

DWG NO

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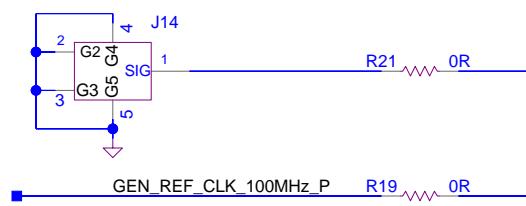
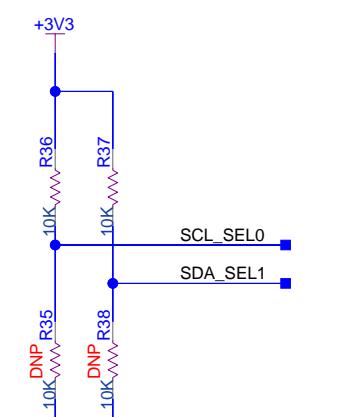
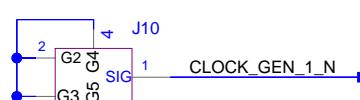
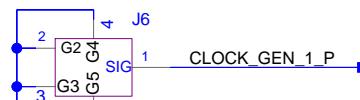
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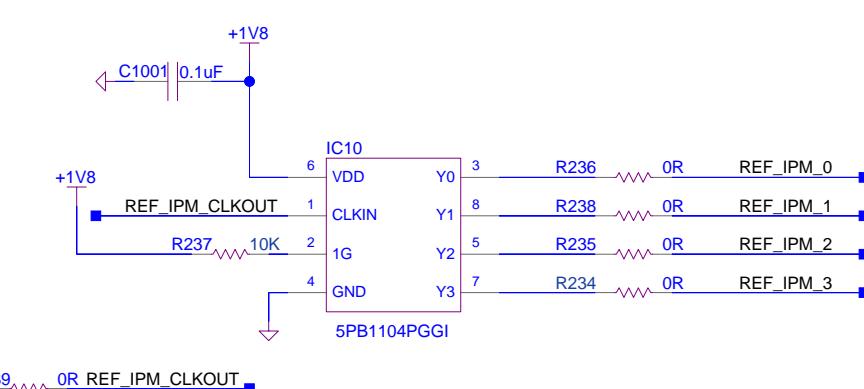
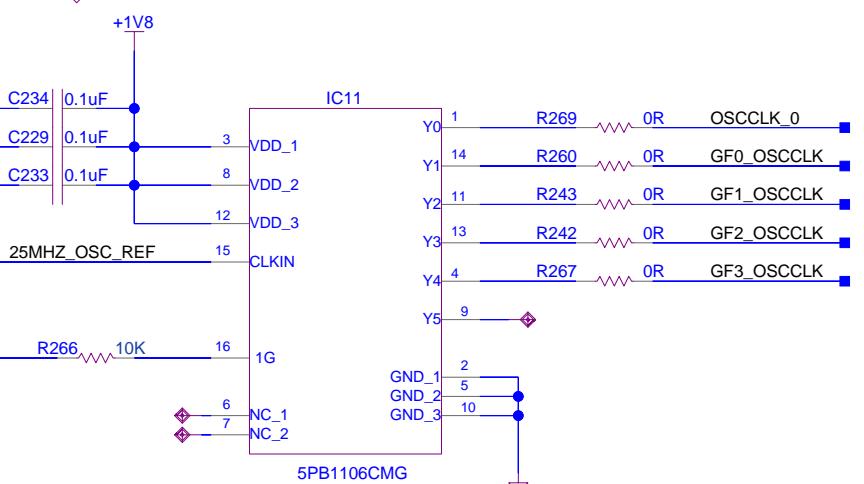
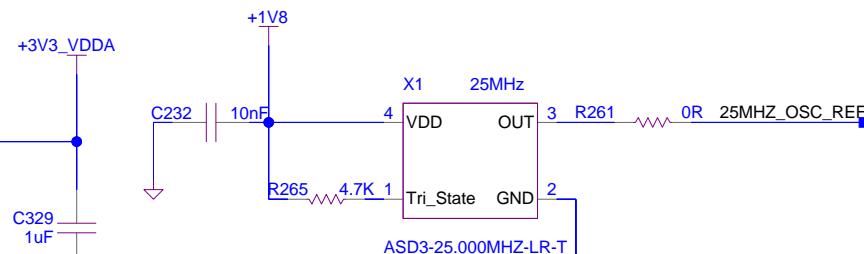
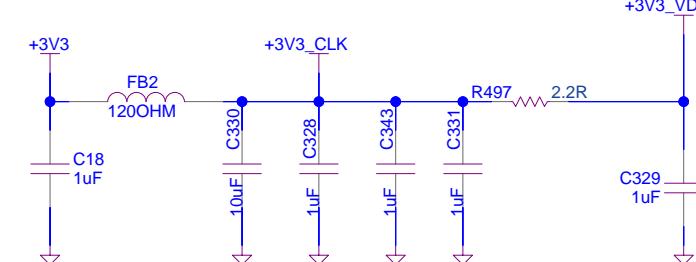
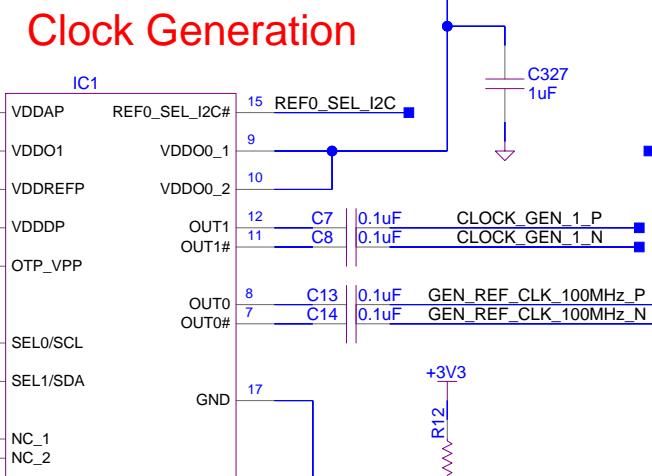
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MKB_I2C_SCL_3V3 R152 DNP OR SCL_SEL0
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Zynq_I2C0_SCL_3V3 R145 OR SCL_SEL0
Zynq_I2C0_SDA_3V3 R39 OR SDA_SEL1



Clock Generation

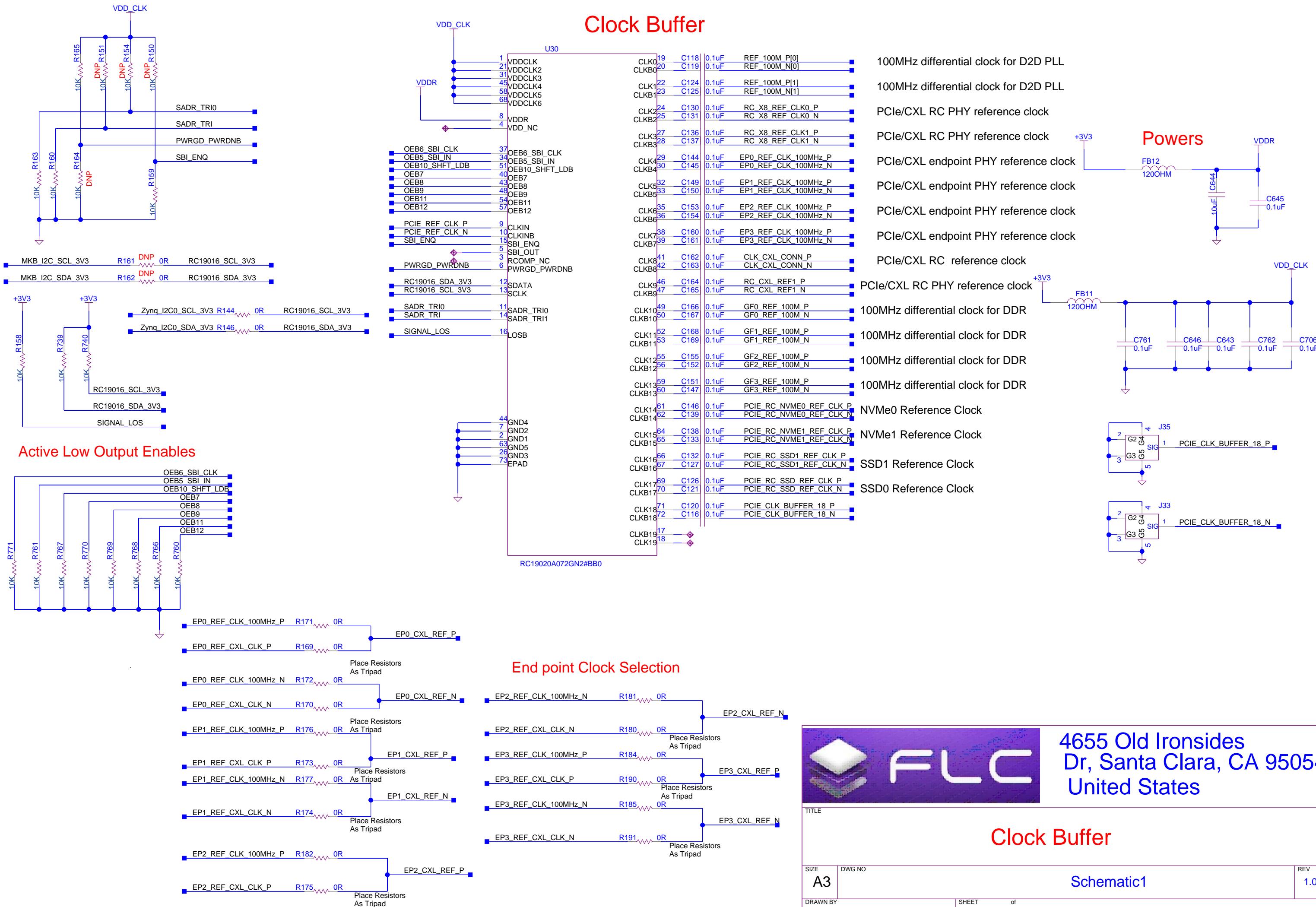


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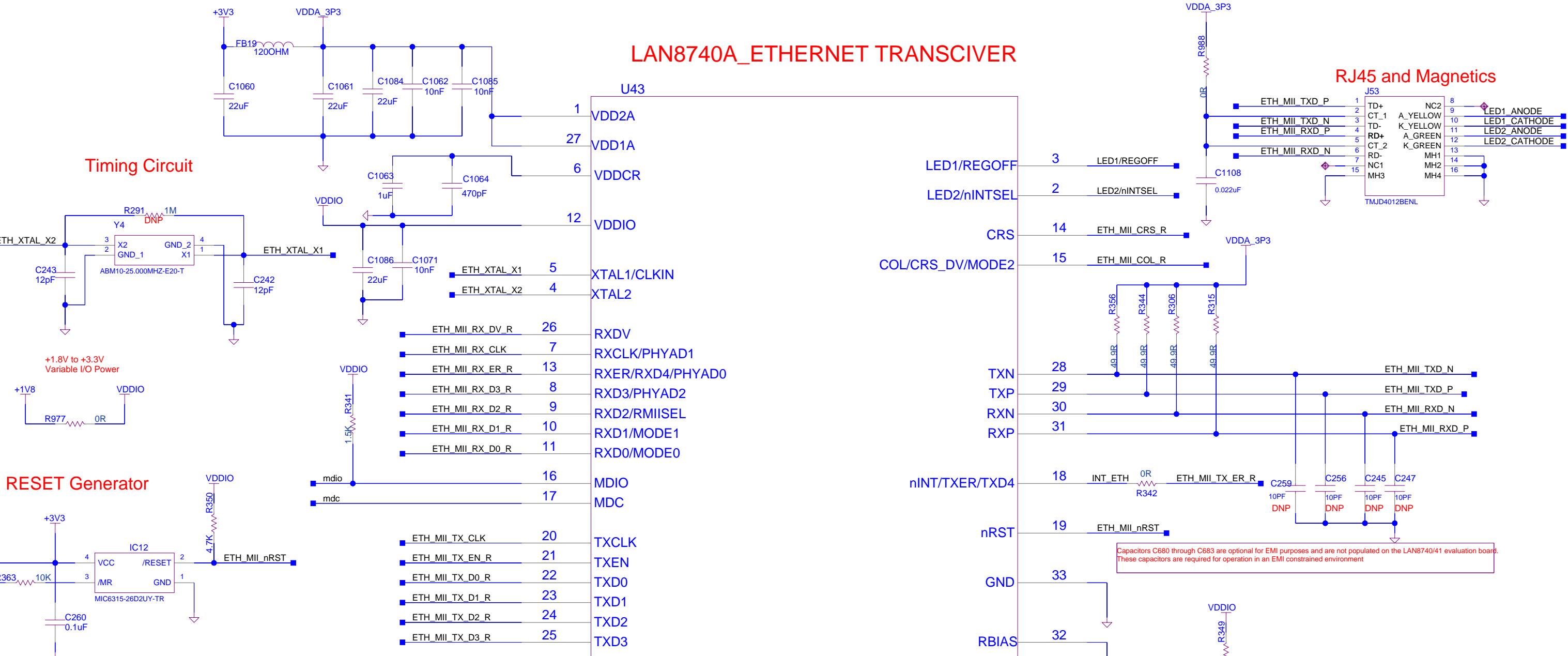
Clock Generation

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Clock Buffer



LAN8740A_ETHERNET TRANSCEIVER



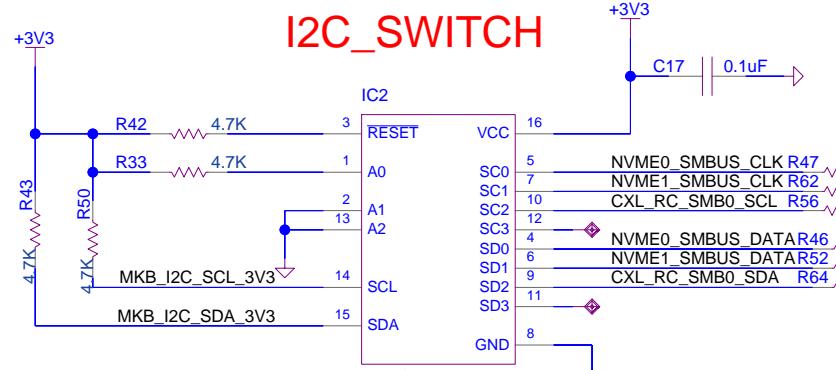
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LAN8740A_ETHERNET TRANSCEIVER

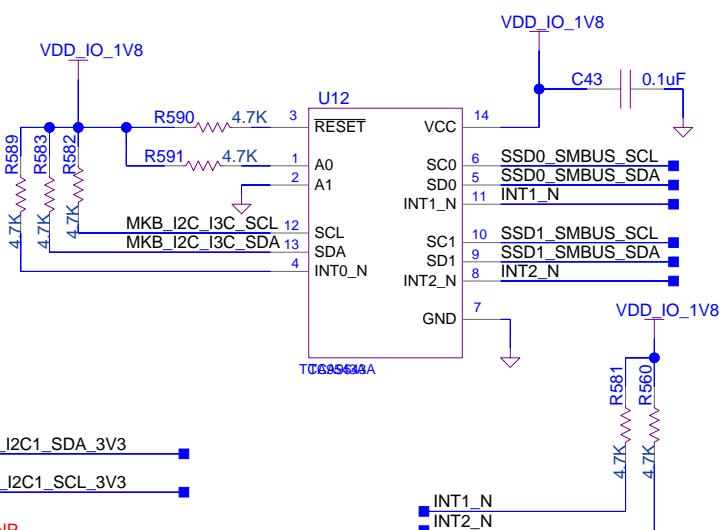
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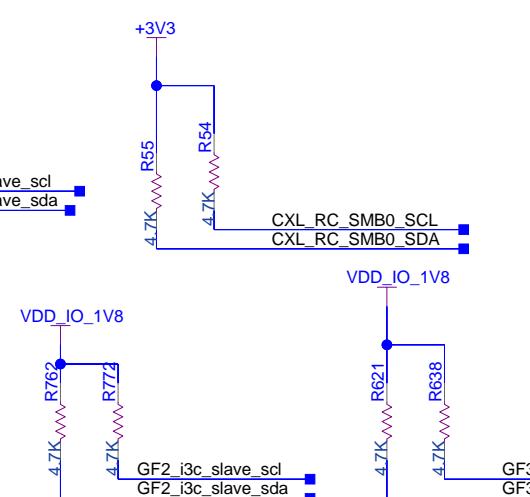
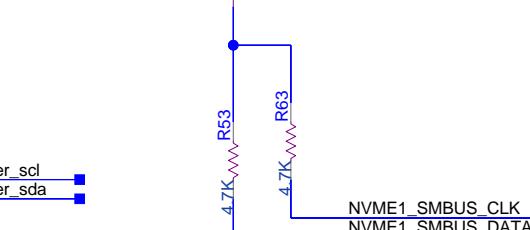
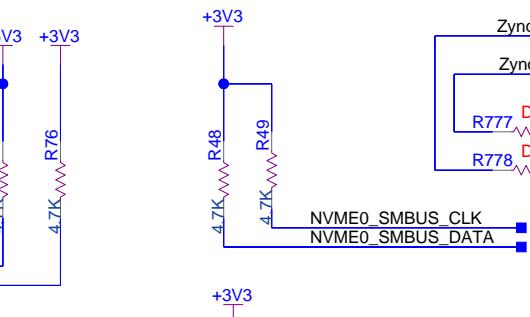
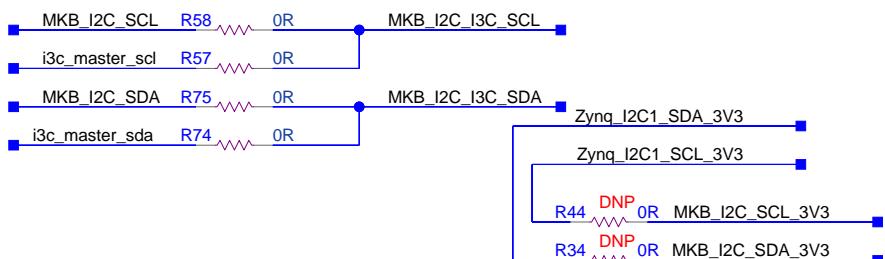
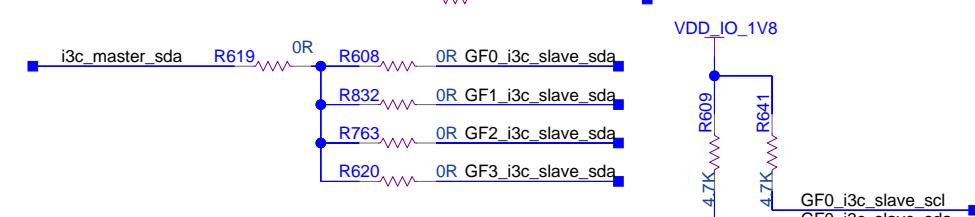
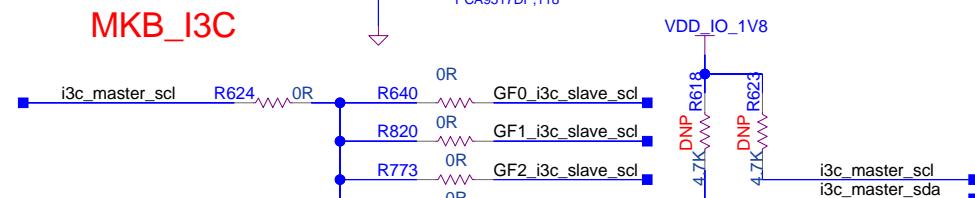
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MKB_I2C_CONN



MKB_I3C



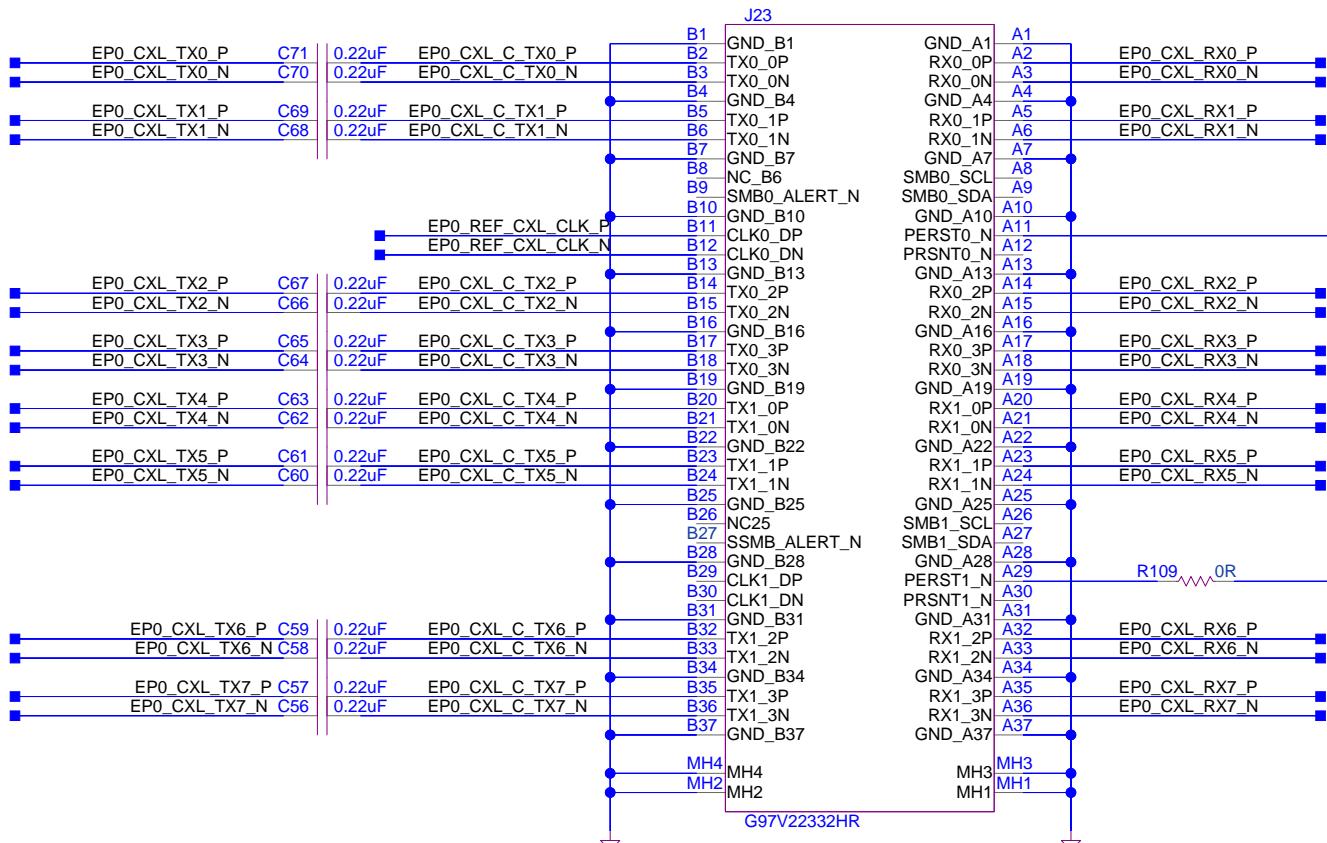
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United States

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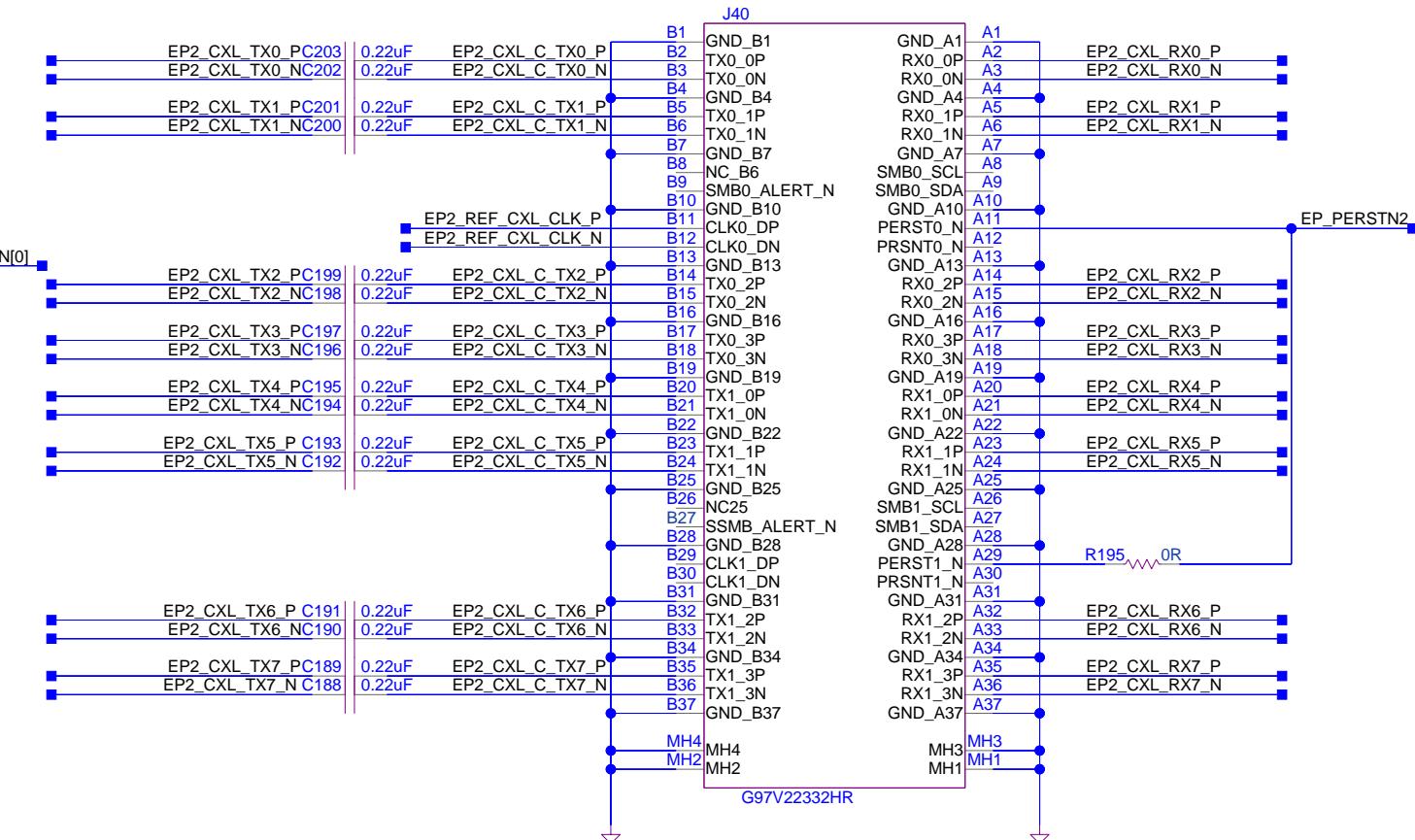
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MCIO_CONN_EP0



MCIO_CONN_EP2



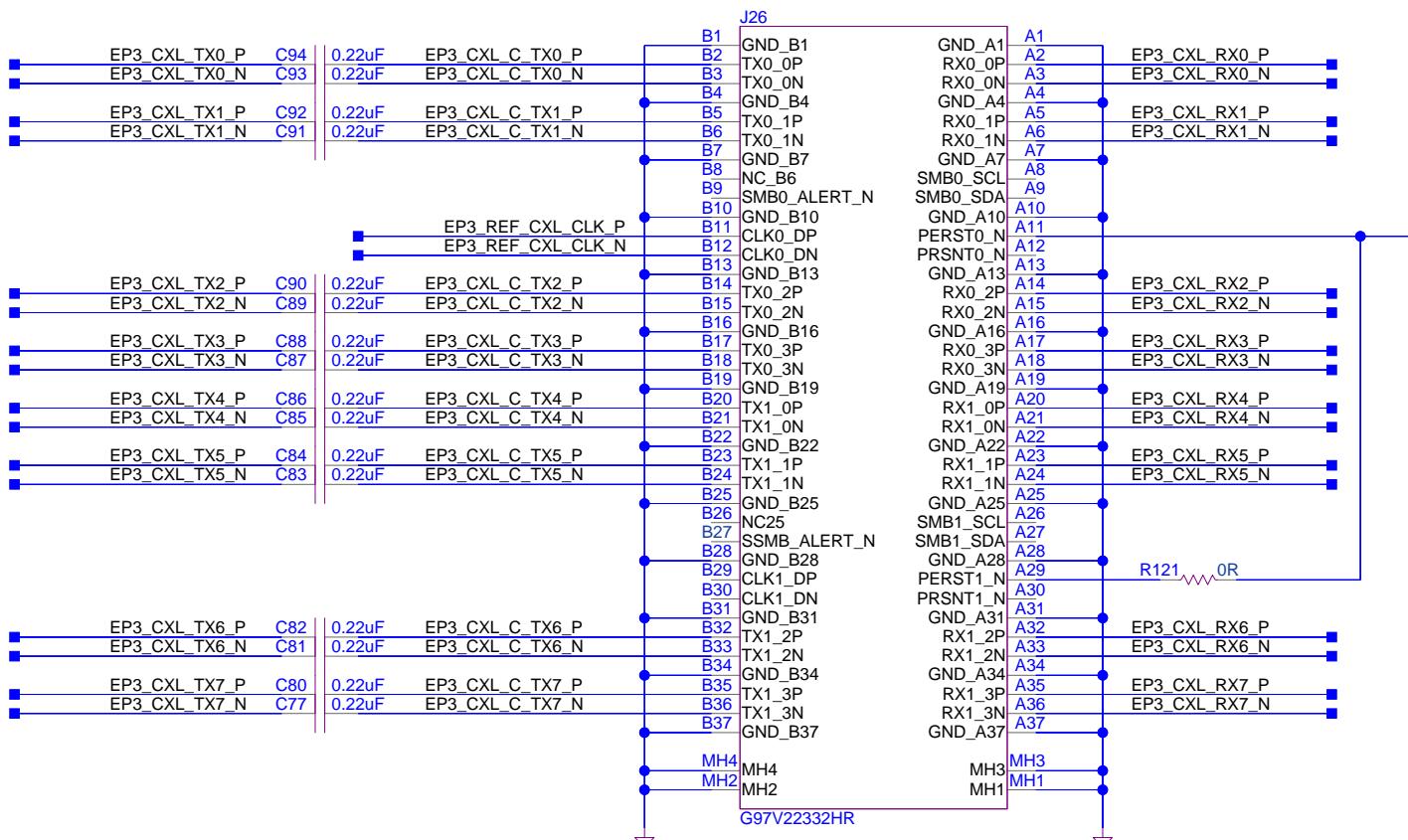
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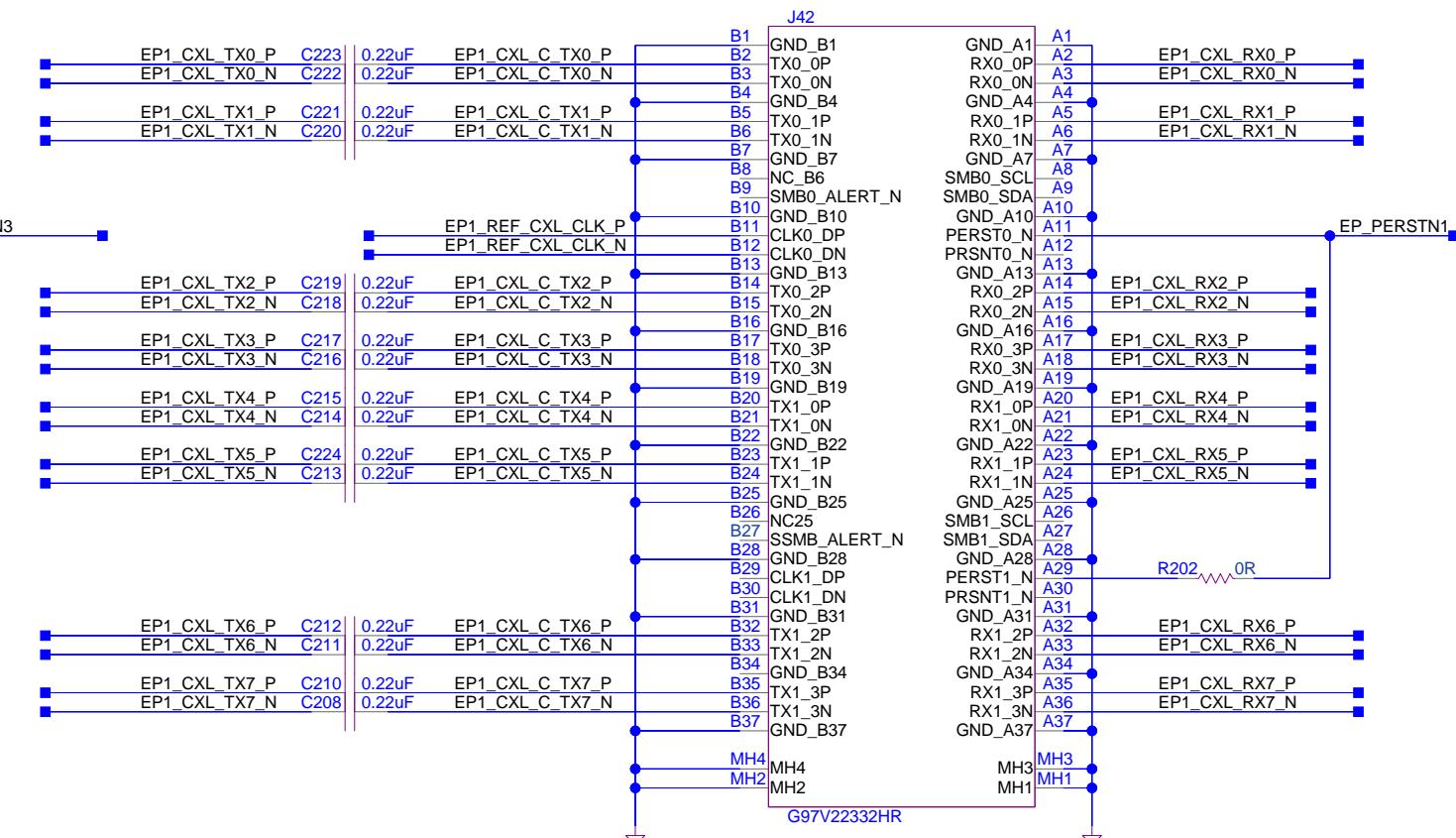
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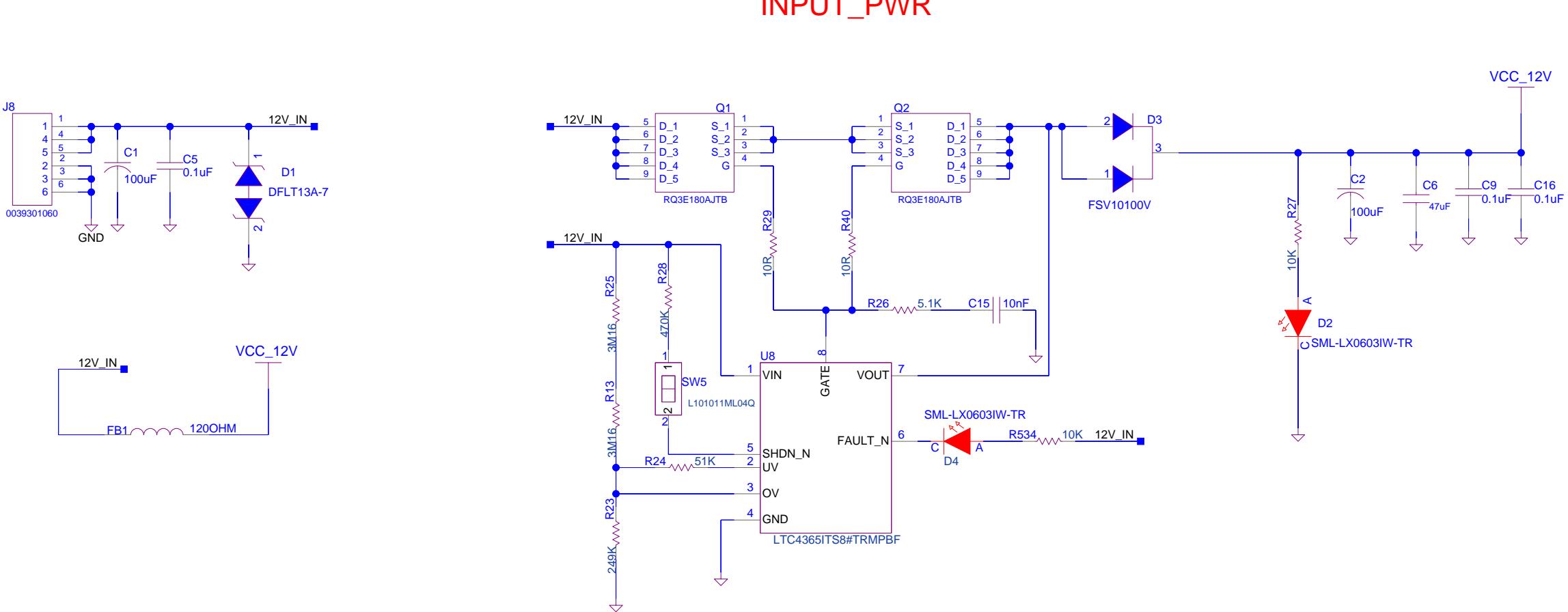
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MCIO_CONNECTORS

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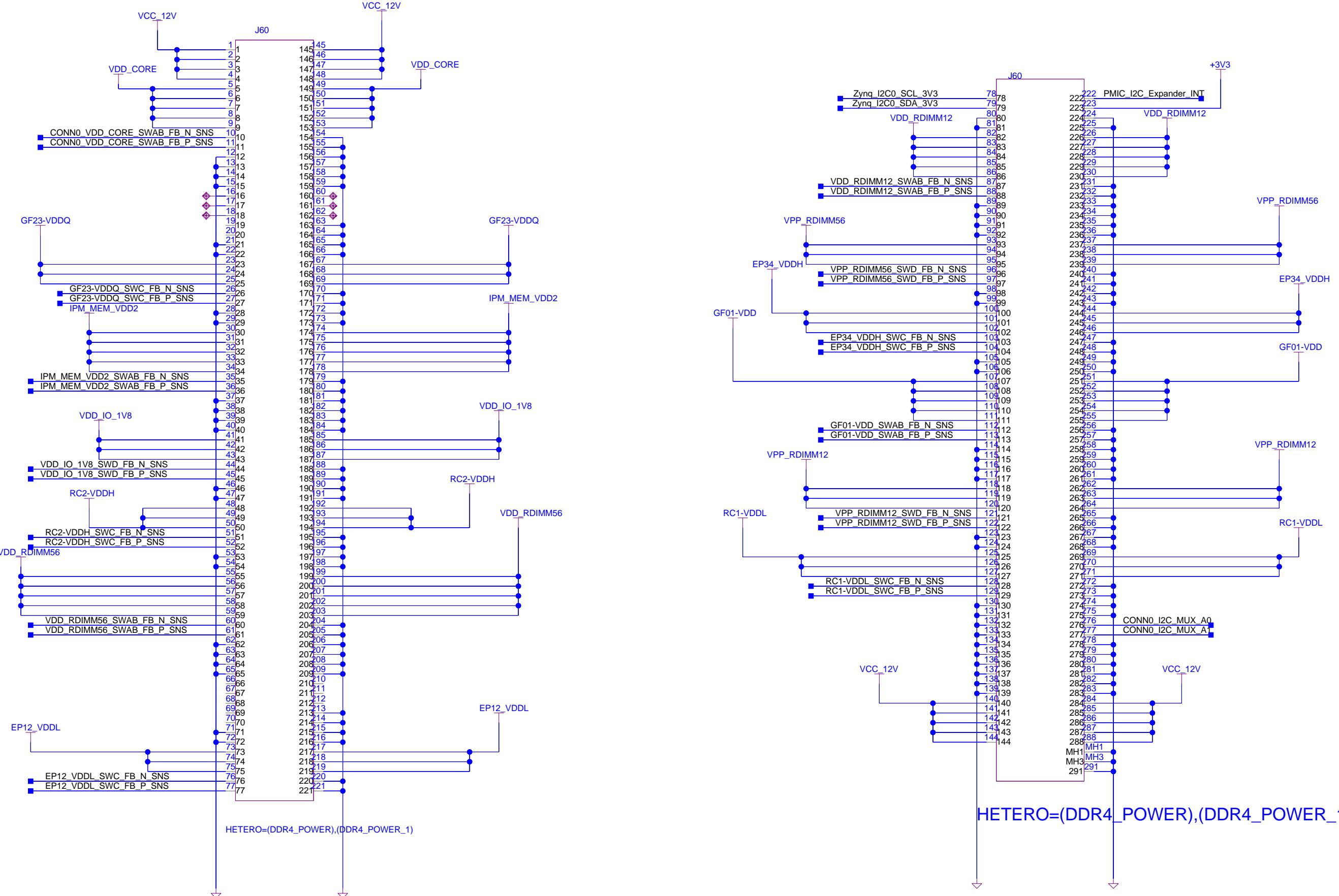


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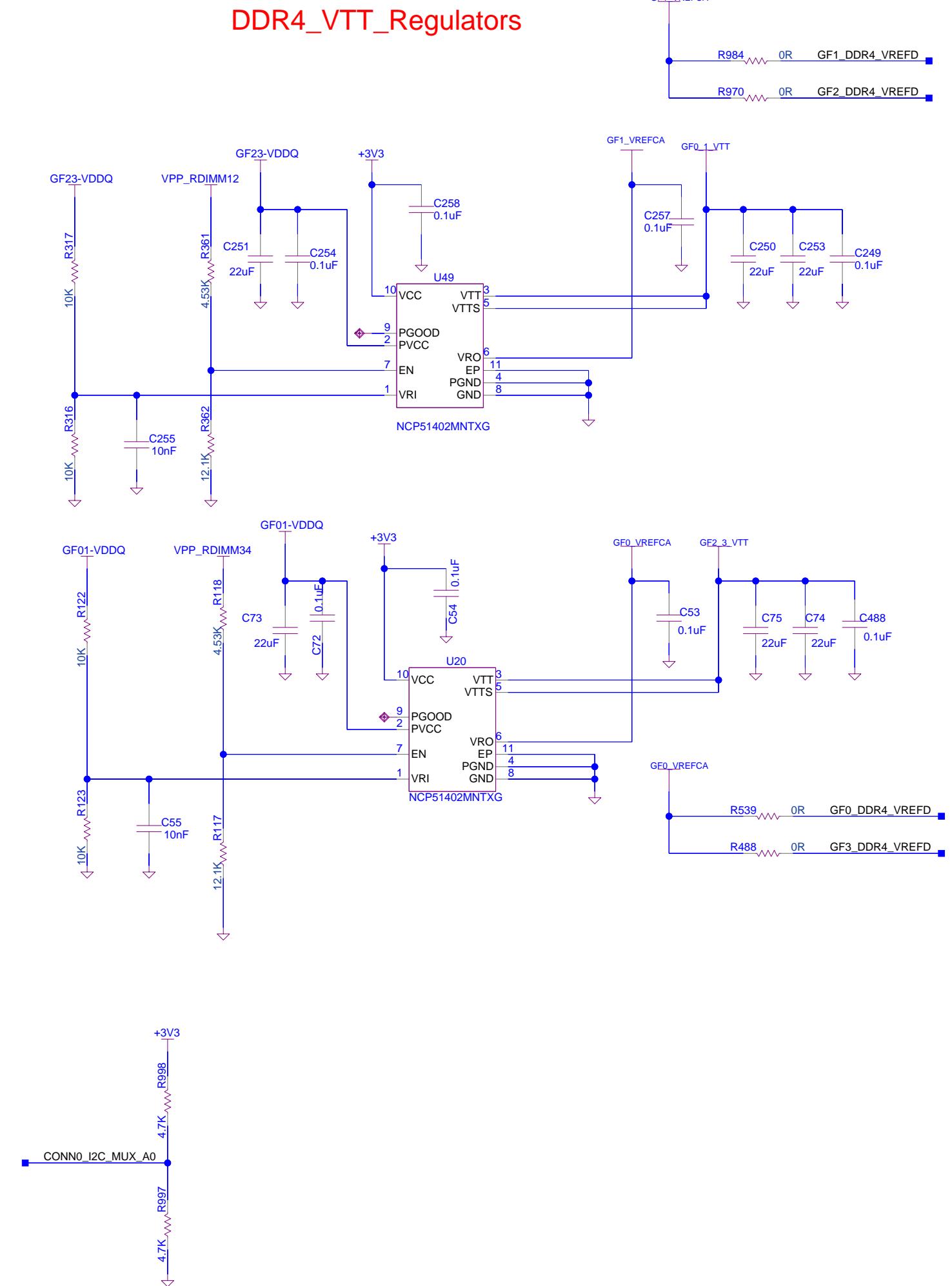


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MKB_Power_Conn



DDR4_VTT_Regulators

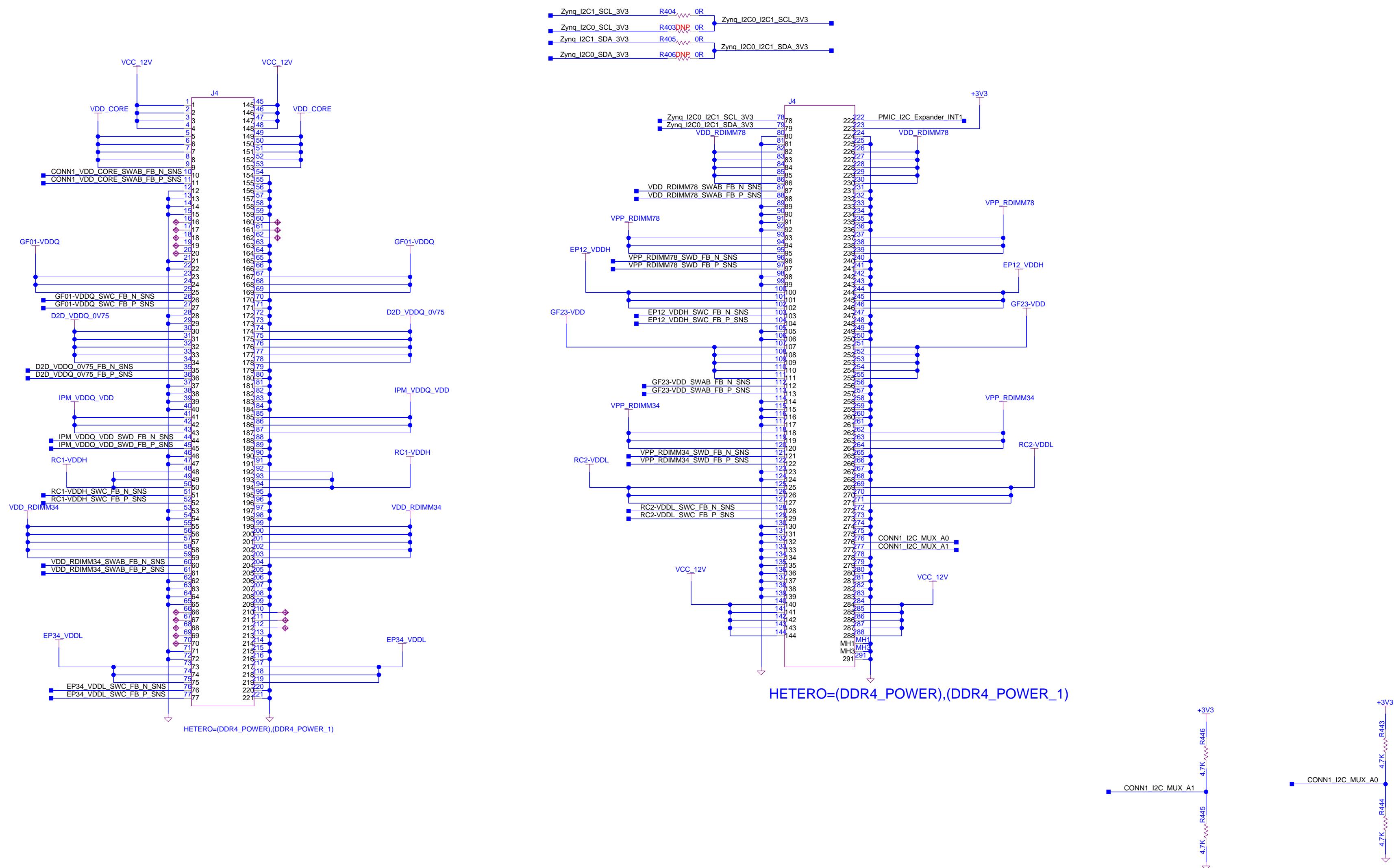


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MKB_Power_Conn



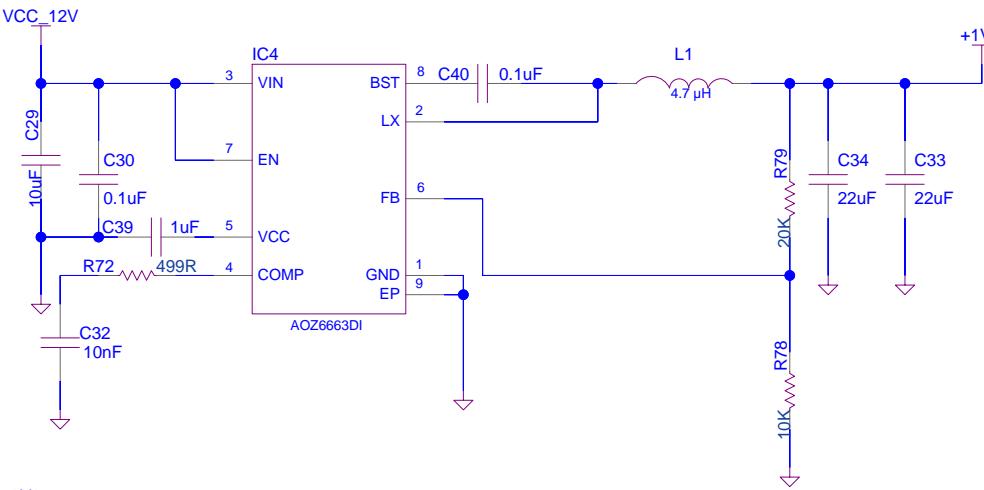
MKB_Power_Conn1



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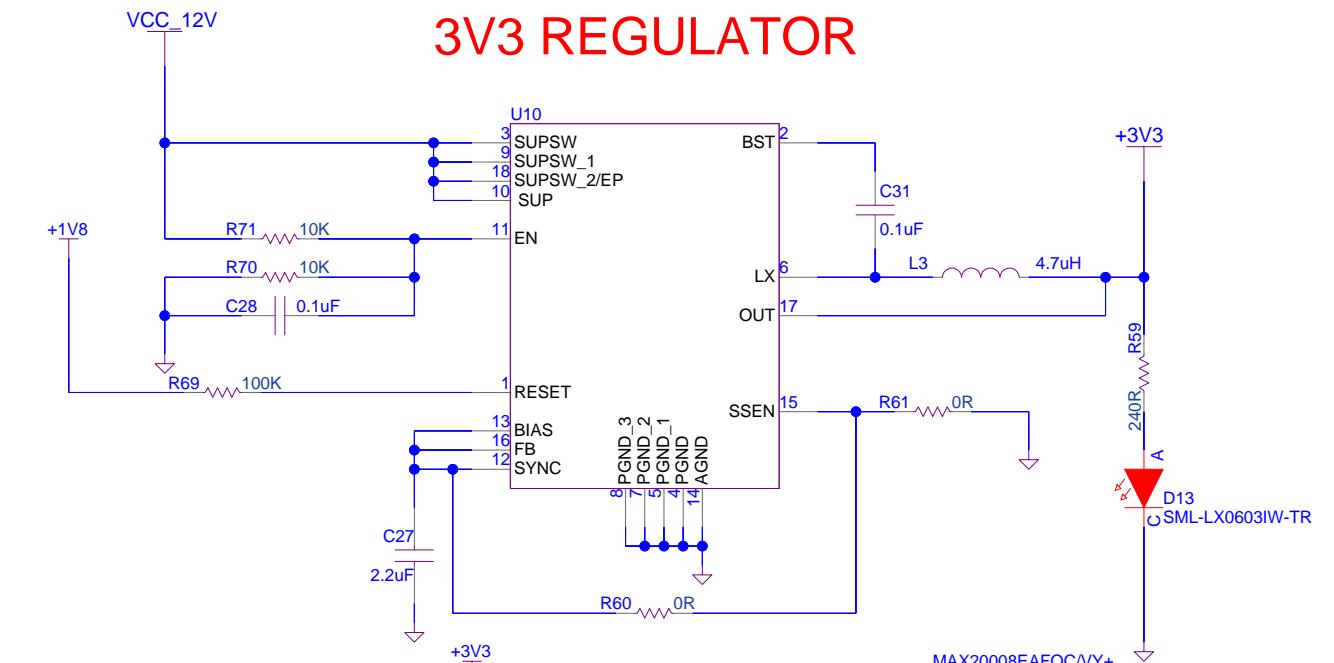
MKB_Power_Conn1

1V8 REGULATOR

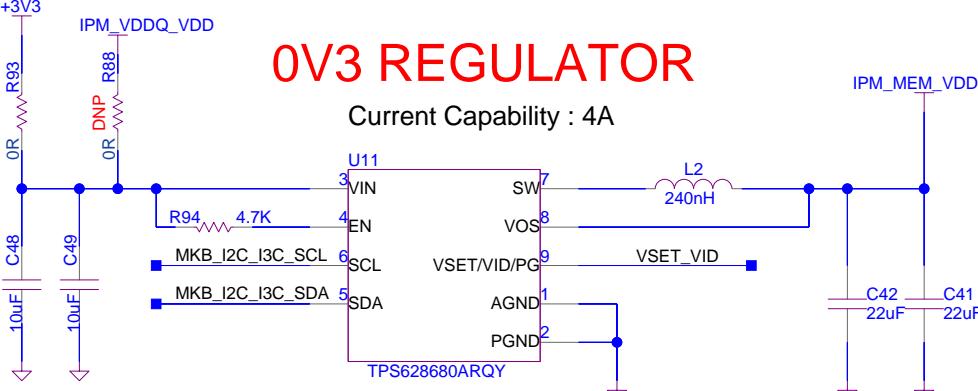


REGULATORS

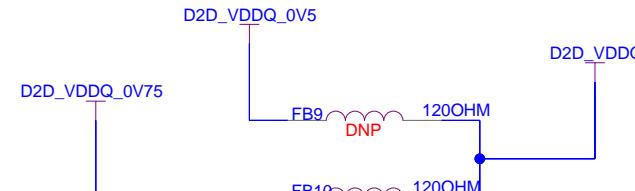
3V3 REGULATOR



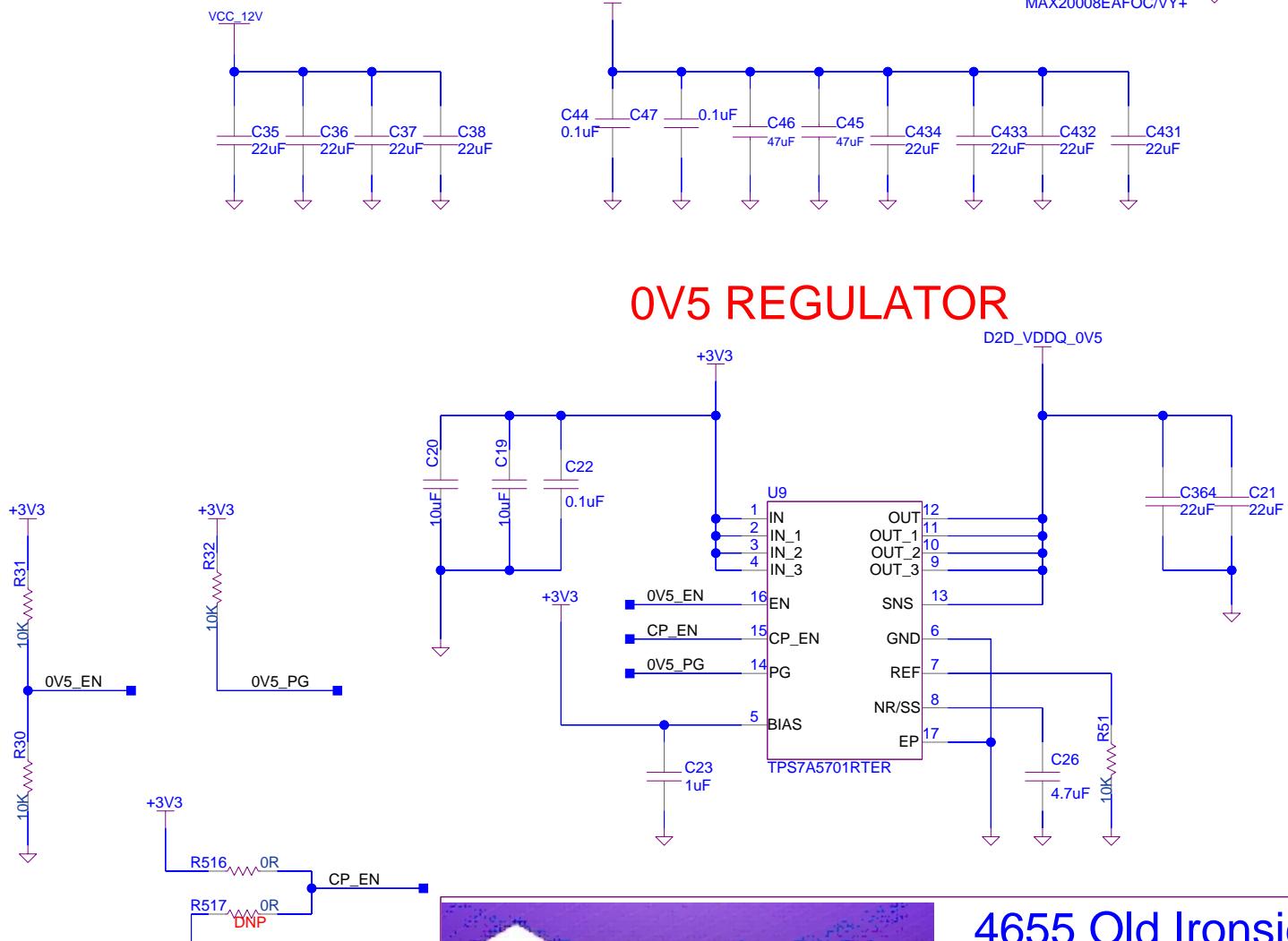
0V3 REGULATOR



Current Capability : 4A



0V5 REGULATOR



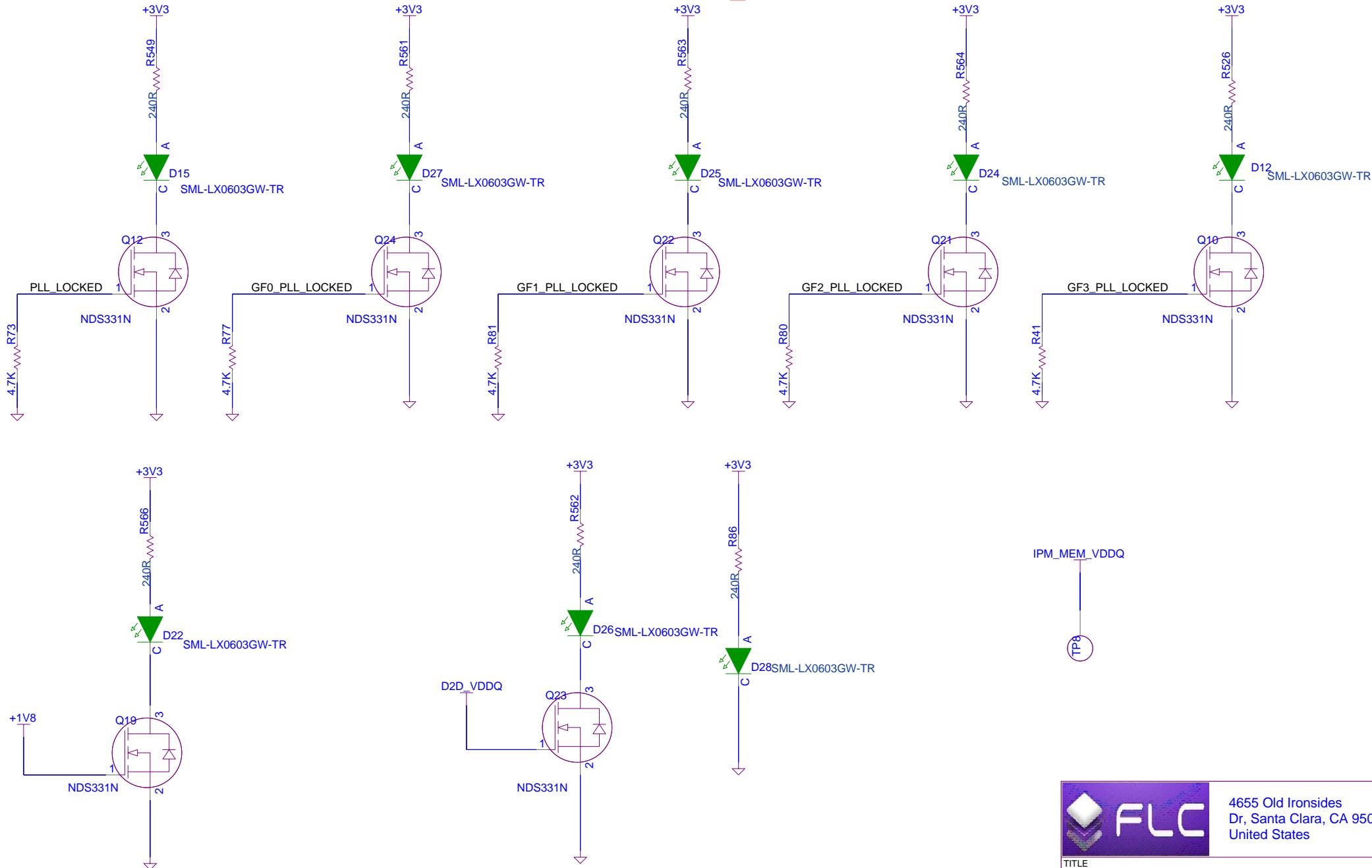
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REGULATORS

SHEET	DWG NO	REV
A3	Schematic1	1.0
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LED_INDICATORS



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TITLE

LED_INDICATORS

SIZE

A4

DWG NO

Schematic1

REV

SHEET

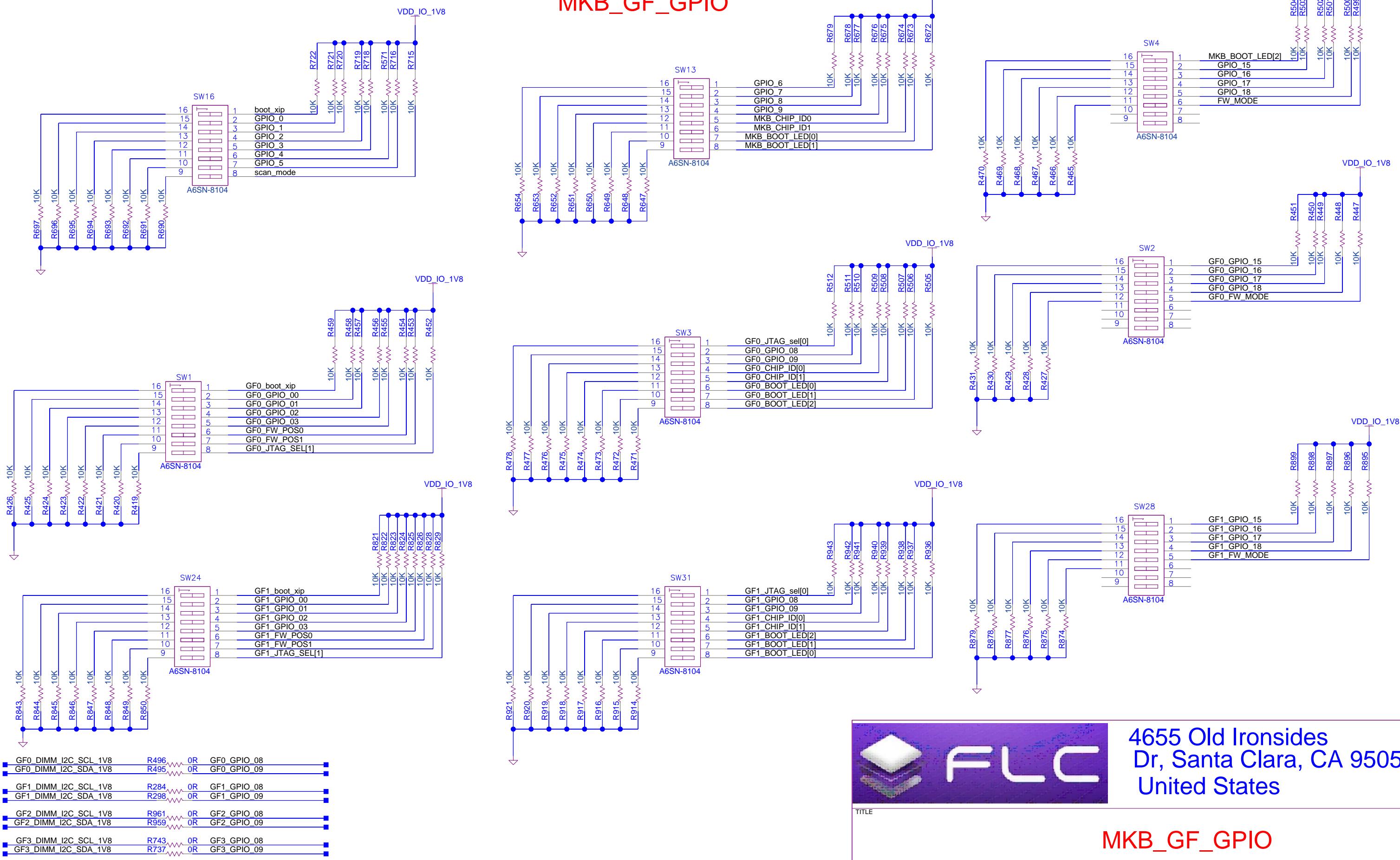
31

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MKB_GF_GPIO



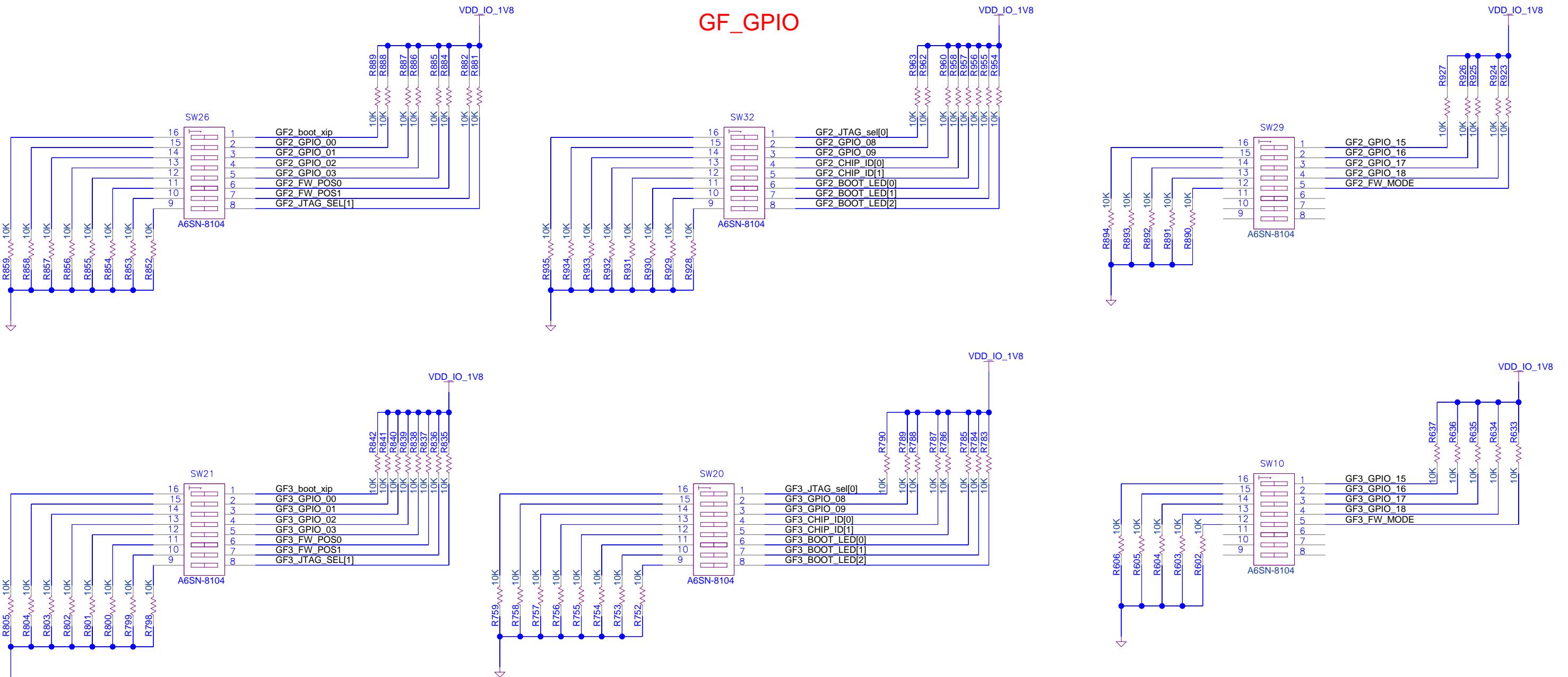
GF0_DIMM_I2C_SCL_1V8	R496 OR	GF0_GPIO_08
GF0_DIMM_I2C_SDA_1V8	R495 OR	GF0_GPIO_09
GF1_DIMM_I2C_SCL_1V8	R284 OR	GF1_GPIO_08
GF1_DIMM_I2C_SDA_1V8	R298 OR	GF1_GPIO_09
GF2_DIMM_I2C_SCL_1V8	R961 OR	GF2_GPIO_08
GF2_DIMM_I2C_SDA_1V8	R959 OR	GF2_GPIO_09
GF3_DIMM_I2C_SCL_1V8	R743 OR	GF3_GPIO_08
GF3_DIMM_I2C_SDA_1V8	R737 OR	GF3_GPIO_09

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MKB_GF_GPIO



TITLE	DWG NO	REV
Schematic1		
A3		1.0
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MKB GPIO LIST

GPIO4 -----> SPI_MOSI	GPIO12 -----> BOOT_LED[0]
GPIO5 -----> SPI_MISO	GPIO13 -----> BOOT_LED[1]
GPIO6 -----> SPI_CS	GPIO14 -----> BOOT_LED[2]
GPIO7 -----> SPI_CLK	GPIO15 -----> GF3_I3C_ready_GPIO18
GPIO8 -----> SCL	GPIO16 -----> GF2_I3C_ready_GPIO18
GPIO9 -----> SDA	GPIO17 -----> GF1_I3C_ready_GPIO18
GPIO10 -----> CHIP_ID0	GPIO18 -----> GF0_I3C_ready_GPIO18
GPIO11 -----> CHIP_ID1	GPIO19 -----> FW_MODE

GPIO0 -----> UART_RTS	GPIO11 -----> CHIP_ID[1]
GPIO1 -----> UART_CTS	GPIO12 -----> BOOT_LED[0]
GPIO2 -----> UART_TXD	GPIO13 -----> BOOT_LED[1]
GPIO3 -----> UART_RXD	GPIO14 -----> BOOT_LED[2]
GPIO4 -----> SPI_MOSI	GPIO15 -----> EXT_PHY_RESET_N
GPIO5 -----> SPI_MISO	GPIO16 -----> SPLSS
GPIO6 -----> SPL_CS	GPIO17 -----> SPI_CLK
GPIO7 -----> SPL_CLK	GPIO18 -----> I2C_SCL
GPIO8 -----> SCL	GPIO19 -----> I2C_SDA
GPIO9 -----> SDA	GPIO10 -----> CHIP_ID[0]
GPIO10 -----> FW_MODE	

GPIO11 -----> CHIP_ID[1]	GPIO12 -----> BOOT_LED[0]
GPIO13 -----> BOOT_LED[1]	GPIO14 -----> BOOT_LED[2]
GPIO15 -----> EXT_PHY_RESET_N	GPIO16 -----> SPLSS
GPIO16 -----> SPLSS	GPIO17 -----> SPI_CLK
GPIO17 -----> SPI_CLK	GPIO18 -----> I2C_SCL
GPIO18 -----> I2C_SCL	GPIO19 -----> I2C_SDA
GPIO19 -----> I2C_SDA	GPIO10 -----> CHIP_ID[0]
GPIO10 -----> CHIP_ID[0]	

GF GPIO LIST



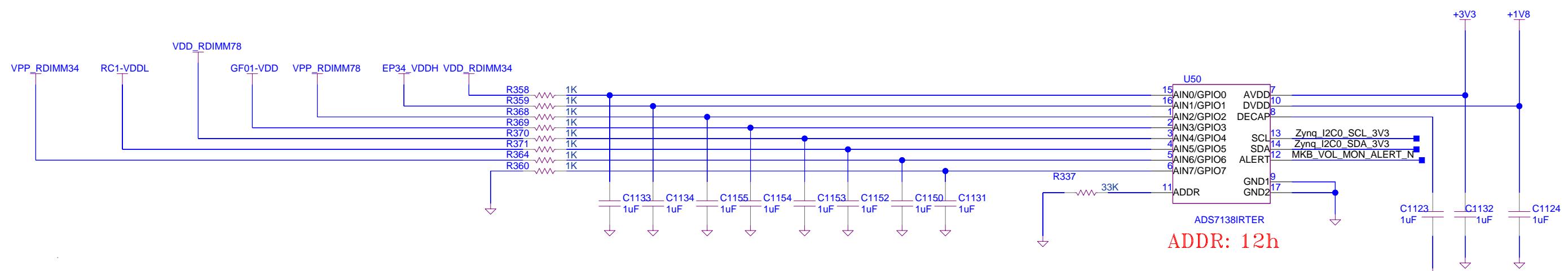
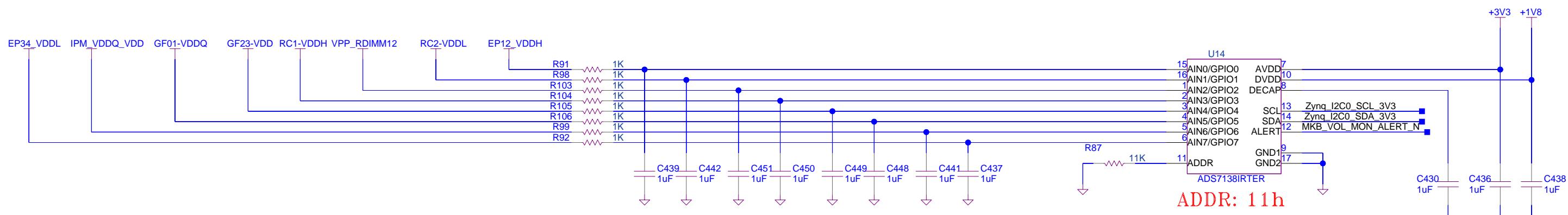
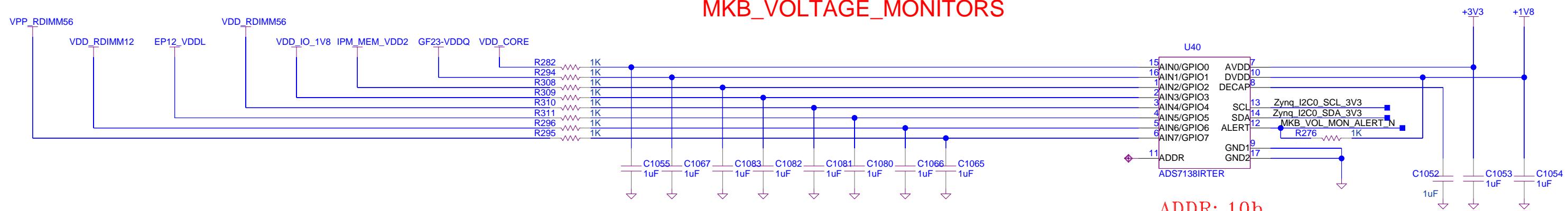
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GF_GPIO

Schematic1

1.0

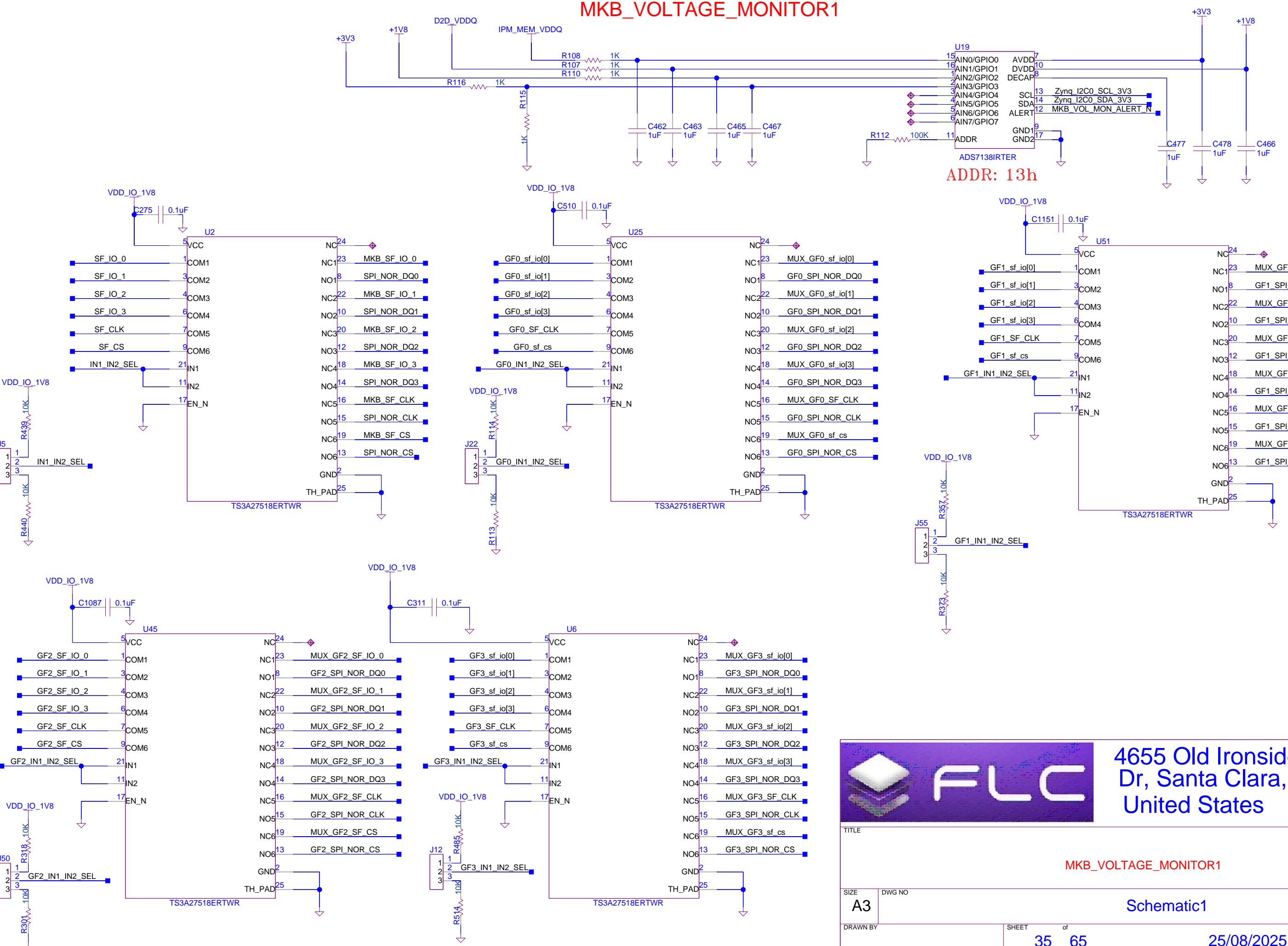
MKB_VOLTAGE_MONITORS



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TITLE	
SIZE	DWG NO
A3	Schematic1
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MKB_VOLTAGE_MONITOR1



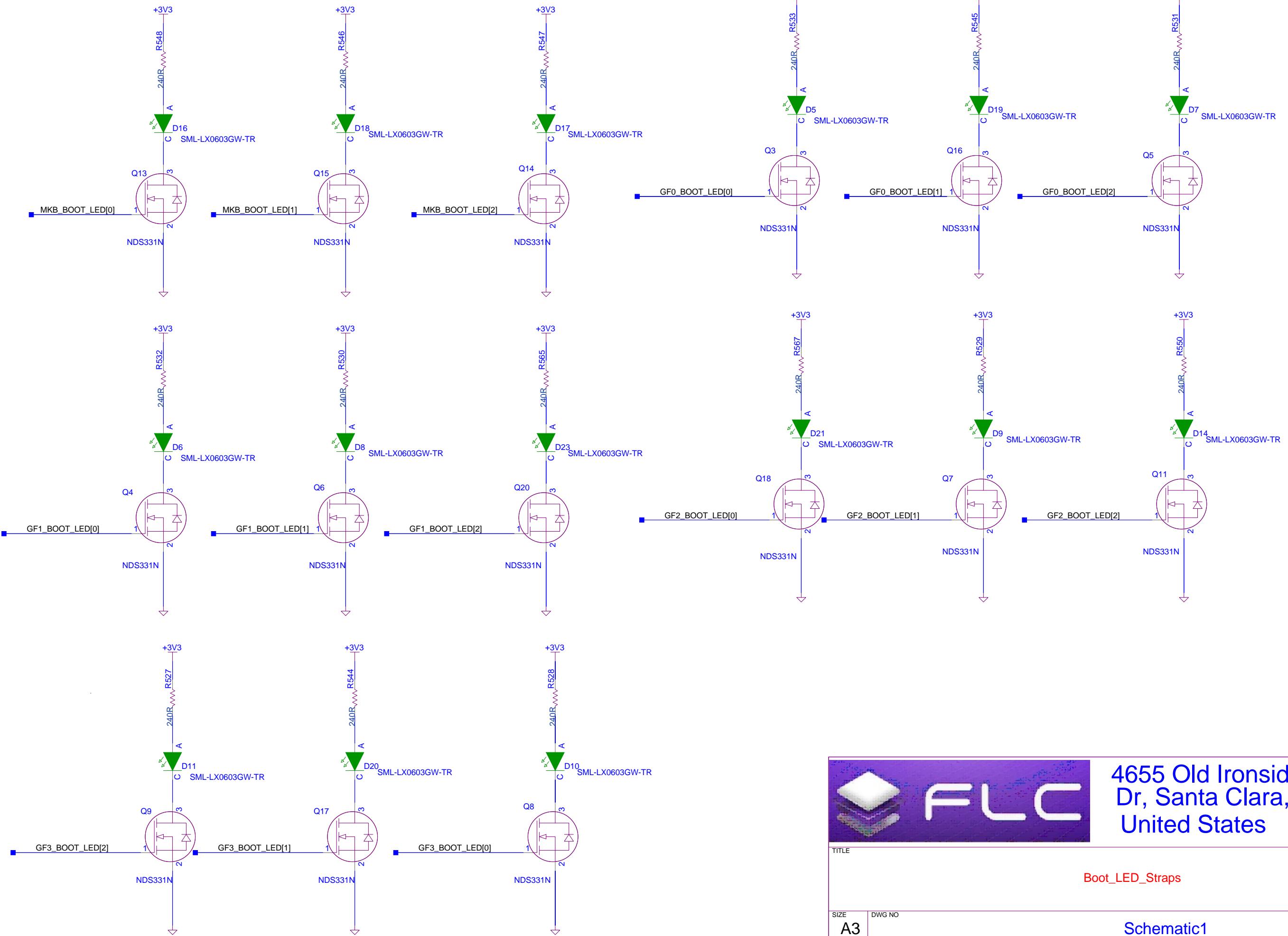
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MKB_VOLTAGE_MONITOR1

Schematic1

Boot_LED_Straps

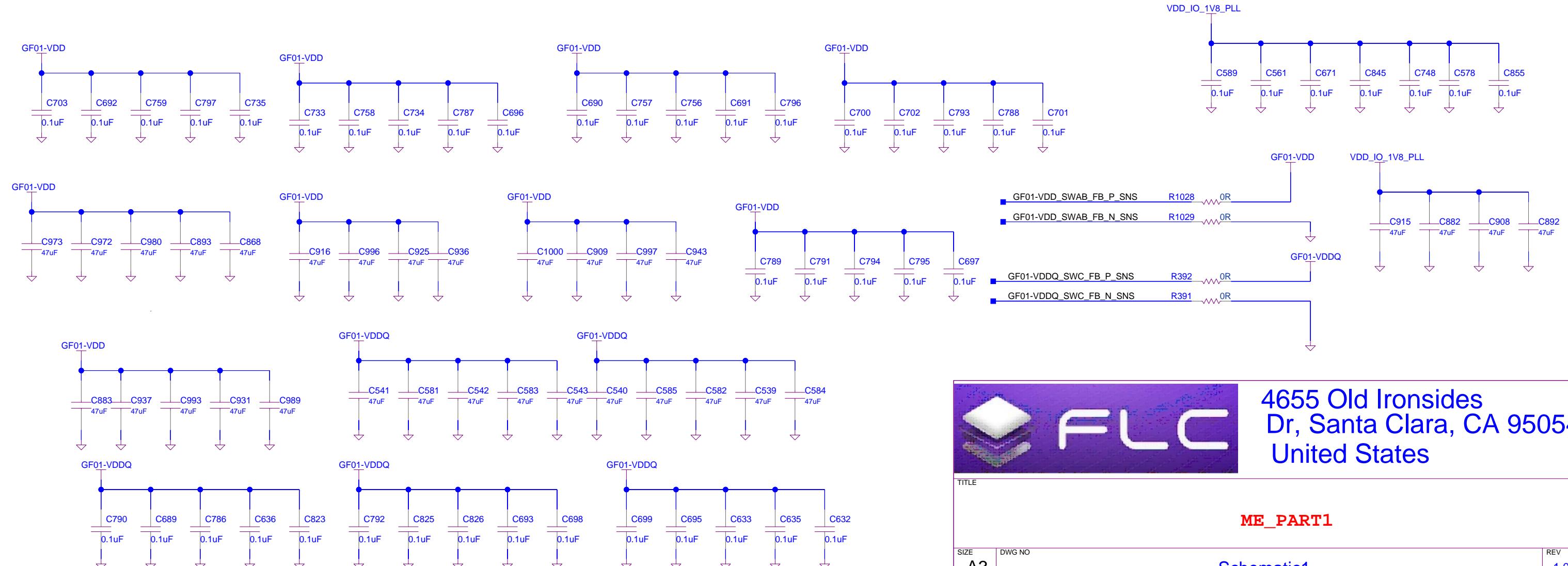
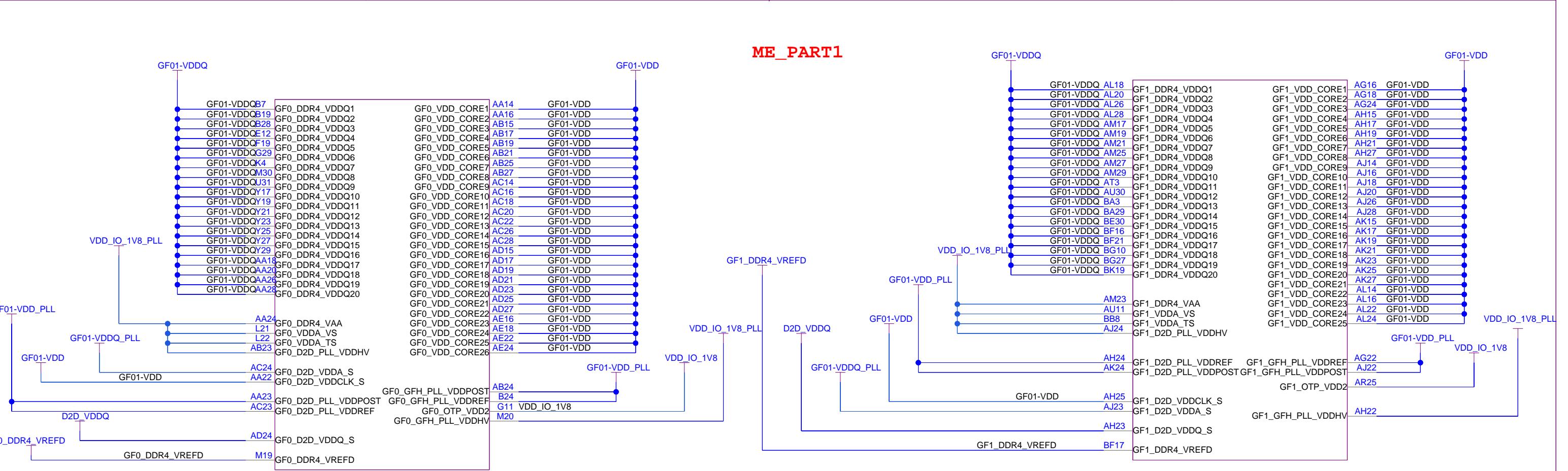


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Boot_LED_Straps

SIZE	DWG NO	REV
A3		1.0
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Schematic1

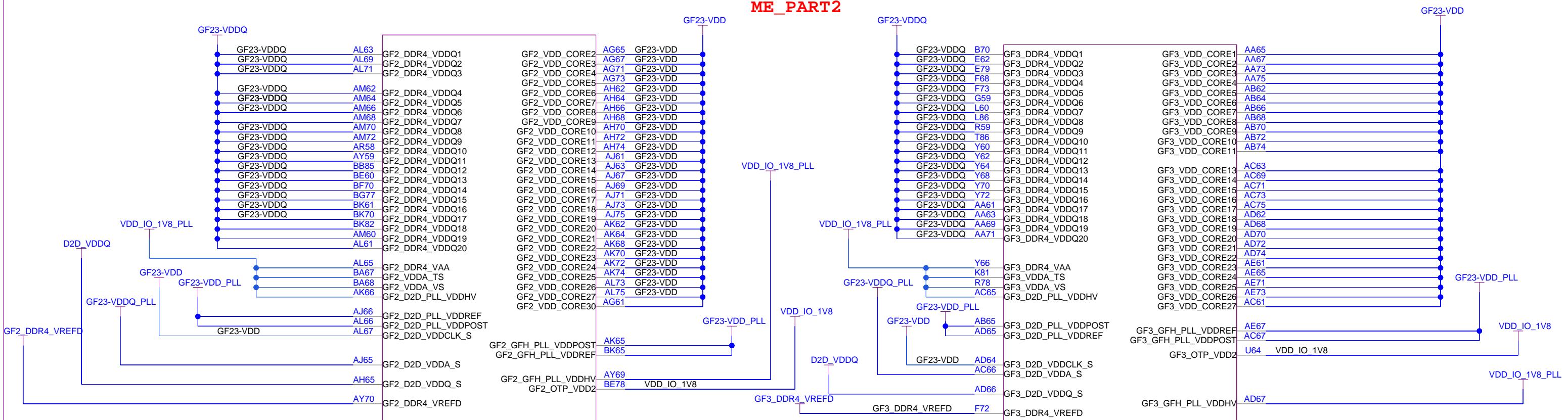


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ME_PART1

Schematic1

ME_PART2



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ME_PART2

SIZE	DWG NO	REV
A3	Schematic1	1.0
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GF1_DDR4_DQ63	AR2
GF1_DDR4_DQ58	AR3
GF1_DDR4_DQ59	AR4
GF1_DDR4_DQ0	AR28
GF1_DDR4_DQ2	AR29
GF1_DDR4_DQ1	AR30
GF1_DDR4_RDQSB_0	AR31
GF1_DDR4_DQ5	AR32
GF1_DDR4_DQ6	AT30
GF1_DDR4_DQS7_t	AT1
GF1_DDR4_DQS7_c	AT2
GF1_DDR4_DQSB_7	AT31
GF1_DDR4_DQS0_c	AT32
GF1_DDR4_DQS0_t	AT33
GF1_DDR4_DQ7	AU1
GF1_DDR4_DQ4	AT28
GF1_DDR4_DQ5	AT29
GF1_DDR4_DQ6	AT30
GF1_DDR4_DQS0	AT31
GF1_DDR4_DQS0_t	AT32
GF1_DDR4_DQ7	AU1
GF1_DDR4_DQ4	AU2
GF1_DDR4_RDQSB_7	AU3
GF1_DDR4_DQ56	AU4
GF1_DDR4_DQ57	AU4
GF1_DDR4_DQ3	AU29
GF1_DDR4_DQ7	AU31
GF1_DDR4_DQ54	AY2
GF1_DDR4_DQ61	AY3
GF1_DDR4_DQ60	AY4
GF1_DDR4_DQ9	AY29
GF1_DDR4_DQ12	AY30
GF1_DDR4_DQ13	AY31
GF1_DDR4_DQ8	AY32
GF1_DDR4_DQS6_c	BA1
GF1_DDR4_DQS6_t	BA2
GF1_DDR4_DQ51	BA4
GF1_DDR4_DQ14	BA30
GF1_DDR4_RDQSB_1	BA31
GF1_DDR4_DM1	BA32
GF1_DDR4_DM6	BB1
GF1_DDR4_RDQSB_6	BB2
GF1_DDR4_DQ55	BB3
GF1_DDR4_DQ49	BB4
GF1_DDR4_DQ50	BB5
GF1_DDR4_DQ11	BB29
GF1_DDR4_DQ10	BB30
GF1_DDR4_DQS1_c	BB31
GF1_DDR4_DQS1_t	BB32
GF1_DDR4_DQ48	BE2
GF1_DDR4_DQ53	BE3
GF1_DDR4_DQ52	BE4
GF1_DDR4_CID2	BE17
GF1_DDR4_DQ19	BE29
GF1_DDR4_DQ15	BE31
GF1_DDR4_DQ43	BF1
GF1_DDR4_DQ42	BF2
GF1_DDR4_DQ45	BF3
GF1_DDR4_DQ44	BF4
GF1_DDR4_DQ35	BF5
GF1_DDR4_DQ38	BF6
GF1_DDR4_DQ32	BF7
GF1_DDR4_CS1_n	BF8
GF1_DDR4_ODT1	BF9
GF1_DDR4_CS0_n	BF10
GF1_DDR4_BA1	BF11
GF1_DDR4_A0	BF12
GF1_DDR4_A1	BF15
GF1_DDR4_CID0	BF18
GF1_DDR4_CID_0	BF19
GF1_DDR4_A9	BF20
GF1_DDR4_A11	BF22
GF1_DDR4_RESET_N	BF23
GF1_DDR4_DQ67	BF24
GF1_DDR4_DQ66	BF25
GF1_DDR4_DQ68	BF26
GF1_DDR4_DQ27	BF27
GF1_DDR4_DQ24	BF28
GF1_DDR4_DQ28	BF29
GF1_DDR4_DQ16	BF30
GF1_DDR4_DQ20	BF31
GF1_DDR4_DQ21	BF32
GF1_DDR4_DQ47	BG1
GF1_DDR4_DM5	BG2
GF1_DDR4_RDQSB_5	BG3
GF1_DDR4_DQ34	BG4

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GF0_DDR4_DQS2_t	A2	GF0_DDR4_DQS_2	F10
GF0_DDR4_DQ23	A3	GF0_DDR4_DQ_23	F11
GF0_DDR4_DQS3_c	A5	GF0_DDR4_DQ_1	F12
GF0_DDR4_DQ30	A6	GF0_DDR4_RESET_N	F13
GF0_DDR4_DQ_30	A7	GF0_DDR4_ADDR_9	F14
GF0_DDR4_DQS8_c	A8	GF0_DDR4_DQ_65	F15
GF0_DDR4_CKE0	A10	GF0_DDR4_DQS8_8	F17
GF0_DDR4_A12	A12	GF0_DDR4_CKE_0	F18
GF0_DDR4_CID1	A14	GF0_DDR4_ADDR_12	F21
GF0_DDR4_CLK3_c	A15	GF0_DDR4_ADDR_6	F22
GF0_DDR4_CLK1_c	A16	GF0_DDR4_DQ_3	F23
GF0_DDR4_CLK2_c	A17	GF0_DDR4_CID_0	F25
GF0_DDR4_CLK0_c	A18	GF0_DDR4_ODT_1	F26
GF0_DDR4_CLKN_2	A20	GF0_DDR4_DQ_37	F27
GF0_DDR4_A0	A21	GF0_DDR4_DQ39	F28
GF0_DDR4_ODT2	A22	GF0_DDR4_DQ_35	F29
GF0_DDR4_CID2	A23	GF0_DDR4_DQ44	F30
GF0_DDR4_ODT3	A24	GF0_DDR4_DQ47	F31
GF0_DDR4_ODT0	A26	GF0_DDR4_DQ_42	G1
GF0_DDR4_DQ33	A27	GF0_DDR4_DQ_33	G2
GF0_DDR4_DQS4_c	A28	GF0_DDR4_DQS8_4	G3
GF0_DDR4_DQ38	A29	GF0_DDR4_DQ_38	G4
GF0_DDR4_DQ45	A30	GF0_DDR4_DQ_45	G7
GF0_DDR4_DQ41	B1	GF0_DDR4_DQ_41	G19
GF0_DDR4_DQS2_c	B2	GF0_DDR4_DQM_2	G20
GF0_DDR4_DQ18	B3	GF0_DDR4_DQS8_2	G21
GF0_DDR4_DQ25	B4	GF0_DDR4_DQ_18	G26
GF0_DDR4_DQS3_t	B5	GF0_DDR4_DQ_25	G28
GF0_DDR4_DQS3	B6	GF0_DDR4_DQ_52	G30
GF0_DDR4_DQ31	B7	GF0_DDR4_DQ_43	G31
GF0_DDR4_DQ_31	B9	GF0_DDR4_DQ_49	K2
GF0_DDR4_DQ70	B10	GF0_DDR4_DQ_15	K3
GF0_DDR4_BG1	B11	GF0_DDR4_DQ14	K14
GF0_DDR4_PARITY	B12	GF0_DDR4_DQ_53	K28
GF1_DDR4_CLK1_t	B13	GF0_DDR4_ALERT_N	K29
GF0_DDR4_CLK3_t	B14	GF0_DDR4_ALERT_N	K48
GF1_DDR4_CLK0_t	B15	GF0_DDR4_ADDR_11	K30
GF1_DDR4_CLK2_t	B16	GF0_DDR4_ADDR_5	K31
GF1_DDR4_A3	B17	GF0_DDR4_CLK_3	L1
GF1_DDR4_ALERT_N	B18	GF0_DDR4_CLK_1	L2
GF1_DDR4_BG_1	B19	GF0_DDR4_CLK_2	L3
GF1_DDR4_CKE0	B20	GF0_DDR4_CLK_9	L4
GF1_DDR4_DQ_50	B21	GF0_DDR4_CLK_13	L18
GF1_DDR4_DQ70	B22	GF0_DDR4_CKE2	L29
GF1_DDR4_RDQSB_8	B23	GF0_DDR4_BA_0	L54
GF1_DDR4_DM8	B24	GF0_DDR4_CS2_n	L30
GF1_DDR4_DQ26	B25	GF0_DDR4_CSN_2	M1
GF1_DDR4_DQ26	B26	GF0_DDR4_CS0_n	M2
GF1_DDR4_DQ30	B27	GF0_DDR4_DQ_32	M3
GF1_DDR4_DQS3_t	B28	GF0_DDR4_DQS_4	M4
GF1_DDR4_DQ29	B29	GF0_DDR4_DQ_40	M18
GF1_DDR4_DQ18	B30	GF0_DDR4_DQS_5	M21
GF1_DDR4_DQS2_c	B31	GF0_DDR4_DQS5_c	M21
GF1_DDR4_DM2	B32	GF0_DDR4_RDQSB_2	M28
GF1_DDR4_DQ46	B33	GF0_DDR4_DQ_51	M29
GF1_DDR4_DQS5_c	B34	GF0_DDR4_DQ_50	M31
GF1_DDR4_DQ41	B35	GF0_DDR4_DQ_55	R2
GF1_DDR4_DQS4_c	B36	GF0_DDR4_DQ_6	R3
GF1_DDR4_DQ36	B37	GF0_DDR4_DQ_24	R4
GF1_DDR4_DQ33	B38	GF0_DDR4_DQ_3	R28
GF1_DDR4_ODT3	B39	GF0_DDR4_DQ_60	R29
GF1_DDR4_A15	B40	GF0_DDR4_DQ_61	R30
GF1_DDR4_DQS5_c	B41	GF0_DDR4_DQ_56	R31
GF1_DDR4_DQ16	B42	GF0_DDR4_DQ_57	T1
GF1_DDR4_DQ16	B43	GF0_DDR4_DQS0_t	T2
GF1_DDR4_DQ19	B44	GF0_DDR4_DQS0_c	T2
GF1_DDR4_DQ19	B45	GF0_DDR4_DQ51	T3
GF1_DDR4_DQ17	B46	GF0_DDR4_DQ50	M29
GF1_DDR4_DQ17	B47	GF0_DDR4_DQ55	M31
GF1_DDR4_DQ19	B48	GF0_DDR4_DQ66	R2
GF1_DDR4_DQ19	B49	GF0_DDR4_DQ67	T27
GF1_DDR4_DQ19	B50	GF0_DDR4_DQ68	T28
GF1_DDR4_DQ19	B51	GF0_DDR4_DQ69	F1
GF1_DDR4_DQ19	B52	GF0_DDR4_DQ71	E25
GF1_DDR4_DQ19	B53	GF0_DDR4_DQ71	E26
GF1_DDR4_DQ19	B54	GF0_DDR4_DQ72	E27
GF1_DDR4_DQ19	B55	GF0_DDR4_DQ73	E28
GF1_DDR4_DQ19	B56	GF0_DDR4_DQ74	E29
GF1_DDR4_DQ19	B57	GF0_DDR4_DQ75	E30
GF1_DDR4_DQ19	B58	GF0_DDR4_DQ76	E31
GF1_DDR4_DQ19	B59	GF0_DDR4_DQ77	F1
GF1_DDR4_DQ19	B60	GF0_DDR4_DQ78	F2
GF1_DDR4_DQ19	B61	GF0_DDR4_DQ79	F4
GF1_DDR4_DQ19	B62	GF0_DDR4_DQ80	F5
GF1_DDR4_DQ19	B63	GF0_DDR4_DQ81	F6
GF1_DDR4_DQ19	B64	GF0_DDR4_DQ82	F7
GF1_DDR4_DQ19	B65	GF0_DDR4_DQ83	F8
GF1_DDR4_DQ19	B66	GF0_DDR4_DQ84	F9

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ME_PART3



TITLE

SIZE DWG NO

A3

Schematic1

REV

1.0

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ME_PART4

GF2_DDR4_DQ4	AM85	GF2_DDR4_DQ_4	BF83	GF2_DDR4_DQ27
GF2_DDR4_DQ0	AM87	GF2_DDR4_DQ_0	BF84	GF2_DDR4_DM3
GF2_DDR4_DQ63	AR59	GF2_DDR4_DQM_3	BF85	GF2_DDR4_DQ29
GF2_DDR4_DQ58	AR60	GF2_DDR4_DQ_63	BF87	GF2_DDR4_DQ22
GF2_DDR4_DQ59	AR61	GF2_DDR4_DQ_58	BF88	GF2_DDR4_DQ21
GF2_DDR4_DQ5	AR85	GF2_DDR4_DQ_59	BF58	GF2_DDR4_DQ46
GF2_DDR4_DQ1	AR86	GF2_DDR4_DQ_5	BF59	GF2_DDR4_RDQSB_5
GF2_DDR4_RDQSB_0	AR87	GF2_DDR4_RDQSB_0	BF60	GF2_DDR4_DM5
GF2_DDR4_DM0	AR88	GF2_DDR4_DQM_0	BF61	GF2_DDR4_DQ34
GF2_DDR4_DQS7_c	AT58	GF2_DDR4_DQM_0	BF62	GF2_DDR4_DM4
GF2_DDR4_DQS7_t	AT59	GF2_DDR4_DQS_7	BF63	GF2_DDR4_RDQSB_4
GF2_DDR4_RDQSB_7	AT60	GF2_DDR4_RDQSB_7	BF64	GF2_DDR4_A17
GF2_DDR4_DM7	AT61	GF2_DDR4_ADDR_17	BF66	GF2_DDR4_A13
GF2_DDR4_DQ62	AT62	GF2_DDR4_DQM_7	BF68	GF2_DDR4_A15
GF2_DDR4_DQ7	AT86	GF2_DDR4_DQ_62	BF75	GF2_DDR4_A7
GF2_DDR4_DQS0_c	AT87	GF2_DDR4_DQ_7	BT76	GF2_DDR4_A4
GF2_DDR4_DQS0_t	AT88	GF2_DDR4_DQS_0	BT78	GF2_DDR4_ACT_N
GF2_DDR4_DQ57	AU58	GF2_DDR4_DQ_57	BT80	GF2_DDR4_DQS_0
GF2_DDR4_DQ56	AU59	GF2_DDR4_DQM_56	BT81	GF2_DDR4_DQ71
GF2_DDR4_DQ61	AU60	GF2_DDR4_DQ_61	BT82	GF2_DDR4_DM8
GF2_DDR4_DQ60	AU61	GF2_DDR4_DQ_60	BT83	GF2_DDR4_DQ26
GF2_DDR4_DQ3	AU85	GF2_DDR4_DQ_3	BT84	GF2_DDR4_RDQSB_3
GF2_DDR4_DQ2	AU86	GF2_DDR4_DQ_2	BT85	GF2_DDR4_DQ24
GF2_DDR4_DQ6	AU87	GF2_DDR4_DQ_6	BT86	GF2_DDR4_DQ19
GF2_DDR4_DQ55	AY58	GF2_DDR4_DQM_55	BT87	GF2_DDR4_DQ16
GF2_DDR4_DQ50	AY60	GF2_DDR4_DQ_50	BT88	GF2_DDR4_DQ17
GF2_DDR4_DQ51	AY61	GF2_DDR4_DQ_51	BT89	GF2_DDR4_RDQSB_2
GF2_DDR4_CS3_n	AY68	GF2_DDR4_CSN_3	BK58	GF2_DDR4_DQS5_c
GF2_DDR4_CKE3	AY71	GF2_DDR4_CKE_3	BK59	GF2_DDR4_DQS5_t
GF2_DDR4_DQ12	AY85	GF2_DDR4_DQ_12	BK60	GF2_DDR4_DQ40
GF2_DDR4_DQ8	AY86	GF2_DDR4_DQ_8	BK62	GF2_DDR4_DQS4_t
GF2_DDR4_RDQSB_1	AY87	GF2_DDR4_RDQSB_1	BK63	GF2_DDR4_DQ32
GF2_DDR4_DM1	AY88	GF2_DDR4_DQM_1	BK64	GF2_DDR4_CS1_n
GF2_DDR4_DQS6_t	BA58	GF2_DDR4_DQS_6	BK66	GF2_DDR4_CS0_n
GF2_DDR4_DQS6_c	BA59	GF2_DDR4_DQS_0	BK67	GF2_DDR4_CS2_n
GF2_DDR4_DQ54	BA60	GF2_DDR4_DQS_6	BK68	GF2_DDR4_BA0
GF2_DDR4_CKE2	BA71	GF2_DDR4_CKE_2	BK69	GF2_DDR4_PARITY
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GF2_DDR4_DQ9	BA86	GF2_DDR4_DQ_9	BK72	GF2_DDR4_CLK2_t
GF2_DDR4_DQS1_t	BA87	GF2_DDR4_DQS_1	BK73	GF2_DDR4_CLK1_t
GF2_DDR4_DQS1_c	BA88	GF2_DDR4_DQS_1	BK74	GF2_DDR4_CLK3_t
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GF2_DDR4_DM6	BB59	GF2_DDR4_DQM_6	BK76	GF2_DDR4_A11
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GF2_DDR4_DQ53	BB61	GF2_DDR4_DQ_53	BK78	GF2_DDR4_BG0
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GF3DDR4_ALERT_N	B69	GF3DDR4_ALERT_N	K87	GF3DDR4_RDQSB_6
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GF3DDR4_CLK2_t	B72	GF3DDR4_CLK2_t	L57	GF3DDR4_DM1
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GF3DDR4_CLK3_t	B74	GF3DDR4_CLK3_t	L59	GF3DDR4_DQ14
GF3DDR4_CLK1_t	B75	GF3DDR4_CLK1_t	L65	GF3DDR4_DQ51
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ME_PART5



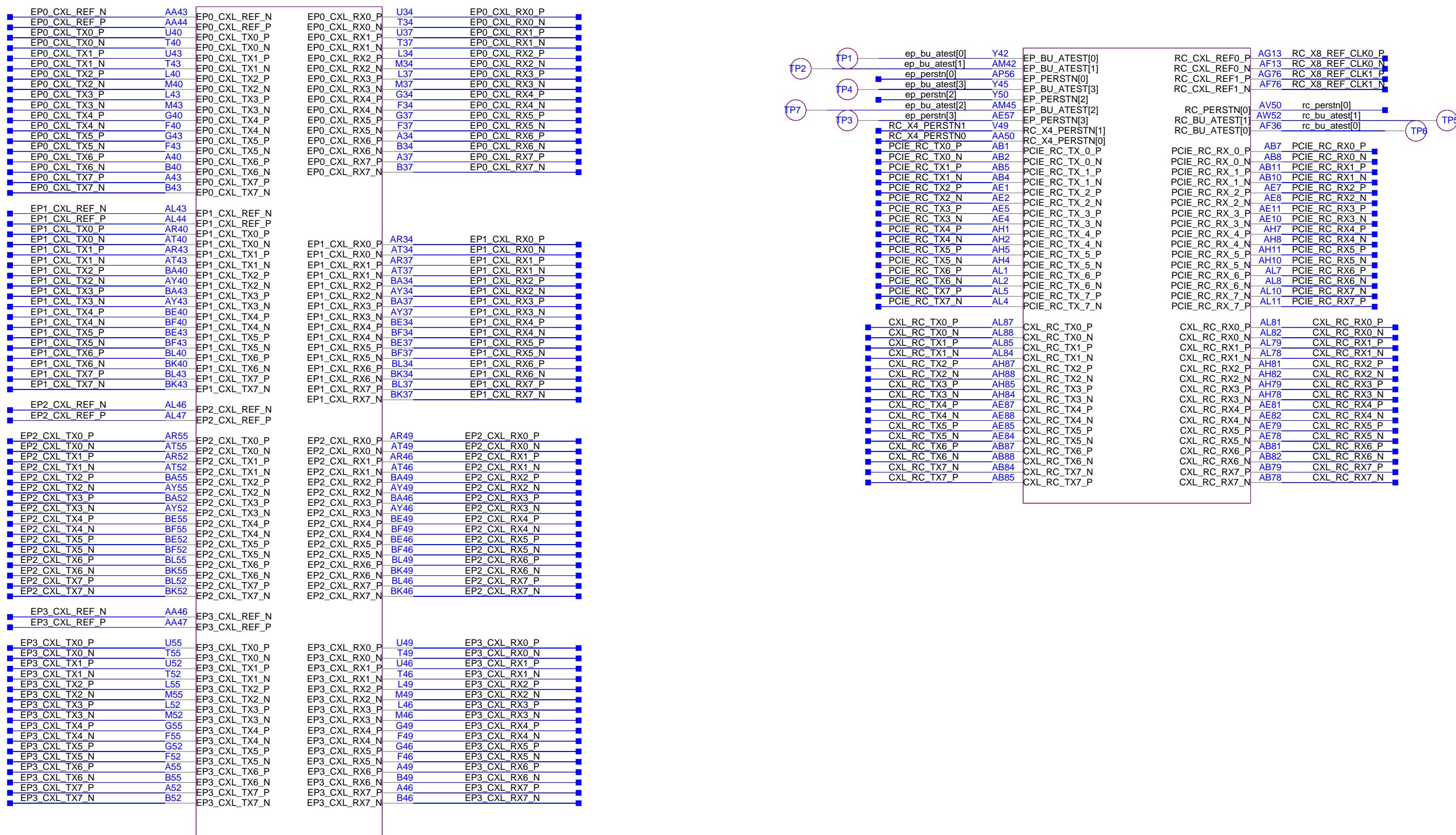
4655 Old Ironsides
Dr, Santa Clara, CA 95054,
United States



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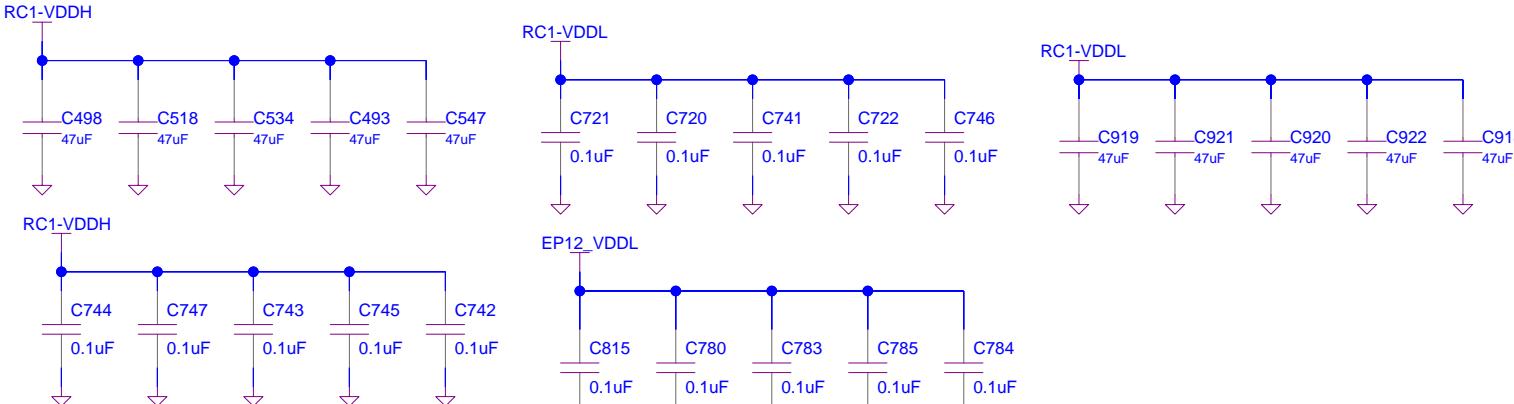
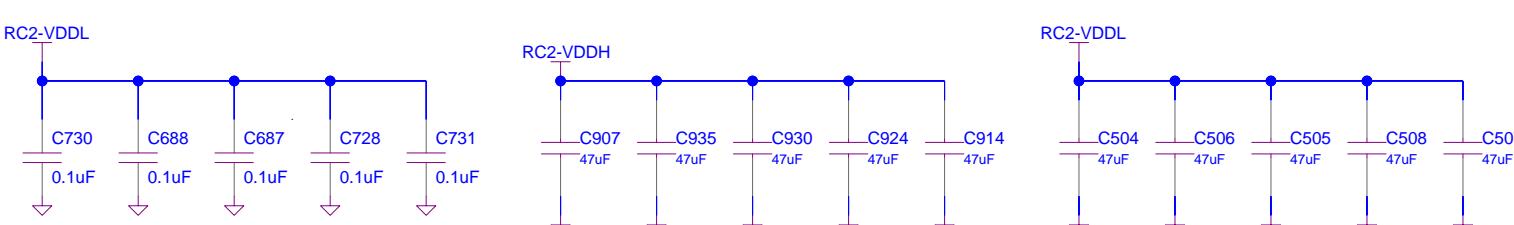
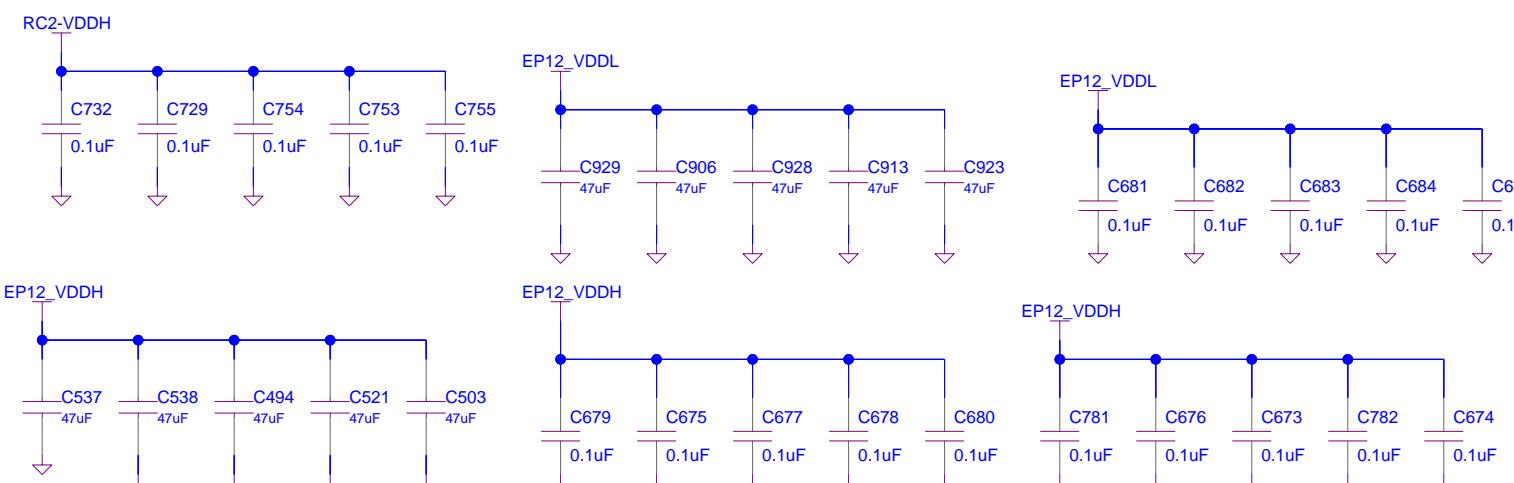
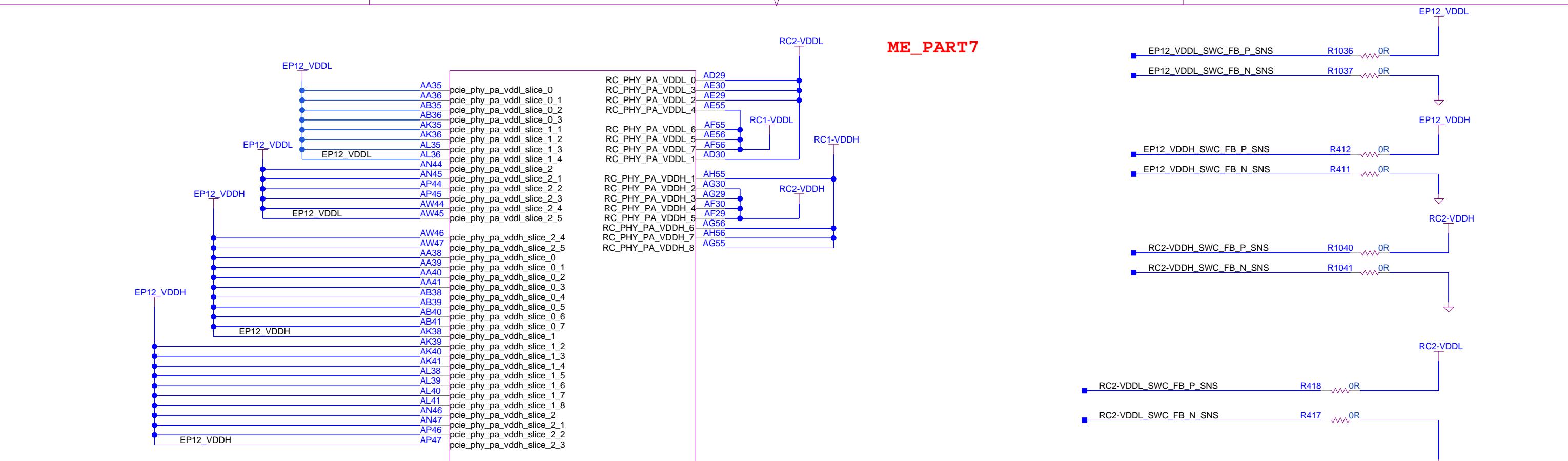
ME PART 6



4655 Old Ironsides
Dr, Santa Clara, CA 95054,
United States

ME PART6

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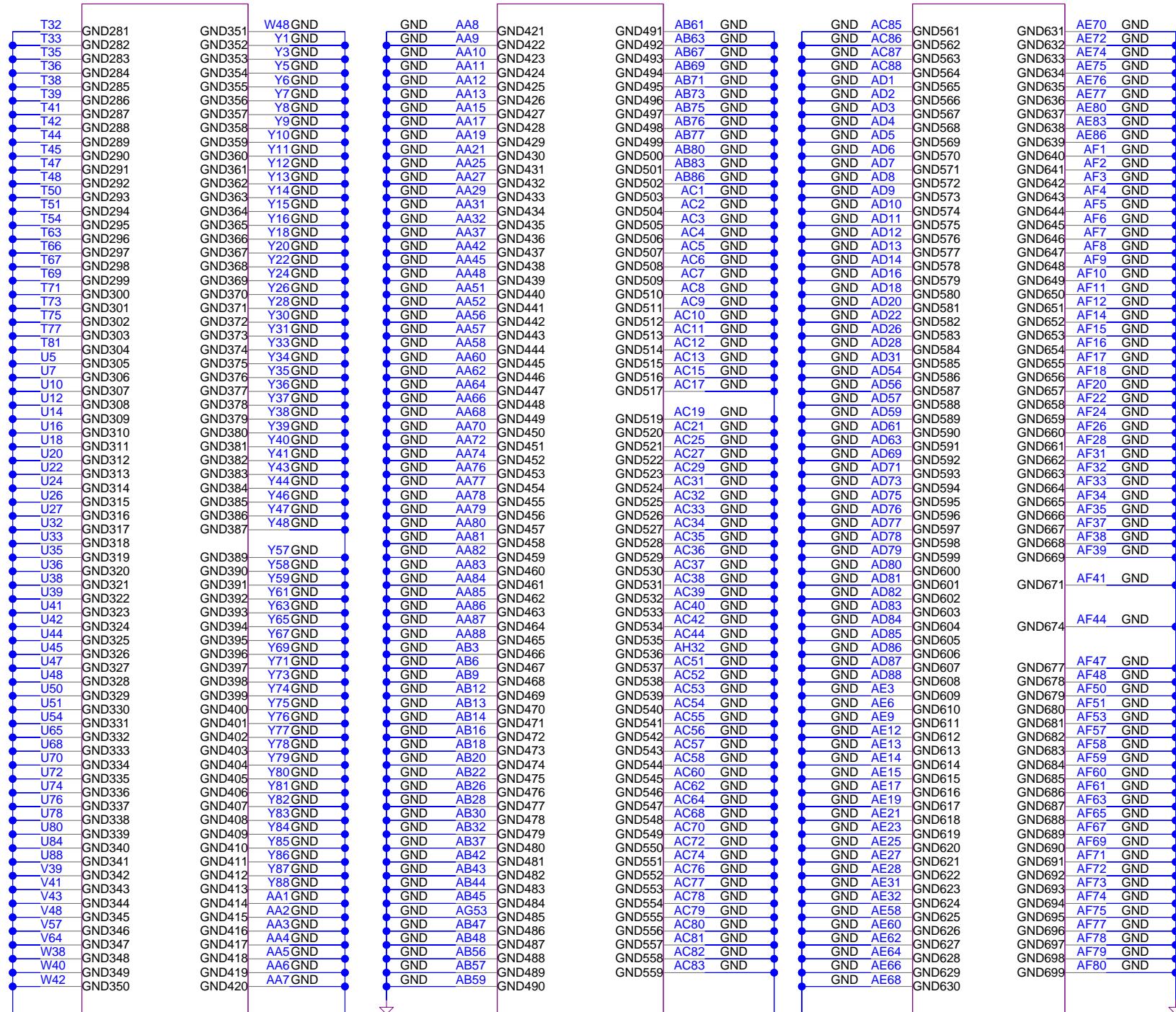


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United States

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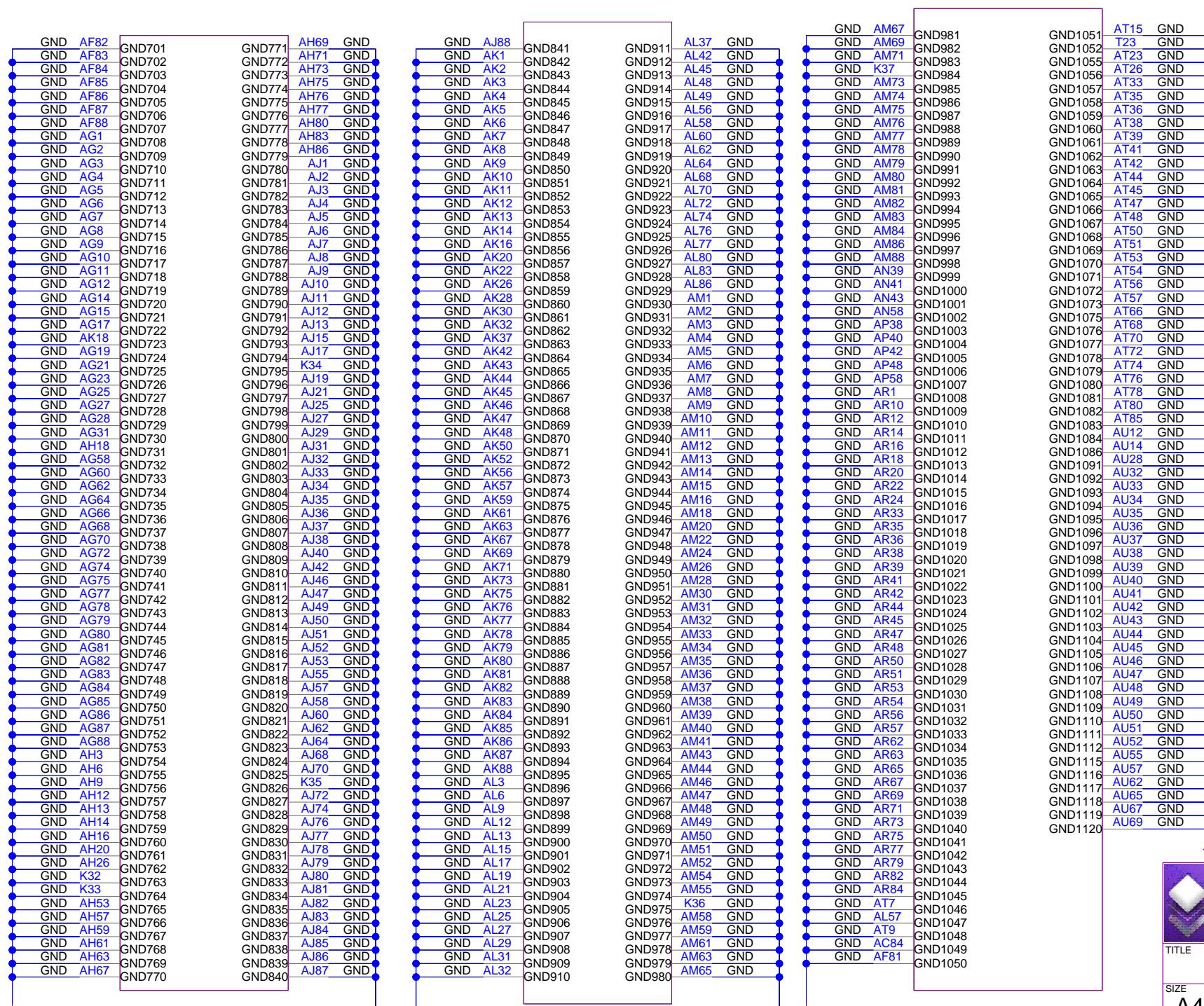
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ME_PART8



ME_PART8

ME_PART9



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United States

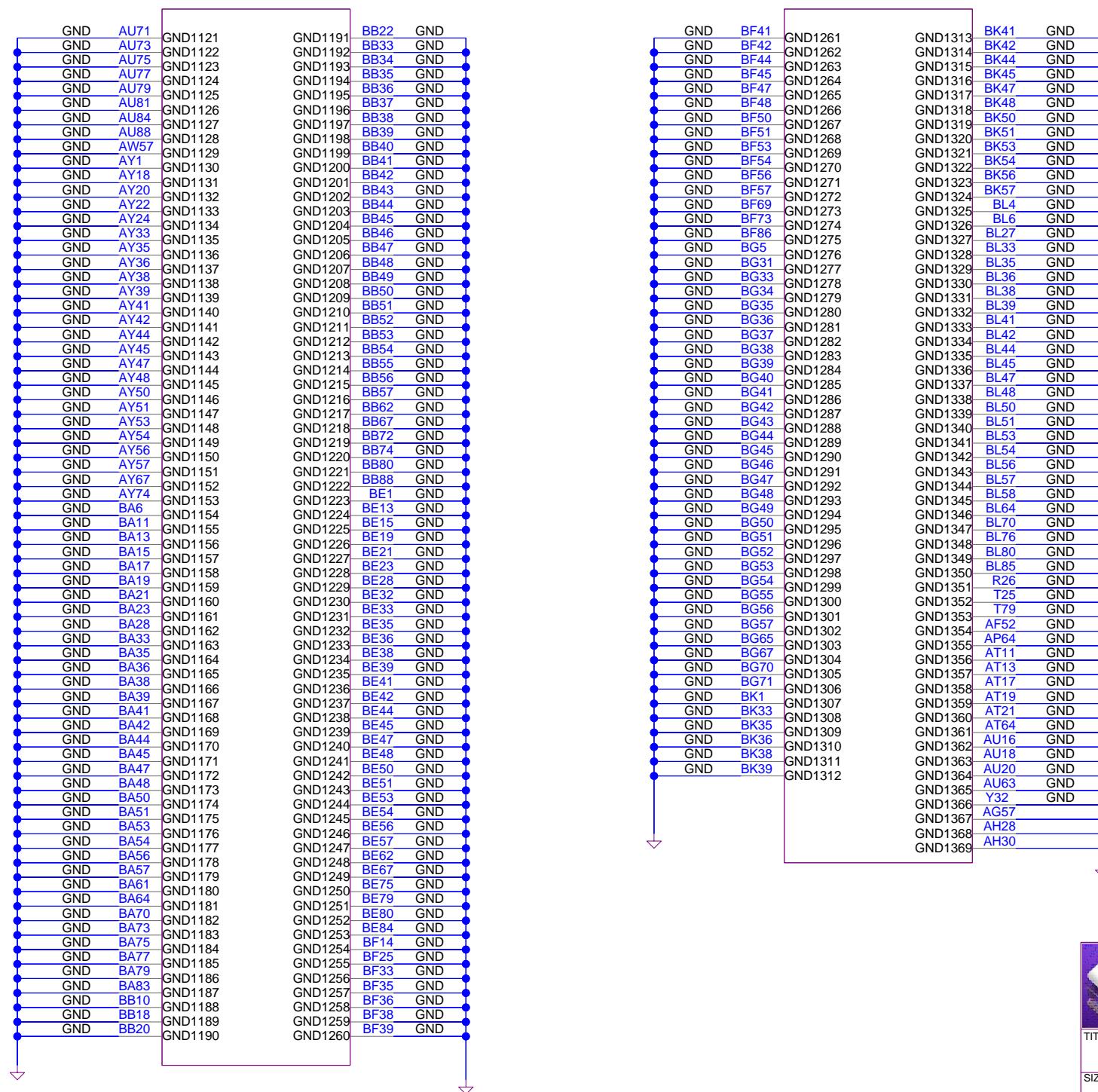
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ME_PART10



4655 Old Ironsides
Dr, Santa Clara, CA 95054,
United States

TITLE

ME_PART10

SIZE	DWG NO	Schematic1	REV
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ME_PART11

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ME_PART12

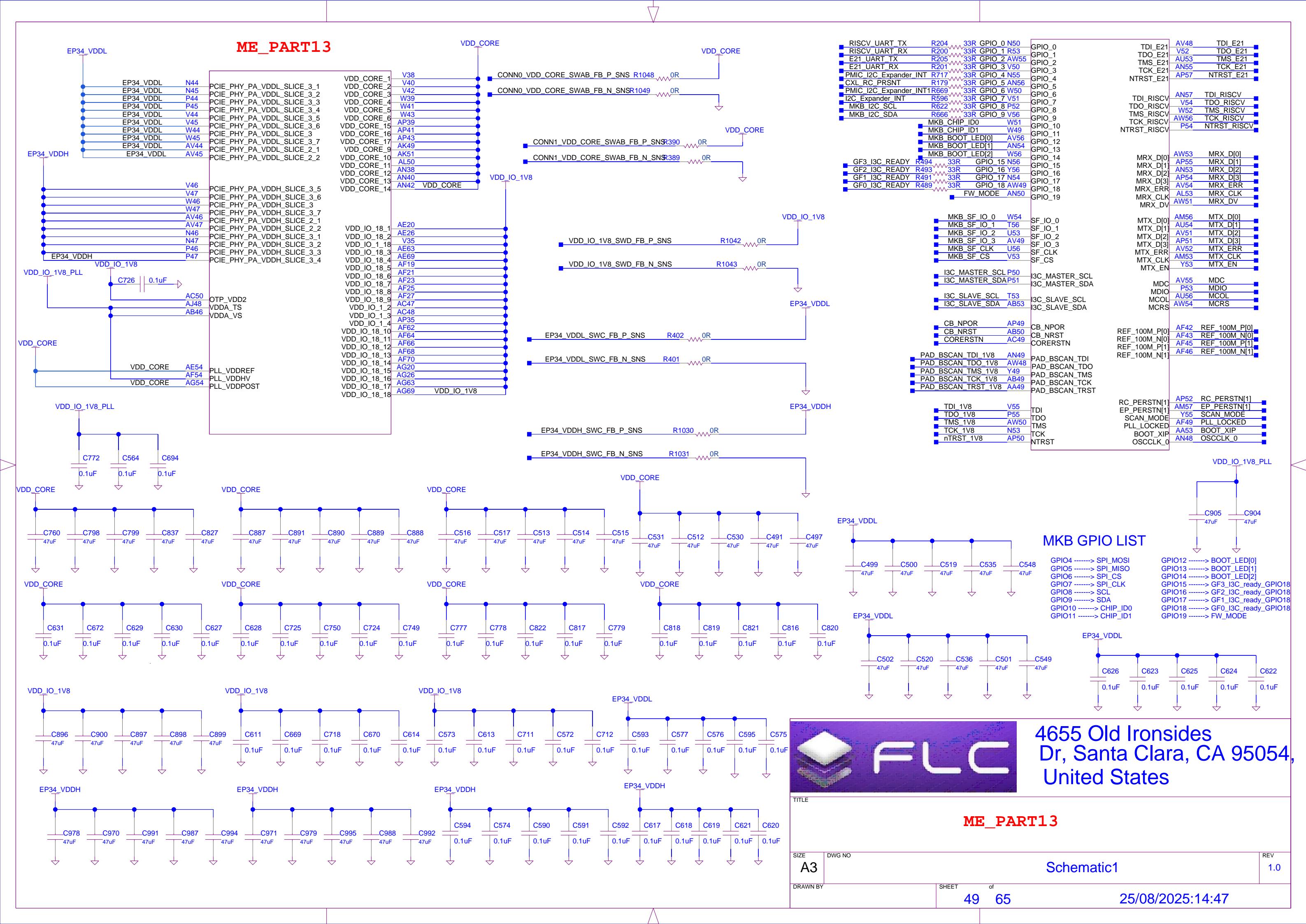
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AW83	NC985	AV10	NC926
AW84	NC986	AV11	NC927
AW85	NC987	AV12	NC928
AW86	NC988	AV13	NC929
AW87	NC989	AV14	NC930
AW88	NC989	AV15	NC931
AY11	NC991	AV16	NC932
AY12	NC992	AV17	NC933
AY13	NC993	AV18	NC934
AY14	NC994	AV19	NC935
AY15	NC995	AV20	NC936
AY16	NC996	AV21	NC937
AY17	NC997	AV22	NC938
AY18	NC998	AV23	NC939
AY19	NC999	AV24	NC940
AY20	NC1000	AV25	NC941
BA22	NC994	AV26	NC942
BA24	NC1001	AV27	NC943
BA12	NC995	AV28	NC944
BA14	NC996	AV29	NC945
BA16	NC997	AV30	NC946
BA18	NC998	AV31	NC947
BA20	NC999	AV32	NC948
BA22	NC1000	AV33	NC949
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BB31	NC1014	AV43	NC959
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BC9	NC1023	AV52	NC968
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BC18	NC1032	AV61	NC977
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BC21	NC1035	AV64	NC980
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BD21	NC1192	BE7	NC1193
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BD23	NC1194	BE9	NC1195
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BD26	NC1197	BE12	NC1198
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BD47	NC1218	BE33	NC1219
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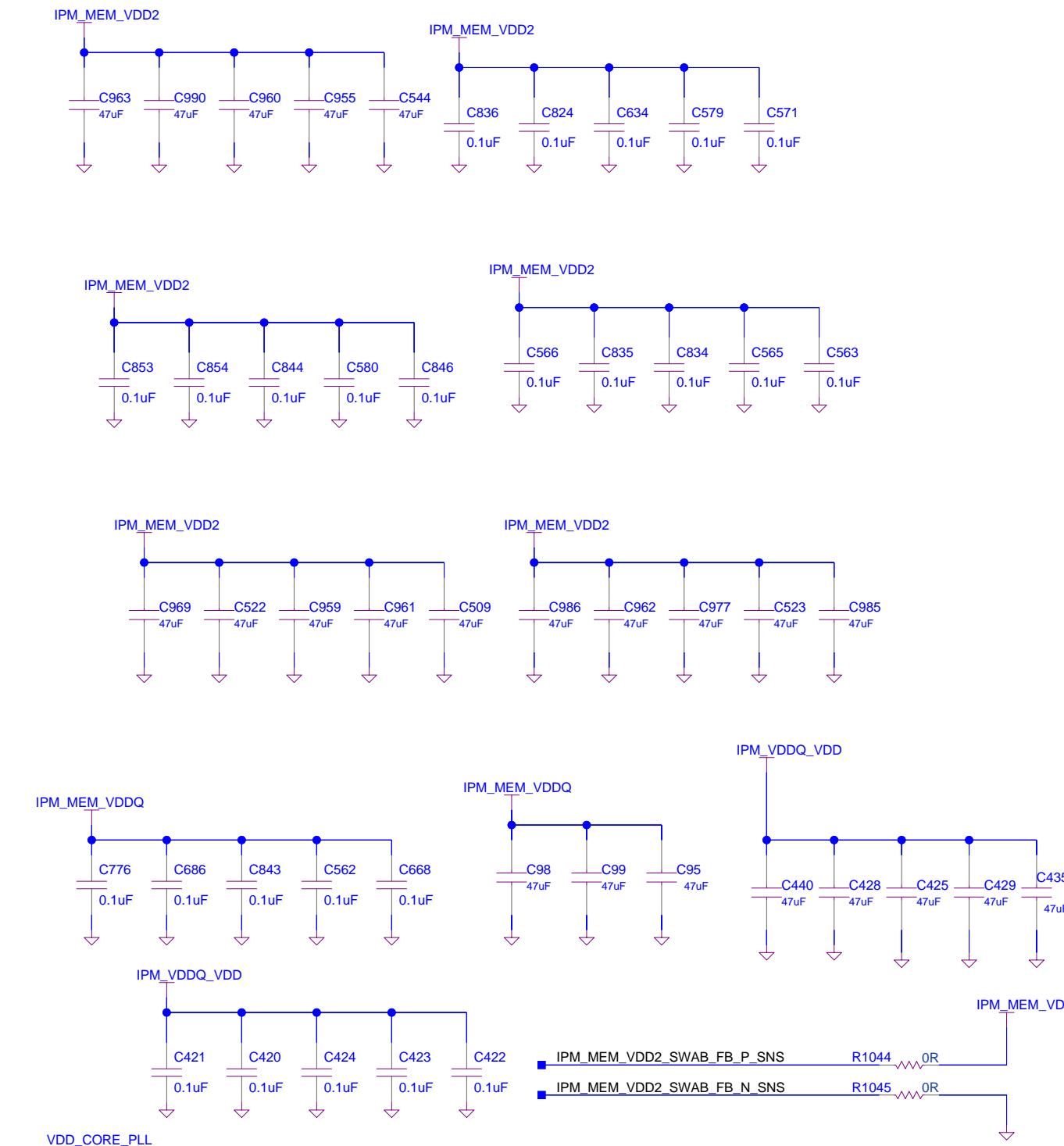
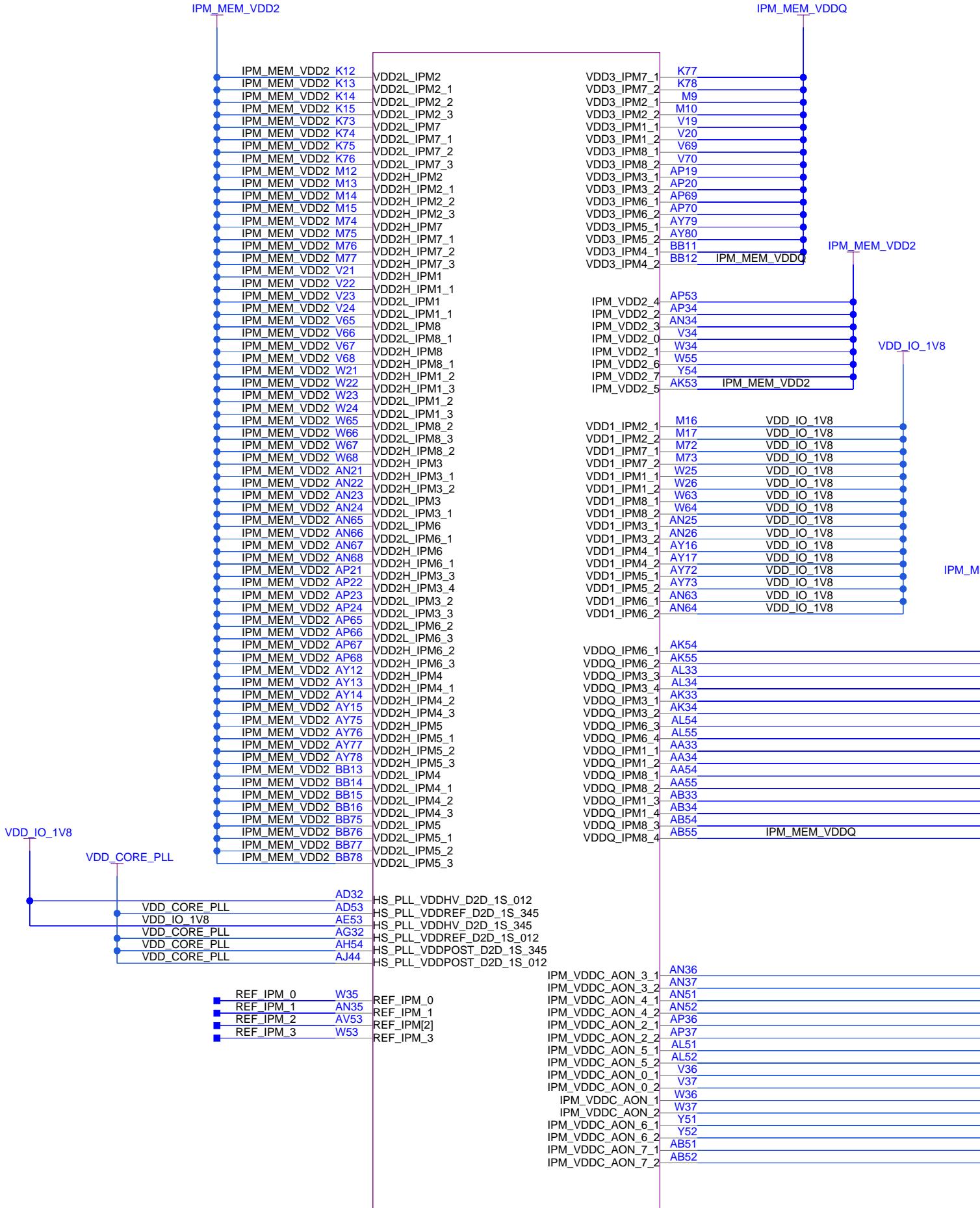
4655 Old Ironsides
Dr, Santa Clara, CA 95054,
United States

ME_PART12

SIZE	DWG NO	TITLE		REV
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DRAWN BY				



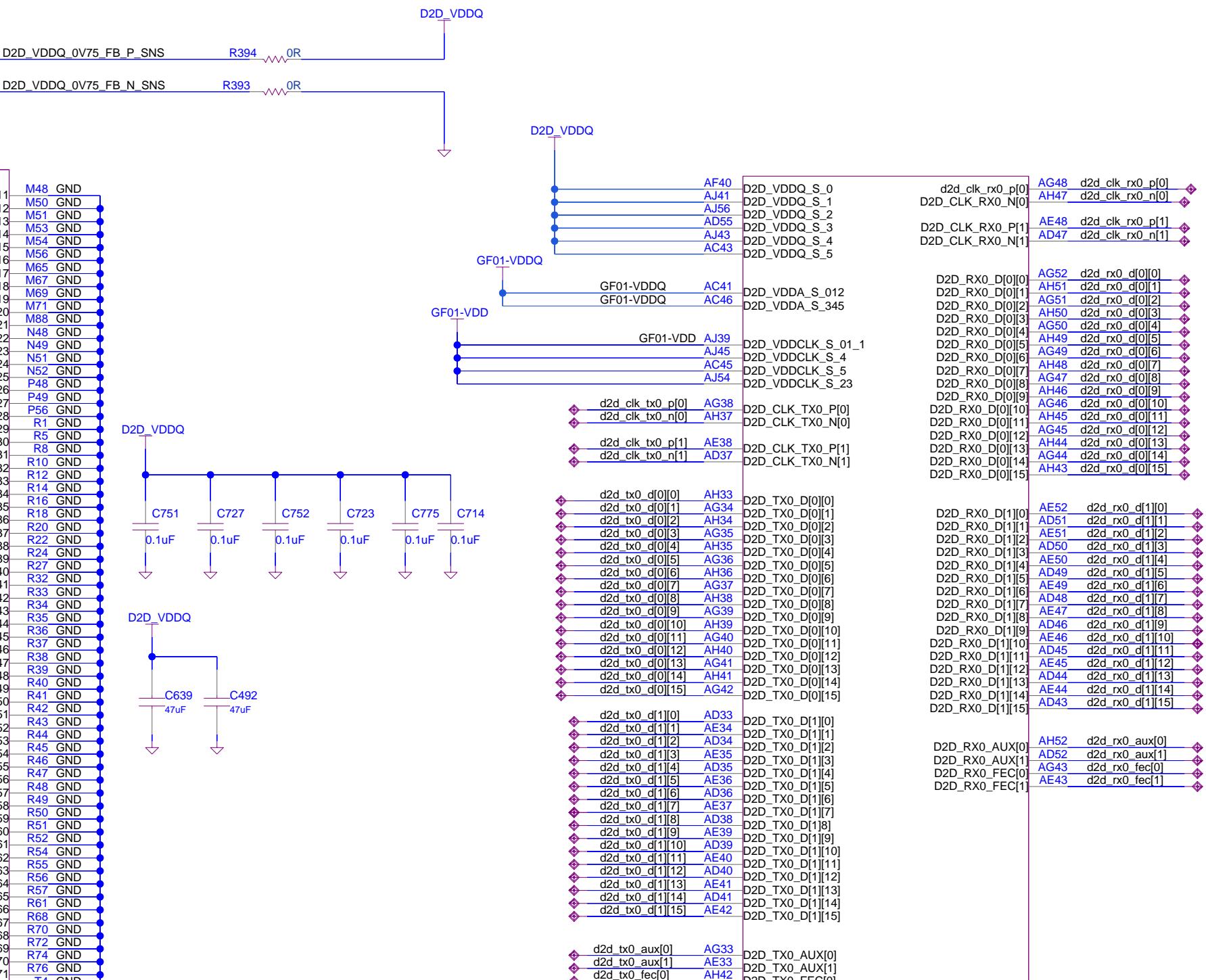
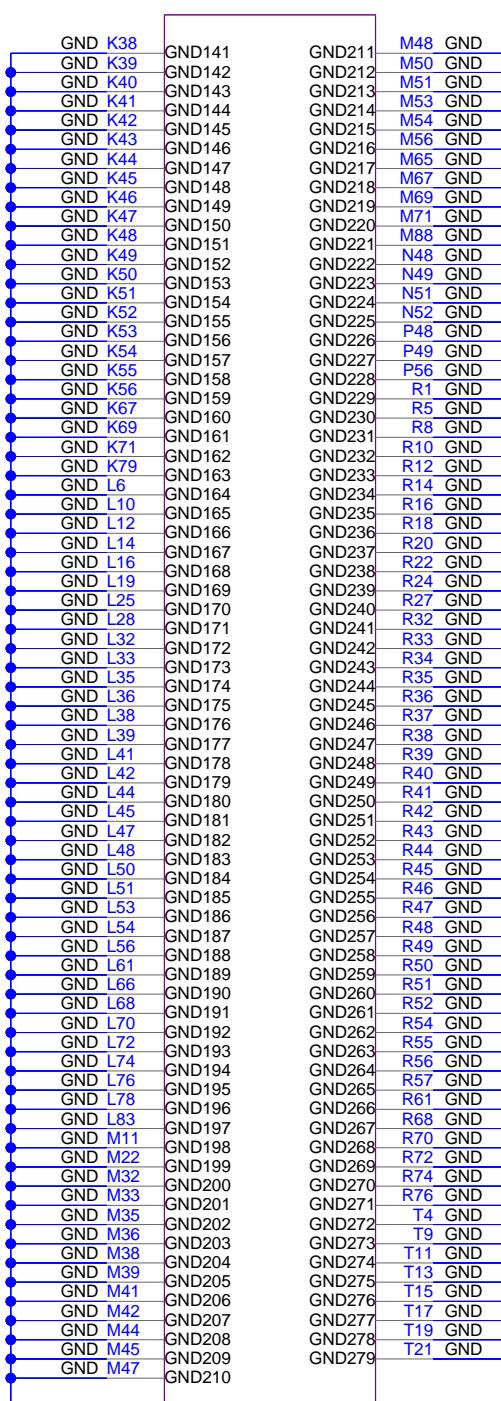
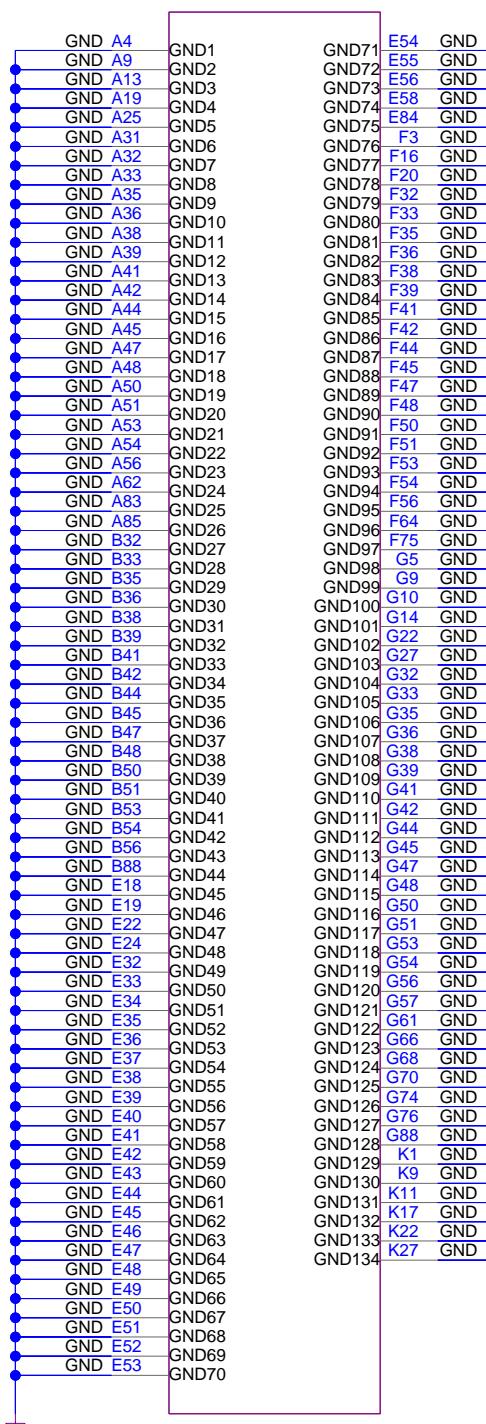
ME_PART14



ME_PART14

SIZE	DWG NO	REV
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	Schematic1	
DRAWN BY	50	65
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ME_PART15



TITLE

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ME_PART15

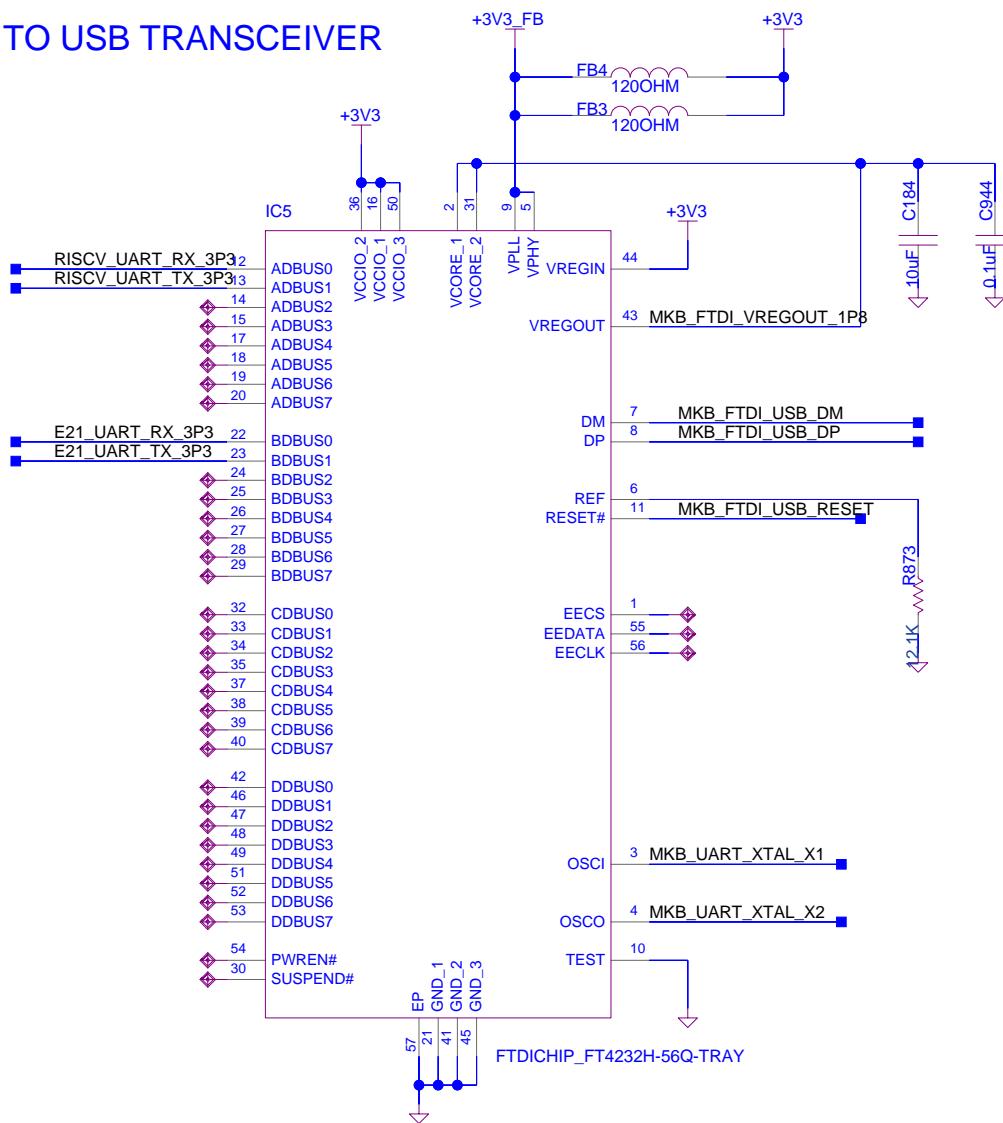
SHEET	of	
DRAWN BY		
51	65	12/08/2025:15:03

Schematic1

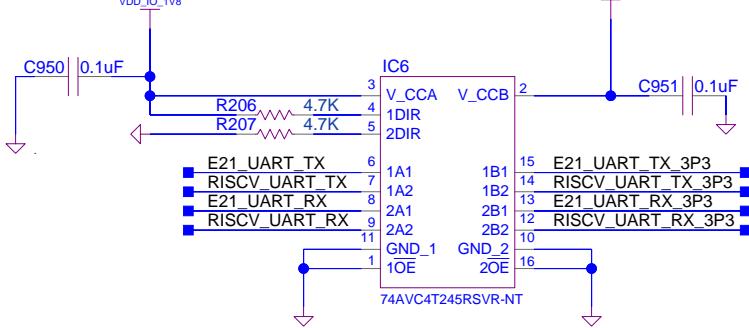
REV
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MKB USB UART CONN

UART TO USB TRANSCEIVER

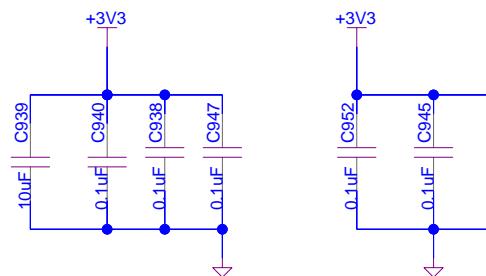


1V8 to 3V3 Voltage Translator

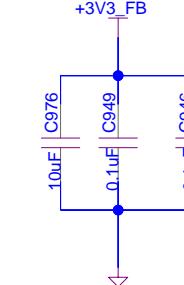


IF DIR IS LOW THEN A PORT IS ENABLED AND THE OPERATION IS FROM B TO A
IF DIR IS HIGH THEN B PORT IS ENABLED AND THE OPERATION IS FROM A TO B

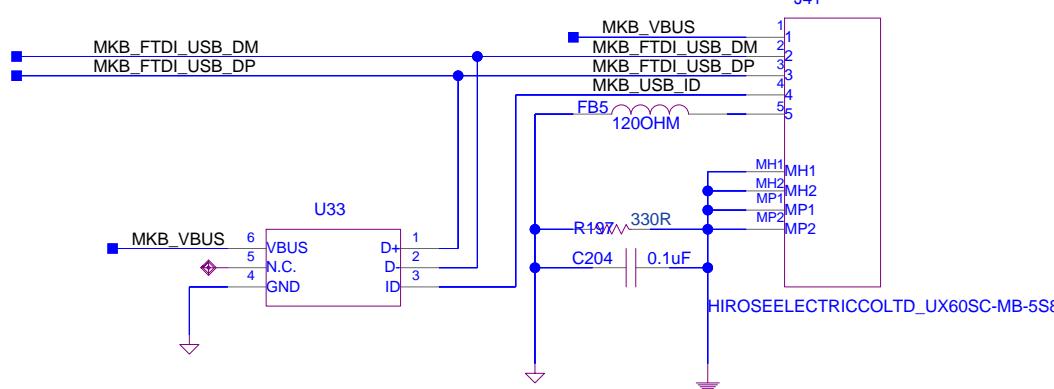
For REGIN



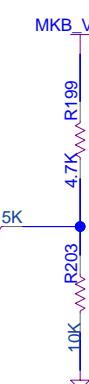
For VPLL,VPHY



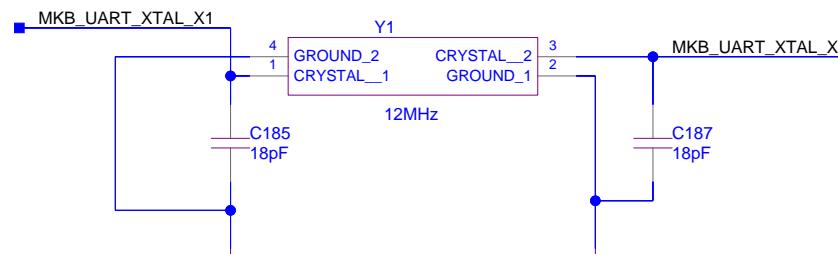
Micro USB_Conn



USB RESET

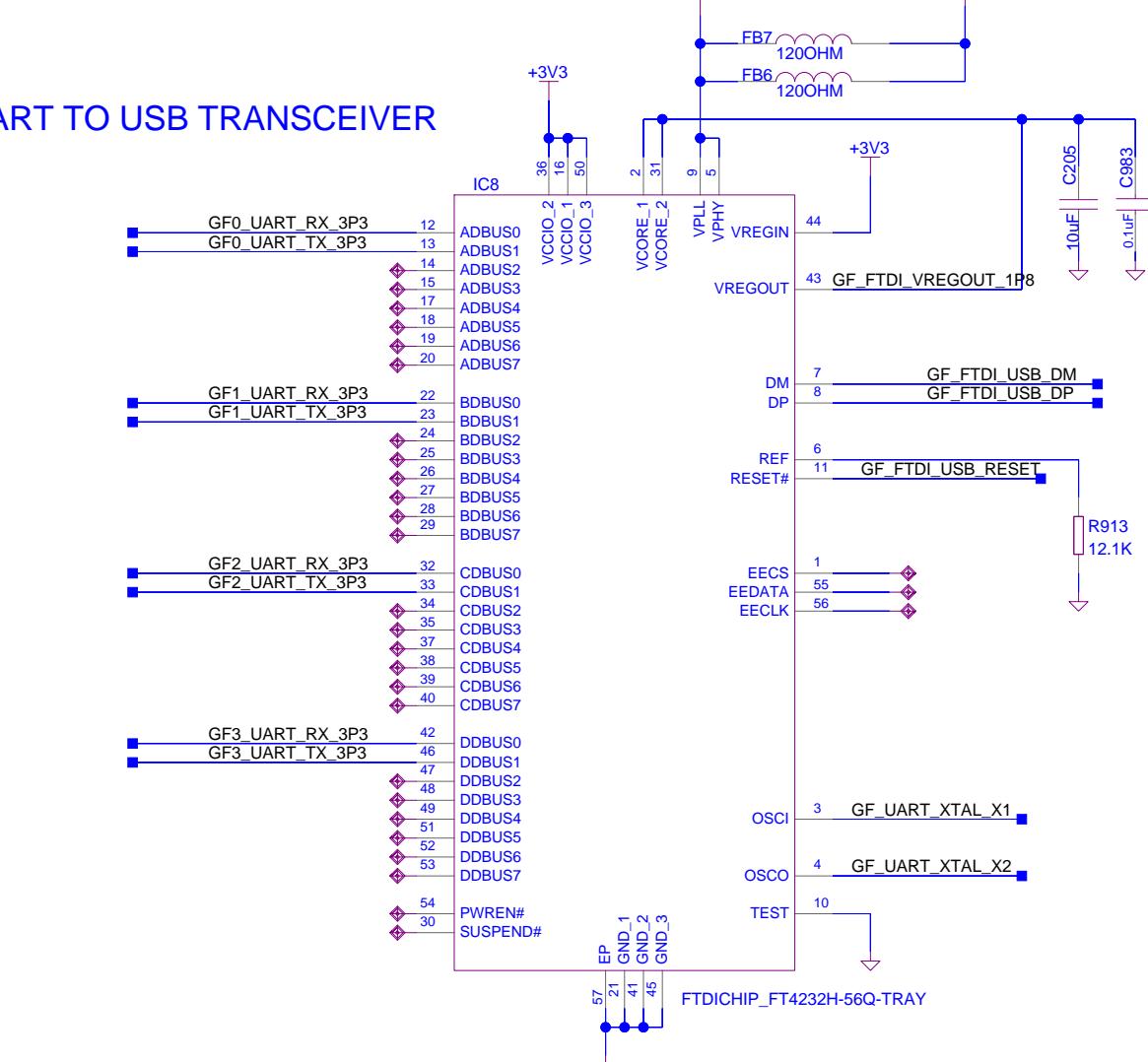


Timing Circuit



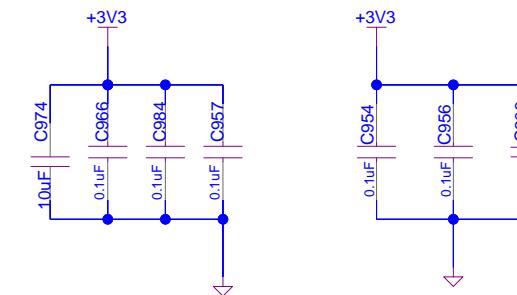
4655 Old Ironsides
Dr, Santa Clara, CA 95054,
United States

UART TO USB TRANSCEIVER

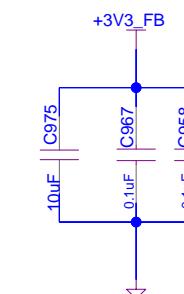


GF_UART_USB_CONN

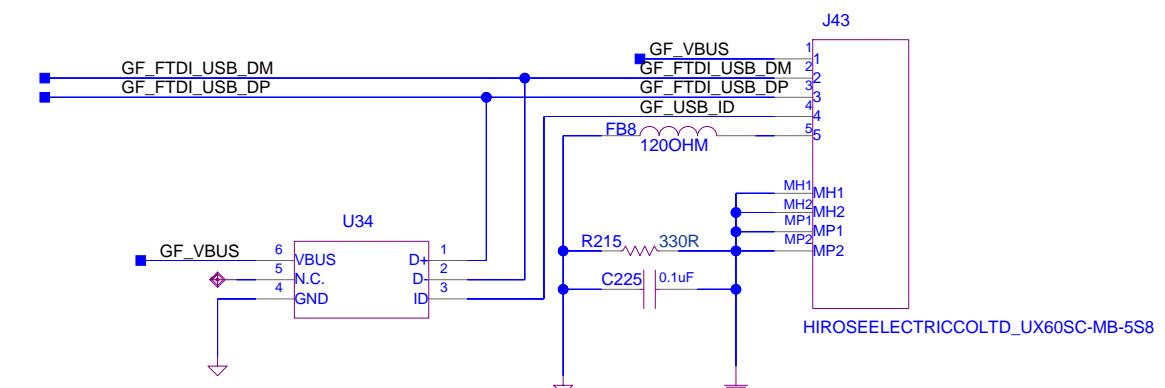
For REGIN



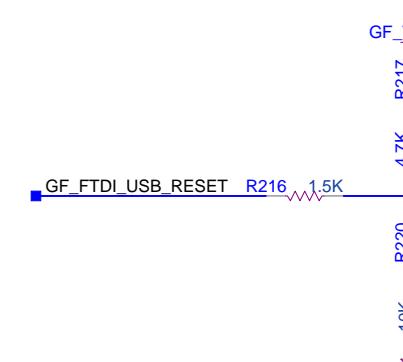
For VPLL,VPHY



Micro USB_Conn



USB_RESET



Timing Cirucit



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GF_UART_USB_CONN

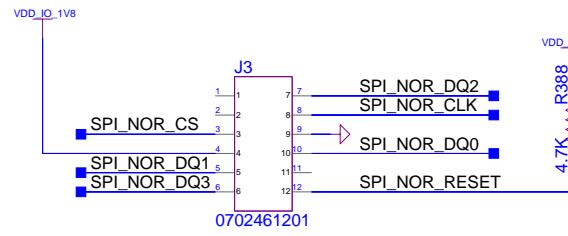
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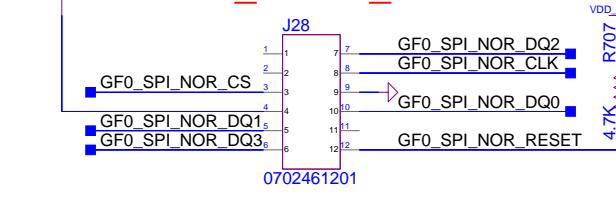
IF DIR IS LOW THEN A PORT IS ENABLED AND THE OPERATION IS FROM B TO A
IF DIR IS HIGH THEN B PORT IS ENABLED AND THE OPERATION IS FROM A TO B

Schematic1

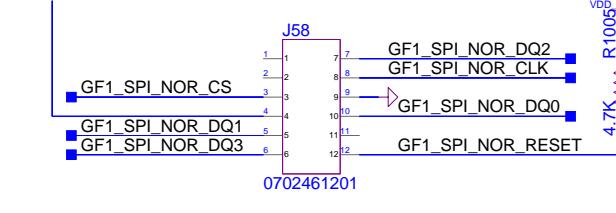
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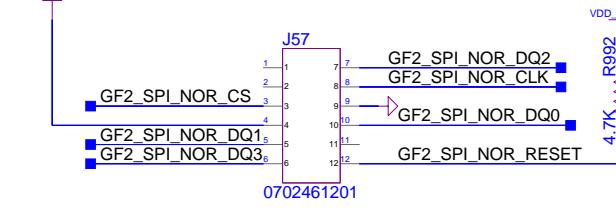
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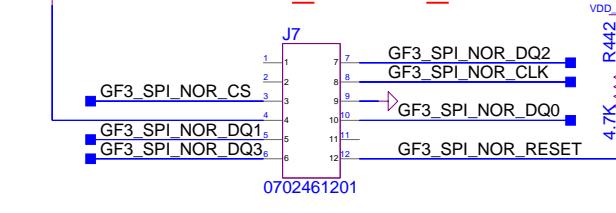
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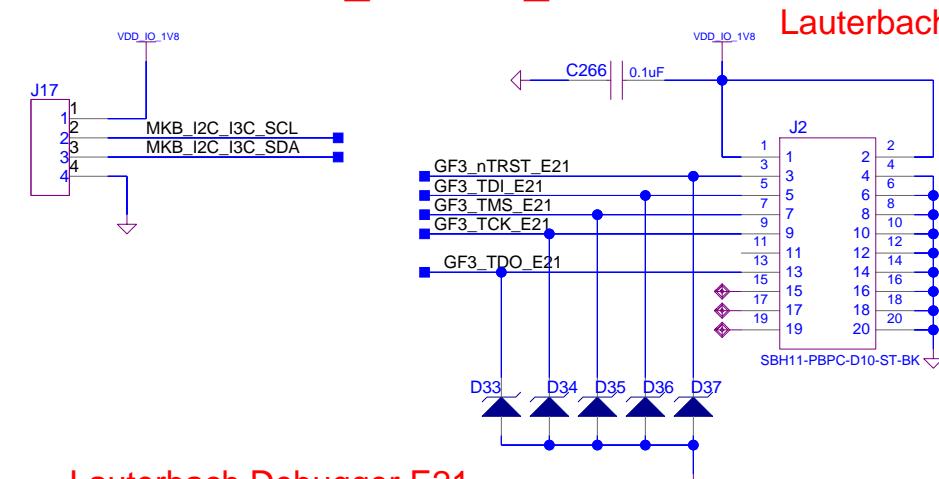
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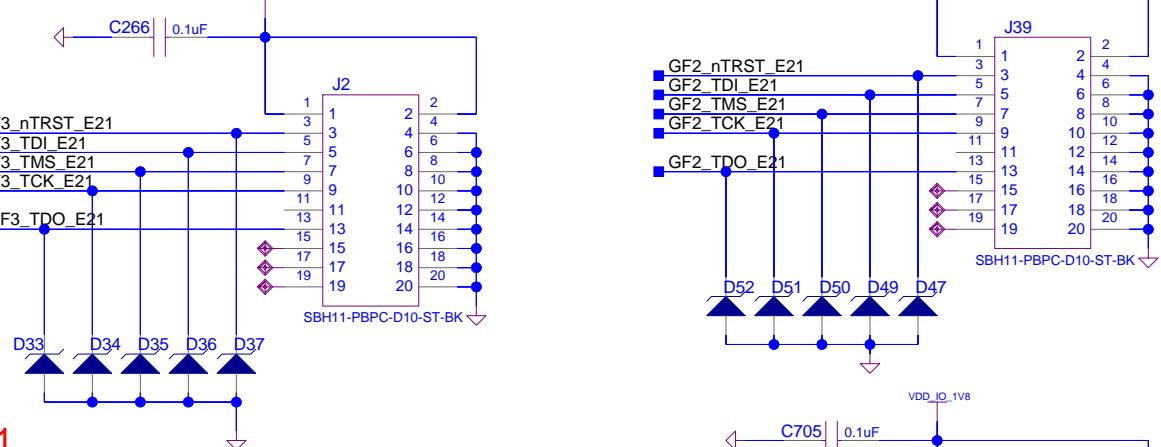
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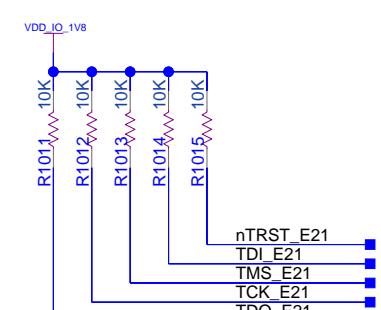
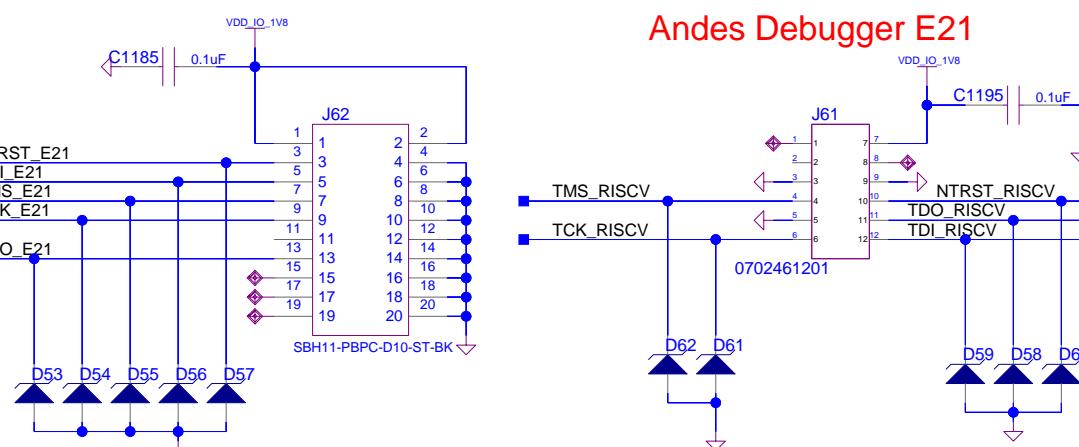
JTAG_HEADER_CONN



Lauterbach Debugger E21



Andes Debugger E21

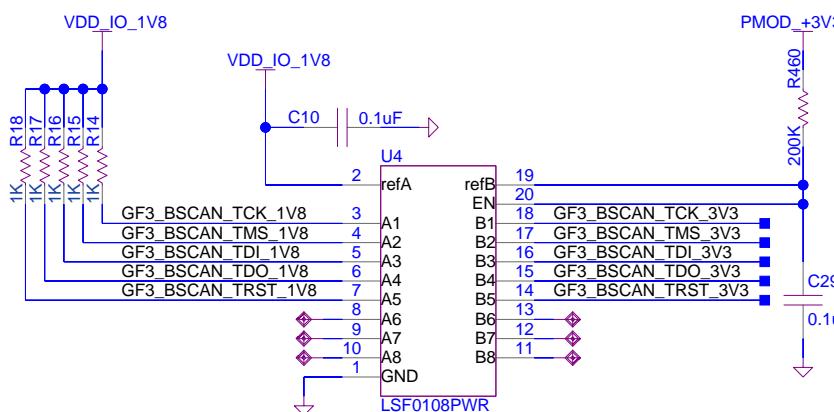
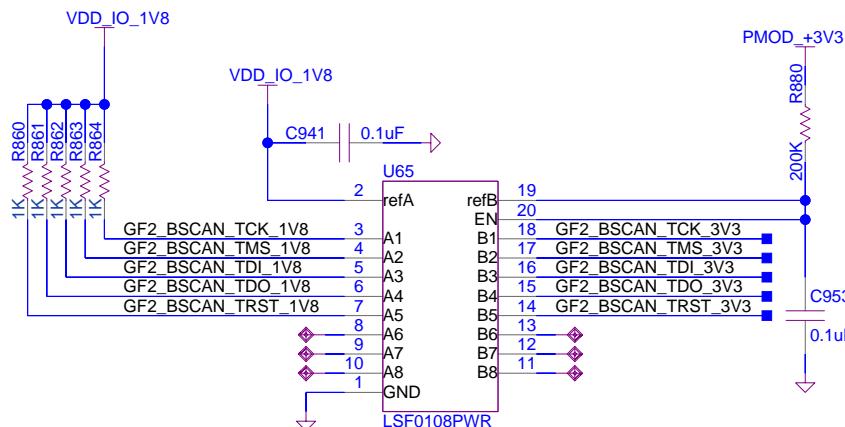
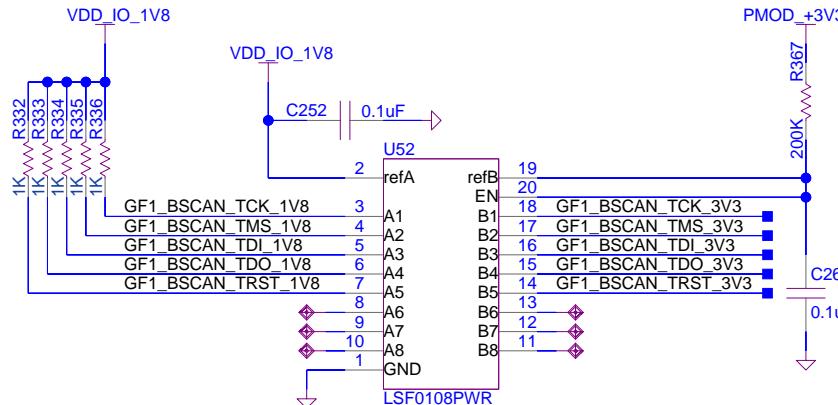
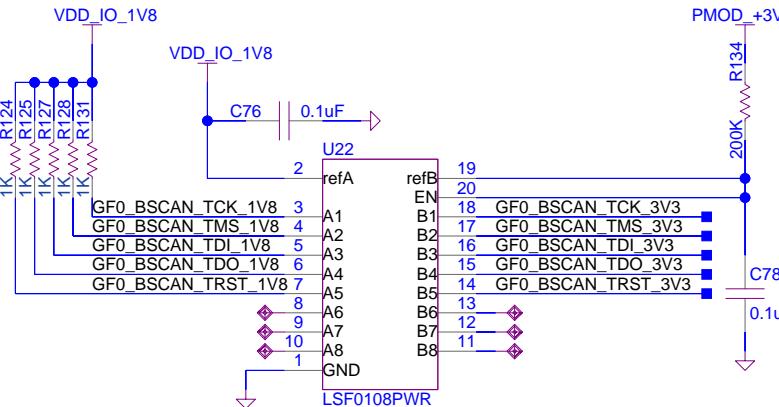


JTAG_HEADER_CONN

A3 Schematic1
54 65
25/08/2025:15:40

4655 Old Ironsides
Dr, Santa Clara, CA 95054,
United States

LEVEL_GF_BSCAN_JTAG



4655 Old Ironsides
Dr, Santa Clara, CA 95054,
United States

TITLE

LEVEL_GF_BSCAN_JTAG

SIZE

A4

DWG NO

Schematic1

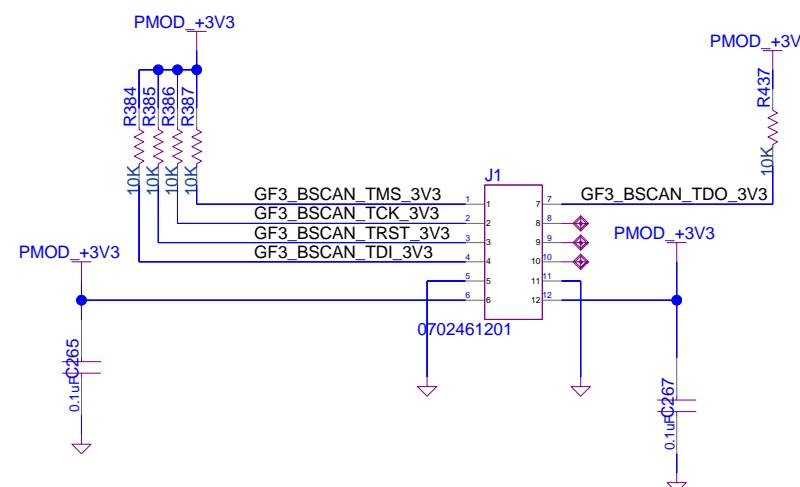
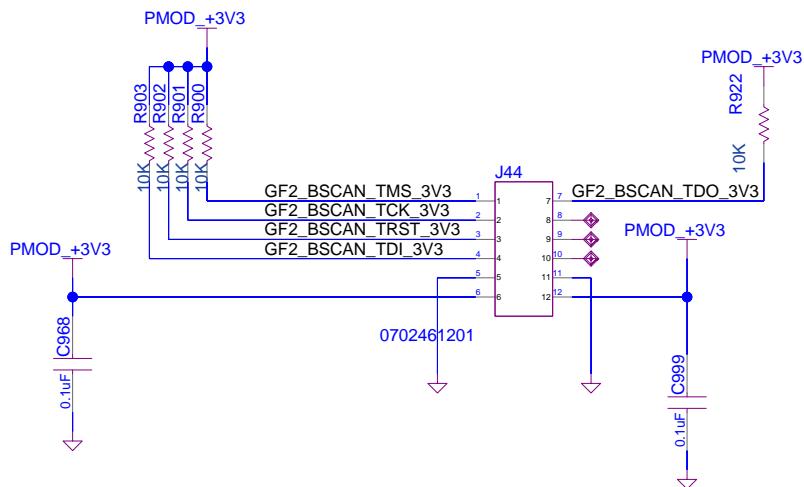
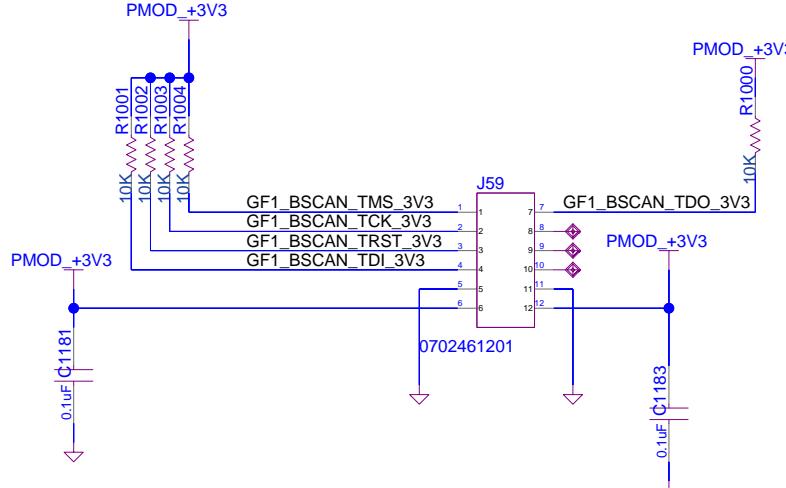
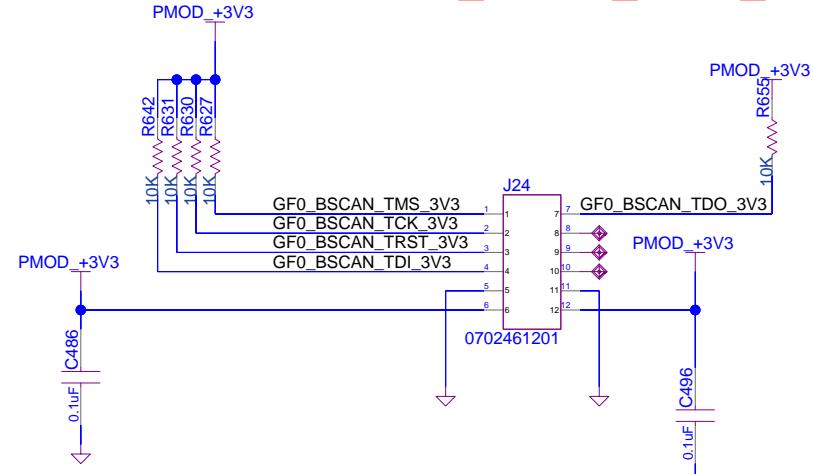
REV

SHEET

of 5565

25/08/2025:16:54

GF_BSCAN_JTAG_HDR



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TITLE

GF_BSCAN_JTAG_HDR

SIZE

A4

DWG NO

Schematic1

REV

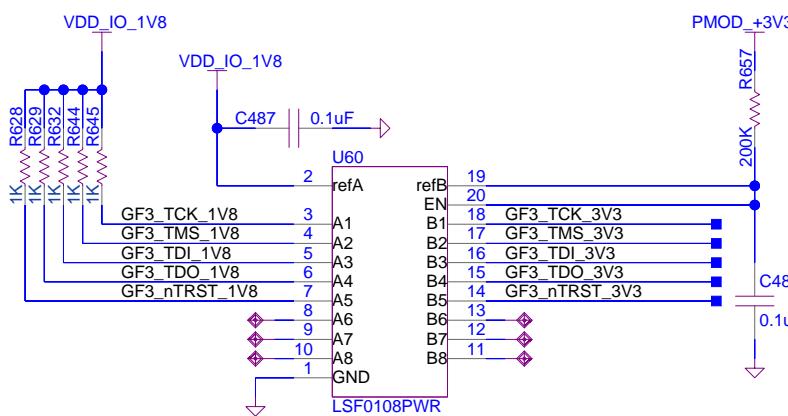
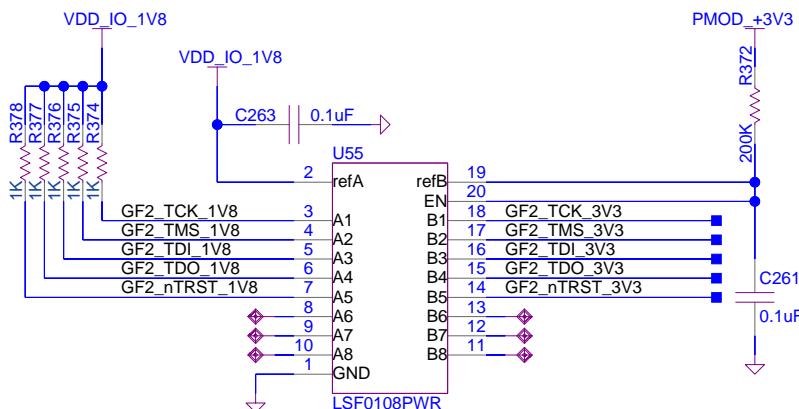
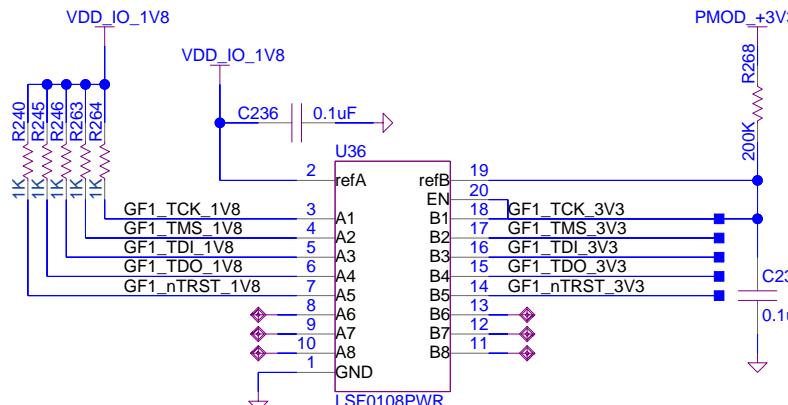
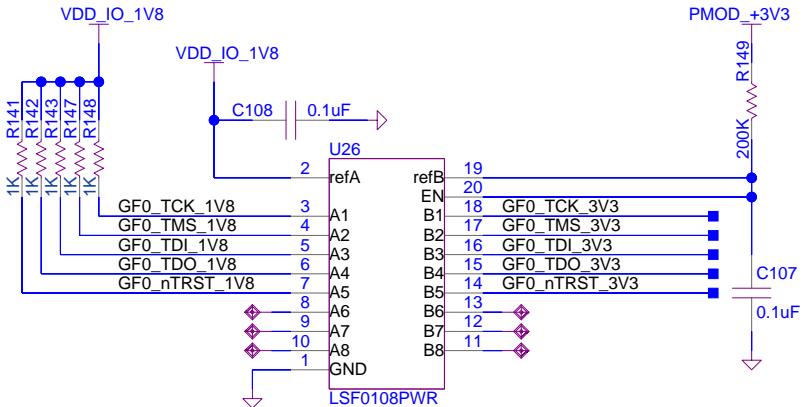
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of

565

25/08/2025 15:40

LEVEL_TRANS_GF_JTAG

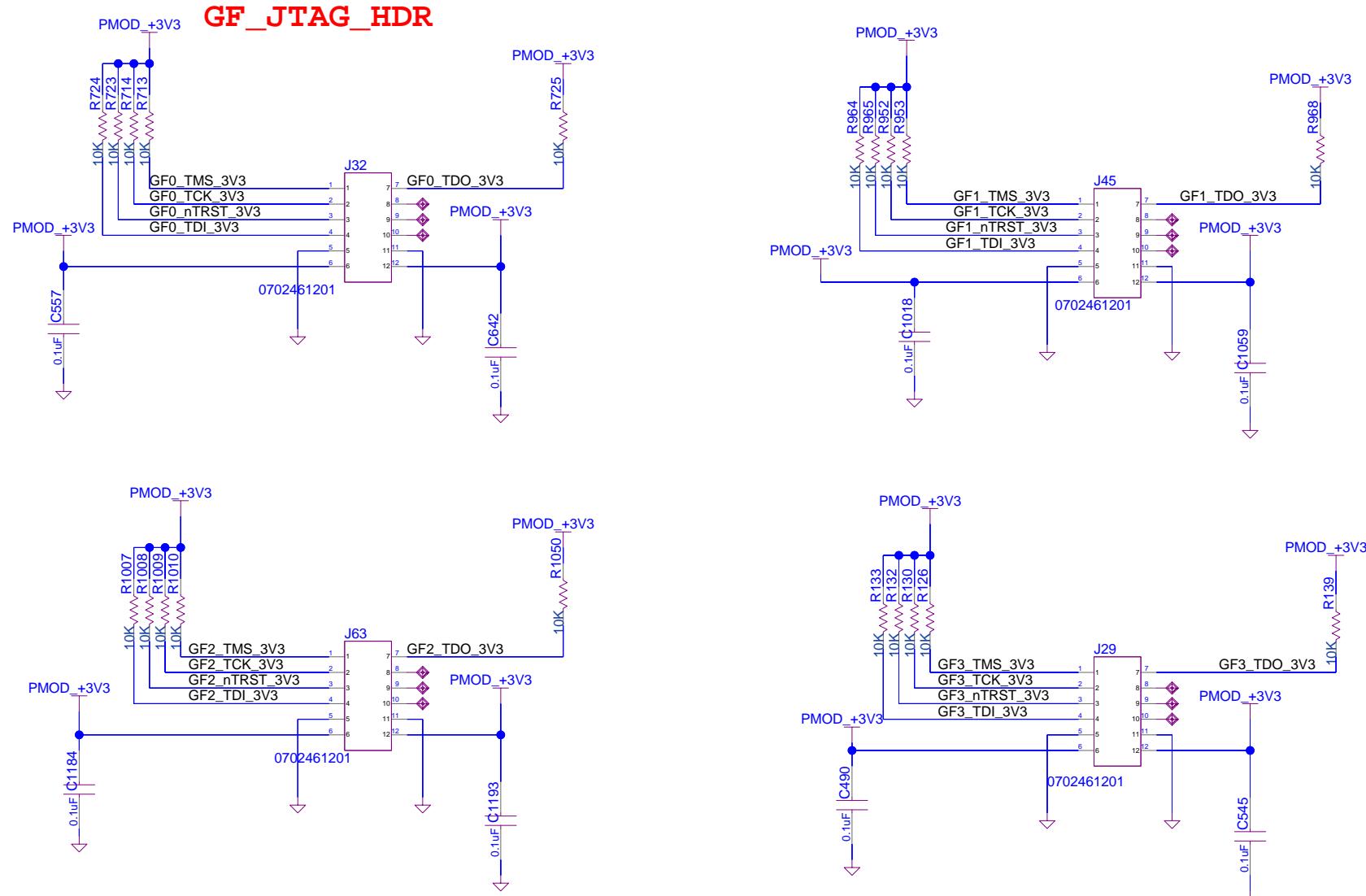


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United States

TITLE
LEVEL_TRANS_GF_JTAG

SIZE DWG NO REV
A4 Schematic1

SHEET of 5765 25/08/2025:16:54

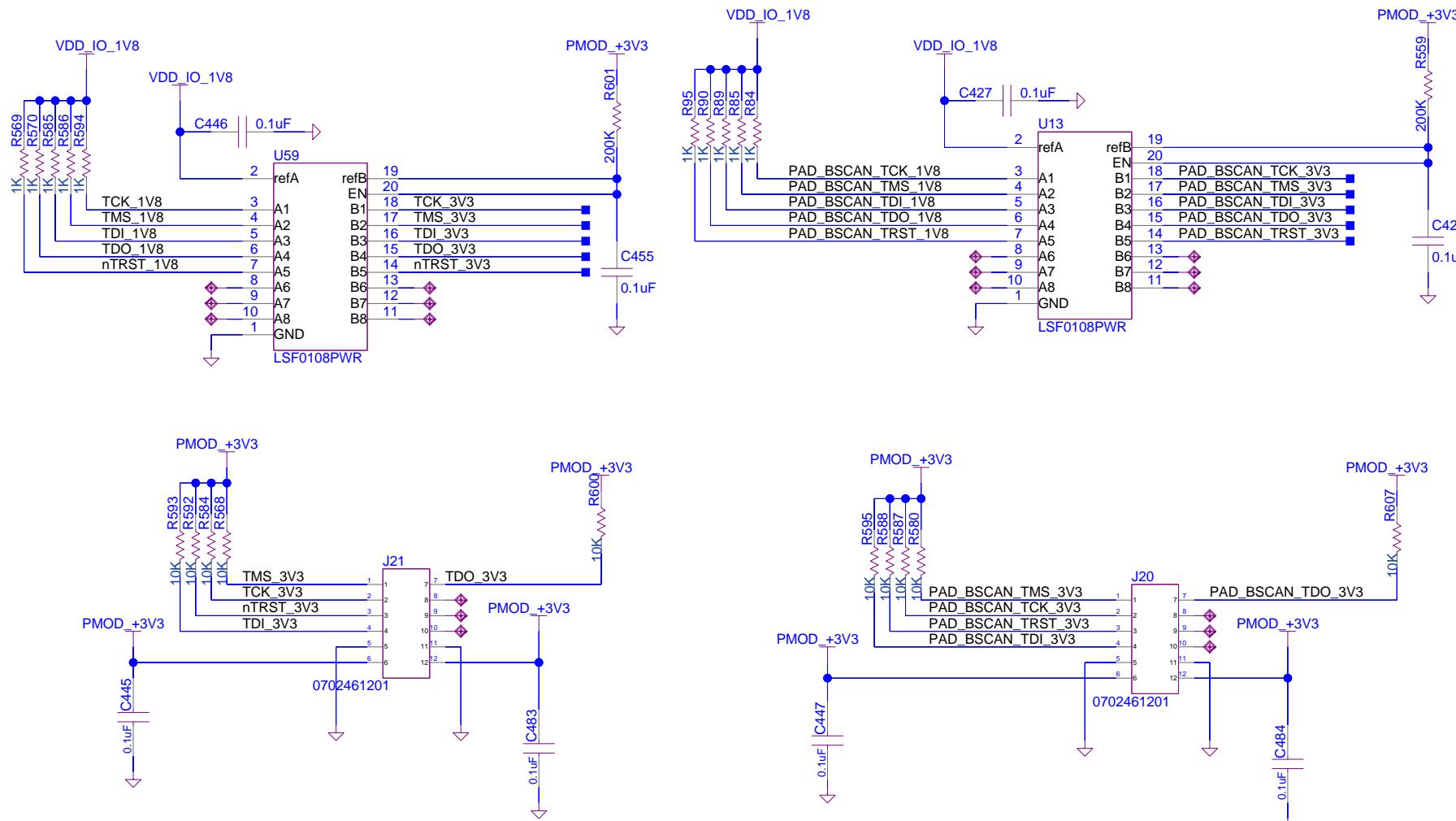


4655 Old Ironsides
Dr, Santa Clara, CA 95054,
United States

TITLE		
SIZE	DWG NO	REV
A4	Schematic1	
	SHEET of 58 65	25/08/2025 15:40

GF_JTAG_HDR

MKB_JTAG_HDR



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Dr, Santa Clara, CA 95054,
United States

T

MKB JTAG HDR

SI

DWG NO

1

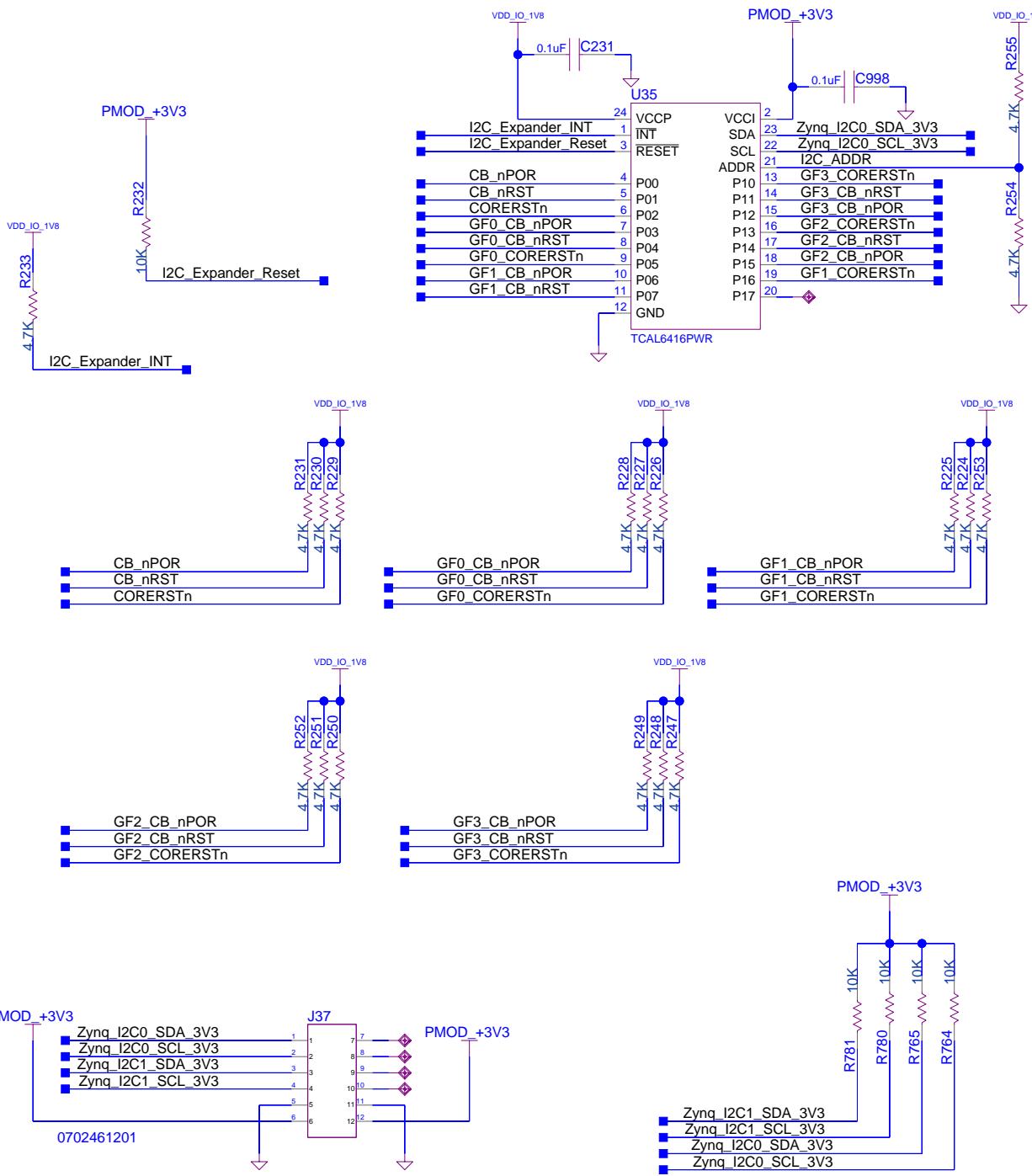
CHIEF

1

SHEE

Page 1

RESET_GF_AND_MKB



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Dr, Santa Clara, CA 95054,
United States

TITLE

RESET_GF_AND_MKB

SIZE

A4

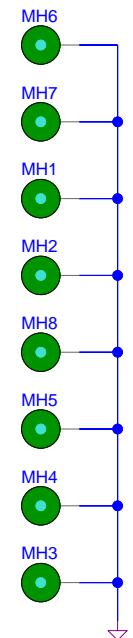
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Schematic1

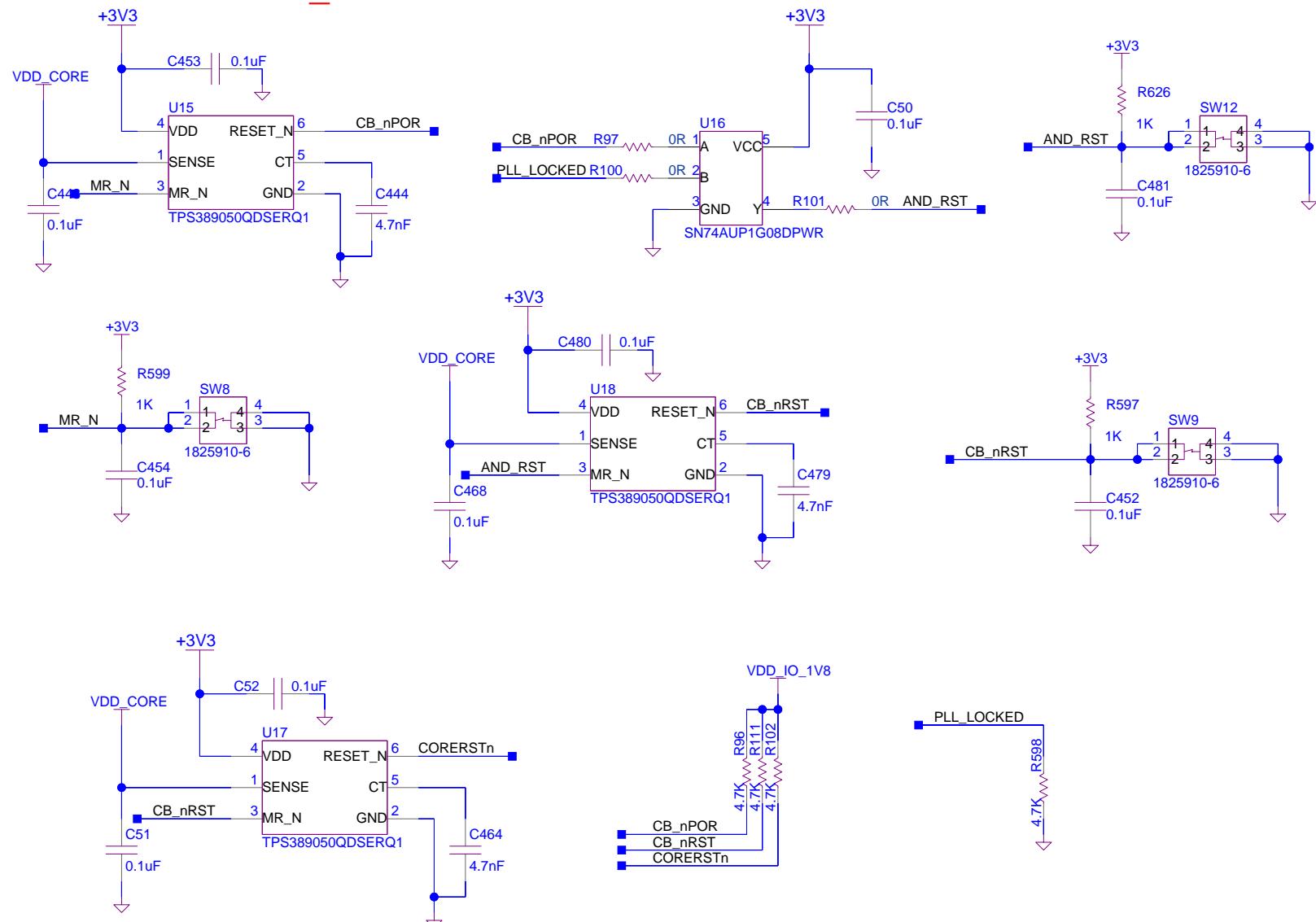
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SHEET of 6065 25/08/2025 15:40

MOUNTING HOLES



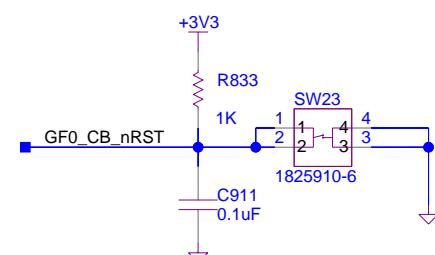
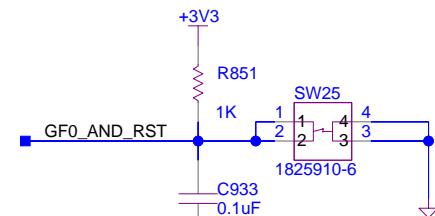
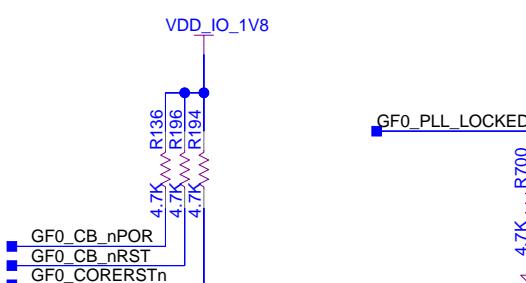
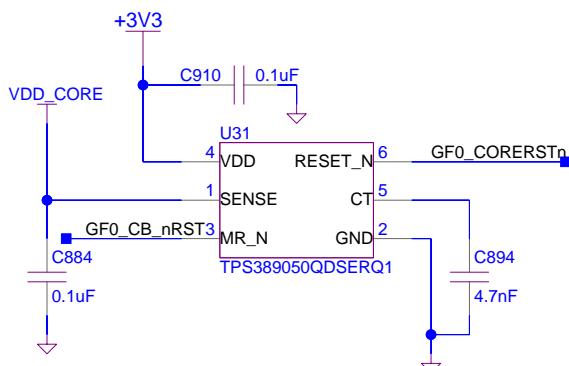
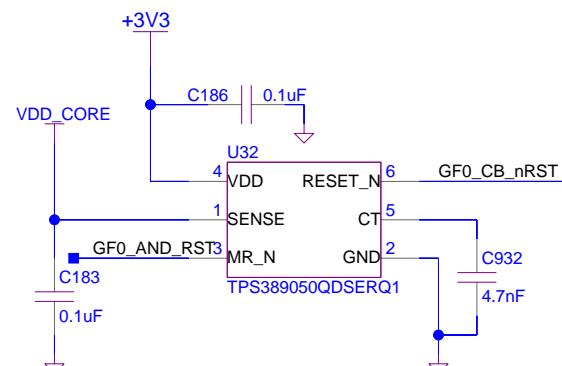
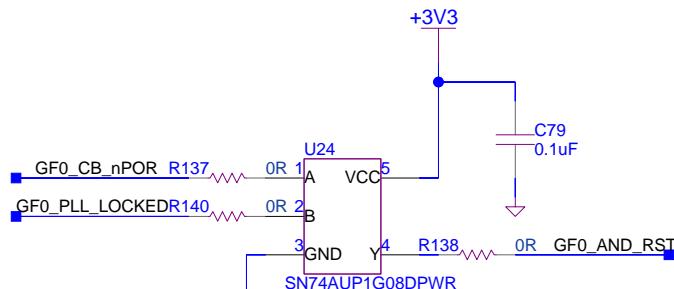
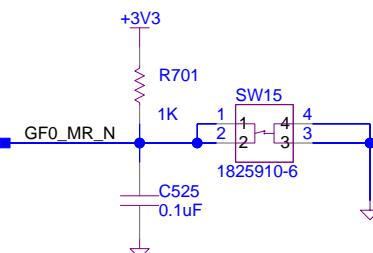
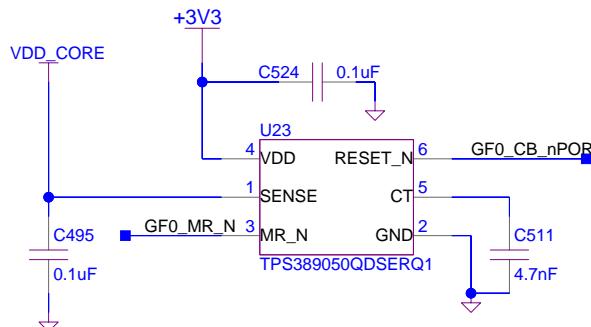
MKB_RESET



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United States

TITLE	Schematic1	REV
A4	MKB_RESET	
	SHEET of 6165	25/08/2025:15:19

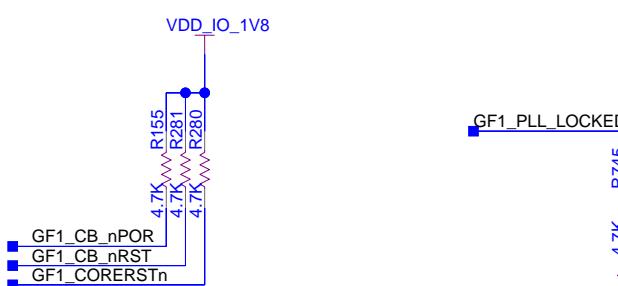
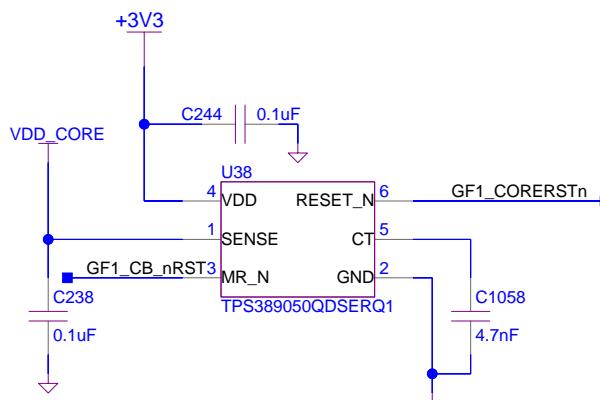
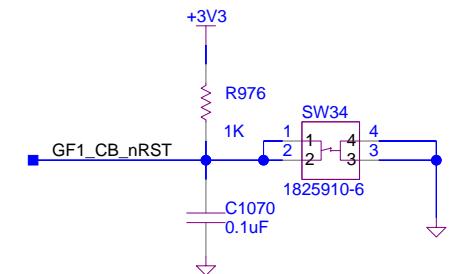
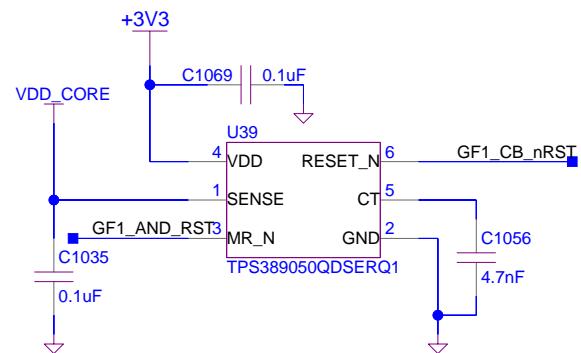
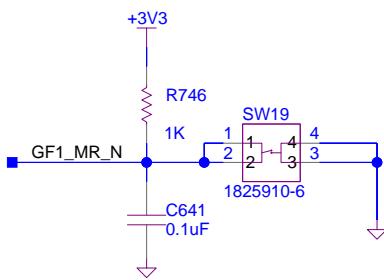
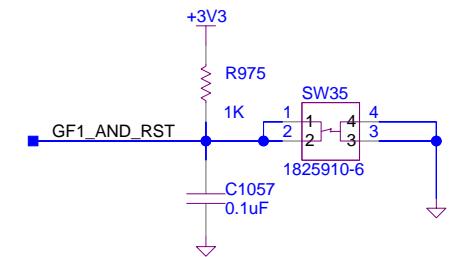
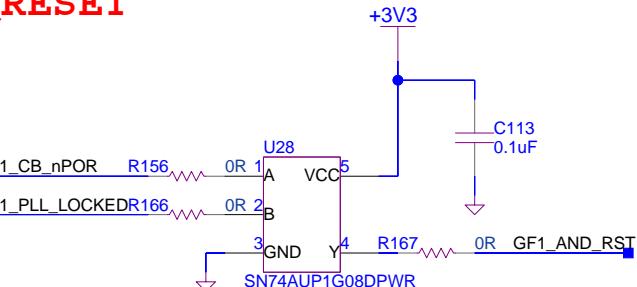
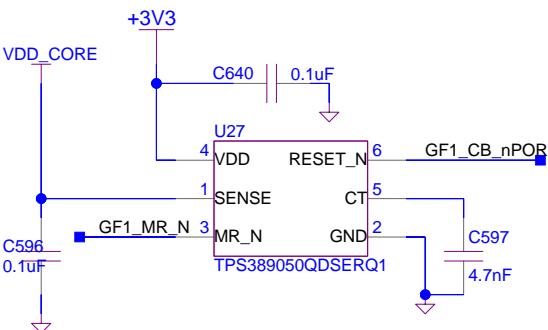
GF0_RESET



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United States

TITLE		
Schematic1		
SIZE	DWG NO	REV
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	SHEET of 6265	25/08/2025:15:19

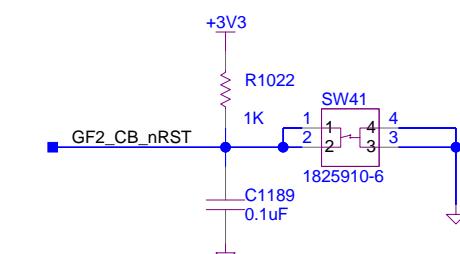
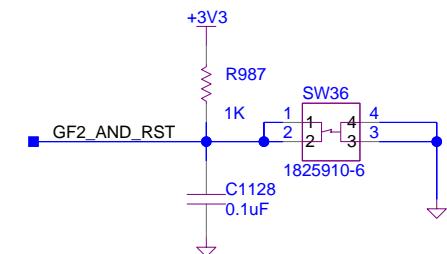
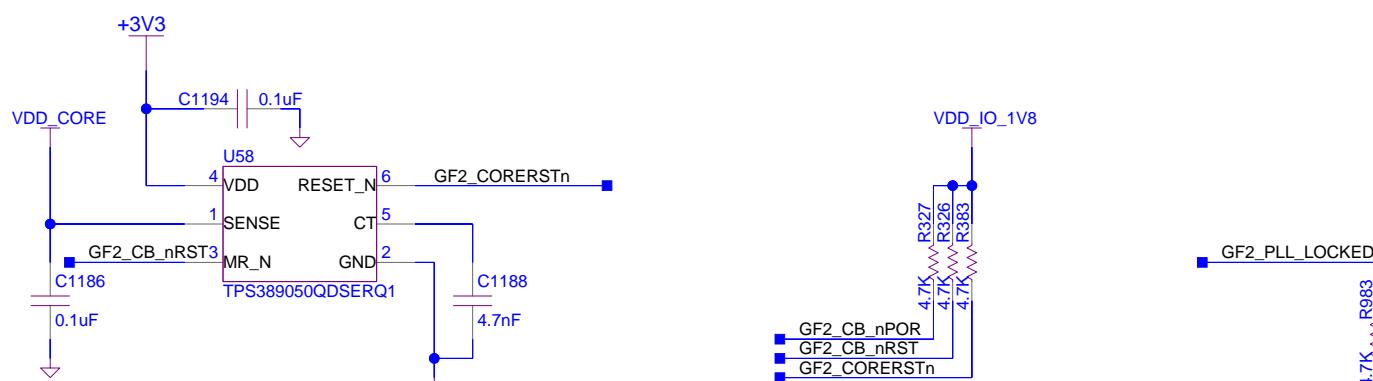
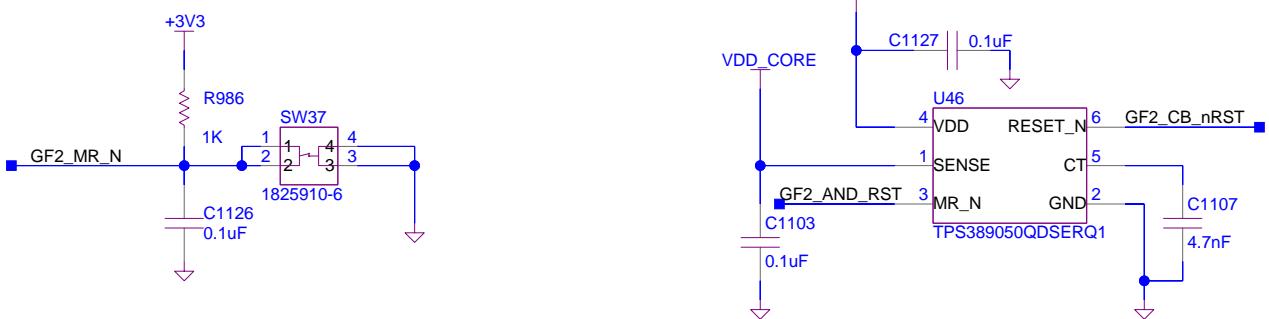
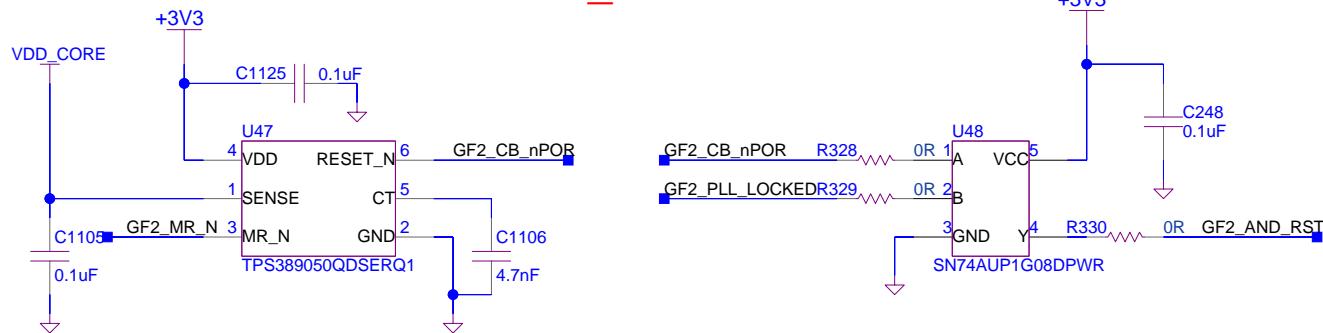
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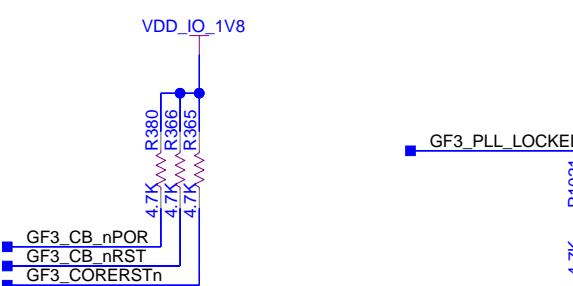
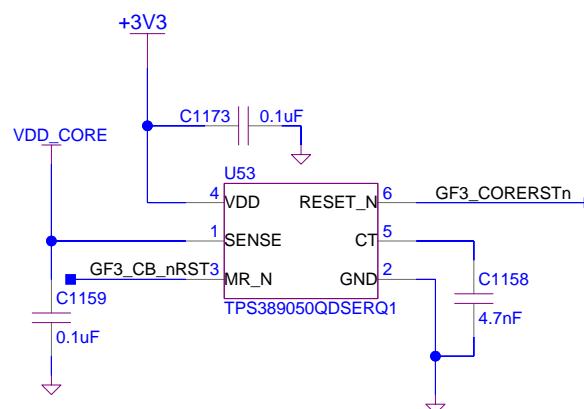
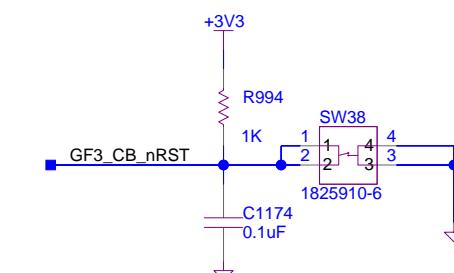
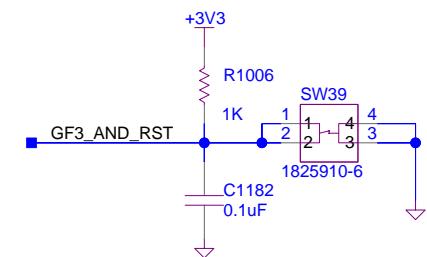
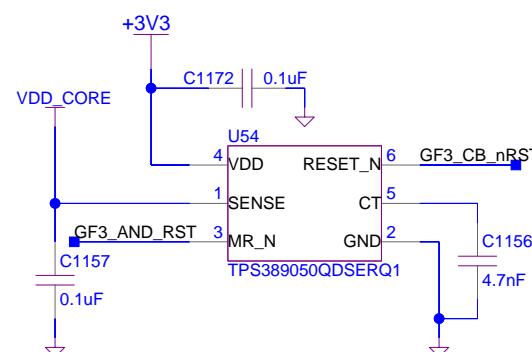
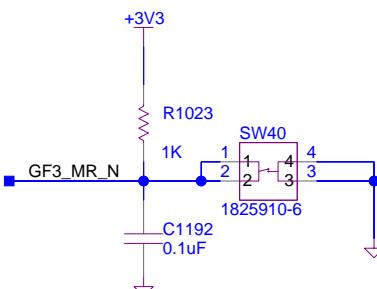
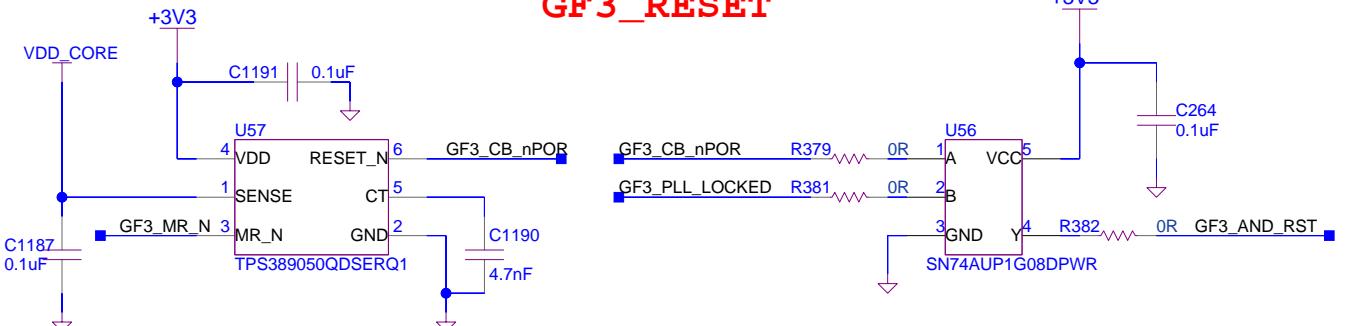
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