PMIC Programming, Power monitor and Resets

- Place the scripts in the BOOT partition of the sd card
- Insert the sd card in the Zybo / Zed board and power on the board and wait for it to boot successfully
- After the Zed or Zybo board is booted successfully -
    - Check for **ls ../../media/**
    - If nothing present in it then run the following commands to mount the BOOT partition onto the sd card
        - i. **mkdir -p /mnt/sd**
        - ii. **mount /dev/mmcblk0p1 /mnt/sd**
        - iii. Check for the script if present in the path **ls /mnt/sd**
        - iv. Navigate to that directory **cd /mnt/sd**
- Make the connections of the Zybo / Zed board PMOD interface with the J37 header of the validation board with proper I2C0 and I2C1 interface having a common ground
- After placing the power modules in their respective slots, power on the validation board
    - a. I2C0 - J60
    - b. I2C1 - J4

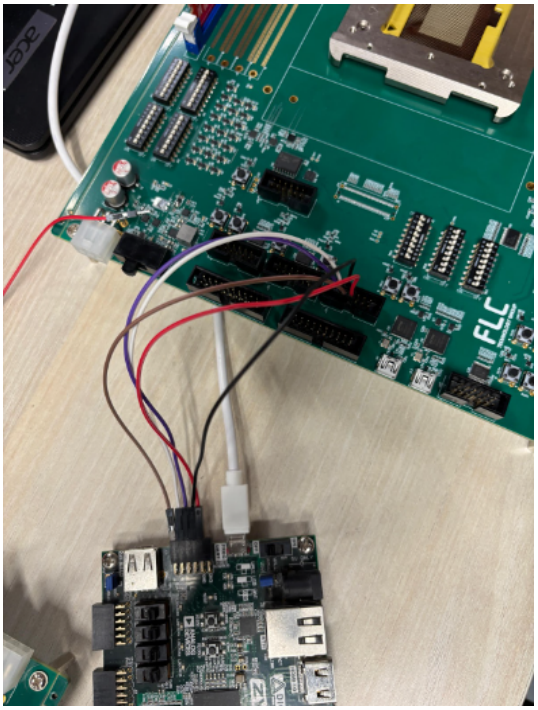
  ***** Note *** Do not interchange the power modules in any case**
  ***** Note *** Wait for some time to stabilise the regulators**
  ***** Note *** After power on ensure that the 12V, 1.8V and 3.3V power supply regulator LEDs were turned on. If not then turn off the power immediately**
- Slaves present on the I2C0 bus -
    - 0x10, 0x11, 0x12, 0x13 - ADS7138 (power monitors)
    - 0x21 - I/O Expander for Resets control (both MKB and GFx)
    - 0x20, 0x70, 0x72 - PMIC power modules (I/O expander to control the power goods of the PMICs and MUX selection channels)
    - 0x6C - Clock buffer
    - 0x68 - 100MHz clock generator
      ***** Note *** If J13 header is closed the clock generator doesn't fall on the I2C0 bus**
- Slaves present on the I2C1 bus -
    - 0x20, 0x70, 0x72 - PMIC power modules (I/O expander to control the power goods of the PMICs and MUX selection channels)

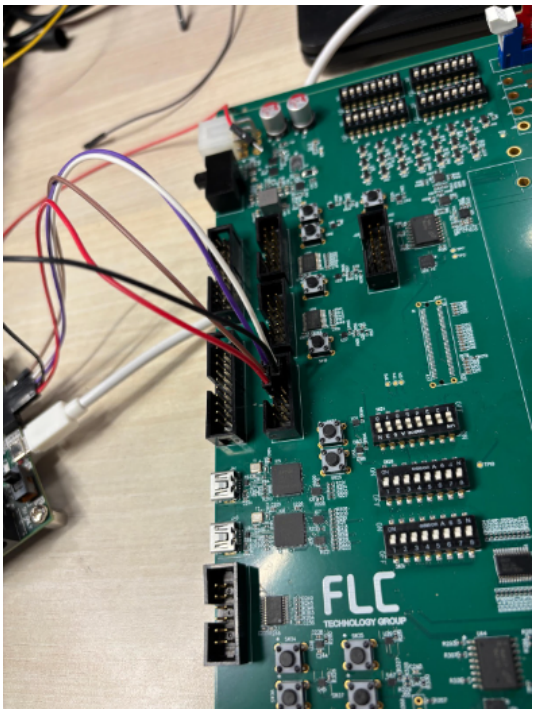
- Run the commands **i2cdetect -y -r -a 0** and **i2cdetect -y -r -a 1** to check if all the slave devices were present on the respective buses with respective slave addresses
  ***** Note *** The I/O expander (0x21) won't present initially on the I2C0. It can be seen after the voltage programming of the PMIC power modules as it has a dependency of VDD_IO_1V8 (1.8V) supply**
- To power-up the rails of J4 slot run **./J4_PMIC_ENABLE_VER2.sh** script
- To power-up the rails of the J60 slot run **./J60_PMIC_ENABLE_VER2.sh** script
- To monitor the power rails have been programmed successfully run **./power_monitor.sh** script
- Ensure that all the voltage values are within the ranges
  ***** Note *** If any of the power rail noted to be recorded as zero value then immediately turn off the board**
  ***** Note *** Wait for some time to stabilise the power rails and start your respective work**
- Rerun the commands **i2cdetect -y -r -a 0** and **i2cdetect -y -r -a 1** to check if all the slave devices were present on the respective buses with respective slave addresses
  ***** Note *** Now you should be seeing the I/O expander (0x21) on the I2C0 bus**
- To check the status of the Power goods of the PMIC power modules run the following commands -
  - **i2cget -y 0 0x20 0x01** - This should return **0x1f** confirming that all the PMICs on I2C0 (J60 slot) have been programmed successfully and in a good state
  - **i2cget -y 1 0x20 0x01** - This should return **0x1f** confirming that all the PMICs on I2C0 (J60 slot) have been programmed successfully and in a good state
- To issue a reset for the MKB (using the I/O control) run **./MKB_RESET.sh** script
- To issue a reset for the GFx (using the I/O control) run **./GF_RESET.sh** script
- To issue all the resets at once (using the I/O control) run **./GLOBAL_RESET.sh** script
- For the 100MHz clock generator and clock buffer to operate close the J13 header (short pins 1,2) with a jumper before power on the validation board
- To reprogram the J4 (I2C1 slot) PMIC power module if necessary run **./RESET_J4_I2C1_PMIC.sh** script
- To reprogram the J60 (I2C0 slot) PMIC power module if necessary run **./RESET_J60_I2C0_PMIC.sh** script

***** Note *** Run these scripts if incase any voltage reading has exceeded its limit and a reprogramming is to be done to nullify it by disabling the power goods of the PMICs**

***** Note *** If the Power goods were downed then for the next power on of the validation board the PMICs of J4 (I2C1) and J60 (I2C0) slots should be programmed with their respective voltage values and to placed in their respective slots**

S.NO	PMIC Channel	Power Rail Name	Voltage (V)	Regulator Capacity(A)	Design Consideration Current(A)	PMIC Channel	Power Rail Name	Voltage (V	Regulator Capacity(A)	ign Consideration Current(A)
1	PMIC1_SWAB	VDD_CORE	0.8	10	3.8	PMIC6_SWAB	VDD_CORE	0.8	10	3.8
2	PMIC1_SWD	NC	NC	NC	NC	PMIC6_SWD	NC	NC	NC	NC
3	PMIC1_SWC	GF23_VDDQ	1.2	5	2	PMIC6_SWC	GF01_VDDQ	1.2	5	2
4										
5	PMIC2_SWAB	IPM_MEM_VDD2	1.1	10	5.4	PMIC7_SWAB	D2D_VDDQ_0V75	0.75	5	2
6	PMIC2_SWD	VDD_IO_1V8	1.8	5	1.5	PMIC7_SWD	IPM_VDDQ_VDD	3.3	5	1
7	PMIC2_SWC	RC2-VDDH	1.2	5	1.07	PMIC7_SWC	RC1-VDDH	1.2	5	1.07
8										
9	PMIC3_SWAB	VDD_RDIMM56	1.2	10	5	PMIC8_SWAB	VDD_RDIMM34	1.2	10	5
10	PMIC3_SWD	NC	NC	NC	NC	PMIC8_SWD	NC	NC	NC	NC
11	PMIC3_SWC	EP12_VDDL	0.8	5	2.105	PMIC8_SWC	EP34_VDDL	0.8	5	2.105
12										
13	PMIC4_SWAB	VDD_RDIMM12	1.2	10	5	PMIC9_SWAB	VDD_RDIMM78	1.2	10	5
14	PMIC4_SWD	VPP_RDIMM56	2.5	5	2	PMIC9_SWD	VPP_RDIMM78	2.5	5	2
15	PMIC4_SWC	EP12_VDDH	1.2	5	2.14	PMIC9_SWC	EP34_VDDH	1.2	5	2.14
16										
17	PMIC5_SWAB	GF01-VDD	0.8	10	4	PMIC10_SWAB	GF23-VDD	0.8	10	4
18	PMIC5_SWD	VPP_RDIMM12	2.5	5	2	PMIC10_SWD	VPP_RDIMM34	2.5	5	2
19	PMIC5_SWC	RC1-VDDL	0.8	5	1.064	PMIC10_SWC	RC2-VDDL	0.8	5	1.064
20										





Powers {I2C1 - J60 (PMIC1), I2C2 - J4 (PMIC2)}			
MKB			
SI NO	**Power Rail Name**	**Voltage**	**Description**
1	VDD_CORE	0.8 V	Core Power (MKB / GF)
2	VDD_CORE	0.8 V	
3	VDD_IO_1V8	1.8 V	I/O Power
4	IPM_MEM_VDD2	1.1 V	IPM
5	IPM_VDDQ_VDD	3.3 V	
6	RC1-VDDH	1.2 V	RC
7	RC1-VDDL	0.8 V	
8	RC2-VDDH	1.2 V	
9	RC2-VDDL	0.8 V	
10	EP12-VDDH	1.2 V	EP
11	EP12-VDDL	0.8 V	
12	EP34-VDDH	1.2 V	
13	EP34-VDDL	0.8 V	
14	D2D_VDDQ_0V75	0.75 V	D2D
GF			
SI NO	**Power Rail Name**	**Voltage**	**Description**
1	GF01-VDD	0.8 V	GF0 / GF1 (combined)
2	GF01-VDDQ	1.2 V	
3	GF23-VDD	0.8 V	GF2 / GF3 (combined)
4	GF23-VDDQ	1.2 V	
5	VDD_RDIMM12	1.2 V	DDR4 Memory
6	VDD_RDIMM34	1.2 V	
7	VDD_RDIMM56	1.2 V	
8	VDD_RDIMM78	1.2 V	
9	VPP_RDIMM12	2.5 V	
10	VPP_RDIMM34	2.5 V	
11	VPP_RDIMM56	2.5 V	
12	VPP_RDIMM78	2.5 V	

Resets			
MKB and GF			
SI NO	**Rest Name**	**Switch**	**Test Point**
1	CB_nPOR	SW8	R231, R96
2	CB_nRST	SW8, SW12	R230, R111
3	CORERSTn	SW8, SW12, SW9	R229, R102
4	GF0_CB_nPOR	SW15	R228, R136

5	GF0_CB_nRST	SW15, SW25	R227, R196
6	GF0_CORERSTn	SW15, SW25, SW23	R229, R194
7	GF1_CB_nPOR	SW19	R225, R155
8	GF1_CB_nRST	SW19, SW35	R224, R281
9	GF1_CORERSTn	SW19, SW35, SW34	R223, R280
10	GF2_CB_nPOR	SW37	R252, R327
11	GF2_CB_nRST	SW37, SW36	R251, R326
12	GF2_CORERSTn	SW37, SW36, SW41	R250, R383
13	GF3_CB_nPOR	SW40	R249, R380
14	GF3_CB_nRST	SW40, SW39	R248, R366
15	GF3_CORERSTn	SW40, SW39, SW38	R247, R365

Clocks			
SI NO	**Reference CLK**	**CLK / CLK Buffer**	**Test Point**
1	25MHz	Oscillator - X1	R261
2		OSCCLK_0	R269
3		GF0_OSCCLK	R260
4		GF1_OSCCLK	R243
5		GF2_OSCCLK	R242
6		GF3_OSCCLK	R267
7	133.33MHz	Oscillator - Y3	R239
8		REF_IPM_0	R236
9		REF_IPM_1	R238
10		REF_IPM_2	R235
11		REF_IPM_3	R234
12	100MHz	Reference clock for Clock Generator CLOCK_GEN_1_P / CLOCK_GEN_1_N	C7, C8
13		Clock Generator Output GEN_REF_CLK_100MHz_P / GEN_REF_CLK_100MHz_N	C13, C14
14		Clock Buffer Input PCIE_REF_CLK_P / PCIE_REF_CLK_N	R19, R20
15		100MHz differential clock for D2D PLL REF_100M_P[0] / REF_100M_N[0]	C118, C119
16		100Mz differential clock for D2D PLL	C124, C125

		REF_100M_P[1] / REF_100M_N[1]	
17		PCIe/CXL RC PHY reference clock RC_X8_REF_CLK0_P / RC_X8_REF_CLK0_N	C130, C131
18		PCIe/CXL RC PHY reference clock RC_X8_REF_CLK1_P / RC_X8_REF_CLK1_N	C136, C137
19		PCIe/CXL endpoint PHY reference clock EP0_REF_CLK_100MHz_P / EP0_REF_CLK_100MHz_N	C144, C145
20		PCIe/CXL endpoint PHY reference clock EP1_REF_CLK_100MHz_P / EP1_REF_CLK_100MHz_N	C149, C150
21		PCIe/CXL endpoint PHY reference clock EP2_REF_CLK_100MHz_P / EP2_REF_CLK_100MHz_N	C153, C154
22		PCIe/CXL endpoint PHY reference clock EP3_REF_CLK_100MHz_P / EP3_REF_CLK_100MHz_N	C160, C161
23		PCIe/CXL RC reference clock CLK_CXL_CONN_P / CLK_CXL_CONN_N	C162, C163
24		PCIe/CXL RC PHY reference clock RC_CXL_REF1_P / RC_CXL_REF1_N	C164, C165
25		100MHz differential clock for DDR GF0_REF_100M_P / GF0_REF_100M_N	C166, C167
26		100MHz differential clock for DDR GF1_REF_100M_P / GF1_REF_100M_N	C168, C169
27		100MHz differential clock for DDR	C155, C52

		GF2_REF_100M_P / GF2_REF_100M_N	
28		100MHz differential clock for DDR GF3_REF_100M_P / GF3_REF_100M_N	C151, C147
29		NVMe0 reference clock PCIE_RC_NVME0_REF_CLK_P / PCIE_RC_NVME0_REF_CLK_N	C146, C139
30		NVMe1 reference clock PCIE_RC_NVME1_REF_CLK_P / PCIE_RC_NVME1_REF_CLK_N	C138, C133
31		SSD1 reference clock PCIE_RC_SSD1_REF_CLK_P / PCIE_RC_SSD1_REF_CLK_N	C132, C127
32		SSD0 reference clock PCIE_RC_SSD_REF_CLK_P / PCIE_RC_SSD_REF_CLK_N	C126, C121
33		PCIE_CLK_BUFFER_18_P / PCIE_CLK_BUFFER_18_N	C120, C116