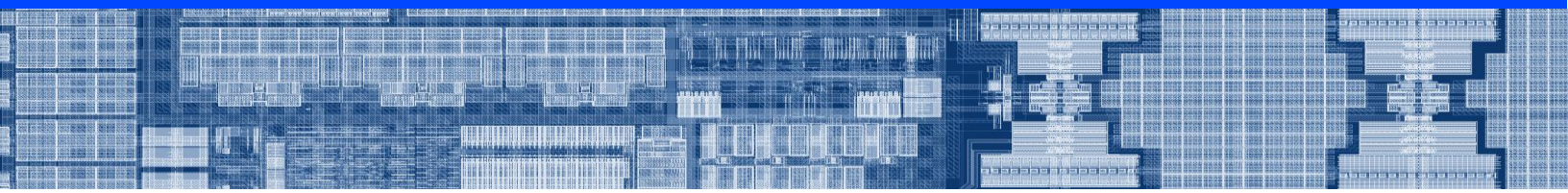
PLLTS12FFCFRACF
Programmable Fractional PLL
TSMC 12nm FFC

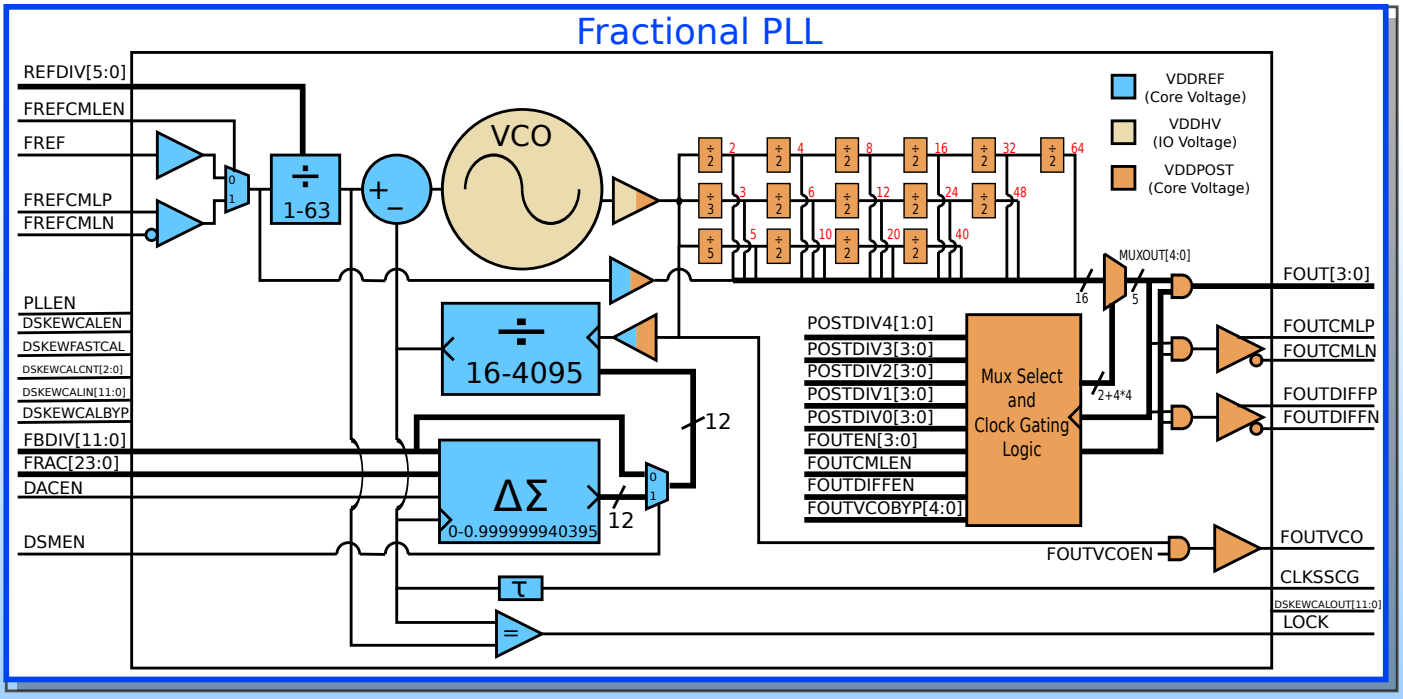


Overview

The Silicon Creations Programmable Delta-Sigma Fractional PLL is a multi-function, general purpose frequency synthesizer. Ultra-wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for almost any clocking application. With excellent supply noise immunity, the PLL is ideal for use in noisy mixed-signal SoC environments. By combining ultra-low jitter output clocks into a low power, low area, widely programmable design, Silicon Creations can greatly simplify an SoC by enabling a single macro to be used for all clocking applications in the system.

Features

- Input frequency range: 8MHz to 650MHz
  - 10MHz to 650MHz (fractional mode)
- Output frequency range: 31MHz to 8000MHz
- 24 bit fractional accuracy
  - ΔΣ noise cancellation DAC allows fractional mode jitter performance to nearly match integer mode performance
- 4:1 VCO frequency range allows PLL to be optimized for minimum jitter or minimum power
- Isolated analog supply (1.8V) allows for excellent supply rejection in noisy SoC applications
- Lock Detect Signal indicates when frequency lock has been achieved
- CML Input and Output clocks
- Five independent outputs with glitch-free post divide switching
- Low area (0.09mm^2)



Specified Operating Conditions

Parameter	Condition	Minimum	Typical	Maximum
VDDHV	Analog Supply Voltage	1.62V	1.8V	1.98V
VDDREF, **VDDPOST**	Digital Supply Voltage	0.72V	0.8V	1.05V
VDDREF, **VDDPOST**	AC Supply Noise Limit	0.68V		0.93V
T_J	Junction Temperature	-40°C	25°C	125°C

PLL Specifications

Parameter	Units	Min.	Typical	Max.	Comments
VDDHV Current Consumption (FVCO = 2.5GHz) INT mode	mA		0.95	1.37	Current Scales as $(\frac{FVCO}{2.5GHz})^{1.5}$. Example: For FVCO = 8000MHz, current = $(\frac{8000MHz}{2.5GHz})^{1.5} * 0.95$mA = 5.72mA.
VDDHV Current Consumption (FVCO = 2.5GHz) FRAC mode	mA		1.00	1.47	Current Scales as $(\frac{FVCO}{2.5GHz})^{1.5}$. Example: For FVCO = 8000MHz, current = $(\frac{8000MHz}{2.5GHz})^{1.5} * 1.00$mA = 6.13mA.
VDDREF Current Consumption	μA/MHz		0.2	0.24	Specification is based on VCO frequency. VDD = 0.8V. Power scales as VDD^2
VDDPOST Current Consumption	μA/MHz		0.7	0.84	Specification is based on FVCO=8000MHz with POSTDIV#[3:0]=4'b0001 and POSTDIV4[1:0]=2'b00. VDD = 0.8V. Power scales as VDD^2
CML Input Current Consumption	mA		2.1	2.94	CML input current is on VDDREF. **FREFCMLEN**==1.
CML Output Current Consumption	mA		2.0	2.80	CML output current is on VDDPOST. **FOUTCMLEN**==1.

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Parameter	Units	Min.	Typical	Max.	Comments
VDDHV Power Down Leakage	nA		10		TT Corner, Nom VDD, TEMP=25C
VDDREF Power Down Leakage	μA		10		TT Corner, Nom VDD, TEMP=25C
VDDPOST Power Down Leakage	μA		20		TT Corner, Nom VDD, TEMP=25C
Reference Frequency Range	MHz	8		650	
PFD Frequency Range	MHz	8		160	
VCO Frequency Range	MHz	2000		8000	
Output Duty Cycle	%	47	50	53	Even Divides @ FOUT=4000MHz (falling edge error is ±7ps)
Output Duty Cycle	%	47	50	53	Odd Divides @ FOUT=2666MHz (falling edge error is ±11ps)
Output Duty Cycle	%	46	50	54	**FOUTVCO** at any frequency
CML Input Low Voltage	mV	-100	0	100	Ground-referenced **FREFCMLP** and **FREFCMLN** input logic LOW voltage
CML Input High Voltage	mV	300	400	880	Ground-referenced **FREFCMLP** and **FREFCMLN** input logic HIGH voltage
CML Output Low Voltage	mV	0	0	100	Ground-referenced **FOUTCMLP** and **FOUTCMLN** output logic LOW voltage
CML Output High Voltage	mV	300	400	500	Ground-referenced **FOUTCMLP** and **FOUTCMLN** output logic HIGH voltage
CML Output Load Resistance	Ω	160	200	240	CML output driver uses p+ poly resistors referenced to **VSS**
Lock Time (frequency)	Input clock cycles		1300	2000	Input clock cycle is **REFDIV**/**FREF**. Example: **FREF** = 25MHz, **REFDIV** = 1, Lock time = 52.0μs

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Parameter	Units	Min.	Typical	Max.	Comments
Lock Time (phase)	Input clock cycles			2000	Input clock cycle is **REFDIV/FREF**. Example: **FREF** = 25MHz, **REFDIV** = 1, Lock time = 80.0μs, settled to within LTJ spec
Phase calibration without initial condition	PFD Cycles		2000	10000	PFD cycle is REFDIV/FREF. Example: FREF = 25MHz, REFDIV = 1, lock time = 80.0μs, **DSKEWCALBYP**=0, **DSKEWCALEN**=1, **DSKEWFASTCAL**=1
Phase calibration with previous calibration	PFD Cycles		100	500	PFD cycle is REFDIV/FREF. Example: FREF = 25MHz, REFDIV = 1, lock time = 4.0μs, **DSKEWCALBYP**=1, **DSKEWCALEN**=1
Reference Divide		1		63	Maximum divided reference clock frequency should be FVCO/16
Feedback Divide (Int)		16		1000	
Feedback Divide (Frac)		20		1000	
Post Divide to **FOUT**[3:0]		2		64	Four independent outputs each with 4-bit programmable post divide
Post Divide to differential outputs		4		12	Selectable pseudo-differential or CML outputs with common 2-bit programmable post divide
Maximum frequency for post divider glitch-free switching	MHz		1600		The output clock is glitch-free when switching between different POSTDIV values

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Parameter	Units	Min.	Typical	Max.	Comments
Delay from POSTDIV to output between switching	Output clock cycles			64	Settling time after POSTDIV value is changed. Example, for FVCO = 2000MHz, POSTDIV changed from divide-by-2 to divide-by-3, the delay from POSTDIV to static output state is approximately 64*3/2000MHz=0.10usec.
Delay from previous output state to current output state between switching	Output clock cycles			16	Settling time from previous output state. Example, for FVCO = 2000MHz, POSTDIV changed from divide-by-2 to divide-by-3, the delay from FOUT=1000MHz to FOUT=666MHz is approximately 16*3/2000MHz=24nsec.
Initial settling time for post divider	VCO clock cycles			4096	Worst case wait time required for correct output clock after PLL is enabled. Based on initial condition of post divider.
Period jitter (random)	ps (RMS)			0.09	@VCO= 8000MHz. Random jitter scales as $\sqrt{\frac{8000MHz}{FVCO}} \times \sqrt{\frac{8000MHz}{FOUT}}$
Integrated jitter (10kHz-Nyquist) (Integer Mode)	ps (RMS)			3.7	FPFD = 25MHz, FVCO = 8000MHz. Jitter scales as $\sqrt{\frac{25MHz}{FPFD}} \times \sqrt{\frac{8000MHz}{FVCO}}$
Integrated jitter (10kHz-Nyquist) (Fractional Mode)	ps (RMS)			4.4	FPFD = 25MHz, FVCO = 8000MHz. Jitter scales as $\sqrt{\frac{25MHz}{FPFD}} \times \sqrt{\frac{8000MHz}{FVCO}}$
Filtered Long Term Jitter, PCIeGen3, Common Clocked Architecture	ps (RMS)		0.5	1.0	FPFD≥19.2MHz, FVCO≥2.4GHz. Analysis excludes **VDDHV** supply noise, so careful filtering of in-band noise components is required.

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Parameter	Units	Min.	Typical	Max.	Comments
Filtered Long Term Jitter, PCIeGen3, Data Clocked Architecture	ps (RMS)		0.5	1.0	FPFD≥19.2MHz, FVCO≥2.4GHz. Analysis excludes **VDDHV** supply noise, so careful filtering of in-band noise components is required.
Closed Loop Bandwidth (Integer Mode)	MHz		FPFD/30		Transfer function is an approximately single-pole phase filter with -3dB bandwidth as specified and -20dB/dec roll-off. FPFD is defined as FREF/**REFDIV**
Closed Loop Bandwidth (Fractional Mode)	MHz		FPFD/35		Transfer function is an approximately single-pole phase filter with -3dB bandwidth as specified and -20dB/dec roll-off. FPFD is defined as FREF/**REFDIV**
VDDHV supply noise sensitivity	fs/mV			1.5	This is an open loop transfer function. To calculate the total accumulated phase jitter please refer to the JITTERDOC specification.
Forward path period jitter gain (Int) @FVCO=8GHz				0.0007	K_f as specified in the Jitterdoc Scales with $\sqrt{\frac{8000MHz}{FVCO}}$
Forward path period jitter gain (Frac) @FVCO=8GHz				0.0005	K_f as specified in the Jitterdoc Scales with $\sqrt{\frac{8000MHz}{FVCO}}$
Total Output delay (For FVCO)	ps		60	120	Typ Corner: TT, 27C, 0.9v W/c Corner: SS,-40C,0.81v
Total Output delay sensitivity (For FVCO)	ps/mV		0.12	0.24	Typ Corner: TT, 27C, 0.9v W/c Corner: SS,-40C,0.81v
Total Output delay (For Bypass Path)	ps		300	600	Typ Corner: TT, 27C, 0.9v W/c Corner: SS,-40C,0.81v
Total Output delay sensitivity (For Bypass Path)	ps/mV		0.60	1.20	Typ Corner: TT, 27C, 0.9v W/c Corner: SS,-40C,0.81v
Total Output delay (Longest Delay)	ps		480	960	Typ Corner: TT, 27C, 0.9v W/c Corner: SS,-40C,0.81v

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Parameter	Units	Min.	Typical	Max.	Comments
Total Output delay sensitivity (Longest Delay)	ps/mV		0.96	1.92	Typ Corner: TT, 27C, 0.9v W/c Corner: SS,-40C,0.81v (CMOS path)
Area	mm^2		0.09		300μm x 300μm
IP Version List					
IP Version	1.2.0.x		2Xa 1Xd_h 2Xe_vh 0.8V/1.8V		Compatible with all metal options 6M and above. SVT and uLVT masks are required.

Pin List

Signal	Direction	Comments
CLKSSCG	output	Synchronization clock for spread spectrum modulation. Minimum pulse width is 1.0ns. Hold time for **FBDIV** and **FRAC** is negative when synchronized with **CLKSSCG** Setup time is 1/FPFD - 10/FVCO
DACEN	input	Enable fractional noise canceling DAC in FRAC mode (this has no function in integer mode) 0 -> Fractional noise canceling DAC is not active (test mode only) 1 -> Fractional noise canceling DAC is active (default mode)
DSKEWCALBYP	input	Deskew calibration bypass 1'b0 - use the skew calibration output (when **DSKEWCALEN**=1) to set the phase correction 1'b1 - use the **DSKEWCALIN**[11:0] value (when **DSKEWCALEN**=1) to set the phase correction
DSKEWCALCNT[2:0]	input	Programmable counter for deskew calibration loop Selects the number of PFD edges to wait after each deskew calibration step. Count is defined as $2^{DSKEWCALCNT+5}$ (e.g. if **DSKEWCALCNT**=3'd5, the loop will wait 1024 PFD periods before trying a new setting) Default setting is 3'd2
DSKEWCALEN	input	Deskew calibration enable to actively adjust for input skew 1'b0 - skew calibration is disabled. Static phase offset is determined by analog matching only. 1'b1 - skew calibration is enabled. Static phase offset is adjusted by sensing phase at the input.

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Signal	Direction	Comments
DSKEWCALIN[11:0]	input	DSKEWCALBYP == 1'b0: Initial condition for deskew calibration logic. DSKEWCALBYP == 1'b1: Override value for deskew calibration. It is a signed integer with positive values delaying the reset of the faster path, and negative values delaying the reset of the slower path. 5'b0 is the minimum value, with each count increasing the reset time by one buffer delay. If **DSKEWCALEN**=1, this can be used to force a skew correction value based on a previous readout of **DSKEWCALOUT**[11:0]. If **DSKEWCALBYP**=1 this value is forced directly into the calibration logic. If **DSKEWCALBYP**=0 this is the initial condition for the calibration sequence.
DSKEWCALLOCK	output	Deskew Calibration settled indicator for the PLL 1'b0 –> Deskew calibration not yet settled 1'b1 –> Deskew calibration settled
DSKEWCALOUT[11:0]	output	This is the output of either the skew calibration block (if **DSKEWCALBYP**=0) or a buffered version of **DSKEWCALIN**[11:0] (if **DSKEWCALBYP**=1). It can be used to read out the phase calibration state to use as an override value so that skew calibration can be bypassed for faster locking. The value changes on the rising edge of FREF, so it can be clocked out on the falling edge of FREF.
DSKEWFASTCAL	input	Deskew fast calibration enable Set this to 1 for initial calibration if an initial value is not already known Should be set to 0 for normal operation
DSMEN	input	Enable Delta-Sigma Modulator 0 -> DSM is powered down (integer mode) 1 -> DSM is active (fractional mode)
FBDIV[11:0]	input	PLL Feedback divide value (16 to 1000 in integer mode, 20 to 1000 in fractional mode)
FOUT[3:0]	output	PLL post divided CMOS outputs (31MHz to 4000MHz) VCO frequency divided by selected post divide value
FOUTCMLEN	input	0 -> **FOUTCMLP** CML positive phase output clock is powered down (output at 0V) **FOUTCMLN** CML negative phase output clock is powered down (output at 0V) 1 -> **FOUTCMLP** CML positive phase output clock is enabled (Frequency is FVCO/(**POSTDIV4** value)) **FOUTCMLN** CML negative phase output clock is enabled (Frequency is FVCO/(**POSTDIV4** value))

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Signal	Direction	Comments
FOUTCMLN	output	Negative phase CML output clock (166MHz to 2000MHz) Enabled with **FOUTCMLEN** Output goes to 0V when disabled
FOUTCMLP	output	Positive phase CML output clock (166MHz to 2000MHz) Enabled with **FOUTCMLEN** Output goes to 0V when disabled
FOUTDIFFEN	input	For glitch-free operation when enable goes high, **FOUTCMLEN** must be 0 (or changed to 1 after **FOUTDIFFEN** is enabled) 0 -> **FOUTDIFFP** pseudo-differential positive phase output clock is powered down (output held at 1'b0) **FOUTDIFFN** pseudo-differential negative phase output clock is powered down (output held at 1'b1) 1 -> **FOUTDIFFP** pseudo-differential positive phase output clock is enabled (Frequency is FVCO/(**POSTDIV4** value)) **FOUTDIFFN** pseudo-differential negative phase output clock is enabled (Frequency is FVCO/(**POSTDIV4** value))
FOUTDIFFN	output	Require clock gating circuit for glitch-free output when enable goes high Negative phase pseudo-differential output clock (166MHz to 2000MHz) Enabled with **FOUTDIFFEN** Output driven high when disabled
FOUTDIFFP	output	Require clock gating circuit for glitch-free output when enable goes high Positive phase pseudo-differential output clock (166MHz to 2000MHz) Enabled with **FOUTDIFFEN** Output driven low when disabled
FOUTEN[3:0]	input	Bit-wise Post Divide Enable FOUTEN[3] enables FOUT[3] FOUTEN[2] enables FOUT[2] FOUTEN[1] enables FOUT[1] FOUTEN[0] enables FOUT[0] 0 -> Respective **FOUT** clock is powered down (output held at 1'b0) 1 -> Respective **FOUT** clock is enabled
FOUTVCO	output	VCO rate output clock (2000MHz to 8000MHz)

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Signal	Direction	Comments
FOUTVCOBYP[4:0]	input	Bypasses undivided VCO clock to respective output **FOUTVCOBYP**[4]=1 bypasses the VCO clock to **FOUTCMLP**, (inverted to) **FOUTCMLN**, **FOUTDIFFP**, (inverted to) **FOUTDIFFN** **FOUTVCOBYP**[3]=1 bypasses the VCO clock to **FOUT**[3] **FOUTVCOBYP**[2]=1 bypasses the VCO clock to **FOUT**[2] **FOUTVCOBYP**[1]=1 bypasses the VCO clock to **FOUT**[1] **FOUTVCOBYP**[0]=1 bypasses the VCO clock to **FOUT**[0]
FOUTVCOEN	input	VCO rate output clock (**FOUTVCO**) enable 0 -> **FOUTVCO** is powered down (output is held at 1'b0) 1 -> **FOUTVCO** is enabled
FRAC[23:0]	input	Fractional portion of feedback divide value
FREF	input	Single-ended CMOS reference clock input (8MHz to 650MHz, in integer mode, 10MHz to 650MHz, in fractional mode) Only the rising edge is used by the PLL
FREFCMLEN	input	Enable FREF CML Input 0 -> Reference clock input is taken from single-ended CMOS level input **FREF** 1 -> Reference clock input is taken from differential CML level inputs **FREFCMLP** and **FREFCMLN**
FREFCMLN	input	CML negative phase reference clock input (ground-referenced) (8MHz to 650MHz, in integer mode, 10MHz to 650MHz, in fractional mode)
FREFCMLP	input	CML positive phase reference clock input (ground-referenced) (8MHz to 650MHz, in integer mode, 10MHz to 650MHz, in fractional mode)
LOCK	output	Lock signal Lock detector can measure frequency accuracy down to 0.8% of programmed target frequency 0.8% is the value of the lock circuit measurement uncertainty Actual frequency will be much closer to the final target. Phase settling is guaranteed by design after 2000 PFD cycles.
PLLEN	input	Global enable signal for PLL 0 -> FREF bypassed to all Outputs (except FOUTVCO) 1 -> Entire PLL is enabled

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Signal	Direction	Comments
POSTDIV0[3:0]	input	PLL post divide 0 setting (2 to 64) 4'b1111=divide-by-64 4'b1110=divide-by-48 4'b1101=divide-by-40 4'b1100=divide-by-32 4'b1011=divide-by-24 4'b1010=divide-by-20 4'b1001=divide-by-16 4'b1000=divide-by-12 4'b0111=divide-by-10 4'b0110=divide-by-8 4'b0101=divide-by-6 4'b0100=divide-by-5 4'b0011=divide-by-4 4'b0010=divide-by-3 4'b0001=divide-by-2 4'b0000=**FREF** bypassed to output
POSTDIV1[3:0]	input	PLL post divide 1 setting (2 to 64) 4'b1111=divide-by-64 4'b1110=divide-by-48 4'b1101=divide-by-40 4'b1100=divide-by-32 4'b1011=divide-by-24 4'b1010=divide-by-20 4'b1001=divide-by-16 4'b1000=divide-by-12 4'b0111=divide-by-10 4'b0110=divide-by-8 4'b0101=divide-by-6 4'b0100=divide-by-5 4'b0011=divide-by-4 4'b0010=divide-by-3 4'b0001=divide-by-2 4'b0000=**FREF** bypassed to output

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Signal	Direction	Comments
POSTDIV2[3:0]	input	PLL post divide 2 setting (2 to 64) 4'b1111=divide-by-64 4'b1110=divide-by-48 4'b1101=divide-by-40 4'b1100=divide-by-32 4'b1011=divide-by-24 4'b1010=divide-by-20 4'b1001=divide-by-16 4'b1000=divide-by-12 4'b0111=divide-by-10 4'b0110=divide-by-8 4'b0101=divide-by-6 4'b0100=divide-by-5 4'b0011=divide-by-4 4'b0010=divide-by-3 4'b0001=divide-by-2 4'b0000=**FREF** bypassed to output
POSTDIV3[3:0]	input	PLL post divide 3 setting (2 to 64) 4'b1111=divide-by-64 4'b1110=divide-by-48 4'b1101=divide-by-40 4'b1100=divide-by-32 4'b1011=divide-by-24 4'b1010=divide-by-20 4'b1001=divide-by-16 4'b1000=divide-by-12 4'b0111=divide-by-10 4'b0110=divide-by-8 4'b0101=divide-by-6 4'b0100=divide-by-5 4'b0011=divide-by-4 4'b0010=divide-by-3 4'b0001=divide-by-2 4'b0000=**FREF** bypassed to output
POSTDIV4[1:0]	input	PLL post divide 4 setting (4 to 12) 2'b11=divide-by-12 2'b10=divide-by-8 2'b01=divide-by-6 2'b00=divide-by-4
REFDIV[5:0]	input	Reference divide value (1 to 63)
VDDHV	supply1	1.8V analog supply
VDDPOST	supply1	0.8V supply for post dividers
VDDREF	supply1	0.8V supply for reference rate circuits

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Signal	Direction	Comments
VSS	supply0	0V supply and substrate connection

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