EVL5475-U-00B

Fully Integrated, 12V, 6A, Quad-Buck PMIC with I²C Evaluation Board

DESCRIPTION

The EVL5475-U-00B is an evaluation board designed to demonstrate the capabilities of the MP5475, a complete power management IC (PMIC) that integrates four high-efficiency, step-down DC/DC converters and a flexible logic interface.

The MP5475 adopts constant-on-time (COT) control. The device's DC/DC converter also provides fast transient response and eases loop stabilization. Full protection features include under-voltage lockout (UVLO), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown. Refer to the MP5475 datasheet for more detailed information.

It is recommended to read the MP5475 datasheet prior to making any changes to the EVL5475-U-00B.

PERFORMANCE SUMMARY (1)

Specifications are at T_A = 25°C, unless otherwise noted.

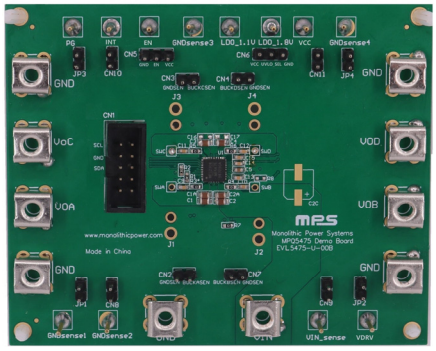
Parameters	Conditions	Value
Input voltage (V_{IN}) range		3V to 16V
Output voltage (V_{OUT})		Refer to I²C setting
Single-phase maximum output current (I_{OUT})	V_{IN} = 3V to 16V	6A
Dual-phase maximum output current (I_{OUT})	V_{IN} = 3V to 16V	12A
Single-phase full load efficiency	V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 6A	87.5%
Single-phase peak efficiency	V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 4A	88%
Dual-phase full load efficiency	V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 12A	86.5%
Dual-phase peak efficiency	V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 7A	88%

Note:

1) For different V_{IN} and V_{OUT} specifications with different output capacitors and inductors, the application circuit parameters may require changes.

MPL Optimized Performance with MPS Inductor MPL-AL4020 Series

EVALUATION BOARD



LxWxH (9.5cmx7.7cmx2.5cm)

Board Number	MPS IC Number
EVL5475-U-00B	MP5475GU

QUICK START GUIDE

The EVL5475-U-00B evaluation board is easy to set up and use to evaluate the performance of the MP5475. For proper measurement equipment set-up, refer to Figure 1 on page 3 and follow the steps below:

1. Preset power supply 1 (V_{DRV}) to 3.3V.
2. Preset power supply 2 (V_{IN}) between 3V and 16V. No timing relationship exists between the two power supplies. (2)
3. Turn off the V_{DRV} and V_{IN} power supplies.
4. Connect the power supply 1 terminals to:
   a. Positive (+): VDRV
   b. Negative (-): GND
5. Connect the power supply 2 terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
6. Connect the load terminals to: (3)
   a. Positive (+): VOUT (4)
   b. Negative (-): GND
7. After making the connections, turn on the V_{DRV} and V_{IN} power supplies.
8. Set SYSEN (register 40h, bit[7]) to 1, which should start up the board. The DC/DC regulators turn on sequentially based on their enable bits (register 40h, bits[5:2]) and start-up delay setting.
9. Check for the proper output voltages.
10. Once the proper output voltage (V_{OUT}) is established, adjust the load within the operating range and measure the efficiency, output ripple voltage, and other parameters. (5)
11. After completing all tests, adjust the load to 0A, then turn off the V_{DRV} and V_{IN} power supplies.

Notes:

2) Make sure that V_{IN} does not exceed 16V.
3) There is no initial load by default.
4) Every single-phase channel connects to one load. Choose one channel in two dual-phase channels to connect the load.
5) When measuring the output voltage ripple or input voltage ripple, do not use the oscilloscope probe's long ground lead.

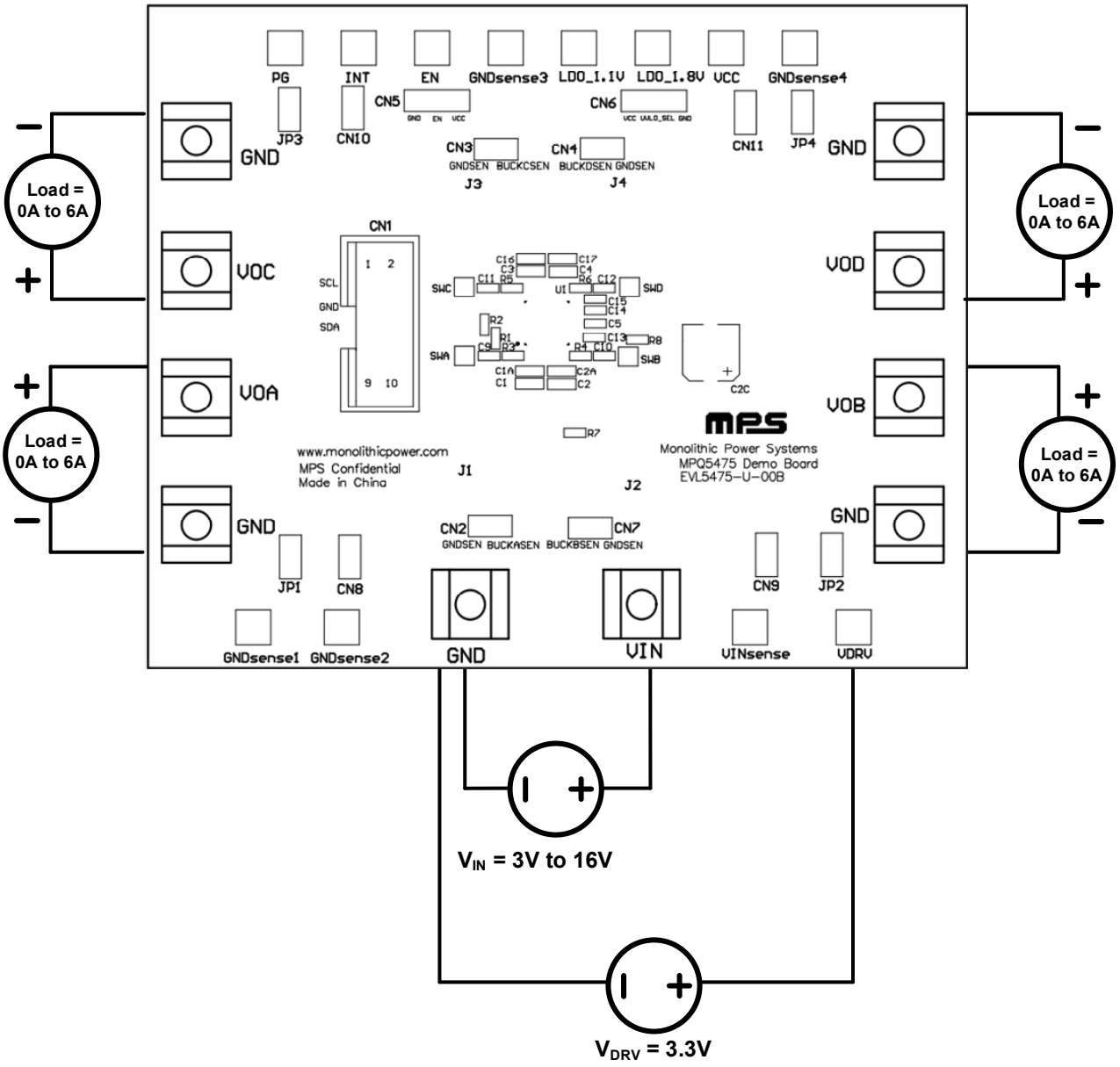


Figure 1: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

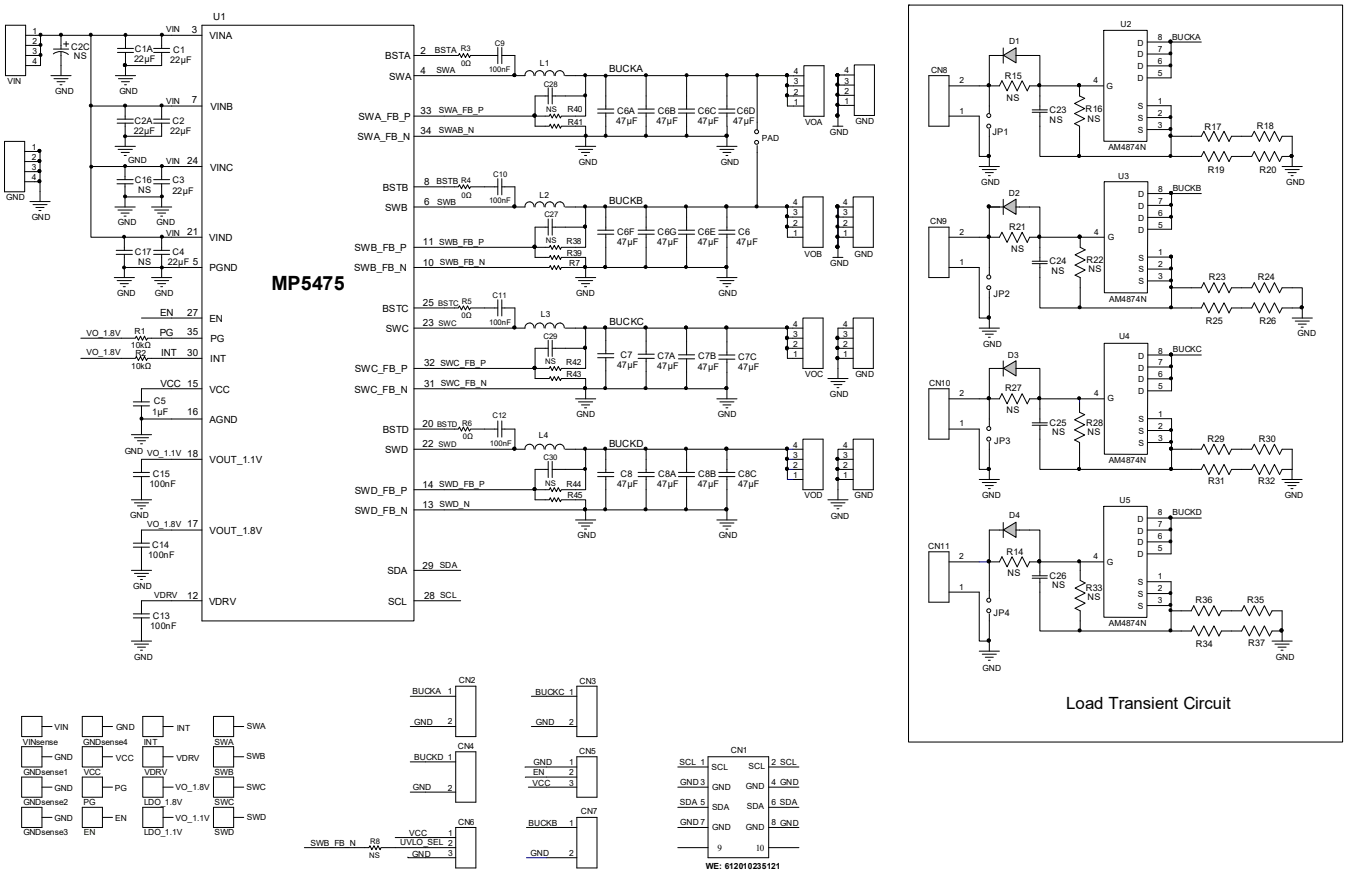


Figure 2: Evaluation Board Schematic

EVL5475-U-00B BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	L1, L2, L3, L4 (6)	Option 1: 0.47µH	Inductor, R_{DC} = 6.2mΩ, I_{SAT} = 12.5A	SMD	MPS	MPL-AL4020-R47
		Option 2: 0.68µH	Inductor, R_{DC} = 7.5mΩ, I_{SAT} = 11A	SMD	MPS	MPL-AL4020-R68
		Option 3: 1µH	Inductor, R_{DC} = 10.1mΩ, I_{SAT} = 8.6A	SMD	MPS	MPL-AL4020-1R0
		Option 4: 1.5µH	Inductor, R_{DC} = 14.5mΩ, I_{SAT} = 7.1A	SMD	MPS	MPL-AL4020-1R5
6	C1, C1A, C2, C2A, C3, C4	22µF	Ceramic capacitor, 25V, X5R	0805	Murata	GRM21BR61E226ME44L
1	C5	1µF	Ceramic capacitor, 10V, X7S	0603	Murata	GRM188R71A105KA61D
16	C6, C6A, C6B, C6C, C6D, C6E, C6F, C6G, C7, C7A, C7B, C7C, C8, C8A, C8B, C8C	47µF	Ceramic capacitor, 6.3V, X5R	0805	Murata	GRM21BR60J476ME5L
7	C9, C10, C11, C12, C13, C14, C15	100nF	Ceramic capacitor, 16V, X5R	0603	Murata	GRM033R60J104KE19D
0	C2C, C16, C17, C23, C24, C25, C26, C27, C28, C29, C30	NS				
2	R1, R2	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
11	R3, R4, R5, R6, R7	0Ω	Film resistor, 1%	0603	Yageo	RC0402FR-070RL
0	R8, R14-R37, R38, R39, R40, R41, R42, R43, R44, R45	NS				
4	U2, U3, U4, U5	30V	N-channel MOSFET	SOIC8	Analog Power	AM4874N
0	D1, D2, D3, D4	NS				
1	U1	MP5475GU	12V, 6A, quad-buck PMIC with I^2C	QFN-36 (5mmx 5mm)	MPS	MP5475GU

Note:

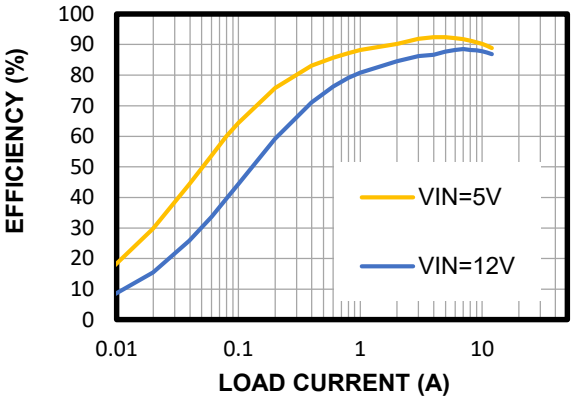
6) It is recommended to use the MPL-AL4020-xxx. Choose an inductor with a suitable value based on V_{OUT}. Refer to the MP5475 datasheet for more details on selecting the inductor.

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

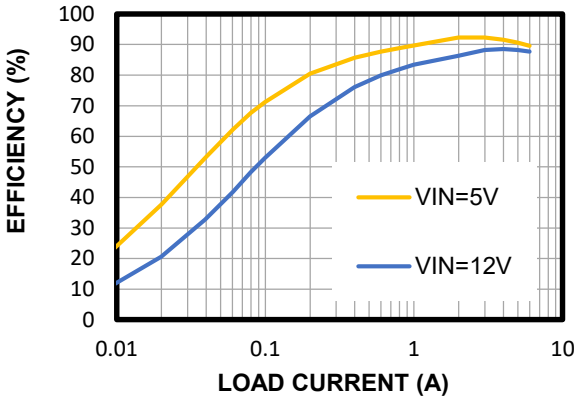
Efficiency vs. Load Current

$V_{OUT1/2}$ = 0.86V, PFM mode



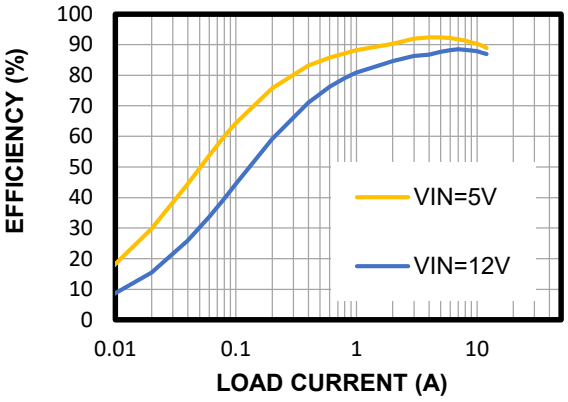
Efficiency vs. Load Current

V_{OUT3} = 0.9V, PFM mode



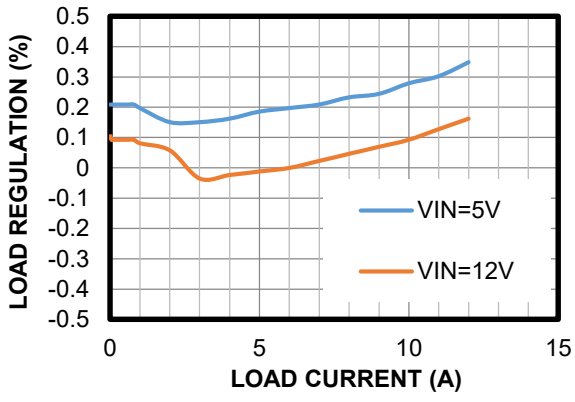
Efficiency vs. Load Current

V_{OUT4} = 0.9V, PFM mode



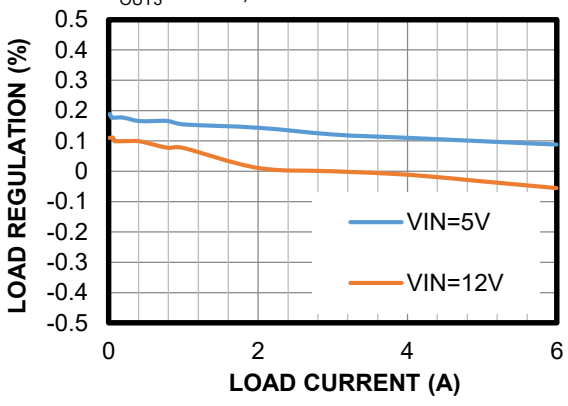
Load Regulation

$V_{OUT1/2}$ = 0.86V, PFM mode



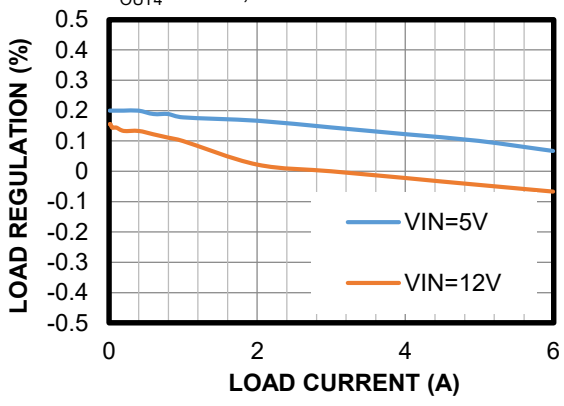
Load Regulation

V_{OUT3} = 0.9V, PFM mode



Load Regulation

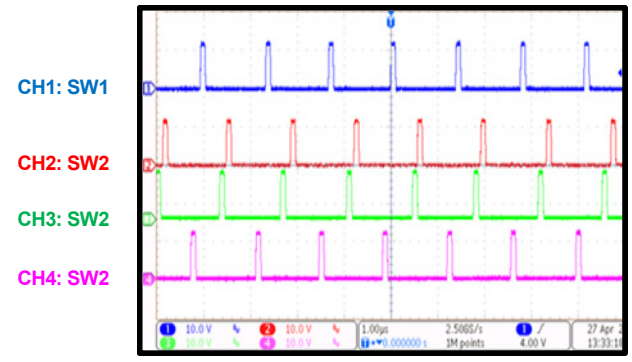
V_{OUT4} = 0.9V, PFM mode



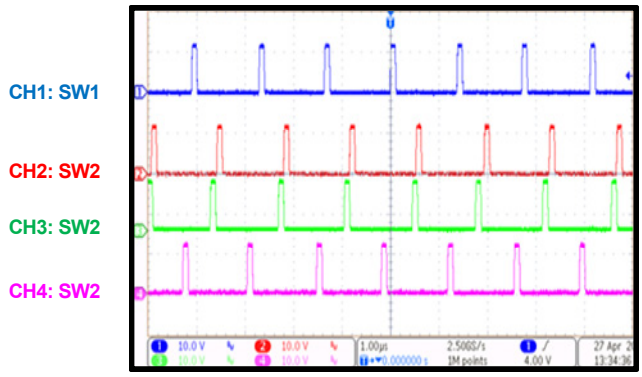
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

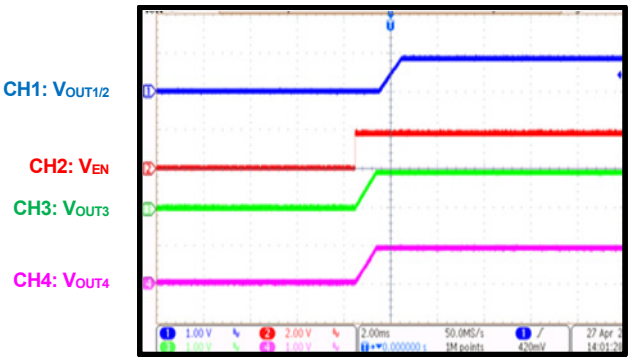
Steady State
Each buck channel with half load



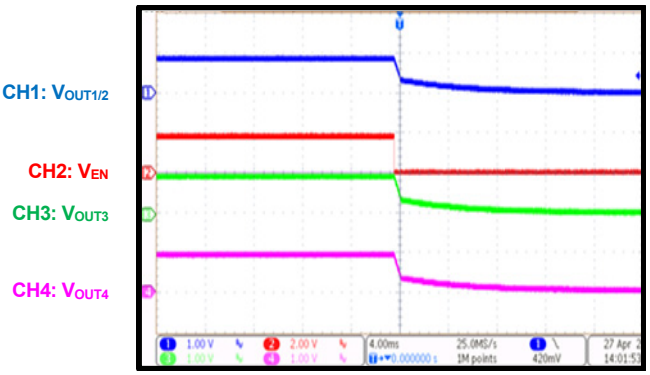
Steady State
Each buck channel with full load



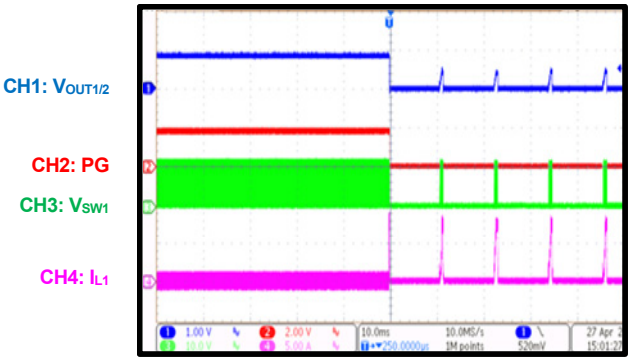
Start-Up through EN
Each buck channel without load



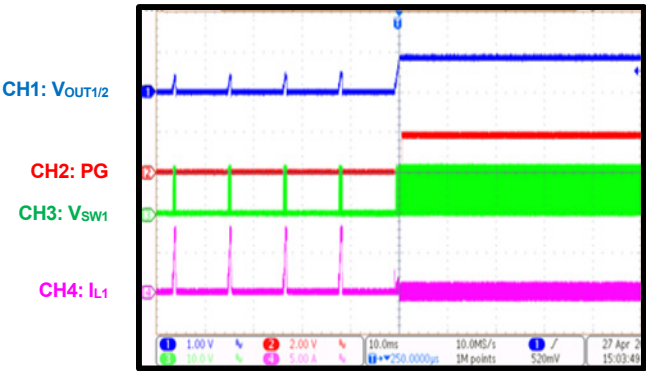
Shutdown through EN
Each buck channel without load



SCP Entry
Buck 1/2 output is 0.86V, I_{OUT} = 0A



SCP Recovery
Buck 1/2 output is 0.86V, I_{OUT} = 0A

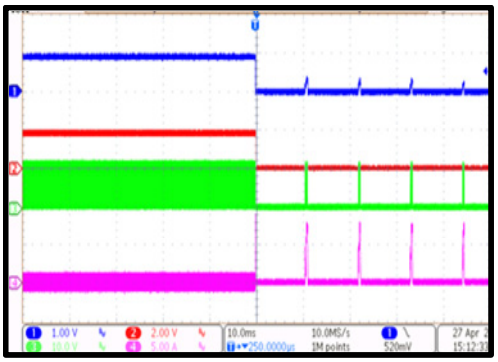


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

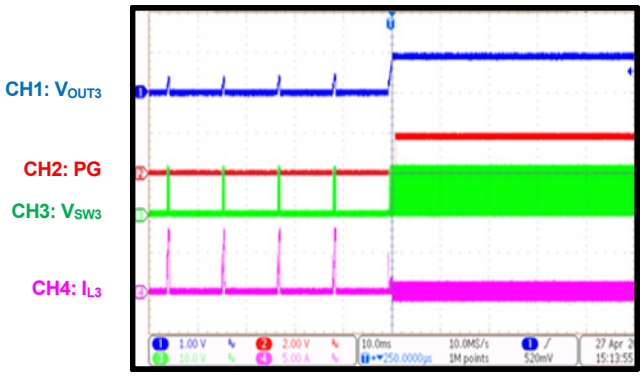
SCP Entry

Buck 3 output is 0.9V, I_{OUT} = 0A



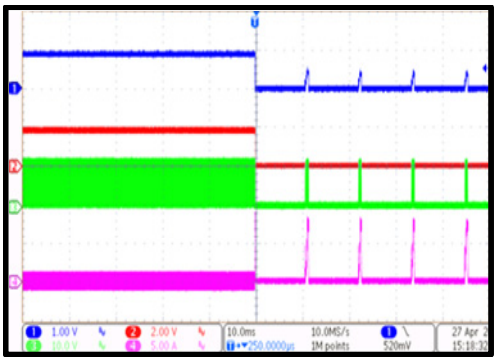
SCP Recovery

Buck 3 output is 0.9V, I_{OUT} = 0A



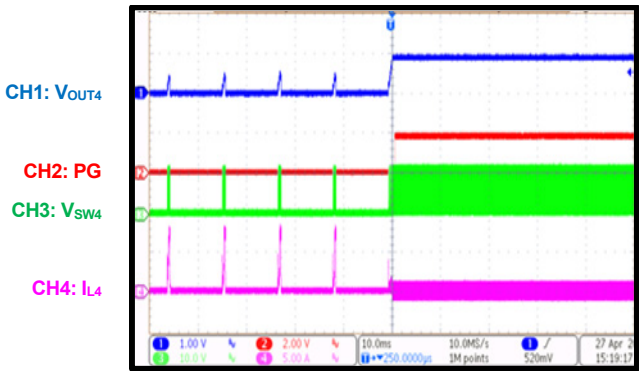
SCP Entry

Buck 4 output is 0.9V, I_{OUT} = 0A



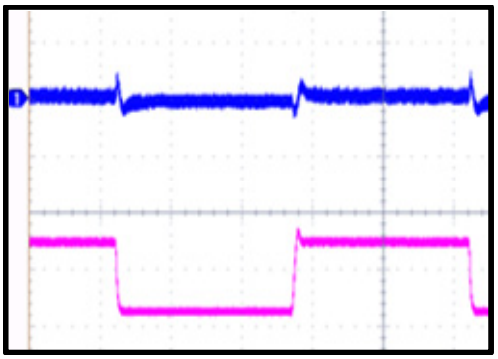
SCP Recovery

Buck 4 output is 0.9V, I_{OUT} = 0A



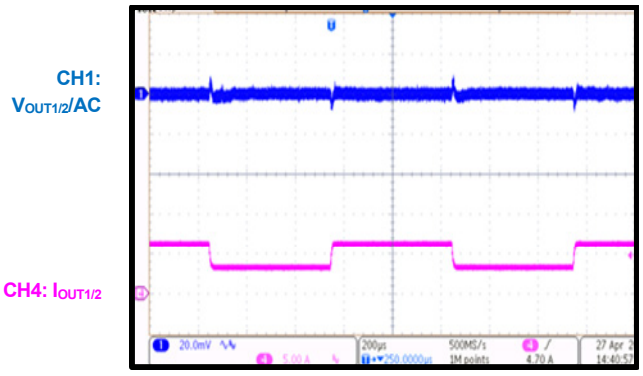
Load Transient

I_{OUT} = 6A to 12A,
slew rate = 2.5A/µs by e-load



Load Transient

I_{OUT} = 3A to 6A,
slew rate = 2.5A/µs by e-load



EVB TEST RESULTS *(continued)*

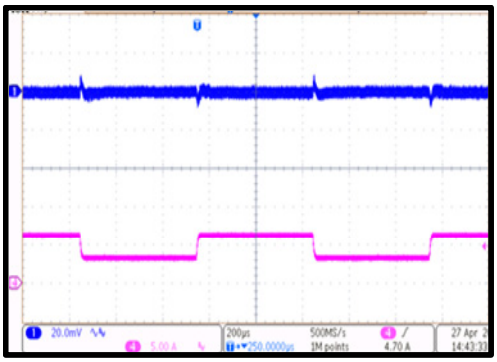
Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Load Transient

I_{OUT} = 3A to 6A, slew rate = 2.5A/μs by e-load

CH1: $V_{OUT1/2}$/AC

CH4: $I_{OUT1/2}$



PCB LAYOUT

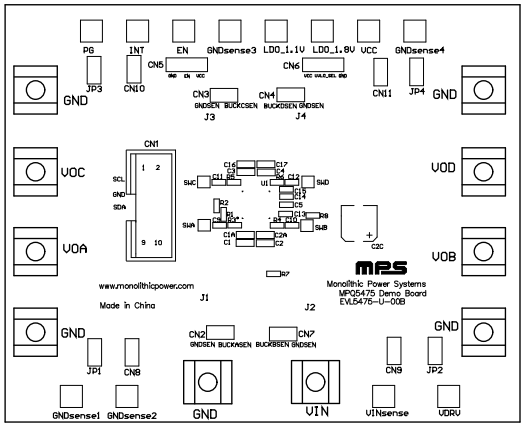


Figure 3: Top Silk

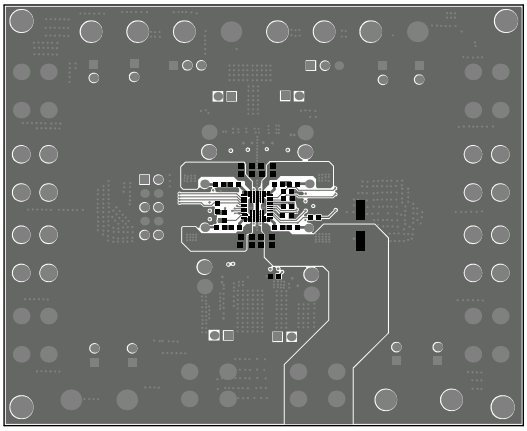


Figure 4: Top Layer

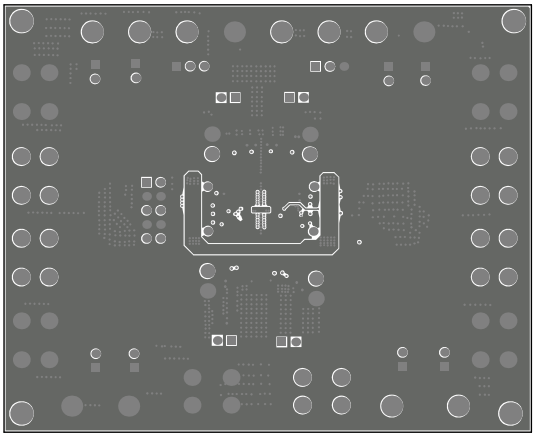


Figure 5: Mid-Layer 1

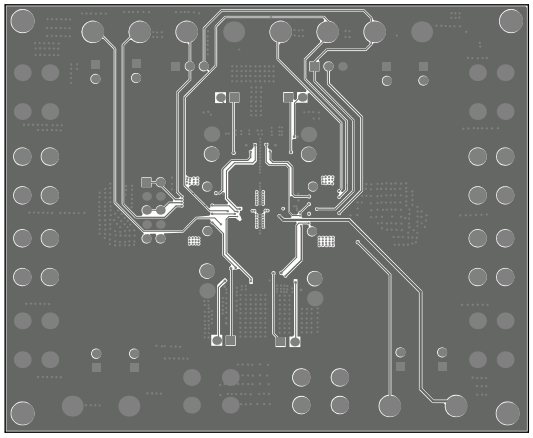


Figure 6: Mid-Layer 2

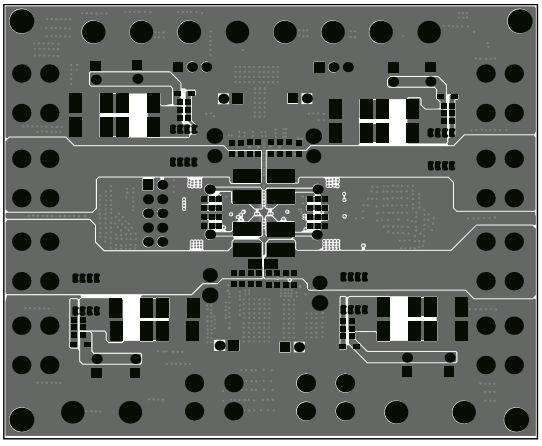


Figure 7: Bottom Layer

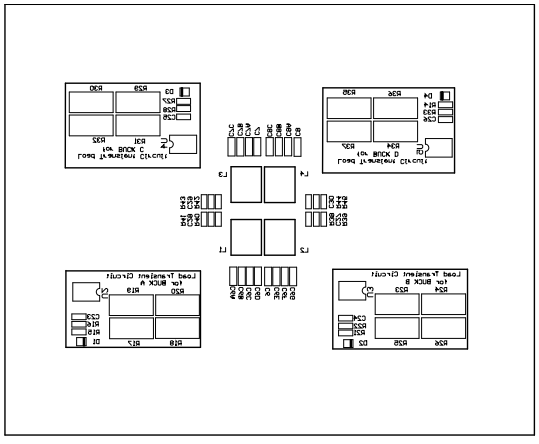


Figure 8: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/14/2021	Initial Release	-
1.1	4/3/2023	Added register information to step 8	2
		Changed the values of C5–C17, C6A–C6G, C7A-C7C, C8A-C8C, C27–C30, R3–R6, R8, R14–R16, R21, R22, R27, R28, R33; removed the optional values of L1, L2, L3, and L4	4
		Moved L1, L2, L3, and L4 to the top of the BOM; corrected the L1, L2, L3, and L4 note number; updated NC values to NS to match the schematic; added C5 row; added R8 reference	5