ECURIE PISTON SPORT AUTO

Liste des composants électronique Standard EPSA

Abaque

Departement BASTIE et CHAIPE

Auteurs :

Eymeric **Chauchat**

Versionnement :

V2 du 18 Octobre 2022 (ECT) : Forme Finale V2. ★★★★☆

V1.5 du 17 Octobre 2022 (ECT) : Finalisation de la liste de composants. ★★★☆☆

V1.0 du 2 Octobre 2022 (ECT) : Rédaction initiale. ★☆☆☆☆

25 octobre 2022- V2

ÉCOLE CENTRALE LYON

Table des matières

1 Introduction **3**

2 Résistance **3**
2.1 Résistance à usage générale 3
2.2 Résistance variable (triming Potentiometer) 3

3 Condensateurs **3**

4 Timer et dérivée 555 **4**

5 Comparateur de Tension **4**
5.1 Comparateur Simple 4
5.2 Comparateur double 4

6 Alimentation Régulé **4**
6.1 Alimentation abaisseur de tension 5
6.2 Alimentation d'isolation 5

7 Porte Logique **5**

8 Opto-coupleur **5**

9 Bascule D **6**

10 Diode **6**

11 Mosfet **6**

12 Annexes **6**
12.1 Liste de tous les composants 6
12.2 Taille CMS 7
12.3 Datasheet Resistance Générale 8
12.4 Datasheet Resistance Variable 14
12.5 Datasheet Condensateur 16
12.6 555 Datasheet 17
12.6.1 Typical 555 Application 22
12.7 Comparateur TS391 Datasheet 24
12.7.1 Schematic Diagram 25
12.8 Comparateur double LM393LV-Q1 Datasheet 31
12.9 Alimentation Isolé Datasheet 60
12.10 Alimentation Datasheet 63
12.11 Porte Logique 69
12.11.1 Porte And Datasheet 69
12.11.2 Porte Or Datasheet 79
12.11.3 Porte NAnd Datasheet 89

12.11.4 Porte NOr Datasheet 100
12.11.5 Porte XOr Datasheet 104
12.12 Solid State Relay Datasheet 116
12.13 Bascule D Datasheet 121
12.14 Diode Datasheet 135
12.15 NMOS Datasheet 139
12.16 PMOS Datasheet 142

1 Introduction

Lors de la création de cartes électroniques au sein de l'EPSA uniquement une liste de composants standard est autorisé (hormis dérogation pour carte spécifique). Cette liste doit être actualisée chaque année par le Directeur du département BASTIE.

Cette démarche permet de simplifier grandement la logistique concernant les cartes électroniques et permet d'avoir une politique long terme des cartes électroniques. Aucun achat d'un composant supplémentaire sans avoir concerté le directeur technique, le directeur BASTIE et le directeur Chaipe ne sera toléré. Cette liste permet de restreindre le nombre de boitier de composant

2 Résistance

A l'EPSA nous avons avoir l'usage de deux types de résistances : les résistances à valeur fixe et les résistances variable. Les résistance variables sont faite pour rajouter un réglage sur une carte (capteur de tension etc).

2.1 Résistance à usage générale

Toutes les résistances proviennent du cahier de résistance MP003365 de la marque MultiComp. Les résistances sont des CMS de la taille 1206 et les valeurs permises sont celle trouvables dans le tableau des résistances. Leur tension nominal est de 200V et sont conçues pour un quart de Watt, **Attention alors quand on design une carte pour les capteurs haute tension**

2.2 Résistance variable (triming Potentiometer)

Nous utiliserons les Trimming Potentiometer BOURNS 3296Y (Y est la forme du boitier). Elles ont 25 tours de réglages nominale, 0.5W nominal et 250V nominal. La valeur des résistances disponibles est la suivante :

— 200 Ω
— 20 k Ω
— 200 k Ω
— 1 M Ω

Plus spécifiquement ces potentiomètres permettent de faire instantanément un pont diviseur de tension en utilisant les deux côtés de la résistance.

3 Condensateurs

Tous les condensateurs proviennent de la boite de condensateur 885070 de chez Wurth Elektronik. Les condensateur sont des CMS de la taille 0805 et les valeurs permises sont celle trouvable dans le tableau des condensateur

4 Timer et dérivée 555

Pour permettre de compter le temps ou de créer des circuits clignotants nous utilisons à l'EPSA la puce 555 (de ses noms complets NE555,SE555 ou LM555) en version CMS (Composants montée en surface). Les variantes des composants 555 sont interchangeables entre eux et prennent tous la même place sur carte. On peut retrouver en annexe Les deux applications standards du circuit 555 (permettant de générer une horloge (Astable) ou une pulse de durée minimal fixé (Monostable)).

L'encapsulation choisi est SOIC-8. La référence complète choisi cette année est LM555CMX/NOPB.

5 Comparateur de Tension

Nous allons utilisé deux références de comparateurs de tension différentes : les comparateurs simple et les comparateurs double. Les comparateurs simple permettent de comparer une tension par rapport à une autre. Les doubles peuvent servir d'encadrer une tension ou d'exclure une plage de tension .

Les comparateurs possèdent des sorties à collecteur ouvert il faut donc utiliser une résistance de tirage a la sortie pour obtenir une tension à la sortie.

5.1 Comparateur Simple

Nous utilisons les comparateurs de tension TS391 de STelectronics. Ce sont principalement ce qu'on peut appeler des amplis opérationnels.

Ils existent en deux configurations : ILT (la version IYLT possède uniquement une coque vérifiant d'autre norme) et RILT (R pour Right) nous avons choisi la ILT. Nous pouvons retrouver en annexe le schéma de câblage des comparateurs

L'encapsulation utilisé comme pour les portes logiques est le SOT23-5.

5.2 Comparateur double

Nous utilisons les comparateurs à deux entrées LM393LV-Q1 de chez Texas instrument. Ils fonctionnent comme les comparateurs simple sauf qu'il y en a deux dans le même boitier.

L'encapsulation utilisé est le format SOIC-8

6 Alimentation Régulé

Une des parties principales d'un circuit (qu'il ne faut jamais négliger) est son alimentation. Nous avons besoin à l'EPSA d'une alimentation 12V-5V et

d'une alimentation d'isolation 5V-5V (pour permettre l'isolation galvanique du circuit). Nous avons choisi dans les deux cas d'utiliser des alimentations à découplage. Elles sont plus chère que des alimentations linéaires (qui "brulent" la tension en trop) mais permettent de gagner des points sur l'épreuve de Design et de vider moins les batteries.

6.1 Alimentation abaisseur de tension

Nous avons choisi d'utiliser deux alimentations différentes la TSR 2-2450 et la TSR 0.5-2450 de chez Traco Power . Les deux possèdent le même encombrement sur les cartes mais l'une possède un courant nominal de sortie de 2A et l'autre de 0.5A. (question de prix)

6.2 Alimentation d'isolation

L'alimentation d'isolation 5V-5V qui a été choisi est la PDME2-S5-S5-S5 de chez CUI INC. Elle possède une isolation galvanique de 1.5kV (EV 4.3.6). L'utilisation de cette isolation est très simple il suffit de lui fournir une tension en entrée et elle fournit une tension en sortie. Des Condensateurs peuvent être rajouté en entrée et en sorti pour stabiliser encore plus les sources de tensions (voir le schéma de branchement de l'alimentation isolé)

7 Porte Logique

Pour fabriquer des cartes à l'EPSA nous devons utiliser des portes logiques (AND, OR , XOR et NOT). Elles sont encapsulé dans le format SOT23-5. Contrairement au comparateur elle ne sont pas en sortie à collecteur ouverte. Dans ce cas lier deux outputs de porte logique ensemble créera un cour-circuit.

Nous avons choisi les portes logiques SN74AHCT1G de chez Texas instrument.

Voici la liste complète des références :

- AND : SN74AHCT1G08DBVR
- OR : SN74AHCT1G32DBVR
- NAND : SN74AHCT1G00DBVR
- NOR : SN74AHCT1G02DBVR
- XOR : SN74AHCT1G86DBVR

8 Opto-coupleur

Pour permettre le transport isolé galvaniquement d'une information, nous utilisons des opto-coupleurs (coupleur optique) aussi appelé des solid state relay (SSR). Nous avons choisi les CPC1394 de chez IXYS, ils permettent une isolation galvanique de 5kV, une commutation de 600V et une intensité de com-

mutation aux alentours de 4mA. Nous pouvons ainsi les utiliser en sortie de porte logique.

L'encapsulation est en DIP-4.

9 Bascule D

La bascule D nous permet de créer des verrous sur nos cartes (la plupart du temps une protection qui s'installe lors d'une erreur et qui s'enlève uniquement après le redémarrage total du système). Nous avons choisi la puce SN74HCS72QDRQ1 de chez Texas Instruments. C'est une bascule D assez volumineuse mais qui possède des fonctionnalités qui simplifie son utilisation dans notre contexte.

10 Diode

Nous avons besoin de diode au sein de nos cartes électroniques. Nous avons choisi une diode classique bloquante dans un sens. Elle nous permet d'écrêter des signaux et d'éviter les branchements inverses (mais il est préférable d'utiliser un NMOS). Nous avons choisi la diode RFN1VWM2STF de chez ROHM Semiconductor. Elle a la taille d'une capacité, laisse passer au maximum 1A et bloque une tension de 200V maximum.

11 Mosfet

Les mosfet sont des interrupteurs asservis électriquement. Ils nous permettent dans nos montages de commander l'allumage d'une led, d'une partie d'un circuit ou de prévenir les branchement inverse. Le mosfet de type N est le SQ2348ES de chez Vishay et le mosfet de type P est le Si2343CDS de chez Vishay. Les deux mosfets ont un courant continue de ligne de 4A et de 30V. Leur résistance interne à 10V est de 50 m Ωpermettant une chute de tension négligeable pour nos applications .

L'encapsulation est en SOT-23.

12 Annexes

12.1 Liste de tous les composants

Voici la liste de tout les composants électroniques utilisable cette année à l'EPSA :

Fonction	Référence	Boitier	Prix unitaire	Stock recommandé
Résistance	MP003365		197,33 €	1
200 ΩTrim	3296Y-1-201LF	3296Y	2,43 €	10
20 kΩTrim	3296Y-1-203LF	3296Y	2,38 €	10
200 kΩTrim	3296Y-1-204LF	3296Y	2,43 €	10
1 MΩTrim	3296Y-1-105LF	3296Y	2,43 €	10
Condensateur	885070		178,72 €	1
Timer 555	LM555CMX/NOPB	SOIC-8	1,19 €	10
Comparateur Simple	TS391ILT	SOT-23-5	0,87 €	20
Comparateur Double	LM393LVQDRQ1	SOIC-8	0,62 €	10
Alimentation HP	TSR 2-2450	SIP-3	11,10 €	2
Alimentation LP	TSR 0.5-2450	DIP-10	5,20 €	2
Alimentation Isolé	PDM2-S5-S5-S		5,97 €	2
Porte ET	SN74AHCT1G08DBVR	SOT-23-5	0,49 €	10
Porte OU	SN74AHCT1G32DBVR	SOT-23-5	0,40 €	10
Porte NAND	SN74AHCT1G00DBVR	SOT-23-5	0,40 €	10
Porte NOR	SN74AHCT1G02DBVR	SOT-23-5	0,40 €	10
Porte XOR	SN74AHCT1G86DBVR	SOT-23-5	0,54 €	10
SSR	CPC1394GRTR	SMD DIP-4	2,36 €	10
Bascule D	SN74HCS72QDRQ1	SOIC-14	0,65 €	10
Diode	RFN1VWM2STF	PMDE-2	0,68 €	10
NMOS	SQ2348ES-T1$_BE3$	SOT-23-5	0,70 €	10
PMOS	SI2343CDS-T1-BE3	SOT-23-5	0,65 €	10

12.2 Taille CMS

Voici le tableau des tailles de CMS

Type	Longueur L	Largeur l	Hauteur H min-max	Métallisation M min-max
0402	1,00	0,50	0,50	
0603	1,60	0,80	0,80	
0805	2,00	1,25	0,6 ou 0,85 ou 1,25	0,25-0,75
1206	3,20	1,60	0,85 ou 1,15 ou 1,6	0,3-1,0
1210	3,20	2,50	1,15 ou 1,35 ou 1,8 ou 2,5	0,3-1,0
1812	4,50	3,20	2,0 max	0,3-1,0
2220	5,70	5,00	2,0 max	0,3-1,0

12.3 Datasheet Resistance Générale

Chip Resistor Kits

multicomp PRO

RoHS Compliant

1. Scope

This specification for approve relates to the Common Quality Lead-Free and Anti-Sulfurated Thick Film Chip Resistors. Used in automobile. The test items follow the test standard of AEC-Q200.

2. Type designation

The type designation shall be in the following form:

Type	Power Rating	Resistance tolerance	Nominal Resistance
0603	0.1W (1/10W)	F	10Ω

3. Ratings:

Type	0402	0603	0805	1206	1210	2010	2512
Power Rating	1/16W	1/10W	1/8W	1/4W	1/2W	3/4W	1W
Jumper Rated Current	1A	1A	2A	2A	2A	2A	2A
Max. Jumper Rated Current	2A	2A	5A	10A	10A	10A	10A
Max. Working Voltage	50V	75V	150V	200V	200V	200V	200V
Max. Overload Voltage	100V	150V	300V	400V	500V	500V	500V
Dielectric Withstanding Voltage	100V	300V	500V	500V	500V	500V	500V
Temperature Range	-55°C to +155°C						
Ambient Temperature	70°C						

3.1 Power rating:

Resistors shall have a power rating based on continuous load operation at an ambient temperature from -55°C to 70°C. For temperature in excess of 70°C, the load shall be derate as shown in figure 1

Figure 1

Newark.com/multicomp-pro
Farnell.com/multicomp-pro
Element14.com/multicomp-pro

multicomp PRO

Page <1>

02/04/20 V1.0

Chip Resistor Kits

multicomp PRO

3.2 Voltage rating:

Resistors shall have a rated direct-current (DC) continuous working voltage or an approximate sine-wave root-mean-square (RMS) alternating-current (AC) continuous working voltage at commercial line frequency and waveform corresponding to the power rating , as determined from the following formula:

$$RCWV = \sqrt{P \times R}$$

Were : RCWV = Rated DC or RMS AC continuous working voltage at commercial-line frequency and waveform (volt)
P = Power Rating (watt)
R = Nominal Resistance (ohm)

4. Construction :

5. Power rating and dimensions

Dimension

Type	Dimension (mm)				
	L	W	H	ℓ1	ℓ2
0402	1 ±0.1	0.5 ±0.05	0.35 ±0.05	0.2 ±0.1	0.25 ±0.1
0603	1.6 ±0.1	0.8+0.1	0.45 ±0.1	0.3 ±0.2	0.3 ±0.2
0805	2 ±0.15	1.25 +0.15 -0.1	0.55 ±0.1	0.4 ±0.2	0.4 ±0.2
1206	3.1 ±0.15	1.55 +0.15 -0.1	0.55 ±0.1	0.45 ±0.2	0.45 ±0.2
1210	3.1 ±0.1	2.6 ±0.2	0.55 ±0.1	0.5 ±0.25	0.5 ±0.2
2010	5 ±0.1	2.5 ±0.2	0.55 ±0.1	0.6 ±0.25	0.5 ±0.2
2512	6.35 ±0.1	3.2 ±0.2	0.55 ±0.1	0.6 ±0.25	0.5 ±0.2

Chip Resistor Kits

multicomp PRO

Power Rating :

Type	Power Rating at 70	Tolerance	Resistance Range	Standard Series
		Jumper	< 50mΩ	E-24
0402	1/16W	±1%	1Ω to 10MΩ	
0603	1/10W			
0805	1/8W			
1206	1/4W			
1210	1/2W			
2010	3/4W			
2512	1W			

6. Marking :

6.1 Resistors

A. Chip Resistors type 0402 No marking

B. Standard E-96 series values(±1% tolerance) of 0603 size. Due the small size of the resistor's body, 3 digits marking will be used to indicate the accurate resistance value by using the following multiplier & resistance code

Marking for CQ03 E-96 series, the resistance value that no have multiplier code indicate marking follow this:
The first two digits are significant figures of resistance and the third one denoted number of zeros and under line the marking letters.

Ex.

	122	

1.2KΩ

C. Marking for E-96 series in 0805, 1206, 1210, 2010 , 2512 size : 4 Digits
*The first 3 digits are significant figures of resistance and the 4th digit denotes number of zeros.

Ex.

	1003	

100KΩ

*For ohmic values below 100 Ω, letter"R" is for decimal point.

Ex.

	1R80	

1.8Ω

Chip Resistor Kits

multicomp PRO

7. Performance specification :

Characteristics	Limits	Test Methods
Load life	±1%: ±(1% +0.1Ω)Max.	125°C, 35% power, at RCWV or Max. Working Voltage whichever less,1,000 hours(1.5 hours "ON", 0.5hours"OFF"), Measurement at 24 ±2 hours after test conclusion. (MIL-STD-202 Method 108)
Temperature Coefficient	1Ω ≤ R ≤ 100Ω : ±200PPM/°C >10Ω : ±100PPM/°C	Measure between -55°C to +125°C
Short time overload	±1%: ±(1% +0.1Ω)Max.	2.5x Rated voltage or Max. Overload Voltage whichever is lower for 5 seconds, then check the resistance.
Terminal Bending	±(1% +0.05Ω)Max	Bending Distance 3mm, Duration: 60s ±5s, then check the resistance.
Solderability	95% coverage Min.	245 ±3°C; 2~3s
Soldering heat	±(1% +0.05Ω) Max	260 ±5°C; 10 ±1s
Biased Humidity	1%: ± (1% +0.05Ω) Max.	10% rated power, 85°C/85%RH, 1000Hr, Measurement at 24 hours after test conclusion. (MIL-STD-202 Method 103)
Dielectric withstanding voltage	No evidence of flashover, mechanical damage, arcing or insulation breakdown	Resistor shall be clamped in the trough of 90° metallic V-block and shall be tested at AC potential respectively specified in the given list of each product type for 60~70s.
Temperature cycling	1%: ± (0.5% +0.1Ω) Max.	-55 ±3°C 30min ~normal temperature 10min-15min~155 ±2°C 30min~normal temperature 10min-15min 100 cycles, Measurement at 24 hours after test conclusion. (JESD22 Method JA-104)
ESD	±(1% +0.05Ω) Max	With the electrometer in direct contact with the discharge tip, verify the voltage setting at levels of ±500V, ±1KV, ±2KV, ±4KV, ±8KV, The electrometer reading shall be within ±10% for voltages from 500V to ≤800V. (AEC-Q200-002)
Sulfuration test	1%: ± (1% +0.05Ω) Max.	H2S 3 to 5PPM 50°C±2°C 91% to 93% RH 1000H

8. Kit resistors :

8.1 Insert for Chip Kit

Dimension (mm)

Chip Resistor Kits

multicomp PRO

8.2 Album for Chip Kit

Dimension (mm)

Environment Related Substance

This product complies to EU RoHS directive, EU PAHs directive, EU PFOS directive and Halogen free.

Ozone layer depleting substances.

Ozone depleting substances are not used in our manufacturing process of this product.

This product is not manufactured using Chloro fluorocarbons (CFCs), Hydrochlorofluorocarbons (HCFCs), Hydrobromofluorocarbons (HBFCs) or other ozone depleting substances in any phase of the manufacturing process.

Storage Condition

The performance of these products, including the solderability, is guaranteed for a year from the date of arrival at your company, provided that they remain packed as they were when delivered and stored at a temperature of 25°C ± 10°C and a relative humidity of 60%RH ± 10%RH, chemical and dust free atmosphere

Even within the above guarantee periods, do not store these products in the following conditions.

Otherwise, their electrical performance and/or solderability may be deteriorated, and the packaging materials (e.g. taping materials) may be deformed or deteriorated, resulting in mounting failures.

1. In salty air or in air with a high concentration of corrosive gas, such as Cl_2, H_2S, NH_3, SO_2, or NO_2
2. In direct sunlight

Chip Resistor Kits

multicomp PRO

PRODUCT: 1206 Kit +/-1%
E24 Series = 99 values (0R & 1R to 1M)
(With 50 resistors 2 strip per value)
Total Qty: 9,900pcs.)

NO.	Value	NO.	Value	NO.	Value
1	0R	36	360E	71	13K
2	1R	37	390E	72	15K
3	2R2	38	430E	73	18K
4	3R	39	470E	74	22K
5	3R3	40	510E	75	24K
6	4R7	41	560E	76	27K
7	9R1	42	604E	77	33K
8	10R	43	620E	78	36K
9	12R	44	680E	79	39K
10	15R	45	750E	80	43K
11	18R	46	820E	81	47K
12	22R	47	910E	82	51K
13	27R	48	1K	83	56K
14	30R	49	1K1	84	68K
15	33R	50	1K2	85	82K
16	39R	51	1K3	86	100K
17	47R	52	1K5	87	120K
18	56R	53	1K6	88	150K
19	68R	54	1K8	89	180K
20	75R	55	2K	90	200K
21	82R	56	2K2	91	220K
22	91R	57	2K4	92	270K
23	100R	58	2K7	93	330K
24	120R	59	3K	94	390K
25	130R	60	3K3	95	470K
26	140R	61	3K6	96	560K
27	150R	62	3K9	97	680K
28	160R	63	4K7	98	820K
29	180R	64	5K6	99	1M
30	200R	65	6K8		
31	220R	66	7K5		
32	240R	67	8K2		
33	270R	68	10K		
34	300E	69	11K		
35	330E	70	12K		

Newark.com/multicomp-pro
Farnell.com/multicomp-pro
Element14.com/multicomp-pro

multicomp PRO

Page <9>

02/04/20 V1.0

12.4 Datasheet Resistance Variable

Features

- Multiturn / Cermet / Industrial / Sealed
- 5 terminal styles
- Tape and reel packaging available
- Chevron seal design
- Listed on the QPL for style RJ24 per MIL-R-22097 and RJR24 per High-Rel Mil-R-39035
- Mounting hardware available (H-117P)
- RoHS compliant* version available
- For trimmer applications/processing guidelines, click here

3296 - 3/8 ″ Square Trimpot® Trimming Potentiometer

Electrical Characteristics

Standard Resistance Range
.....10 ohms to 2 megohms
(see standard resistance table)
Resistance Tolerance ..... ±10 % std.
(tighter tolerance available)
Absolute Minimum Resistance
..... 1 % or 2 ohms max.
(whichever is greater)
Contact Resistance Variation
..... 1.0 % or 3 ohms max.
(whichever is greater)
Adjustability
Voltage ..... ±0.01 %
Resistance ..... ±0.05 %
Resolution ..... Infinite
Insulation Resistance ..... 500 vdc.
1,000 megohms min.
Dielectric Strength
Sea Level..... 900 vac
70,000 Feet ..... 350 vac
Effective Travel .....25 turns nom.

Environmental Characteristics

Power Rating (300 volts max.)
70 °C .....0.5 watt
125 °C .....0 watt
Temperature Range ... -55 °C to +125 °C
Temperature Coefficient ... ±100 ppm/°C
Seal Test .....85 °C Fluorinert†
Humidity .....MIL-STD-202 Method 103
96 hours
(2 % ΔTR, 10 Megohms IR)
Vibration ..... 20 G (1 % ΔTR; 1 % ΔVR)
Shock ..... 100 G (1 % ΔTR; 1 % ΔVR)
Load Life..1,000 hours 0.5 watt @ 70 °C
(3 % ΔTR; 3 % or 3 ohms,
whichever is greater, CRV)
Rotational Life .....200 cycles
(4 % ΔTR; 3 % or 3 ohms,
whichever is greater, CRV)
Moisture Sensitivity Level.....N/A
ESD Classification (HBM).....2

Physical Characteristics

Torque.....3.0 oz-in. max.
Mechanical Stops.....Wiper idles
Terminals .....Solderable pins
Weight .....0.03 oz.
Marking.....Manufacturer's trademark, resistance code, wiring diagram, date code, mfr's. model number and style
Wiper .....50 % (Actual TR) ±10 %
Flammability .....U.L. 94V-0
Standard Packaging.....50 pcs. per tube
Adjustment Tool.....H-90

WARNING Cancer and Reproductive Harm
www.P65Warnings.ca.gov

Product Dimensions

Common Dimensions

3296P

3296W

3296X

3296Y

3296Z

DIMENSIONS: MM (INCHES)

TOLERANCES: ± 0.25 (.010) EXCEPT WHERE NOTED

Standard Resistance Table

Resistance (Ohms)	Resistance Code
10	**100**
20	**200**
50	**500**
100	**101**
200	**201**
500	**501**
1,000	**102**
2,000	**202**
5,000	**502**
10,000	**103**
20,000	**203**
25,000	**253**
50,000	**503**
100,000	**104**
200,000	**204**
250,000	**254**
500,000	**504**
1,000,000	**105**
2,000,000	**205**

Popular values listed in boldface. Special resistances available.

*RoHS Directive 2015/863, Mar. 31, 2015 and Annex
"Trimpot" is a trademark of Bourns, Inc.
†"Fluorinert" is a registered trademark of 3M Co.

How To Order

3296 W - 1 - 103 __ LF

Model
Style
Standard or Modified
Product Indicator
-1 = Standard Product
Resistance Code
Packaging Designator
Blank = Tube (Standard)
R = Tape and Reel (X and W Pin Styles Only)
A = Ammo Pack (X and W Pin Styles Only)
Tape and reel material meets Antistatic ANSI/ESD 5541-2003 packaging standards.
Terminations
LF = 100 % Tin-plated (RoHS compliant)
Blank = 90 % Tin / 10 % Lead-plated (Standard)
Consult factory for other available options.

Specifications are subject to change without notice. Users should verify actual device performance in their specific applications. The products described herein and this document are subject to specific legal disclaimers as set forth on the last page of this document, and at www.bourns.com/docs/legal/disclaimer.pdf.

3296 - 3/8 ″ Square Trimpot® Trimming Potentiometer

BOURNS®

Packaging Specifications

SIDE ADJUST
3296X-1

TOP ADJUST
3296W-1

Meets EIA Specification 468.

BOURNS®

Asia-Pacific: Tel: +886-2 2562-4117 • Email: asiacus@bourns.com
Europe: Tel: +36 88 885 877 • Email: eurocus@bourns.com
The Americas: Tel: +1-951 781-5500 • Email: americus@bourns.com
www.bourns.com

REV. 08/19

Specifications are subject to change without notice. Users should verify actual device performance in their specific applications. The products described herein and this document are subject to specific legal disclaimers as set forth on the last page of this document, and at www.bourns.com/docs/legal/disclaimer.pdf.

12.5 Datasheet Condensateur

Les valeurs sont les suivantes :

1pF	1.5pF	2.2pF	3.3pF	4.7pF	6.8pF	10pF	15pF
22pF	33pF	47pF	68pF	100pF	150pF	150pF	220pF
330pF	470pF	680pF	1nF	1.5nF	2.2nF	3.3nF	4.7nF
6.8nF	10nF	15nF	22nF	33nF	47nF	68nF	100nF
150nF	220nF	330nF	470nF	680nF	1μF	2.2μF	3.3μF
4.7μF	10μF	22μF	47μF				

WCAP-CSGP
Multilayer Ceramic Chip Capacitors 0805

NP0

885012007009 10V	885012007044 25V	885012007052 50V	885012007060 50V
NP00805103J010DFCT10000	NP00805472J025DFCT10000	NP00805150J050DFCT10000	NP00805331J050DFCT10000
10,000pF, +/-5%, T=1.25mm Q>=1000, IR>=10G Ohm	4,700pF, +/-5%, T=1.25mm Q>=1000, IR>=10G Ohm	15pF, +/-5%, T=0.60mm Q>=400+20C, IR>=10G Ohm	330pF, +/-5%, T=0.60mm Q>=1000, IR>=10G Ohm
885012007037 25V	885012007045 50V	885012007053 50V	885012007061 50V
NP00805331J025DFCT10000	NP00805180D050DFCT10000	NP00805220J050DFCT10000	NP00805471J050DFCT10000
330pF, +/-5%, T=0.60mm Q>=1000, IR>=10G Ohm	1pF, +/-0.5pF, T=0.60mm Q>=400+20C, IR>=10G Ohm	22pF, +/-5%, T=0.60mm Q>=400+20C, IR>=10G Ohm	470pF, +/-5%, T=0.80mm Q>=1000, IR>=10G Ohm
885012007038 25V	885012007046 50V	885012007054 50V	885012007062 50V
NP00805471J025DFCT10000	NP00805180D050DFCT10000	NP00805330J050DFCT10000	NP00805681J050DFCT10000
470pF, +/-5%, T=0.80mm Q>=1000, IR>=10G Ohm	1.5pF, +/-0.5pF, T=0.60mm Q>=400+20C, IR>=10G Ohm	33pF, +/-5%, T=0.60mm Q>=1000, IR>=10G Ohm	680pF, +/-5%, T=0.80mm Q>=1000, IR>=10G Ohm
885012007039 25V	885012007047 50V	885012007055 50V	885012007063 50V
NP00805681J025DFCT10000	NP00805220D050DFCT10000	NP00805470J050DFCT10000	NP00805102J050DFCT10000
680pF, +/-5%, T=0.80mm Q>=1000, IR>=10G Ohm	2.2pF, +/-0.5pF, T=0.60mm Q>=400+20C, IR>=10G Ohm	47pF, +/-5%, T=0.60mm Q>=1000, IR>=10G Ohm	1,000pF, +/-5%, T=0.80mm Q>=1000, IR>=10G Ohm
885012007040 25V	885012007048 50V	885012007056 50V	885012007064 50V
NP00805102J025DFCT10000	NP00805330D050DFCT10000	NP00805680J050DFCT10000	NP00805152J050DFCT10000
1,000pF, +/-5%, T=0.80mm Q>=1000, IR>=10G Ohm	3.3pF, +/-0.5pF, T=0.60mm Q>=400+20C, IR>=10G Ohm	68pF, +/-5%, T=0.60mm Q>=1000, IR>=10G Ohm	1,500pF, +/-5%, T=0.80mm Q>=1000, IR>=10G Ohm
885012007041 25V	885012007049 50V	885012007057 50V	885012007065 50V
NP00805152J025DFCT10000	NP00805470D050DFCT10000	NP00805101J050DFCT10000	NP00805222J050DFCT10000
1,500pF, +/-5%, T=0.80mm Q>=1000, IR>=10G Ohm	4.7pF, +/-0.5pF, T=0.60mm Q>=400+20C, IR>=10G Ohm	100pF, +/-5%, T=0.60mm Q>=1000, IR>=10G Ohm	2,200pF, +/-5%, T=0.80mm Q>=1000, IR>=10G Ohm
885012007042 25V	885012007050 50V	885012007058 50V	885012007066 50V
NP00805222J025DFCT10000	NP00805680D050DFCT10000	NP00805151J050DFCT10000	NP00805332J050DFCT10000
2,200pF, +/-5%, T=0.80mm Q>=1000, IR>=10G Ohm	6.8pF, +/-0.5pF, T=0.60mm Q>=400+20C, IR>=10G Ohm	150pF, +/-5%, T=0.60mm Q>=1000, IR>=10G Ohm	3,300pF, +/-5%, T=1.25mm Q>=1000, IR>=10G Ohm
885012007043 25V	885012007051 50V	885012007059 50V	885012007067 50V
NP00805332J025DFCT10000	NP00805100J050DFCT10000	NP00805221J050DFCT10000	NP00805472J050DFCT10000
3,300pF, +/-5%, T=1.25mm Q>=1000, IR>=10G Ohm	10pF, +/-5%, T=0.60mm Q>=400+20C, IR>=10G Ohm	220pF, +/-5%, T=0.60mm Q>=1000, IR>=10G Ohm	4,700pF, +/-5%, T=1.25mm Q>=1000, IR>=10G Ohm

X7R

885012207026 10V	885012207080 50V	885012207088 50V	885012207096 50V	
X7R0805106K010DFCT10000	X7R0805101K050DFCT10000	X7R0805222K050DFCT10000	X7R0805473K050DFCT10000	
10µF, +/-10%, T=1.25mm DF=<10%, IR>=0.01G Ohm	100pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	2,200pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	47,000pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	
885012207053 16V	885012207081 50V	885012207089 50V	885012207097 50V	
X7R0805475K016DFCT10000	X7R0805151K050DFCT10000	X7R0805332K050DFCT10000	X7R0805683K050DFCT10000	
4.7µF, +/-10%, T=1.25mm DF=<10%, IR>=0.02G Ohm	150pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	3,300pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	68,000pF, +/-10%, T=0.80mm DF=<2.5%, IR>=7.4G Ohm	
885012207074 25V	885012207082 50V	885012207090 50V	885012207098 50V	
X7R0805224K025DFCT10000	X7R0805221K050DFCT10000	X7R0805472K050DFCT10000	X7R0805104K050DFCT10000	
220,000pF, +/-10%, T=1.25mm DF=<3.5%, IR>=2.3G Ohm	220pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	4,700pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	100,000pF, +/-10%, T=0.80mm DF=<2.5%, IR>=5G Ohm	
885012207075 25V	885012207083 50V	885012207091 50V	885012207099 50V	
X7R0805334K025DFCT10000	X7R0805331K050DFCT10000	X7R0805682K050DFCT10000	X7R0805154K050DFCT10000	
330,000pF, +/-10%, T=1.25mm DF=<3.5%, IR>=1.5G Ohm	330pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	6,800pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	150,000pF, +/-10%, T=1.25mm DF=<2.5%, IR>=3.3G Ohm	
885012207076 25V	885012207084 50V	885012207092 50V	885012207100 50V	
X7R0805474K025DFCT10000	X7R0805471K050DFCT10000	X7R0805103K050DFCT10000	X7R0805224K050DFCT10000	
470,000pF, +/-10%, T=1.25mm DF=<3.5%, IR>=1.1G Ohm	470pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	10,000pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	220,000pF, +/-10%, T=1.25mm DF=<3%, IR>=2.3G Ohm	
885012207077 25V	885012207085 50V	885012207093 50V	885012207101 50V	
X7R0805684K025DFCT10000	X7R0805681K050DFCT10000	X7R0805153K050DFCT10000	X7R0805334K050DFCT10000	
680,000pF, +/-10%, T=1.25mm DF=<3.5%, IR>=0.7G Ohm	680pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	15,000pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	330,000pF, +/-10%, T=1.25mm DF=<3%, IR>=1.5G Ohm	
885012207078 25V	885012207086 50V	885012207094 50V	885012207102 50V	
X7R0805105K025DFCT10000	X7R0805102K050DFCT10000	X7R0805223K050DFCT10000	X7R0805474K050DFCT10000	
1µF, +/-10%, T=1.25mm DF=<5%, IR>=0.5G Ohm	1,000pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	22,000pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	470,000pF, +/-10%, T=1.25mm DF=<3%, IR>=1.1G Ohm	
885012207079 25V	885012207087 50V	885012207095 50V	885012207103 50V	
X7R0805225K025DFCT10000	X7R0805152K050DFCT10000	X7R0805333K050DFCT10000	X7R0805105K050DFCT10000	
2.2µF, +/-10%, T=1.25mm DF=<10%, IR>=0.05G Ohm	1,500pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	33,000pF, +/-10%, T=0.80mm DF=<2.5%, IR>=10G Ohm	1µF, +/-10%, T=1.25mm DF=<10%, IR>=0.1G Ohm	

X5R

885012107006 6.3V
X5R0805476M6R3DFCT10000
47µF, +/-20%, T=1.25mm DF=<15%, IR>=0.002G Ohm
885012107011 10V
X5R0805226M010DFCT10000
22µF, +/-20%, T=1.25mm DF=<10%, IR>=0.005G Ohm
885012107013 16V
X5R0805475M016DFCT10000
4.7µF, +/-20%, T=1.25mm DF=<10%, IR>=0.02G Ohm
885012107014 16V
X5R0805106M016DFCT10000
10µF, +/-20%, T=1.25mm DF=<10%, IR>=0.01G Ohm
885012107015 25V
X5R0805105M025DFCT10000
1µF, +/-20%, T=1.25mm DF=<5%, IR>=0.5G Ohm
885012107016 25V
X5R0805225M025DFCT10000
2.2µF, +/-20%, T=1.25mm DF=<10%, IR>=0.05G Ohm
885012107017 25V
X5R0805335M025DFCT10000
3.3µF, +/-20%, T=1.25mm DF=<10%, IR>=0.03G Ohm
885012107018 25V
X5R0805475M025DFCT10000
4.7µF, +/-20%, T=1.25mm DF=<10%, IR>=0.02G Ohm

Dielectric	Operating Temperature
NP0	-55°C to +125°C
X7R	-55°C to +125°C
X5R	-55°C to +85°C

Dielectric	Capacitance Characteristics*
NP0	± 30ppm/°C; ± 0.54%/°C
X7R	± 15%
X5R	± 15%

*within Operating Temperature Range

6.3V
10V
16V
25V
50V

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

EMC COMPONENTS | INDUCTORS | TRANSFORMERS | RF COMPONENTS | CIRCUIT PROTECTION | EMC SHIELDING MATERIAL | **CAPACITORS** | CONNECTORS | SWITCHES | ASSEMBLY TECHNIQUE | POWER ELEMENTS

Important information: Würth Elektronik's design kits contain reference components. These components correspond with the current product development status on the day of supply. Exchange of the reference components to components with up-to-date product development status is not carried out automatically. No liability is taken for the use of these reference components. Therefore, please request new samples prior to releases for series production and product release.

All products ex stock!

Please check datasheets on www.we-online.com for specifications. Würth Elektronik eiSos GmbH & Co. KG, EMC & Inductive Solutions. © 2014

www.we-online.com

12.6 555 Datasheet

Timer — NE/SA/SE555/SE555C

DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

FEATURES

- Turn-off time less than 2µs
- Max. operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

PIN CONFIGURATIONS

APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE555D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE555N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA555N	0404B
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA555D	0174C
8-Pin Hermetic Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CFE	
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555CN	0404B
14-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555N	0405B
8-Pin Hermetic Cerdip	-55°C to +125°C	SE555FE	
14-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CF	0581B

BLOCK DIAGRAM

EQUIVALENT SCHEMATIC

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	SE555	+18	V
	NE555, SE555C, SA555	+16	V
P_D	Maximum allowable power dissipation[1]	600	mW
T_A	Operating ambient temperature range		
	NE555	0 to +70	°C
	SA555	-40 to +85	°C
	SE555, SE555C	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

1. The junction temperature must be kept below 125°C for the D package and below 150°C for the FE, N and F packages. At ambient temperatures above 25°C, where this limit would be derated by the following factors:
   D package 160°C/W
   FE package 150°C/W
   N package 100°C/W
   F package 105°C/W

DC AND AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	V_{CC}=5V, R_L=∞		3	5		3	6	mA
		V_{CC}=15V, R_L=∞		10	12		10	15	mA
	Timing error (monostable)	R_A=2kΩ to 100kΩ							
t_M	Initial accuracy[2]	C=0.1µF		0.5	2.0		1.0	3.0	%
$\Delta t_M/\Delta T$	Drift with temperature			30	100		50	150	ppm/°C
$\Delta t_M/\Delta V_S$	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
	Timing error (astable)	R_A, R_B=1kΩ to 100kΩ							
t_A	Initial accuracy[2]	C=0.1µF		4	6		5	13	%
$\Delta t_A/\Delta T$	Drift with temperature	V_{CC}=15V			500			500	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.15	0.6		0.3	1	%/V
V_C	Control voltage level	V_{CC}=15V	9.6	10.0	10.4	9.0	10.0	11.0	V
		V_{CC}=5V	2.9	3.33	3.8	2.6	3.33	4.0	V
V_{TH}	Threshold voltage	V_{CC}=15V	9.4	10.0	10.6	8.8	10.0	11.2	V
		V_{CC}=5V	2.7	3.33	4.0	2.4	3.33	4.2	V
I_{TH}	Threshold current[3]			0.1	0.25		0.1	0.25	µA
V_{TRIG}	Trigger voltage	V_{CC}=15V	4.8	5.0	5.2	4.5	5.0	5.6	V
		V_{CC}=5V	1.45	1.67	1.9	1.1	1.67	2.2	V
I_{TRIG}	Trigger current	V_{TRIG}=0V		0.5	0.9		0.5	2.0	µA
V_{RESET}	Reset voltage[4]	V_{CC}=15V, V_{TH} =10.5V	0.3		1.0	0.3		1.0	V
I_{RESET}	Reset current	V_{RESET}=0.4V		0.1	0.4		0.1	0.4	mA
	Reset current	V_{RESET}=0V		0.4	1.0		0.4	1.5	mA
V_{OL}	Output voltage (low)	V_{CC}=15V							
		I_{SINK}=10mA		0.1	0.15		0.1	0.25	V
		I_{SINK}=50mA		0.4	0.5		0.4	0.75	V
		I_{SINK}=100mA		2.0	2.2		2.0	2.5	V
		I_{SINK}=200mA		2.5			2.5		V
		V_{CC}=5V							
		I_{SINK}=8mA		0.1	0.25		0.3	0.4	V
		I_{SINK}=5mA		0.05	0.2		0.25	0.35	V
V_{OH}	Output voltage (high)	V_{CC}=15V							
		I_{SOURCE}=200mA		12.5			12.5		V
		I_{SOURCE}=100mA	13.0	13.3		12.75	13.3		V
		V_{CC}=5V							
		I_{SOURCE}=100mA	3.0	3.3		2.75	3.3		V
t_{OFF}	Turn-off time[5]	V_{RESET}=V_{CC}		0.5	2.0		0.5	2.0	µs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

NOTES:
1. Supply current when output high typically 1mA less.
2. Tested at V_{CC}=5V and V_{CC}=15V.
3. This will determine the max value of R_A+R_B, for 15V operation, the max total R=10MΩ, and for 5V operation, the max. total R=3.4MΩ.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to 0.8×V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS

12.6.1 Typical 555 Application

TYPICAL APPLICATIONS

Astable Operation

Monostable Operation

TYPICAL APPLICATIONS

Figure 1. AC Coupling of the Trigger Pulse

Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 1, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bi-stable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the “turn-off time”. This is the measurement of the amount of time required after the threshold reaches 2/3 V_{CC} to turn the output low. To explain further, Q_1 at the threshold input turns on after reaching 2/3 V_{CC}, which then turns on Q_5, which turns on Q_6. Current from Q_6 turns on Q_{16} which turns Q_{17} off. This allows current from Q_{19} to turn on Q_{20} and Q_{24} to given an output low. These steps cause the 2µs max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low, Q_{10} is on and turns on Q_{11} which turns on Q_{15}. Q_{15} turns off Q_{16} and allows Q_{17} to turn on. This turns off current to Q_{20} and Q_{24}, which results in output high. When the trigger is released, Q_{10} and Q_{11} shut off, Q_{15} turns off, Q_{16} turns on and the circuit then follows the same path and time delay explained as “turn off time”. This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.

12.7 Comparateur TS391 Datasheet

TS391

Low-power single voltage comparator

Datasheet — production data

Features

- Wide single supply voltage range or dual supplies +2 V to +36 V or ±1 V to ±18 V
- Very low supply current (0.2 mA) independent of supply voltage (1 mW/comparator at +5 V)
- Low input bias current: 25 nA typ.
- Low input offset current: ±5 nA typ.
- Low input offset voltage: ±1 mV typ.
- Input common-mode voltage range includes ground
- Low output saturation voltage: 250 mV typ. (I_o = 4 mA)
- Differential input voltage range equal to the supply voltage
- TTL, DTL, ECL, CMOS compatible outputs

L
SOT23-5
(Plastic package)

Q2
DFN8 2x2 mm
(Plastic micropackage)

Description

This device consists of a low-power voltage comparator designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

This comparator also has a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

March 2012 Doc ID 6324 Rev 6 1/12

This is information on a product in full production. www.st.com

12.7.1 Schematic Diagram

1 Schematic diagram

Figure 1. Schematic diagram

Figure 2. Pin connections (top view)

2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	±18 or 36	V
V_{id}	Differential input voltage	±36	V
V_i	Input voltage	-0.3 to +36	V
	Output short-circuit to ground(1)	Infinite	
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient(2) SOT23-5 DFN8 2x2	 250 57	°C/W
T_{stg}	Storage temperature range	-65 to +150	°C
ESD	Human body model (HBM)(3)	1500	V
	Machine model (MM)(4)	100	
	Charged device model (CDM)(5)	1000	

1. Short-circuits from the output to V_{CC}^+ can cause excessive heating and potential destruction. The maximum output current is approximately 20 mA independent of the magnitude of V_{CC}^+.
2. Short-circuits can cause excessive heating. These values are typical.
3. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
4. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
5. Charged device model: all pins and package are charged together to the specified voltage and then discharged directly to ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2 to 36 or ±1 to ±18	V
V_{icm}	Input common mode voltage range (1) T_{amb} = 25°C $T_{min} \leq T_{amb} \leq T_{max}$	 0 to V_{CC}^+ -1.5 0 to V_{CC}^+ -2	V
T_{oper}	Operating free-air temperature range	-40 to +125	°C

1. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC}^+ –1.5 V, but either or both inputs can go to +30 V without damage.

3 Electrical characteristics

Table 3. V_{CC}^+ = +5 V, V_{CC}^- = 0 V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (1)	$T_{min} \le T_{amb} \le T_{max}$		1	5 9	mV
I_{io}	Input offset current	$T_{min} \le T_{amb} \le T_{max}$		5	50 150	nA
I_{ib}	Input bias current (2)	$T_{min} \le T_{amb} \le T_{max}$		25	250 400	nA
A_{vd}	Large signal voltage gain	V_{CC}^+ = 15V, R_L = 15kΩ, V_o = 1 to 11V	50	200		V/mV
I_{CC}	Supply current	V_{CC}^+ = 5V, no load V_{CC}^+ = 30V, no load		0.2 0.5	0.5 1.25	mA
V_{id}	Differential input voltage (3)				V_{CC}^+	V
I_{sink}	Output sink current	V_{id} = -1V, V_O = 1.5V	6	16		mA
V_{OL}	Low level output voltage	V_{id} = 1V, V_{CC}^+ = V_O = 30V		250	400 700	mV
I_{OH}	High level output current	V_{id} = 1V, V_{CC}^+ = V_O = 30V		0.1	 1	nA µA
tre	Small signal response time	R_L = 5.1kΩ to V_{CC}^+ (4)		1.3		µs
t_{rel}	Large signal response time	V_i = TTL, V_{ref} = +1.4V, R_L = 5.1kΩ to V_{CC}^+		300		ns

1. At output switch point, $V_O \approx$ 1.4V, R_S = 0Ω with V_{CC}^+ from 5V to 30V and over the full input common-mode range (0 V to V_{CC}^+ -1.5 V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so there is no loading charge on the reference or input lines.
3. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than –0.3 V (or 0.3 V below the negative power supply, if used).
4. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals, 300 ns can be obtained.

Figure 3. Supply current vs. supply voltage

Figure 4. Response time for various input overdrives - negative transition

Figure 5. Input current vs. supply voltage

Figure 6. Response time for various input overdrives - positive transition

Figure 7. Output saturation voltage vs. output current

4.2 SOT23-5L package mechanical data

Figure 10. SOT23-5L package mechanical drawing

Table 5. SOT23-5L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.013	0.015	0.019
C	0.09	0.15	0.20	0.003	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.013	0.023
K	0 degrees		10 degrees			

5 Ordering information

Table 6. Order codes

Part number	Temperature range	Package	Packaging	Marking
TS391ILT	-40°C, +125°C	SOT23-5L	Tape & reel	K511
TS391IYLT (1)		SOT23-5L (Automotive grade)		K510
TS391RILT		SOT23-5L		K509
TS391IQ2T		DFN8 2x2		K5D

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

12.8 Comparateur double LM393LV-Q1 Datasheet

Ordering & quality | Technical documentation | Design & development | Support & training

TEXAS INSTRUMENTS

LM393LV-Q1, LM339LV-Q1
SNOSDB3C – JUNE 2020 – REVISED JANUARY 2022

LM393LV-Q1 Dual and LM339LV-Q1 Quad Low Voltage, RRI Automotive Comparators

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C5
- 1.65 V to 5.5 V supply range
- Rail-to-Rail input with Failsafe
- Low input offset voltage 400 µV typical
- 600ns typical propagation delay
- Low quiescent current 25 µA/Ch typical
- Low input bias current 5 pA typical
- Open-drain output
- Full -40°C to +125°C temperature range
- Power-On-Reset (POR) for known start-up
- 2 kV ESD protection
- Improved replacement for LM393-Q1 & LM339-Q1 family for V_{CC} ≤ 5 V.

2 Applications

- Vacuum robot
- Single phase UPS
- Server PSU
- Cordless power tool
- Wireless infrastructure
- Appliances
- Building automation
- Factory automation & control
- Motor drives
- Infotainment & cluster

3 Description

The LV device family consists of two (LM393LV-Q1), or four (LM339LV-Q1), independent voltage comparators that are designed to operate from a wide range of supply voltages. The LV devices can drop-in replace the standard LM2xx, LM3xx and LM290x-Q1 comparator family in low voltage (≤ 5 V) applications for improved performance and added features.

The LV devices include a Power-On-Reset (POR) feature that ensures the output is in a High-Z state until the minimum supply voltage has been reached. This prevents output transients during system power-up and power-down.

These comparators also feature Rail to Rail inputs and no output phase inversion with inputs that can go up to 6V without damage. This makes this family of comparators well suited for precision voltage monitoring in harsh, noisy environments.

The LV devices are specified for the temperature range of -40°C to +125°C, which covers the temperature ranges of all the LM2xx, LM3xx and LM290x-Q1 comparator families.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
LM393LV-Q1 (Dual)	SOIC (8)	3.91 mm × 4.90 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	WSON (8)	2.00 mm × 2.00 mm
	SOT-23 (8)	1.60 mm × 2.90 mm
LM339LV-Q1 (Quad)	SOIC (14) (Preview)	3.91 mm × 8.65 mm
	TSSOP (14)	4.40 mm × 5.00 mm
	SOT-23 (14) (Preview)	4.20 mm x 2.00 mm
	WQFN (16) (Preview)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Pin Configuration and Functions....3
5.1 Pin Functions: LM393LV-Q1....3
Pin Functions: LM339LV-Q1....4
6 Specifications....5
6.1 Absolute Maximum Ratings....5
6.2 ESD Ratings....5
6.3 Recommended Operating Conditions....5
6.4 Thermal Information, LM393LV-Q1....6
6.5 Thermal Information, LM339LV-Q1....6
6.6 Electrical Characteristics, LM393LV-Q1....7
6.7 Switching Characteristics, LM393LV-Q1....8
6.8 Electrical Characteristics, LM339LV-Q1....9
6.9 Switching Characteristics, LM339LV-Q1....10
6.10 Typical Characteristics....11
7 Detailed Description....16
7.1 Overview....16
7.2 Functional Block Diagram....16
7.3 Feature Description....16
7.4 Device Functional Modes....16
8 Application and Implementation....19
8.1 Application Information....19
8.2 Typical Applications....22
9 Power Supply Recommendations....30
10 Layout....30
10.1 Layout Guidelines....30
10.2 Layout Example....30
11 Device and Documentation Support....31
11.1 Related Documentation....31
11.2 Receiving Notification of Documentation Updates....31
11.3 Support Resources....31
11.4 Trademarks....31
11.5 Electrostatic Discharge Caution....31
11.6 Glossary....31
12 Mechanical, Packaging, and Orderable Information....31

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2021) to Revision C (January 2022)	Page
• Changed LM393LV-Q1 dual package staus	1

Changes from Revision A (December 2020) to Revision B (July 2021)	Page
• Changed LM393LV-Q1 TSSOP package staus	1

Copyright © 2022 Texas Instruments Incorporated

5 Pin Configuration and Functions

Figure 5-1. D, DGK, PW, DDF Packages
8-Pin SOIC, VSSOP, TSSOP, SOT-23-8
Top View

NOTE: Connect exposed thermal pad directly to GND pin.

Figure 5-2. DSG Package
8-Pad WSON With Exposed Thermal Pad
Top View

5.1 Pin Functions: LM393LV-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	Output	Output pin of the comparator 1
IN1–	2	Input	Inverting input pin of comparator 1
IN1+	3	Input	Noninverting input pin of comparator 1
GND	4	—	Negative supply
IN2+	5	Input	Noninverting input pin of comparator 2
IN2–	6	Input	Inverting input pin of comparator 2
OUT2	7	Output	Output pin of the comparator 2
V+	8	—	Positive supply
Thermal Pad	—	—	Connect directly to GND pin

Copyright © 2022 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (GND)	–0.3	6	V
Input pins (IN+, IN–) from GND	–0.3	6	V
Current into Input pins (IN+, IN–)	–10	10	mA
Output (OUT) from GND	–0.3	6	V
Output short circuit duration		10	s
Junction temperature, T_J		150	°C
Storage temperature, Tstg	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), , per AEC Q100-002[1]	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-0111	±1000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (GND)	1.65	5.5	V
Input voltage range (IN+, IN–) from (GND)	–0.1	5.6	V
Ambient temperature, T_A	–40	125	°C

Copyright © 2022 Texas Instruments Incorporated

6.4 Thermal Information, LM393LV-Q1

THERMAL METRIC [1]		LM393LV-Q1					UNIT
		D (SOIC)	PW (TSSOP)	DGK (VSSOP)	DSG (WSON)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	167.7	221.7	215.8	175.2	240.0	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	107.0	109.1	105.2	178.1	151.0	°C/W
R_{qJB}	Junction-to-board thermal resistance	111.2	152.5	137.5	139.5	157.0	°C/W
y_{JT}	Junction-to-top characterization parameter	53.1	36.4	39.6	47.2	32.8	°C/W
y_{JB}	Junction-to-board characterization parameter	110.4	150.7	135.9	138.9	155.4	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	127.3	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information, LM339LV-Q1

THERMAL METRIC[1]		LM339LV-Q1				UNIT
		D (SOIC)	PW (TSSOP)	RTE (WQFN)	DYY (SOT-23)	
		14 PINS	14 PINS	16 PINS	14 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	136.0	155.0	134.1	–	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	91.2	82.0	122.6	–	°C/W
R_{qJB}	Junction-to-board thermal resistance	92.0	98.5	109.3	–	°C/W
y_{JT}	Junction-to-top characterization parameter	46.9	25.7	30.9	–	°C/W
y_{JB}	Junction-to-board characterization parameter	91.6	97.6	108.3	–	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	98.7	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Copyright © 2022 Texas Instruments Incorporated

6.6 Electrical Characteristics, LM393LV-Q1

For V_S (Total Supply Voltage) = (V+) – (GND) = 5 V, V_{CM} = (GND) at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 V	–2	±0.4	2	mV
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	–3		3	mV
dV_{IO}/dT	Input offset voltage drift	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C		±1.5		µV/°C
POWER SUPPLY						
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low		25	35	µA
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low, T_A = –40°C to +125°C			50	µA
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C	70	80		dB
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2		5		pA
I_{OS}	Input offset current	V_{CM} = V_S/2		1		pA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential	V_{CM} = V_S/2		2		pF
C_{IC}	Input Capacitance, Common Mode	V_{CM} = V_S/2		3		pF
INPUT VOLTAGE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	(GND)		(V+)	V
CMRR	Common-mode rejection ratio	V_S = 5 V, (GND) < V_{CM} < (V+), T_A = –40°C to +125°C	60	65		dB
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (GND) < V_{CM} < (V+), T_A = –40°C to +125°C	50	60		dB
OPEN-LOOP GAIN						
A_{VD}	Large signal gain		50	200		V/mV
OUTPUT						
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4 mA, T_A = 25°C		150	200	mV
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4 mA, T_A = –40°C to +125°C			300	mV
I_{LKG}	Open-drain output leakage current	V_{PULLUP} = (V+), T_A = 25°C		100		pA
I_{SC}	Short-circuit current	V_S = 5 V, Sinking	60	100		mA

Copyright © 2022 Texas Instruments Incorporated

6.7 Switching Characteristics, LM393LV-Q1

For V_S (Total Supply Voltage) = (V+) – (GND) = 5 V, V_{CM} = V_S / 2, C_L = 15 pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-HL}	Propagation delay time, high-to-low	V_{ID} = –10 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ)		600		ns
T_{PD-LH}	Propagation delay time, low-to-high	V_{ID} = 10 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ)		600		ns
T_{FALL}	5V Output Fall Time, 80% to 20%	V_{ID} = –100 mV		20		ns
F_{TOGGLE}	5V, Toggle Frequency	V_{ID} = 100 mV (R_P = 2.5 KΩ)		1		MHz
POWER ON TIME						
P_{ON}	Power on-time	V_S = 1.8 V and 5 V, V_{CM} = (GND) , V_{ID} = –0.1 V, $V_{PULL-UP}$ = V_S / 2, Delay from V_S / 2 to V_{OUT} = 0.1 x V_S / 2 (R_P = 2.5 KΩ)		50		µs

Copyright © 2022 Texas Instruments Incorporated

6.8 Electrical Characteristics, LM339LV-Q1

For V_S (Total Supply Voltage) = (V+) – (GND) = 5 V, V_{CM} = (GND) at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 V	–2	±0.4	2	mV
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	–3		3	mV
dV_{IO}/dT	Input offset voltage drift	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C		±1.5		μV/°C
POWER SUPPLY						
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low		25	35	μA
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low, T_A = –40°C to +125°C			50	μA
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C	70	80		dB
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2		5		pA
I_{OS}	Input offset current	V_{CM} = V_S/2		1		pA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential	V_{CM} = V_S/2		2		pF
C_{IC}	Input Capacitance, Common Mode	V_{CM} = V_S/2		3		pF
INPUT VOLTAGE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	(GND)		(V+)	V
CMRR	Common-mode rejection ratio	V_S = 5 V, (GND) < V_{CM} < (V+), T_A = –40°C to +125°C	60	65		dB
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (GND) < V_{CM} < (V+), T_A = –40°C to +125°C	50	60		dB
OPEN-LOOP GAIN						
A_{VD}	Large signal gain		50	200		V/mV
OUTPUT						
V_{OL}	Voltage swing from (GND)	I_{SINK} = 4 mA, T_A = 25°C		150	200	mV
V_{OL}	Voltage swing from (GND)	I_{SINK} = 4 mA, T_A = –40°C to +125°C			300	mV
I_{LKG}	Open-drain output leakage current	V_{PULLUP} = (V+), T_A = 25°C		100		pA
I_{SC}	Short-circuit current	V_S = 5 V, Sinking	60	125		mA

Copyright © 2022 Texas Instruments Incorporated

6.9 Switching Characteristics, LM339LV-Q1

For V_S (Total Supply Voltage) = (V+) – (GND) = 5 V, V_{CM} = V_S / 2, C_L = 15 pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-HL}	Propagation delay time, high-to-low	V_{ID} = –10 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ)		600		ns
T_{PD-LH}	Propagation delay time, low-to-high	V_{ID} = 10 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ)		600		ns
T_{FALL}	5V Output Fall Time, 80% to 20%	V_{ID} = –100 mV		20		ns
F_{TOGGLE}	5V, Toggle Frequency	V_{ID} = 100 mV (R_P = 2.5 KΩ)		1		MHz
POWER ON TIME						
P_{ON}	Power on-time	V_S = 1.8 V and 5 V, V_{CM} = (GND) , V_{ID} = –0.1 V, $V_{PULL-UP}$ = V_S / 2, Delay from V_S / 2 to V_{OUT} = 0.1 x V_S / 2 (R_P = 2.5 KΩ)		50		µs

Copyright © 2022 Texas Instruments Incorporated

6.10 Typical Characteristics

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = GND, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

Figure 6-1. Supply Current vs. Supply Voltage

Figure 6-2. Supply Current vs. Temperature

Figure 6-3. Supply Current vs. Input Voltage, 1.8V

Figure 6-4. Supply Current vs. Input Voltage, 3.3V

Figure 6-5. Supply Current vs. Input Voltage, 5V

Figure 6-6. Input Bias Current vs. Temperature

Copyright © 2022 Texas Instruments Incorporated

6.10 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = GND, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

Figure 6-7. Output Sinking Current vs. Output Voltage, 1.8V

Figure 6-8. Output Sinking Current vs. Output Voltage, 3.3V

Figure 6-9. Output Sinking Current vs. Output Voltage, 5V

Figure 6-10. Sinking Short Circuit Current vs. Temperature

Figure 6-11. Risetime vs. Capacitive Load

Figure 6-12. Falltime vs. Capacitive Load

Copyright © 2022 Texas Instruments Incorporated

6.10 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = GND, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

Figure 6-13. Propagation Delay, High to Low, 1.8V

Figure 6-14. Propagation Delay, Low to High, 1.8V

Figure 6-15. Propagation Delay, High to Low, 3.3V

Figure 6-16. Propagation Delay, Low to High, 3.3V

Figure 6-17. Propagation Delay, High to Low, 5V

Figure 6-18. Propagation Delay, Low to High, 5V

Copyright © 2022 Texas Instruments Incorporated

6.10 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = GND, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

Figure 6-19. Offset Voltage vs. Input Votlage at 125°C, 1.8V

Figure 6-20. Offset Voltage vs. Input Votlage at 125°C, 5V

Figure 6-21. Offset Voltage vs. Input Votlage at 25°C, 1.8V

Figure 6-22. Offset Voltage vs. Input Votlage at 25°C, 5V

Figure 6-23. Offset Voltage vs. Input Votlage at -40°C, 1.8V

Figure 6-24. Offset Voltage vs. Input Votlage at -40°C, 5V

Copyright © 2022 Texas Instruments Incorporated

6.10 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = GND, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

Figure 6-25. Offset Voltage vs. Supply Voltage at 125°C, VIN=V+

Figure 6-26. Offset Voltage vs. Supply Voltage at 125°C, VIN=0V

Figure 6-27. Offset Voltage vs. Supply Voltage at 25°C, VIN=V+

Figure 6-28. Offset Voltage vs. Supply Voltage at 25°C, VIN=0V

Figure 6-29. Offset Voltage vs. Supply Voltage at -40°C, VIN=V+

Figure 6-30. Offset Voltage vs. Supply Voltage at -40°C, VIN=0V

Copyright © 2022 Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The LV Family devices are micro-power comparators with open-drain outputs and improved input offset voltage that operate down to 1.65 V while only consuming only 25 µA per channel. The LV family are ideally suited for portable, automotive and industrial applications. An internal power-on reset circuit ensures that the output remains in a known state during power-up and power-down while fail-safe inputs can tolerate input transients without damage or false outputs.

7.2 Functional Block Diagram

7.3 Feature Description

The LV family devices are micro-power comparators that have low input offset voltages and are capable of operating at low voltages. The LV family feature a rail-to-rail input stage capable of operating up to 100 mV beyond the power supply rails. The comparators also feature an open-drain output stage options with Power On Reset for known start-up conditions.

7.4 Device Functional Modes

7.4.1 Open Drain Output

The LV family features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0 V up to 5.5 V, independent of the comparator supply voltage (V+). The open-drain output also allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower pull-up resistor values will help increase the rising edge risetime, but at the expense of increasing V_{OL} and higher power dissipation. The risetime will be dependant on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 MΩ) will create an exponential rising edge due to the RC time constant and increase the risetime.

Unused open drain outputs should be left floating, or can be tied to the GND pin if floating pins are not allowed. While an individual output can typically sink up to 100 mA, the total combined current for all channels must be less than 200 mA.

Copyright © 2022 Texas Instruments Incorporated

7.4.2 Power-On-Reset (POR)

The LV family has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry will be activated for up to 30µs after the minimum supply voltage threshold of 1.5V is crossed, or immediately when the supply voltage drops below 1.5V. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

The POR circuit will keep the output high impedance (HI-Z) during the POR period (t_{on}).

Figure 7-1. Power-On-Reset Timing Diagram

Note that it is the nature of an open collector output that the output will rise with the pull-up voltage during the POR period.

A light pull-up (to V+) or pull-down (to GND) resistor can be used to pre-bias the output condition to prevent the output from floating.

7.4.3 Inputs

7.4.3.1 Rail to Rail Input

The LV family input voltage range extends from 100mV below GND to 100 mV above V+. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output will occur when the input pins exceed V+ or GND.

7.4.3.2 Fault Tolerant Inputs

The LV family inputs are fault tolerant up to 5.5V independent of V+. Fault tolerant is defined as maintaining the same high input impedance when V+ is unpowered or within the recommended operating ranges.

The fault tolerant inputs can be any value between 0 V and 5.5 V, even while V+ is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the specified ranges. This is possible since the inputs are not clamped to V+ and the input current maintains its value even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input range, and the supply voltage is valid and not in POR, the output state will be correct.

The following is a summary of input voltage excursions and their outcomes:

1. When both IN- and IN+ are within the specified input voltage range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low.
   b. If IN- is lower than IN+ and the offset voltage, the output is high.
2. When IN- is outside the specified input voltage range and IN+ is within the specified voltage range, the output is low.
3. When IN+ is higher than the specified input voltage range and IN- is within the specified input voltage range, the output is high
4. When IN- and IN+ are both outside the specified input voltage range, the output is **indeterminate** (random). *Do not* operate in this region.

Even with the fault tolerant feature, TI *strongly* recommends keeping the inputs within the specified input voltage range during normal system operation to maintain datasheet specifications. Operating outside the specified input range can cause changes in specifications such as propagation delay, which can lead to unpredictable behavior.

Copyright © 2022 Texas Instruments Incorporated

7.4.3.3 Input Protection

The input bias current is typically 5 pA for input voltages between V+ and GND. The comparator inputs are protected from reverse voltage by the internal ESD diodes connected to GND. As the input voltage goes under GND, or above the input Absolute Maximum ratings the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles for each 10°C temperature increase.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents should the clamps conduct. The current should be limited 10 mA or less. This series resistance can be part of any resistive input dividers or networks.

7.4.4 ESD Protection

The LV family incorporates internal ESD protection circuits on all pins. The inputs, and the open-drain output, use a proprietary "snapback" type ESD clamp from each pin to GND, which allows the pins to exceed the supply voltage (V+). While shown as Zener diodes, snapbacks momentarily "short" and go low impedance (like an SCR) when the threshold is exceeded, as opposed to clamping to a defined voltage like a Zener. There is no ESD clamp from the inputs to V+.

The open-drain output protection also consists of a ESD clamp between the output and GND to allow the output to be pulled above V+ to a maximum of 5.5V. There is no ESD clamp from the output to V+.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents should the clamps conduct. The current should be limited 10 mA or less. This series resistance can be part of any resistive input dividers or networks.

TI does not specify the performance of the ESD clamps and external clamping diodes should be added if the inputs or output could exceed the maximum ratings as part of normal operation.

7.4.5 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs should be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even V+ (as long as the input is directly connected to the V+ pin to avoid transients).

7.4.6 Hysteresis

The LV family does not have internal hysteresis. Due to the wide effective bandwidth and low input offset voltage, it is possible for the output to "chatter" (oscillate) when the absolute differential voltage near zero, as the comparator triggers on it's own internal wideband noise. TI recommends that the user add external hysteresis if slow moving signals are expected. See Section 8.1.2 in the following section.

Copyright © 2022 Texas Instruments Incorporated

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Basic Comparator Definitions

8.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Figure 8-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Table 8-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 8-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

8.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in Figure 8-1 and is measured from the mid-point of the input to the midpoint of the output.

Figure 8-1. Comparator Timing Diagram

8.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the Figure 8-1 example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, it is recommended to apply the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

8.1.2 Hysteresis

The basic comparator configuration may oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in Figure 8-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

Figure 8-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

8.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 8-3.

Figure 8-3. Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 8-3. Note that R_{PU} should be considered in series with R3 when the output is high. R_{PU} should be at least 10x less than R3.

Copyright © 2022 Texas Instruments Incorporated

Figure 8-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown in Figure 8-4.

Equation 1 below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in Equation 2.

Use Equation 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

Equation 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

8.1.2.2 Non-Inverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in Figure 8-5,

Figure 8-5. Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 8-6 Note that R_{PU} should be considered in series with R2 when the output is high. R_{PU} should be at least 10x less than R2.

Copyright © 2022 Texas Instruments Incorporated

Figure 8-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than $V_{REF,}$, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use Equation 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use Equation 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

8.2 Typical Applications

8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 8-7 shows a simple window comparator circuit. Window comparators require open drain outputs if the outputs are directly connected together.

Figure 8-7. Window Comparator

Copyright © 2022 Texas Instruments Incorporated

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 8-7. Connect V_{CC} to a 3.3-V power supply and V_{EE} to ground. Make R1, R2 and R3 each 10-MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and V_{TH-}).

With each resistor being equal, V_{TH+} is 2.2 V and V_{TH-} is 1.1 V. Large resistor values such as 10-MΩ are used to minimize power consumption. The resistor values may be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs will be low when the sensor is less than 1.1 V or greater than 2.2 V. The respective comparator outputs will be high when the sensor is in the range of 1.1 V to 2.2 V (within the "window"), as shown in Figure 8-8.

8.2.1.3 Application Curve

Figure 8-8. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

8.2.2 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source.

Figure 8-9. Square-Wave Oscillator

Copyright © 2022 Texas Instruments Incorporated

8.2.2.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor C_1 and resistor R_4. The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help to reduce BOM cost and board space. R4 should be over several kilo-ohms to minimize loading the output.

8.2.2.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

Figure 8-10. Square-Wave Oscillator Timing Thresholds

First consider the output of Figure Figure 8-9 as high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at the point is calculated by Equation 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \| R_3} \tag{7}$$

if $R_1 = R_2 = R_3$, then $V_{A1} = 2\ V_{CC}/\ 3$

At this time the comparator output trips pulling down the output to the negative rail. The value of $V_A$at this point is calculated by Equation 8.

$$V_{A2} = \frac{V_{CC}(R_2 \| R_3)}{R_1 + R_2 \| R_3} \tag{8}$$

if $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until it reaches V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for C_1 from $2V_{CC}/3$ to V_{CC} / 3 then back to $2V_{CC}/3$, which is given by $R_4C_1 \times \ln 2$ for each trip. Therefore, the total time duration is calculated as $2\ R_4C_1 \times \ln 2$.

The oscillation frequency can be obtained by Equation 9:

$$f = 1/(2\ R4 \times C1 \times \ln 2) \tag{9}$$

8.2.2.3 Application Curve

Figure 8-11 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
- $C_1 = 100$ pF, $C_L = 20$ pF
- V+ = 5 V, V– = GND

Copyright © 2022 Texas Instruments Incorporated

- C_{stray} (not shown) from V_A TO GND = 10 pF

Figure 8-11. Square-Wave Oscillator Output Waveform

8.2.3 Adjustable Pulse Width Generator

Figure 8-12 is a variation on the square wave oscillator that allows adjusting the pulse widths.

R_4 and R_5 provide separate charge and discharge paths for the capacitor C depending on the output state.

Figure 8-12. Adjustable Pulse Width Generator

The charge path is set through R_5 and D_2 when the output is high. Similarly, the discharge path for the capacitor is set by R_4 and D_1 when the output is low.

The pulse width t_1 is determined by the RC time constant of R_5 and C. Thus, the time t_2 between the pulses can be changed by varying R_4, and the pulse width can be altered by R_5. The frequency of the output can be changed by varying both R_4 and R_5. At low voltages, the effects of the diode forward drop (0.8 V, or 0.15 V for Shottky) must be taken into account by altering output high and low voltages in the calculations. R_{PU} should be at least 10x less than the smallest value of R4 or R5.

8.2.4 Time Delay Generator

The circuit shown in Figure 8-13 provides output signals at a prescribed time interval from a time reference and automatically resets the output low when the input returns to 0V. This is useful for sequencing a "power on" signal to trigger a controlled start-up of power supplies.

Copyright © 2022 Texas Instruments Incorporated

Figure 8-13. Time Delay Generator

Consider the case of V_{IN} = 0. The output of comparator 4 is also at ground, "shorting" the capacitor and holding it at 0V. This implies that the outputs of comparators 1, 2, and 3 are also at 0V. When an input signal is applied, the output of open drain comparator 4 goes High-Z and C charges exponentially through R. This is indicated in the graph. The output voltages of comparators 1, 2, and 3 switch to the high state in sequence when V_C rises above the reference voltages V_1, V_2 and V_3. A small amount of hysteresis has been provided by the 10 kΩ and 10 MΩ resistors to insure fast switching when the RC time constant is chosen to give long delay times. A good starting point is R = 100 kΩ and C = 0.01 µF to 1 µF.

All outputs will immediately go low when V_{IN} falls to 0V, due to the comparator output going low and immediately discharging the capacitor.

Comparator 4 must be a open-drain type output (TLV902x), whereas comparators 1 though 3 may be either open drain or push-pull output, depending on system requirements. R_{PU} is not required for push-pull output devices.

8.2.5 Logic Level Shifter

The output is the uncommitted drain of the output transistor. Many open-drain outputs can be tied together to provide an output OR'ing function if desired.

Figure 8-14. Universal Logic Level Shifter

Copyright © 2022 Texas Instruments Incorporated

The two 10 kΩ resistors bias the input to half of the input logic supply level to set the threshold in the mid-point of the input logic levels. Only one shared output pull-up resistor is needed and may be connected to any pull-up voltage between 0 V and 5.5 V. The pullup voltage should match the driven logic input "high" level.

8.2.6 One-Shot Multivibrator

Figure 8-15. One-Shot Multivibrator

A monostable multivibrator has one stable state in which it can remain indefinitely. It can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of C_2 and R_4. The resistor divider of R_1 and R_2 can be used to determine the magnitude of the input trigger pulse. The output will change state when $V_1 < V_2$. Diode D_2 provides a rapid discharge path for capacitor C_2 to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

8.2.7 Bi-Stable Multivibrator

Figure 8-16. Bi-Stable Multivibrator

A bi-stable multivibrator has two stable states. The reference voltage is set up by the voltage divider of R_2 and R_3. A pulse applied to the SET terminal will switch the output of the comparator high. The resistor divider of R_1, R_4, and R_5 now clamps the non-inverting input to a voltage greater than the reference voltage. A pulse applied to RESET will now toggle the output low.

Copyright © 2022 Texas Instruments Incorporated

8.2.8 Zero Crossing Detector

Figure 8-17. Zero Crossing Detector

A voltage divider of R_4 and R_5 establishes a reference voltage V_1 at the non-inverting input. By making the series resistance of R_1 and R_2 equal to R_5, the comparator will switch when V_{IN} = 0. Diode D_1 insures that V_3 clamps near ground. The voltage divider of R_2 and R_3 then prevents V_2 from going below ground. A small amount of hysteresis is setup to ensure rapid output voltage transitions.

Copyright © 2022 Texas Instruments Incorporated

8.2.9 Pulse Slicer

A Pulse Slicer is a variation of the Zero Crossing Detector and is used to detect the zero crossings on an input signal with a varying baseline level. This circuit works best with symmetrical waveforms. The RC network of R_1 and C_1 establishes an mean reference voltage V_{REF}, which tracks the mean amplitude of the V_{IN} signal. The noninverting input is directly connected to V_{REF} through R2. R2 and R3 are used to produce hysteresis to keep transitions free of spurious toggles. The time constant is a tradeoff between long-term symmetry and response time to changes in amplitude.

If the waveform is data, it is recommended that the data be encoded in NRZ (Non-Return to Zero) format to maintain proper average baseline. Asymmetrical inputs may suffer from timing distortions caused by the changing V_{REF} average voltage.

Figure 8-18. Pulse Slicer

For this design, follow these design requirements:

- The RC constant value (R_2 and C_1) must support the targeted data rate in order to maintain a valid tripping threshold.
- The hysteresis introduced with R_2 and R_{43} helps to avoid spurious output toggles.

Figure 8-19 shows the results of a 9600 baud data signal riding on a varying baseline.

Figure 8-19. Pulse Slicer Waveforms

Copyright © 2022 Texas Instruments Incorporated

9 Power Supply Recommendations

Due to the fast output edges, it is critical to have bypass capacitors on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1 µF ceramic bypass capacitor directly between V_{CC} pin and ground pins. Narrow, peak currents will be drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device may also be powered from "split" supplies (V+, V- and GND), with V- applied to the GND pin.

Input signals must stay within the specified input range (between V+ and V-) for both supply types.

Note that the ouptut will now swing "low" (VOL) to V- potential and not system GND on split supplies.

10 Layout

10.1 Layout Guidelines

For accurate comparator applications it is important maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and should be treated as high speed logic devices. The bypass capacitor should be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the V_{CC} and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V_{CC} or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor may also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations should be used when routing long distances.

10.2 Layout Example

Figure 10-1. Dual Layout Example

Copyright © 2022 Texas Instruments Incorporated

12.9 Alimentation Isolé Datasheet

TRACO POWER

Non-Isolated DC/DC Converter (POL) — TSR 2 Series, 2 A

- **Ultra compact SIP package 0.55 x 0.30 x 0.40 inch**
- **Up to 96% efficiency – No heat-sink required**
- **Pin compatible with LMxx linear regulators**
- **Built in filter capacitors**
- **Operating temperature range -40°C to +85°C**
- **Excellent line / load regulation**
- **Short circuit protection**
- **3-year product warranty**

The new TSR 2 series step-down switching regulators are drop-in replacement for inefficient LMxx linear regulators. A high efficiency up to 96% allows full load operation up to +67°C ambient temperature without the need of any heat-sink or forced cooling. The TSR 2 switching regulators provide other significant features over linear regulators, i.e. better output accuracy (±2%), lower standby current of 2 mA and no requirement of external capacitors. The high efficiency and low standby power consumption makes these regulators an ideal solution for many battery powered applications.

Models

Order Code	Output Current max.	Input Voltage Range	Output Voltage nom.	Efficiency typ.
TSR 2-0512	2'000 mA	3 - 5.5 VDC (5 VDC nom.)	1.2 VDC	90 %
TSR 2-0515			1.5 VDC	91 %
TSR 2-0518			1.8 VDC	92 %
TSR 2-0525		3.8 - 5.5 VDC (5 VDC nom.)	2.5 VDC	95 %
TSR 2-2412		4.6 - 36 VDC (12 VDC nom.)	1.2 VDC	84 %
TSR 2-2415			1.5 VDC	86 %
TSR 2-2418			1.8 VDC	87 %
TSR 2-2425			2.5 VDC	89 %
TSR 2-2433		4.75 - 36 VDC (12 VDC nom.)	3.3 VDC	91 %
TSR 2-2450		6.5 - 36 VDC (12 VDC nom.)	5 VDC	94 %
TSR 2-2465		9 - 36 VDC (12 VDC nom.)	6.5 VDC	94 %
TSR 2-2490		12 - 36 VDC (24 VDC nom.)	9 VDC	95 %
TSR 2-24120		15 - 36 VDC (24 VDC nom.)	12 VDC	95 %
TSR 2-24150		18 - 36 VDC (24 VDC nom.)	15 VDC	96 %

Note - If the input is switched electromechanically, a 22 µF / 50 V electrolytic capacitor at the input is recommended (12 & 24 Vin models only)

TRACO POWER

TSR 2 Series, 2 A

Input Specifications

Input Current	- At no load	5 Vin models:	1 mA typ.
		12 Vin models:	1 mA typ.
		24 Vin models:	1 mA typ.
Recommended Input Fuse		5 Vin models:	2'000 mA (slow blow)
		24 Vin models:	3'150 mA (slow blow)
	- 12 Vin input	1.2 Vout models:	1'600 mA (slow blow)
		1.5 Vout models:	1'600 mA (slow blow)
		1.8 Vout models:	1'600 mA (slow blow)
		2.5 Vout models:	2'500 mA (slow blow)
		3.3 Vout models:	2'500 mA (slow blow)
		5 Vout models:	2'500 mA (slow blow)
		6.5 Vout models:	2'500 mA (slow blow)
			(The need of an external fuse has to be assessed in the final application.)
Input Filter			Internal Capacitor

Output Specifications

Voltage Set Accuracy			±2% max.
Regulation	- Input Variation (Vmin - Vmax)		0.5% max.
	- Load Variation (0 - 100%)		1% max.
Ripple and Noise (20 MHz Bandwidth)		1.2 Vout models:	50 mVp-p typ.
		1.5 Vout models:	50 mVp-p typ.
		1.8 Vout models:	50 mVp-p typ.
		2.5 Vout models:	50 mVp-p typ.
		3.3 Vout models:	50 mVp-p typ.
		5 Vout models:	50 mVp-p typ.
		6.5 Vout models:	50 mVp-p typ.
		9 Vout models:	75 mVp-p typ.
		12 Vout models:	75 mVp-p typ.
		15 Vout models:	75 mVp-p typ.
Capacitive Load		1.2 Vout models:	2'500 µF max.
		1.5 Vout models:	2'000 µF max.
		1.8 Vout models:	1'600 µF max.
		2.5 Vout models:	1'200 µF max.
		3.3 Vout models:	900 µF max.
		5 Vout models:	600 µF max.
		6.5 Vout models:	470 µF max.
		9 Vout models:	330 µF max.
		12 Vout models:	270 µF max.
		15 Vout models:	200 µF max.
Minimum Load			Not required
Temperature Coefficient			±0.02 %/K max.
Start-up Time			5 ms typ.
Short Circuit Protection			Continuous, Automatic recovery
Overload Protection			Foldback Mode
Output Current Limitation			400% typ. of Iout max. (5 Vin models) 180% typ. (other input models)
Transient Response	- Peak Variation		300 mV typ. / 500 mV max. (50% Load Step) (24 Vin models) 150 mV typ. / 250 mV max. (50% Load Step) (other models)
	- Response Time		150 µs typ. / 200 µs max. (50% Load Step)

All specifications valid at nominal voltage, full load and +25°C after warm-up time unless otherwise stated.

TRACO POWER

TSR 2 Series, 2 A

General Specifications

Relative Humidity		95% max. (non condensing)
Temperature Ranges	- Operating Temperature	−40°C to +85°C
	- Case Temperature	+105°C max.
	- Storage Temperature	−55°C to +125°C
Power Derating	- High Temperature	See application note: www.tracopower.com/overview/tsr2
Over Temperature Protection Switch Off	- Protection Mode	150°C typ. (Automatic recovery)
	- Measurement Point	Internal IC temperature
Cooling System		Natural convection (20 LFM)
Switching Frequency		1200 kHz typ. (PWM) (5 Vout models) 410 kHz typ. (PWM) (other models)
Insulation System		Non-isolated
Reliability	- Calculated MTBF	13'520'000 h (MIL-HDBK-217F, ground benign)
Environment	- Vibration	MIL-STD-810F
	- Thermal Shock	MIL-STD-810F
Housing Material		Non-conductive Plastic (UL94 V-0 rated)
Potting Material		Silicone (UL 94 V-0 rated)
Pin Material		Copper
Pin Foundation Plating		Nickel (2 - 3 µm)
Pin Surface Plating		Tin (3 - 5 µm), matte
Soldering Profile		260°C / 10 s max.
Connection Type		THD (Through-Hole Device)
Weight		2.6 g
Environmental Compliance	- Reach	www.tracopower.com/info/reach-declaration.pdf
	- RoHS	www.tracopower.com/info/rohs-declaration.pdf

Supporting Documents

Overview Link (for additional Documents)	www.tracopower.com/overview/tsr2

Outline Dimensions

Dimensions in mm (inch)
Tolerances: x.xx ±0.5 (±0.02)
Tolerances: x.xxx ±0.25 (±0.01)
Pin pich tolerances: ±0.25 (±0.01)
Pin dimension tolerance: ±0.1 (±0.004)

Pinout

Pin	Function
1	+Vin
2	GND
3	+Vout

© Copyright 2020 Traco Electronic AG
Specifications can be changed without notice.

12.10 Alimentation Datasheet

Additional Resources: Product Page | 3D Model | PCB Footprint

CUI INC
a bel group

date 05/24/2022
page 1 of 9

SERIES: PDME2-S | **DESCRIPTION:** DC-DC CONVERTER

FEATURES
- 2 W isolated output
- single/dual unregulated output
- 1500 Vdc isolation
- continuous short circuit protection
- extended temperature range (-40~105°C)
- no-load input current as low as 8mA
- efficiency up to 86%
- EN 62368-1
- UL 62368-1

MODEL	input voltage typ (Vdc)	input voltage range (Vdc)	output voltage (Vdc)	output current min (mA)	output current max (mA)	output power max (W)	ripple & noise[1] max (mVp-p)	efficiency[2] typ (%)
PDME2-S5-D3-S[5]	5	4.5~5.5	±3.3	±30	±303	2	200	75
PDME2-S5-D5-S[5]	5	4.5~5.5	±5	±20	±200	2	200	84
PDME2-S5-D9-S[5]	5	4.5~5.5	±9	±11	±111	2	200	85
PDME2-S5-D12-S[5]	5	4.5~5.5	±12	±8	±83	2	200	85
PDME2-S5-D15-S[5]	5	4.5~5.5	±15	±7	±67	2	200	86
PDME2-S5-D24-S[5]	5	4.5~5.5	±24	±4	±42	2	200	86
PDME2-S5-S3-S[5]	5	4.5~5.5	3.3	40	400	1.32	200	78
PDME2-S5-S5-S[5]	5	4.5~5.5	5	40	400	2	200	84
PDME2-S5-S7-S[5]	5	4.5~5.5	7.2	28	278	2	200	84
PDME2-S5-S9-S[5]	5	4.5~5.5	9	22	222	2	200	85
PDME2-S5-S12-S[5]	5	4.5~5.5	12	17	167	2	200	85
PDME2-S5-S15-S[5]	5	4.5~5.5	15	13	133	2	200	86
PDME2-S5-S24-S[5]	5	4.5~5.5	24	8	83	2	200	86
PDME2-S12-D3-S	12	10.8~13.2	±3.3	±30	±303	2	180	75
PDME2-S12-D5-S	12	10.8~13.2	±5	±20	±200	2	180	80
PDME2-S12-D9-S[4,5]	12	10.8~13.2	±9	±11	±111	2	180	82
PDME2-S12-D12-S	12	10.8~13.2	±12	±8	±83	2	180	83
PDME2-S12-D15-S	12	10.8~13.2	±15	±7	±67	2	180	83
PDME2-S12-D24-S[4,5]	12	10.8~13.2	±24	±4	±42	2	180	83
PDME2-S12-S5-S	12	10.8~13.2	5	40	400	2	180	82
PDME2-S12-S9-S[4,5]	12	10.8~13.2	9	22	222	2	180	82
PDME2-S12-S12-S	12	10.8~13.2	12	17	167	2	180	84
PDME2-S12-S15-S	12	10.8~13.2	15	13	133	2	180	85
PDME2-S12-S24-S	12	10.8~13.2	24	8	83	2	180	86
PDME2-S15-D5-S[4,5]	15	13.5~16.5	±5	±20	±200	2	180	80
PDME2-S15-D15-S[4,5]	15	13.5~16.5	±15	±7	±67	2	180	82
PDME2-S15-S5-S[4,5]	15	13.5~16.5	5	40	400	2	180	80

MODEL (CONTINUED)

	input voltage		output voltage	output current		output power	ripple & noise[1]	efficiency[2]
	typ (Vdc)	range (Vdc)	(Vdc)	min (mA)	max (mA)	max (W)	max (mVp-p)	typ (%)
PDME2-S15-S15-S[4,5]	15	13.5~16.5	15	13	133	2	180	81
PDME2-S15-S24-S[4,5]	15	13.5~16.5	24	8	83	2	180	81
PDME2-S24-D3-S[4,5]	24	21.6~26.4	±3.3	±30	±300	2	180	76
PDME2-S24-D5-S	24	21.6~26.4	±5	±20	±200	2	180	80
PDME2-S24-D9-S[4,5]	24	21.6~26.4	±9	±11	±111	2	180	81
PDME2-S24-D12-S	24	21.6~26.4	±12	±8	±83	2	180	83
PDME2-S24-D15-S	24	21.6~26.4	±15	±7	±67	2	180	83
PDME2-S24-D24-S[4,5]	24	21.6~26.4	±24	±4	±42	2	180	83
PDME2-S24-S3-S[4,5]	24	21.6~26.4	3.3	40	400	1.32	180	76
PDME2-S24-S5-S	24	21.6~26.4	5	40	400	2	180	80
PDME2-S24-S9-S[4,5]	24	21.6~26.4	9	22	222	2	180	81
PDME2-S24-S12-S	24	21.6~26.4	12	17	167	2	180	84
PDME2-S24-S15-S	24	21.6~26.4	15	13	133	2	180	86
PDME2-S24-S24-S	24	21.6~26.4	24	8	83	2	180	86

Notes:
1. Measured at nominal input, 20 MHz bandwidth oscilloscope, with 10 µF tantalum and 1 µF ceramic capacitors on the output.
2. Measured at nominal input voltage, full load.
3. All specifications are measured at Ta=25°C, humidity < 75%, nominal input voltage, and rated output load unless otherwise specified.
4. Model is not CE certified.
5. Model is not UL certified.

PART NUMBER KEY

Additional Resources: Product Page | 3D Model | PCB Footprint

INPUT

parameter	conditions/description		min	typ	max	units
operating input voltage	5 Vdc input models		4.5	5	5.5	Vdc
	12 Vdc input models		10.8	12	13.2	Vdc
	15 Vdc input models		13.5	15	16.5	Vdc
	24 Vdc input models		21.6	24	26.4	Vdc
surge voltage	for maximum of 1 second					
	5 Vdc input models		-0.7		9	Vdc
	12 Vdc input models		-0.7		18	Vdc
	15 Vdc input models		-0.7		21	Vdc
	24 Vdc input models		-0.7		30	Vdc
current	5 Vdc input models	3.3 Vdc output			564	mA
		5 & 7.2 Vdc output			500	mA
		9 & 12 Vdc output			494	mA
		15 & 24 Vdc output			488	mA
	12 Vdc input models				208	mA
	15 Vdc input models				167	mA
	24 Vdc input models				104	mA
filter	filter capacitor					

OUTPUT

parameter	conditions/description	min	typ	max	units
maximum capacitive load[5]	3.3, 5 Vdc output models			2,400	µF
	±3.3, ±5 Vdc output models			1,200	µF
	9 Vdc output models			1,000	µF
	12, 15 Vdc output models			560	µF
	24, ±12, ±15 Vdc output models			220	µF
	±9 Vdc output models			470	µF
	±24 Vdc output models			100	µF
voltage accuracy	see output regulation curves				
line regulation	for Vin change of 1%				
	3.3 Vdc output models			±1.5	%
	all other output models			±1.2	%
load regulation	from 10% to full load				
	3.3 Vdc output models		10		%
	5 Vdc output models		8		%
	9, 12 & 15 Vdc output models		7		%
	24 Vdc output models		5		%
	from 10% to full load				
	3.3 Vdc output models		15		%
	5 Vdc output models		7		%
	9, 12 Vdc output models		5		%
	15 Vdc output models		4		%
	24 Vdc output models		3		%
switching frequency	100% load, nominal input voltage				
	5 Vdc input models		220		kHz
	all other input models		260		kHz
temperature coefficient	at full load		±0.02		%/°C

Note: 5. Tested at input voltage range and full load.

PROTECTIONS

parameter	conditions/description	min	typ	max	units
short circuit protection	continuous, auto recovery				

SAFETY AND COMPLIANCE

parameter	conditions/description	min	typ	max	units
isolation voltage	input to output for 1 minute at 1 mA	1,500			Vdc
isolation resistance	input to output at 500 Vdc	1,000			MΩ
isolation capacitance	input to output, 100 kHz / 0.1 V		20		pF
safety approvals	certified to 62368: EN, IEC, UL				
conducted emissions	CISPR 32/EN 55032 Class B				
radiated emissions	CISPR 32/EN 55032 Class B				
ESD	IEC/EN 61000-4-2 Air ±8kV, Contact ±6kV				
MTBF	as per MIL-HDBK-217F, 25°C	3,500,000			hours
RoHS	yes				

ENVIRONMENTAL

parameter	conditions/description	min	typ	max	units
operating temperature	see derating curves	-40		105	°C
storage temperature		-55		125	°C
storage humidity	non-condensing	5		95	%
case temperature rise	at 25°C		15		°C

DERATING CURVES

TEMPERATURE DERATING CURVE

OUTPUT REGULATION CURVE
5 Vdc input / 3.3 Vdc output
(nominal input)

OUTPUT REGULATION CURVE
5 Vdc input / all other output models
(nominal input)

OUTPUT REGULATION CURVE
all other input models / 3.3 Vdc output models
(nominal input)

OUTPUT REGULATION CURVE
all other input models / 5 Vdc output models
(nominal input)

OUTPUT REGULATION CURVE
all other input models / all other output models
(nominal input)

Additional Resources: Product Page | 3D Model | PCB Footprint

MECHANICAL

parameter	conditions/description	min	typ	max	units
dimensions	19.65 x 7.05 x 10.16 [0.773 x 0.277 x 0.400 inch]				mm
case material	black flame-retardant and heat-resistant plastic (UL94V-0)				
weight			2.4		g

MECHANICAL DRAWING

units: mm [inch]
tolerance: ±0.25[±0.010]
pin section tolerance: ±0.10[±0.004]

PIN CONNECTIONS		
PIN	Function / Single output	Function / Dual output
1	Vin	Vin
2	GND	GND
4	0V	-Vo
5	No pin	0V
6	+Vo	+Vo

12.11 Porte Logique

12.11.1 Porte And Datasheet

Product Folder | Sample & Buy | Technical Documents | Tools & Software | Support & Community

TEXAS INSTRUMENTS

SN74AHCT1G08

SCLS315Q – MARCH 1996 – REVISED APRIL 2016

SN74AHCT1G08 Single 2-Input Positive-AND Gate

1 Features

- Operating Range: 4.5 V to 5.5 V
- Maximum t_{pd} of 7.1 ns at 5 V
- Low Power Consumption: Maximum I_{CC} of 10-µA
- ±8-mA Output Drive at 5 V
- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Applications

- TV, Set-Top Box, and Audio
- Wireless Infrastructure
- Factory Automation and Control
- PC and Notebooks
- Building Automation
- Grid Infrastructure
- Medical, Healthcare, and Fitness
- Printers
- Test and Measurement
- EPOS (Electronic Point of Sale)
- Telecom Infrastructure
- Projectors

3 Description

The SN74AHCT1G08 device is a single 2-input positive-AND gate. The device performs the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic. Low I_{CC} current allows this device to be used in power-sensitive or battery-powered applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AHCT1G08DBVR	SOT-23 (5)	2.90 mm x 1.60 mm
SN74AHCT1G08DCKR	SC70 (5)	2.00 mm x 1.25 mm
SN74AHCT1G08DRLR	SOT (5)	1.60 mm x 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 3
6.1 Absolute Maximum Ratings ... 3
6.2 ESD Ratings ... 3
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 4
6.6 Switching Characteristics ... 5
6.7 Operating Characteristics ... 5
6.8 Typical Characteristics ... 5
7 Parameter Measurement Information ... 6
8 Detailed Description ... 7
8.1 Overview ... 7
8.2 Functional Block Diagram ... 7
8.3 Feature Description ... 7
8.4 Device Functional Modes ... 7
9 Application and Implementation ... 8
9.1 Application Information ... 8
9.2 Typical Application ... 8
10 Power Supply Recommendations ... 9
11 Layout ... 9
11.1 Layout Guidelines ... 9
11.2 Layout Example ... 9
12 Device and Documentation Support ... 10
12.1 Documentation Support ... 10
12.2 Community Resources ... 10
12.3 Trademarks ... 10
12.4 Electrostatic Discharge Caution ... 10
12.5 Glossary ... 10
13 Mechanical, Packaging, and Orderable Information ... 10

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision P (May 2013) to Revision Q	Page
• Added *Applications* section, *Device Information* table, *Table of Contents*, *Pin Configuration and Functions* section, *Specifications* section, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics* section, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision O (June 2005) to Revision P	Page
• Extended operating temperature range to 125°C	4

Copyright © 1996–2016, Texas Instruments Incorporated

5 Pin Configuration and Functions

DBV, DCK, and DRL Packages
5-Pin SOT-23, SC70, and SOT
Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	1	I	Input A
B	2	I	Input B
GND	3	—	Ground Pin
V_{CC}	5	—	Supply Pin
Y	4	O	Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).[1]

		MIN	MAX	UNIT
Supply voltage		–0.5	7	V
Input voltage[2]		–0.5	7	V
Output voltage[2]		–0.5	V_{CC} + 0.5	V
Input clamp current	$V_I < 0$		–20	mA
Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
Continuous current through V_{CC} or GND			±50	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Copyright © 1996–2016, Texas Instruments Incorporated

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
Δt/Δv	Input transition rise and fall rate		20	ns/V
T_A	Operating free-air temperature	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC(1)		SN74AHCT1G08			UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	226	277.5	242.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	165	92.9	77.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.1	64.2	77.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	45.5	1.9	9.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.3	63.5	77.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –50 µA, V_{CC} = 4.5 V	T_A = 25°C	4.4	4.5		V
			T_A = –40°C to 125°C	4.4			
		I_{OH} = –8 mA, V_{CC} = 4.5 V	T_A = 25°C	3.94			
			T_A = –40°C to 125°C	3.8			
V_{OL}	Low-level output voltage	I_{OL} = 50 µA, V_{CC} = 4.5 V				0.1	V
		I_{OL} = 8 mA, V_{CC} = 4.5 V	T_A = 25°C			0.36	
			T_A = –40°C to 125°C			0.44	
I_I	Input current	V_I = 5.5 V or GND, V_{CC} = 0 V to 5.5 V	T_A = 25°C			±0.1	µA
			T_A = –40°C to 125°C			±1	
I_{CC}	Supply current	V_I = V_{CC} or GND, I_O = 0, V_{CC} = 5.5 V	T_A = 25°C			1	µA
			T_A = –40°C to 125°C			10	
ΔI_{CC}(1)	Change in supply current	One input at 3.4 V, Other Inputs at V_{CC} or GND, V_{CC} = 5.5 V	T_A = 25°C			1.35	mA
			T_A = –40°C to 125°C			1.5	
C_I	Input capacitance	V_I = V_{CC} or GND, V_{CC} = 5 V			4	10	pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

Copyright © 1996–2016, Texas Instruments Incorporated

6.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low to high transition	A or B	Y	C_L = 15 pF	T_A = 25°C		5	6.2	ns
					T_A = –40°C to 85°C	1		7.1	
					T_A = –40°C to 125°C	1		7.5	
t_{PHL}	Propagation delay, high to low transition	A or B	Y	C_L = 15 pF	T_A = 25°C		5	6.2	ns
					T_A = –40°C to 85°C	1		7.1	
					T_A = –40°C to 125°C	1		7.5	
t_{PLH}	Propagation delay, low to high transition	A or B	Y	C_L = 50 pF	T_A = 25°C		5.5	7.9	ns
					Propagation delay, high to low transition	1		9	
					T_A = –40°C to 125°C	1		10	
t_{PHL}	Propagation delay, high to low transition	A or B	Y	C_L = 50 pF	T_A = 25°C		5.5	7.9	ns
					T_A = –40°C to 85°C	1		9	
					T_A = –40°C to 125°C	1		10	

6.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	18	pF

6.8 Typical Characteristics

C_L = 15 pF

Figure 1. T_{pd} vs Temperature

7 Parameter Measurement Information

C_L includes probe and jig capacitance.

Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

The outputs are measured one at a time with one input transition per measurement.

All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

Copyright © 1996–2016, Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The SN74AHCT1G08 device is a single 2-input positive-AND gate. The device performs the Boolean AND function ($Y = A \bullet B$ or $Y = \overline{A + B}$) in positive logic. Low I_{CC} current allows this device to be used in power-sensitive or battery-powered applications. Robust inputs allow the device to up-translate with a propagation delay of 20 ns.

8.2 Functional Block Diagram

Figure 3. Logic Diagram (Positive Logic)

8.3 Feature Description

The V_{CC} for the device is optimized at 5 V.

Up voltage translation from 3.3 V to 5 V is allowed. The inputs accept V_{IH} levels of 2 V.

Output ringing is minimized by slow edge rates.

Inputs are TTL-Voltage compatible.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74AHCT1G08.

Table 1. Function Table

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

Copyright © 1996–2016, Texas Instruments Incorporated

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AHCT1G08 device is a single AND gate, which is often used for many common functions like power sequencing or an *on* LED indicator. Because the device is configured to output LOW unless all inputs are HIGH, an LED tied to the output of the device will only turn HIGH when all systems connected are sending a HIGH, or *ready* signal.

9.2 Typical Application

Figure 4. Typical Application Diagram

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in *Recommended Operating Conditions*.
   - For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended Output Conditions
   - Load currents must not exceed 25 mA per output and 50 mA total for the part.
   - Outputs must not be pulled above V_{CC}.

Copyright © 1996–2016, Texas Instruments Incorporated

Typical Application (continued)

9.2.3 Application Curve

V_{CC} = 5 V Load = 50 Ω / 50 pF

Figure 5. Typical Switching Characteristics

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. TI recommends a 0.1-µF capacitor for devices with a single supply; and a 0.01-µF or 0.022-µF capactor for each power pin if there are multiple V_{CC} pins. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Observe the following rules under all circumstances.

- All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating.
- The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever make more sense or is more convenient.

11.2 Layout Example

Figure 6. Layout Diagram

Copyright © 1996–2016, Texas Instruments Incorporated

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

Copyright © 1996–2016, Texas Instruments Incorporated

12.11.2 Porte Or Datasheet

Product Folder | Sample & Buy | Technical Documents | Tools & Software | Support & Community

TEXAS INSTRUMENTS

SN74AHCT1G32

SCLS320O – MARCH 1996 – REVISED DECEMBER 2014

SN74AHCT1G32 Single 2-Input Positive-OR Gate

1 Features

- Operating Range of 4.5 V to 5.5 V
- Max t_{pd} of 8 ns at 5 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±8-mA Output Drive at 5 V
- Inputs are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1000-V Charged-Device Model

2 Applications

- I/O Modules; Analog PLC/DCS Inputs
- Server Motherboards
- Automotive Clusters
- Motor Drives and Controls
- DLP Front Projection Systems
- TVs
- Set-top-boxes
- Audio

3 Description

The SN74AHCT1G32 device is a single 2-input positive-OR gate. The device performs the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AHCT1G32	SOT-23 (5)	2.90 mm x 1.60 mm
	SC-70 (5)	2.00 mm x 1.30 mm
	SOT-553 (5)	1.65 mm x 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Simplified Schematic ... 1
5 Revision History ... 2
6 Pin Configuration and Functions ... 3
7 Specifications ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 4
7.5 Electrical Characteristics ... 5
7.6 Switching Characteristics ... 5
7.7 Operating Characteristics ... 5
7.8 Typical Characteristics ... 5
8 Parameter Measurement Information ... 6
9 Detailed Description ... 7
9.1 Overview ... 7
9.2 Functional Block Diagram ... 7
9.3 Feature Description ... 7
9.4 Device Functional Modes ... 7
10 Application and Implementation ... 8
10.1 Application Information ... 8
10.2 Typical Application ... 8
11 Power Supply Recommendations ... 9
12 Layout ... 10
12.1 Layout Guidelines ... 10
12.2 Layout Example ... 10
13 Device and Documentation Support ... 10
13.1 Trademarks ... 10
13.2 Electrostatic Discharge Caution ... 10
13.3 Glossary ... 10
14 Mechanical, Packaging, and Orderable Information ... 10

5 Revision History

Changes from Revision N (June 2005) to Revision O	Page
• Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Deleted *Ordering Information* table.	1
• Changed MAX operating temperature to 125°C in *Recommended Operating Conditions* table.	4

Copyright © 1996–2014, Texas Instruments Incorporated

6 Pin Configuration and Functions

See mechanical drawings for dimensions.

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	A	I	Input A
2	B	I	Input B
3	GND	—	Ground Pin
4	Y	O	Output Y
5	V_{CC}	—	Power Pin

Copyright © 1996–2014, Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range[2]		–0.5	7	V
V_O	Output voltage range[2]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

7.4 Thermal Information

THERMAL METRIC[1]		SN74AHCT1G32			UNIT
		DBV	DCK	DRL	
		5 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	231.3	287.6	328.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	119.9	97.7	105.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	65.	150.3	
ψ_{JT}	Junction-to-top characterization parameter	17.8	2.0	6.9	
ψ_{JB}	Junction-to-board characterization parameter	60.1	64.2	148.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

Copyright © 1996–2014, Texas Instruments Incorporated

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	4.5 V	4.4	4.5		4.4		4.4		V
	I_{OH} = –8 mA		3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			1		10		10	µA
ΔI_{CC} (1)	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		2	10		10		10	pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

7.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15 pF		5	6.9	1	8	1	9	ns
t_{PHL}					5	6.9	1	8	1	9	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	1	10	ns
t_{PHL}					5.5	7.9	1	9	1	10	

7.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	11.5	pF

7.8 Typical Characteristics

Figure 1. TPD vs Temperature

Copyright © 1996–2014, Texas Instruments Incorporated

8 Parameter Measurement Information

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

Copyright © 1996–2014, Texas Instruments Incorporated

9 Detailed Description

9.1 Overview

The SN74AHCT1G32 device is a single 2-input positive-OR gate. The device performs the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

The device has TTL inputs that allow up translation from 3.3 V to 5 V. The inputs are high impedance when $V_{CC} = 0$ V.

9.2 Functional Block Diagram

Figure 3. Logic Diagram (Positive Logic)

9.3 Feature Description

- Slow rise and fall time on outputs allow for low noise outputs.
- TTL inputs
  - Allows up translation from 3.3 V to 5 V

9.4 Device Functional Modes

Table 1. Function Table

INPUTS		OUTPUT Y
A	B	
H	X	H
X	H	H
L	L	L

Copyright © 1996–2014, Texas Instruments Incorporated

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

SN74AHCT1G125 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The TTL inputs can accept voltages down to 3.3 V and translate up to 5 V.

10.2 Typical Application

Figure 4. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *Recommended Operating Conditions* table.
   - For specified High and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
2. Recommend Output Conditions
   - Load currents should not exceed 25 mA per output and 50 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

Copyright © 1996–2014, Texas Instruments Incorporated

Typical Application (continued)

10.2.3 Application Curves

Figure 5. Switching Characterstics Comparison

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

Copyright © 1996–2014, Texas Instruments Incorporated

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 6 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

12.2 Layout Example

Figure 6. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 1996–2014, Texas Instruments Incorporated

12.11.3 Porte NAnd Datasheet

Product Folder | Sample & Buy | Technical Documents | Tools & Software | Support & Community

TEXAS INSTRUMENTS

SN74AHCT1G00

SCLS316N – MARCH 1995 – REVISED MARCH 2015

SN74AHCT1G00 Single 2-Input Positive-NAND Gate

1 Features

- Operating Range of 4.5 V to 5.5 V
- Maximum t_{pd} of 7.1 ns at 5 V
- Low Power Consumption, 10-μA Maximum I_{CC}
- ±8-mA Output Drive at 5 V
- Inputs Are TTL-Voltage Compatible
- Latch-up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- IP Phones
- Notebook PCs
- Printers
- Access Control and Security
- Solar Inverters

3 Description

The SN74AHCT1G00 device performs the Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AHCT1G00	SOT-23 (5)	2.90 mm × 1.60 mm
	SC-70 (5)	2.00 mm × 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 3
6.1 Absolute Maximum Ratings ... 3
6.2 ESD Ratings ... 3
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 4
6.6 Switching Characteristics ... 5
6.7 Operating Characteristics ... 5
6.8 Typical Characteristics ... 5
7 Parameter Measurement Information ... 6
8 Detailed Description ... 7
8.1 Overview ... 7
8.2 Functional Block Diagram ... 7
8.3 Feature Description ... 7
8.4 Device Functional Modes ... 7
9 Application and Implementation ... 8
9.1 Application Information ... 8
9.2 Typical Application ... 8
10 Power Supply Recommendations ... 10
11 Layout ... 10
11.1 Layout Guidelines ... 10
11.2 Layout Example ... 10
12 Device and Documentation Support ... 11
12.1 Trademarks ... 11
12.2 Electrostatic Discharge Caution ... 11
12.3 Glossary ... 11
13 Mechanical, Packaging, and Orderable Information ... 11

4 Revision History

Changes from Revision M (January 2003) to Revision N	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted Ordering Information table.	1
• Extended operating temperature range to 125°C.	4

Copyright © 1995–2015, Texas Instruments Incorporated

5 Pin Configuration and Functions

DBV or DCK Package
5-PIN SOT-23 OR SC-70
Top View

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	A	I	Input A
2	B	I	Input B
3	GND	—	Ground Pin
4	Y	O	Output Y
5	V_{CC}	—	Power Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Output voltage(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$	–20	20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	–25	25	mA
	Continuous current through V_{CC} or GND		–50	50	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Copyright © 1995–2015, Texas Instruments Incorporated

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level Input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
Δt/Δv	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC[1]		SN74AHCT1G00		UNIT
		DBV (SOT-23)	DCK (SC-70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	208.2	287.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.1	97.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	52.5	65	
ψ_{JT}	Junction-to-top characterization parameter	4	2	
ψ_{JB}	Junction-to-board characterization parameter	51.8	64.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	4.5 V	4.4	4.5		4.4		4.4		V
	I_{OH} = –8 mA		3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			1		10		10	µA
ΔI_{CC}[1]	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		2	10		10		10	pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

Copyright © 1995–2015, Texas Instruments Incorporated

6.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		–40°C to 85°C		–40°C to 125°C		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15 pF	5	6.2	1	7.1	1	8	ns
t_{PHL}				5	6.2	1	7.1	1	8	
t_{PLH}	A or B	Y	C_L = 15 pF	5.5	7.9	1	9	1	10	ns
t_{PHL}				5.5	7.9	1	9	1	10	

6.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	10.5	pF

6.8 Typical Characteristics

Figure 1. TPD vs Temperature

Copyright © 1995–2015, Texas Instruments Incorporated

7 Parameter Measurement Information

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuits and Voltage Waveforms

Copyright © 1995–2015, Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The SN74AHCT1G00 device performs the Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The device has TTL inputs that allow up translation from 3.3 V to 5 V. The inputs are high impedance when Vcc = 0 V.

8.2 Functional Block Diagram

Figure 3. Logic Diagram (Positive Logic)

8.3 Feature Description

The device is ideal for operating in a 5-V logic system. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low power consumption makes this device a good choice for portable and battery power-sensitive applications.

8.4 Device Functional Modes

Table 1. Function Table

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

Copyright © 1995–2015, Texas Instruments Incorporated

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AHCT1G00 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The TTL inputs can except voltages down to 3.3 V and translate up to 5 V.

9.2 Typical Application

Figure 4. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- Recommended output conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above V_{CC}.

Copyright © 1995–2015, Texas Instruments Incorporated

Typical Application (continued)

9.2.3 Application Curves

Figure 5. Switching Characteristics Comparison

Copyright © 1995–2015, Texas Instruments Incorporated

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor and if there are multiple V_{CC} terminals then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

11.2 Layout Example

Figure 6. Layout Recommendation

Copyright © 1995–2015, Texas Instruments Incorporated

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 1995–2015, Texas Instruments Incorporated

12.11.4 Porte NOr Datasheet

SN74AHCT1G02
SINGLE 2-INPUT POSITIVE-NOR GATE

SCLS341K – APRIL 1996 – REVISED FEBRUARY 2003

- **Operating Range of 4.5 V to 5.5 V**
- **Max t_{pd} of 6.5 ns at 5 V**
- **Low Power Consumption, 10-µA Max I_{CC}**
- **±8-mA Output Drive at 5 V**
- **Inputs Are TTL-Voltage Compatible**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DBV OR DCK PACKAGE
(TOP VIEW)

description/ordering information

This device contains a single 2-input NOR gate that performs the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	SOT (SOT-23) – DBV	Reel of 3000	SN74AHCT1G02DBVR	B02_
		Reel of 250	SN74AHCT1G02DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74AHCT1G02DCKR	BB_
		Reel of 250	SN74AHCT1G02DCKT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
‡ The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic diagram (positive logic)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2003, Texas Instruments Incorporated

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN74AHCT1G02
SINGLE 2-INPUT POSITIVE-NOR GATE

SCLS341K – APRIL 1996 – REVISED FEBRUARY 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package . . . . . 206°C/W
DCK package . . . . . 252°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 µA		4.5 V	4.4	4.5		4.4		V
	I_{OH} = –8 mA			3.94			3.8		
V_{OL}	I_{OL} = 50 µA		4.5 V			0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44	
I_I	V_I = 5.5 V or GND		0 V to 5.5 V			±0.1		±1	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			1		10	µA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at GND or V_{CC}	5.5 V			1.35		1.5	mA
C_i	V_I = V_{CC} or GND		5 V		4	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

SN74AHCT1G02
SINGLE 2-INPUT POSITIVE-NOR GATE

SCLS341K – APRIL 1996 – REVISED FEBRUARY 2003

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		2.4	5.5	1	6.5	ns
t_{PHL}					3.5	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		3.4	7.5	1	8.5	ns
t_{PHL}					4.5	7.5	1	8.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	17	pF

SN74AHCT1G02
SINGLE 2-INPUT POSITIVE-NOR GATE

SCLS341K – APRIL 1996 – REVISED FEBRUARY 2003

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

12.11.5 Porte XOr Datasheet

Ordering & quality | Technical documentation | Design & development | Support & training

TEXAS INSTRUMENTS

SN74AHCT1G86

SCLS324N – MARCH 1996 – REVISED AUGUST 2022

SN74AHCT1G86 Single 2-Input Exclusive-OR Gate

1 Features

- Operating Range of 4.5 V to 5.5 V
- Max t_{pd} of 8 ns at 5 V
- Low Power Consumption, 10-A Maximum I_{CC}
- 8-mA Output Drive at 5 V
- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Applications

- Industrial PCs
- Stepper Motors
- AC Inverter Drives
- Notebook PCs
- Smart Meters: Data Concentrators
- Enterprise Servers

3 Description

The SN74AHCT1G86 is a single 2-input exclusive-OR gate. The device performs the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AHCT1G86	DBV (SOT-23, 5)	2.90 mm × 1.60 mm
	DCK (SC-70, 5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

These five equivalent exclusive-OR symbols are valid for an SN74AHCT1G86 gate in positive logic; negation may be shown at any two ports.

Exclusive-OR Logic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Pin Configuration and Functions....3
6 Specifications....4
6.1 Absolute Maximum Ratings....4
6.2 ESD Ratings....4
6.3 Recommended Operating Conditions....4
6.4 Thermal Information....5
6.5 Electrical Characteristics....5
6.6 Switching Characteristics....6
6.7 Operating Characteristics....6
6.8 Typical Characteristics....6
7 Parameter Measurement Information....7
8 Detailed Description....8
8.1 Overview....8
8.2 Functional Block Diagram....8
8.3 Feature Description....8
8.4 Device Functional Modes....8
9 Application and Implementation....9
9.1 Application Information....9
9.2 Typical Application....9
10 Power Supply Recommendations....11
11 Layout....11
11.1 Layout Guidelines....11
11.2 Layout Example....11
12 Device and Documentation Support....12
12.1 Receiving Notification of Documentation Updates....12
12.2 Support Resources....12
12.3 Trademarks....12
12.4 Electrostatic Discharge Caution....12
12.5 Glossary....12
13 Mechanical, Packaging, and Orderable Information....12

4 Revision History

Changes from Revision M (February 2015) to Revision N (August 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision L (January 2003) to Revision M (February 2015)	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Copyright © 2022 Texas Instruments Incorporated

5 Pin Configuration and Functions

Figure 5-1. DBV or DCK Package 5-Pin SOT-23 Top View

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	A	I	A input
2	B	I	B input
3	GND	–	Ground pin
4	Y	O	Output
5	Vcc	–	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

Copyright © 2022 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage[2]		–0.5	7	V
V_O	Output voltage[2]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}	–20	20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}	–25	25	mA
	Continuous current through V_{CC} or GND		–50	50	mA
T_{stg}	Storage temperature		–65	150	°C
T_J	Junction Temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5		5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		5.5	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			–8	mA
I_{OL}	Low-level output current			8	mA
t/v	Input transition rise or fall rate			20	ns/V
T_A	Operating free-air temperature	–40		125	°C

Copyright © 2022 Texas Instruments Incorporated

6.4 Thermal Information

THERMAL METRIC[1]		SN74AHCT1G86		UNIT
		DBV (SOT-23)	DCK (SC-70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	208.2	287.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.1	97.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	52.5	65	
ψ_{JT}	Junction-to-top characterization parameter	4	2	
ψ_{JB}	Junction-to-board characterization parameter	51.8	64.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High level output voltage	I_{OH} = –50 µA	4.5 V	4.4	4.5		4.4		4.4		V
		I_{OH} = –8 mA		3.94			3.8		3.8		
V_{OL}	Low level output voltage	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	Input leakage current	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			1		10		10	µA
ΔI_{CC} [1]	Supply-current change	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	Input capacitance	$V_I = V_{CC}$ or GND	5 V		2	10		10		10	pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

Copyright © 2022 Texas Instruments Incorporated

6.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		–40°C to 85°C		–40°C to 125°C		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15 pF	5	6.2	1	8	1	9	ns
t_{PHL}				5	6.2	1	8	1	9	
t_{PLH}	A or B	Y	C_L = 50 pF	5.5	7.9	1	9	1	10	ns
t_{PHL}				5.5	7.9	1	9	1	10	

6.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	18	pF

6.8 Typical Characteristics

Figure 6-1. TPD vs. Temperature

Copyright © 2022 Texas Instruments Incorporated

7 Parameter Measurement Information

7.1

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 1 MHz, Z_O = 50 , t_r 3 ns, t_f 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

Copyright © 2022 Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The SN74AHCT1G86 is a single 2-input exclusive-OR gate. The device performs the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

8.2 Functional Block Diagram

Figure 8-1. Exclusive-OR Logic

8.3 Feature Description

The device is ideal for operating in a 5-V logic system. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low power consumption makes this device a good choice for portable and battery power-sensitive applications.

8.4 Device Functional Modes

Table 8-1. Function Table

INPUTS(1)		OUTPUT(2)
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State

Copyright © 2022 Texas Instruments Incorporated

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74AHCT1G86 is a Low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8-V V_{IL} and 2-V V_{IH}. This feature makes it Ideal for translating up from 3.3 V to 5 V.

9.2 Typical Application

Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Rise time and fall time specs. See (Δt/ΔV) in *Section 6.3*.
  - Specified high and low levels. See (V_{IH} and V_{IL}) in *Section 6.3*.
- Recommended output conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above V_{CC}.

Copyright © 2022 Texas Instruments Incorporated

9.2.3 Application Curves

Figure 9-2. Translation From 3.3 V to 5.5 V

Copyright © 2022 Texas Instruments Incorporated

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Section 6.3*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor and if there are multiple Vcc terminals then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

11.2 Layout Example

Figure 11-1. Layout Recommendation

Copyright © 2022 Texas Instruments Incorporated

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2022 Texas Instruments Incorporated

12.12 Solid State Relay Datasheet

IXYS
INTEGRATED CIRCUITS DIVISION

CPC1394
Single-Pole, Normally Open 4-Pin OptoMOS® Relay

Parameter	Rating	Units
Blocking Voltage	600	V_P
Load Current	120	mA_{rms} / mA_{DC}
On-Resistance (max)	35	Ω

Features
- 5000V_{rms} Input/Output Isolation
- 600V_P Blocking Voltage
- 100% Solid State
- Low Drive Power Requirements (TTL/CMOS Compatible)
- Arc-Free With No Snubbing Circuits
- No EMI/RFI Generation
- Small 4-Pin Package
- Machine Insertable, Wave Solderable

Applications
- Instrumentation
  - Multiplexers
  - Data Acquisition
  - Electronic Switching
  - I/O Subsystems
- Meters (Watt-Hour, Water, Gas)
- Medical Equipment—Patient/Equipment Isolation
- Security
- Aerospace
- Industrial Controls

Description
The CPC1394 is a single-pole, normally-open (1-Form-A) Solid State Relay with an enhanced input to output isolation barrier of 5000V_{rms}.

The relay output is constructed with efficient MOSFET switches that use IXYS Integrated Circuits Division's patented OptoMOS architecture. The input, a highly efficient GaAlAS infrared LED, controls the optically coupled output.

Approvals
- UL Certified Component: File E76270
- CSA Certified Component: Certificate 1172007
- EN/IEC 60950-1 Certified Component: TUV Certificate B 10 05 49410 006

Ordering Information

Part Number	Description
CPC1394G	4-Pin DIP (100/Tube)
CPC1394GV	4-Pin DIP V-Bend (100/Tube)
CPC1394GR	4-Pin Surface Mount (100/Tube)
CPC1394GRTR	4-Pin Surface Mount (1000/Reel)

Pin Configuration

Switching Characteristics of Normally Open Devices

Pb RoHS e3

IXYS
INTEGRATED CIRCUITS DIVISION

CPC1394

Absolute Maximum Ratings @ 25°C

Parameter	Ratings	Units
Peak Blocking Voltage	600	V_P
Reverse Input Voltage	5	V
Input Control Current	50	mA
Peak (10ms)	1	A
Input Power Dissipation [1]	100	mW
Total Package Dissipation [2]	550	mW
Isolation Voltage, Input to Output	5000	V_{rms}
Operational Temperature	-40 to +85	°C
Storage Temperature	-40 to +125	°C

[1] Derate linearly 1.33 mW / °C
[2] Derate linearly 3.00 mW / °C

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

Electrical Characteristics @ 25°C

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Output Characteristics						
Load Current						
Continuous	-	I_L	-	-	120	mA_{rms} / mA_{DC}
Peak	t=10ms	I_{LPK}	-	-	±400	mA_P
On-Resistance [1]	I_L=120mA	R_{ON}	-	26	35	Ω
Off-State Leakage Current	V_L=600V_P	I_{LEAK}	-	-	1	µA
Switching Speeds						
Turn-On	I_F=5mA, V_L=10V	t_{on}	-	0.85	5	ms
Turn-Off		t_{off}	-	0.46	3	
Output Capacitance	I_F=0mA, V_L=50V, f=1MHz	C_{OUT}	-	50	-	pF
Input Characteristics						
Input Control Current to Activate [2]	I_L=120mA	I_F	-	0.45	2	mA
Input Control Current to Deactivate	-	I_F	0.2	0.4	-	
Input Voltage Drop	I_F=5mA	V_F	0.9	1.2	1.4	V
Reverse Input Current	V_R=5V	I_R	-	-	10	µA
Common Characteristics						
Input to Output Capacitance	-	$C_{I/O}$	-	3	-	pF

[1] Measurement taken within 1 second of on-time.
[2] For temperatures >60°C, a LED current of 4mA is recommended.

IXYS
INTEGRATED CIRCUITS DIVISION

CPC1394

PERFORMANCE DATA*

*The Performance data shown in the graphs above is typical of device performance. For guaranteed parameters not indicated in the written specifications, please contact our application department.

IXYS
INTEGRATED CIRCUITS DIVISION

CPC1394

PERFORMANCE DATA*

*The Performance data shown in the graphs above is typical of device performance. For guaranteed parameters not indicated in the written specifications, please contact our application department.

IXYS
INTEGRATED CIRCUITS DIVISION

CPC1394

Manufacturing Information

Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
CPC1394G / CPC1394GV / CPC1394GR	MSL 1

ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

Device	Maximum Temperature x Time
CPC1394G / CPC1394GV / CPC1394GR	250°C for 30 seconds

Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable. Since IXYS Integrated Circuits Division employs the use of silicone coating as an optical waveguide in many of its optically isolated products, the use of a short drying bake could be necessary if a wash is used after solder reflow processes. Chlorine- or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

Pb RoHS e3

12.13 Bascule D Datasheet

Product Folder | Order Now | Technical Documents | Tools & Software | Support & Community

TEXAS INSTRUMENTS

SN74HCS72-Q1

SCLS774 – OCTOBER 2019

SN74HCS72-Q1 Automotive Qualified Schmitt-Trigger Input Dual D-Type Negative-Edge-Triggered Flip-Flops With Clear and Preset

1 Features

- AEC-Q100 Qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C, T_A
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classifcation Level C6
- Wide operating voltage range: 2 V to 6 V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
  - Typical I_{CC} of 100 nA
  - Typical input leakage current of ±100 nA
- ±7.8-mA output drive at 5 V

2 Applications

- Convert a momentary switch to a toggle switch
- Input slow edge-rate signals
- Operate in noisy environments
- Enable CAN Controller Power with wake-up pattern

3 Description

This device contains two independent D-type negative-edge-triggered flip-flops. All inputs include Schmitt-triggers, allowing for slow or noisy input signals. A low level at the preset ($\overline{PRE}$) input sets the output high. A low level at the clear ($\overline{CLR}$) input resets the output low. Preset and clear functions are asynchronous and not dependent on the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs (Q, $\overline{Q}$) on the negative-going edge of the clock (CLK) pulse. Following the hold-time interval, data at the data (D) input can be changed without affecting the levels at the outputs (Q, $\overline{Q}$).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HCS72QDRQ1	SOIC (14)	8.70 mm x 3.90 mm
SN74HCS72QPWRQ1	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Benefits of Schmitt-trigger Inputs

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Switching Characteristics ... 5
6.7 Timing Characteristics ... 6
6.8 Typical Characteristics ... 7
7 Parameter Measurement Information ... 8
8 Detailed Description ... 9
8.1 Overview ... 9
8.2 Functional Block Diagram ... 9
8.3 Feature Description ... 9
8.4 Device Functional Modes ... 10
9 Application and Implementation ... 11
9.1 Application Information ... 11
9.2 Typical Application ... 11
10 Power Supply Recommendations ... 13
11 Layout ... 13
11.1 Layout Guidelines ... 13
11.2 Layout Example ... 13
12 Device and Documentation Support ... 14
12.1 Documentation Support ... 14
12.2 Receiving Notification of Documentation Updates 14
12.3 Community Resources ... 14
12.4 Trademarks ... 14
12.5 Electrostatic Discharge Caution ... 14
12.6 Glossary ... 14
13 Mechanical, Packaging, and Orderable Information ... 14

4 Revision History

DATE	REVISION	NOTES
October 2019	*	Initial release.

Copyright © 2019, Texas Instruments Incorporated

5 Pin Configuration and Functions

D and PW Package
14-Pin SOIC and TSSOP
Top View

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1$\overline{CLR}$	1	Input	Clear for channel 1, active low
1D	2	Input	Data for channel 1
1$\overline{CLK}$	3	Input	Clock for channel 1, falling edge triggered
1$\overline{PRE}$	4	Input	Preset for channel 1, active low
1Q	5	Output	Output for channel 1
1$\overline{Q}$	6	Output	Inverted output for channel 1
GND	7	—	Ground
2$\overline{Q}$	8	Output	Inverted output for channel 2
2Q	9	Output	Output for channel 2
2$\overline{PRE}$	10	Input	Preset for channel 2, active low
2$\overline{CLK}$	11	Input	Clock for channel 2, falling edge triggered
2D	12	Input	Data for channel 2
2$\overline{CLR}$	13	Input	Clear for channel 2, active low
V_{CC}	14	—	Positive supply

Copyright © 2019, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current[2]	$V_I < 0$ or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output clamp current[2]	$V_O < 0$ or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_j	Junction temperature[3]			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1] HBM ESD Classification Level 2	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordrance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall rate			Unlimited	ns/V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC		SN74HCS72-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.6	151.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89	79.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	89.5	94.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	45.5	25.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	89.1	94.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

Copyright © 2019, Texas Instruments Incorporated

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
V_{T-}	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
ΔV_T	Hysteresis (V_{T+} - V_{T-})(1)			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = -20 µA	2 V to 6 V	V_{CC} – 0.1	V_{CC} – 0.002		V
			I_{OH} = -6 mA	4.5 V	4	4.3		
			I_{OH} = -7.8 mA	6 V	5.4	5.75		
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V to 6 V		0.002	0.1	V
			I_{OL} = 6 mA	4.5 V		0.18	0.30	
			I_{OL} = 7.8 mA	6 V		0.22	0.33	
I_I	Input leakage current	V_I = V_{CC} or 0		6 V		±100	±1000	nA
I_{CC}	Supply current	V_I = V_{CC} or 0, I_O = 0		6 V		0.1	2	µA
C_i	Input capacitance			2 V to 6 V			5	pF
C_{pd}	Power dissipation capacitance per gate	No load		2 V to 6 V		10		pF

(1) Guaranteed by design.

6.6 Switching Characteristics

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See Parameter Measurement Information

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
f_{max}	Max switching frequency			2 V	20	31		MHz
				4.5 V	64	95		
				6 V	74	105		
t_{pd}	Propagation delay	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		19	42	ns
				4.5 V		8	19	
				6 V		7	15	
		$\overline{CLK}$	Q or $\overline{Q}$	2 V		19	42	ns
				4.5 V		8	19	
				6 V		7	15	
t_t	Transition-time(1)		Q or $\overline{Q}$	2 V		9	16	ns
				4.5 V		5	9	
				6 V		4	8	

(1) t_t = t_r or t_f, whichever is larger

Copyright © 2019, Texas Instruments Incorporated

6.7 Timing Characteristics

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See Parameter Measurement Information.

PARAMETER			V_{CC}	MIN	TYP	MAX	UNIT
f_{clock}	Clock frequency		2 V			20	MHz
			4.5 V			64	
			6 V			74	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	8	7		ns
			4.5 V	7	5		
			6 V	7	5		
		$\overline{CLK}$ high or low	2 V	10	5		ns
			4.5 V	9	3		
			6 V	8	2		
t_{su}	Setup time before $\overline{CLK}$ low	Data	2 V	16	11		ns
			4.5 V	6	1		
			6 V	3	1		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	7			ns
			4.5 V	0			
			6 V	0			
t_h	Hold time	Data after CLK ↓	2 V	5			ns
			4.5 V	3			
			6 V	2			

Copyright © 2019, Texas Instruments Incorporated

6.8 Typical Characteristics

T_A = 25°C

Figure 1. Output driver resistance in LOW state.

Figure 2. Output driver resistance in HIGH state.

Figure 3. Supply current across input voltage, 2-, 2.5-, and 3.3-V supply

Figure 4. Supply current across input voltage, 4.5-, 5-, and 6-V supply

Copyright © 2019, Texas Instruments Incorporated

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 2.5 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.

C_L includes probe and test-fixture capacitance.

Figure 5. Load Circuit

Figure 6. Voltage Waveforms, Pulse Duration

Figure 7. Voltage Waveforms, Setup and Hold Times

Voltage Waveforms, Propagation Delay specifications t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 8. Voltage Waveforms Propagation Delays

Figure 9. Voltage Waveforms, Input and Output Transition Times

Copyright © 2019, Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

Figure 10 describes the SN74HCS72-Q1. As the SN74HCS72-Q1 is a dual D-Type negative-edge-triggered flip-flop with clear and preset, the diagram below describes one of the two device flip-flops.

8.2 Functional Block Diagram

Figure 10. Logic Diagram (Positive Logic) for one channel of SN74HCS72-Q1

8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* must be followed at all times.

8.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics*, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

Copyright © 2019, Texas Instruments Incorporated

Feature Description (continued)

8.3.3 Positive and Negative Clamping Diodes

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 11.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

Figure 11. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74HCS72-Q1.

Table 1. Function Table

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	$\overline{CLK}$	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (1)	H (1)
H	H	↓	H	H	L
H	H	↓	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$
H	H	H	X	Q_0	$\overline{Q}_0$

(1) This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

Copyright © 2019, Texas Instruments Incorporated

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74HCS72-Q1 is an ideal device for taking a CAN wake-up request and converting it to a power supply enable due to its low power consumption and noise rejecting inputs, which eliminate false triggers. CAN communication can occur when the vehicle ignition is off. Therefore, many circuits are designed to work in a standby or low power mode. Because a CAN wake-up request causes the RX pin to pulse LOW, the SN74HCS72-Q1 will trigger off the falling edge enabling the power for the CAN controller. Then the CAN controller powers on for the incoming communication. When communications are finished, the controller sends a reset pulse to the SN74HCS72-Q1 and CAN transceiver putting the circuit back into a standby mode.

9.2 Typical Application

Figure 12. Power Enable Using CAN Wake-up Request

9.2.1 Design Requirements

The SN74HCS72-Q1 device allows flexibility by having complementary outputs for active-high or active-low enables. The supply should be selected such that the device is always powered along with the CAN transceiver. The same supply for both devices is recommended.

With the SN74HCS72-Q1, a power on reset circuit only requires a resistor (R) and capacitor (C) to create a delay. The R and C values create a delay that is approximately 2.2×RC. In this application, it is desired to have the output ($\overline{Q}$) in the HIGH state at startup, so R1 and C1 are connected directly to the $\overline{CLR}$ pin, as shown in Figure 12. A second resistor is needed to limit the current into the CAN controller when it sets the circuit back into standby mode. It is required for the R1 resistor to be at least ten times larger than R2 to avoid a divider circuit (R2 ≤ 10R1).

The D input can be tied either to V_{CC} or ground depending on the desired implementation. In this example, it is tied to V_{CC} to obtain a HIGH signal from $\overline{Q}$ when a wake-up request occurs.

Copyright © 2019, Texas Instruments Incorporated

Typical Application (continued)

9.2.1.1 Output Considerations

In general, the load needs to be considered in the design to determine if the device will have the capability to drive it. For this application, we assume that the flip-flop output is transmitting over a relatively short trace (under 10 cm) to a CMOS input.

Primary load factors to consider:

- Load Capacitance: approximately 15 pF
  - See the *Switching Characteristics* section for the capacitive loads tested with this device.
  - Increasing capacitance will proportionally increase output transition times.
  - Decreasing capacitance will proportionally decrease output transition times, and can produce ringing due to very fast transition rates. A 25-Ω resistor can be added in series with the output if ringing needs to be dampened.
- Load Current: expected maximum of 10 µA
  - Leakage current into connected devices.
  - Parasitic current from other components.
  - Resistive load current.
- Output Voltage: see *Electrical Characteristics* for output voltage ratings at a given current.
  - Output HIGH (V_{OH}) and output LOW (V_{OL}) voltage levels affect the input voltage, V_{IH} and V_{IL}, respectively, to subsequent devices.

9.2.1.2 Input Considerations

The SN74HCS72-Q1 has Schmitt-trigger inputs. Schmitt-trigger inputs have no limitation on transition rate, however the input voltage must be larger than $V_{T+(max)}$ to be guaranteed to be read as a logic high, and below $V_{T-(min)}$ to be guaranteed to be read as a logic low, as defined in the *Electrical Characteristics*. Do not exceed the values specified in the *Absolute Maximum Ratings* or the device could be damaged.

9.2.1.3 Timing Considerations

The SN74HCS72-Q1 is a clocked device. As such, it requires special timing considerations to ensure normal operation.

Primary timing factors to consider:

- Maximum clock frequency: the maximum operating clock frequency defined in *Timing Characteristics* is the maximum frequency at which the device is guaranteed to function. This value refers specifically to the triggering waveform, measuring from one trigger level to the next.
- Pulse duration: ensure that the triggering event duration is larger than the minimum pulse duration, as defined in the *Timing Characteristics*.
- Setup time: ensure that the data has changed at least one setup time prior to the triggering event, as defined in the *Timing Characteristics*.
- Hold time: ensure that the data remains in the desired state at least one hold time after the triggering event, as defined in the *Timing Characteristics*.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - Input signals to Schmitt-trigger inputs, like those found on the HCS family of devices, can support unlimited edge rates.
   - Input thresholds are listed in the *Electrical Characteristics*.
   - Inputs include positive clamp diodes. Input voltages can exceed the device's supply so long as the clamp current ratings are observed from the *Absolute Maximum Ratings*. Do not exceed the absolute maximum voltage rating of the device or it could be damaged.
2. Recommended Output Conditions:
   - Load currents should not exceed the value listed in the *Absolute Maximum Ratings*.
   - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the

Copyright © 2019, Texas Instruments Incorporated

Typical Application (continued)

output current.

9.2.3 Application Curve

Figure 13. Application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* table. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. For this device, a 0.1-µF capacitor is recommended. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminals as possible for best results.

11 Layout

11.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 channels are used. Such input pins should not be left completely unconnected because the unknown voltages result in undefined operational states.

Specified in Figure 14 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is recommended to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This pin keeps the input section of the I/Os from being disabled and floated.

11.2 Layout Example

Figure 14. Layout Example

Copyright © 2019, Texas Instruments Incorporated

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report
- Texas Instruments, *Reduce Noise and Save Power with the New HCS Logic Family* application report
- Texas Instruments, *Understanding Schmitt Triggers* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

Copyright © 2019, Texas Instruments Incorporated

12.14 Diode

RFN1VWM2STF

Ultra Fast Recovery Diode

Data sheet

V_R	200	V
I_o	1	A
I_{FSM}	20	A
$t_{rr(Typ.)}$	14	ns

● Outline

Package Code	PMDE
JEITA Code	-
ROHM Code	PMDE

● Features

Low forward voltage
Low switching loss
High current overload capacity

● Inner Circuit

(1)Cathode
(2)Anode

● Application

General rectification

● Packaging Specifications

Packing	Embossed Tape
Reel Size(mm)	180
Taping Width(mm)	8
Quantity(pcs)	3000
Taping Code	TR
Marking	2F

● Structure

Silicon epitaxial planar

● Absolute Maximum Ratings (T_c=25℃ unless otherwise specified)

Parameter	Symbol	Conditions		Limits	Unit
Repetitive peak reverse voltage	V_{RM}	Duty≦0.5		200	V
Reverse voltage	V_R	Reverse direct voltage		200	V
Average rectified forward current	I_o	60Hz half sin waveform resistive load	T_c=148℃	1	A
Peak forward surge current	I_{FSM}	60Hz half sin waveform, Non-repetitive, T_j=25℃		20	A
Junction temperature	T_j	-		175	℃
Storage temperature	T_{stg}	-		-55 ~ 175	℃

●Electrical Characteristics (T_j=25℃ unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward voltage	V_F	I_F=1A	0.75	0.85	0.93	V
Reverse current	I_R	V_R=200V	-	-	1	μA
Reverse recovery time	t_{rr}	I_F=0.5A, I_R=1.0A, I_{rr}=0.25xI_R	-	14	25	ns

© 2022- ROHM Co., Ltd. All rights reserved.

● Characteristic Curves

V_F-I_F CHARACTERISTICS

V_R-I_R CHARACTERISTICS

V_R-C_t CHARACTERISTICS

© 2022- ROHM Co., Ltd. All rights reserved.

RFN1VWM2STF Data sheet

● Characteristic Curves

IFSM-CYCLE CHARACTERISTICS

IFSM-TIME CHARACTERISTICS

Rth-t CHARACTERISTICS

© 2022- ROHM Co., Ltd. All rights reserved.

● Characteristic Curves

DERATING CURVE(I_o-T_a)

DERATING CURVE(I_o-T_C)

I_o-P_F CHARACTERISTICS

© 2022- ROHM Co., Ltd. All rights reserved.

12.15 NMOS Datasheet

VISHAY
www.vishay.com

SQ2348ES
Vishay Siliconix

Automotive N-Channel 30 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	30
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.024
$R_{DS(on)}$ (Ω) at V_{GS} = 4.5 V	0.032
I_D (A)	8
Configuration	Single

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified [c]
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE
Pb-free
RoHS COMPLIANT
HALOGEN FREE

SOT-23 (TO-236)

Top View

N-Channel MOSFET

Marking Code: 8Vxxx

ORDERING INFORMATION	
Package	SOT-23
Lead (Pb)-free and Halogen-free	SQ2348ES-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25 °C	I_D	8	A
	T_C = 125 °C		5.3	
Continuous Source Current (Diode Conduction)		I_S	3.8	
Pulsed Drain Current [a]		I_{DM}	32	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	15.5	
Single Pulse Avalanche Energy		E_{AS}	12	mJ
Maximum Power Dissipation [a]	T_C = 25 °C	P_D	3	W
	T_C = 125 °C		1	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount [b]	R_{thJA}	166	°C/W
Junction-to-Foot (Drain)		R_{thJF}	50	

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. When mounted on 1" square PCB (FR4 material).
c. Parametric verification ongoing.

For technical questions, contact: automostechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		30	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1.5	2.0	2.5	
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 30 V	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = 30 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 30 V, T_J = 175 °C	-	-	150	
On-State Drain Current [a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	10	-	-	A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 12 A	-	0.020	0.024	Ω
		V_{GS} = 10 V	I_D = 12 A, T_J = 125 °C	-	-	0.036	
		V_{GS} = 10 V	I_D = 12 A, T_J = 175 °C	-	-	0.042	
		V_{GS} = 4.5 V	I_D = 8 A	-	0.026	0.032	
Forward Transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 3 A		-	10	-	S
Dynamic [b]							
Input Capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 15 V, f = 1 MHz	-	430	540	pF
Output Capacitance	C_{oss}			-	100	125	
Reverse Transfer Capacitance	C_{rss}			-	40	50	
Total Gate Charge [c]	Q_g	V_{GS} = 10 V	V_{DS} = 15 V, I_D = 5.5 A	-	7.95	14.5	nC
Gate-Source Charge [c]	Q_{gs}			-	1.6	-	
Gate-Drain Charge [c]	Q_{gd}			-	1.3	-	
Gate Resistance	R_g	f = 1 MHz		8.65	17.3	27	Ω
Turn-On Delay Time [c]	$t_{d(on)}$	V_{DD} = 15 V, R_L = 3.4 Ω I_D ≅ 4.4 A, V_{GEN} = 10 V, R_g = 1 Ω		-	4.5	7	ns
Rise Time [c]	t_r			-	8	12	
Turn-Off Delay Time [c]	$t_{d(off)}$			-	21	32	
Fall Time [c]	t_f			-	6	9	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed Current [a]	I_{SM}			-	-	32	A
Forward Voltage	V_{SD}	I_F = 3.5 A, V_{GS} = 0 V		-	0.8	1.2	V

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For technical questions, contact: automostechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

For technical questions, contact: automostechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

12.16 PMOS Datasheet

Si2343CDS
Vishay Siliconix

P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a, e]	Q_g (Typ.)
- 30	0.045 at V_{GS} = - 10 V	- 5.9	7 nC
	0.075 at V_{GS} = - 4.5 V	- 4.6	

FEATURES
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS
- Load Switch
- Notebook Adaptor Switch
- DC/DC Converter

TO-236
(SOT-23)

Top View
Si2343CDS (P1)*
* Marking Code

P-Channel MOSFET

Ordering Information: Si2343CDS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	- 30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 5.9	A
	T_C = 70 °C		- 4.7	
	T_A = 25 °C		- 4.2[b, c]	
	T_A = 70 °C		- 3.3[b, c]	
Pulsed Drain Current		I_{DM}	- 25	
Continous Source-Drain Diode Current	T_C = 25 °C	I_S	- 2.1	
	T_A = 25 °C		- 1[b, c]	
Maximum Power Dissipation	T_C = 25 °C	P_D	2.5	W
	T_C = 70 °C		1.6	
	T_A = 25 °C		1.25[b, c]	
	T_A = 70 °C		0.8[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[b, d]	t ≤ 5 s	R_{thJA}	75	100	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	40	50	

Notes:
a. Based on T_C = 25 °C.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. Maximum under Steady State conditions is 166 °C/W.
e. Package Limited.

Si2343CDS

Vishay Siliconix

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 19		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			4.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = - 250 µA	- 1.2		- 2.5	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 30 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 30 V, V_{GS} = 0 V, T_J = 55 °C			- 5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ - 5 V, V_{GS} = - 10 V	- 25			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 4.2 A		0.037	0.045	Ω
		V_{GS} = - 4.5 V, I_D = - 3.2 A		0.062	0.075	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 4.2 A		10		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 15 V, V_{GS} = 0 V, f = 1 MHz		590		pF
Output Capacitance	C_{oss}			115		
Reverse Transfer Capacitance	C_{rss}			93		
Total Gate Charge	Q_g	V_{DS} = - 15 V, V_{GS} = - 10 V, I_D = - 4.2 A		13.6	21	nC
		V_{DS} = - 15 V, V_{GS} = - 4.5 V, I_D = - 4.2 A		7	11	
Gate-Source Charge	Q_{gs}			2.3		
Gate-Drain Charge	Q_{gd}			3.2		
Gate Resistance	R_g	f = 1 MHz	1	5	10	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 4.5 Ω I_D ≅ - 3.3 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		30	45	ns
Rise Time	t_r			25	38	
Turn-Off Delay Time	$t_{d(off)}$			16	24	
Fall Time	t_f			8	16	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 4.5 Ω I_D ≅ - 3.3 A, V_{GEN} = - 10 V, R_g = 1 Ω		8	16	
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			18	27	
Fall Time	t_f			8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 4.2	A
Pulse Diode Forward Current	I_{SM}				- 25	
Body Diode Voltage	V_{SD}	I_S = - 3.3 A, V_{GS} = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 3.3 A, dI/dt = 100 A/µs, T_J = 25 °C		17	26	ns
Body Diode Reverse Recovery Charge	Q_{rr}			9	18	nC
Reverse Recovery Fall Time	t_a			10		ns
Reverse Recovery Rise Time	t_b			7		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

Si2343CDS

Vishay Siliconix

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power (Junction-to-Ambient)

* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Current Derating*

Power, Junction-to-Foot

Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Si2343CDS

Vishay Siliconix

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65474.