```
        W R S                              W R H
      S Z E E D A                        V U F C H E
  Z S T W G T E   H U              G L Q J R W X R F
  R C I S C A U C G                X N H A O L P A A
  O E E M J O R P N F              K C D E E J J B W B
  M Z H F U K D O M E              U N S R H D V Z D N
  N U A C Y L T E T O I        D L E L L A R A P R H
    T W Y R Z A Z L S C C H R H O T P Q S S A T
      C E R A W T F O S R S H Q A O X F A N H
        K N Z K I R J K E D H W W S
            C O O C Y P P E Y
        A I S R N N G Y R U G X E
        D G S K R R E S U L T S Y R P
    V W O E E P E R F O R M A N C E I P M
    V B L C F E T A L U C L A C M M Q S T E S
    V X O H C F N E T W O R K F K F P X Z M F
  F D R Z G R F U T U R E D O K Q E H L E O Z O
  F P Y R O A B U F   A L J   R E Q W L L R E U
  A R J J U Y W I Z   S C Y   D Q J L H W Y X V
  S W Z X T T B V     S O N     F I L E I H N T
  T N D E P L F       R P P             L I N G
    G L N U W         F I X             W M N
      W H T           Z H A             R Y
                      T C X
                      A P A
```

ARCHER
BYTE
CALCULATE
CHIP
CODE
COOLING
CRAY
DATA
FAST
FILE

FUTURE
HARDWARE
LOGIC
MEMORY
NETWORK
OUTPUT
PARALLEL
PERFORMANCE
POWER
PROCESSOR

RESEARCH
RESULTS
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