



A E
V C
L O M M
D A A W
E K B R T P
U N R G E S
E Y G T O Q Q Q
T E P G R J E O
S Q H O Y P D R P F
F R C R A Y Q U R C
U N A O T E R N T O W O
K R E S U L T S U S P D
Z T J P E T T Z Y F S A O U
L U Z R S P E E D B E U K I
T C X A R U U U P Y D C M E L A
C M W E E P J Y L O A O J N C F
I E T S P E X K T C L T R X U S Q B
G F E I R E Q X Z P G A P N G G Y D
S O A P F Y X U N L T V D L I C K G F F
S R C O N O I T A L U M I S F K R K Q V
X C Z R S U P E R C O M P U T E R H W E T B
H Q M S M V M O T U P T U O Y G J C R X I Q
L H A O C E F O P A R A L L E L G E A O M C D Z
S N H J Q C X V A Y H Y Y P B F Q W W E O A I F
T C G I G L R P E D P Y O N V Y R D M L I E L W U U
E I P I H C P Q R X X K V U B I R P O W E R L I C U
N L E F O M A L O I R E H C R A A K R O W T E N I N L Z
E G N U E N F N C K L W P H P H B W E Z T F U G J F G X
B A U C X U I Y Z T V A S T O R A G E J V Y R O M E M O T M
G L S E L B A C Q O A Z G C A L C U L A T E L U Q A Y F I Y

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BYTE

CABLES

CALCULATE

CHIP

CODE

COOLING

CRAY

DATA

FAST

FILE

FUTURE

HARDWARE

LOGIC

MEMORY

NETWORK

OUTPUT

PARALLEL

PERFORMANCE

POWER

PROCESSOR

PROGRAM

RESEARCH

RESULTS

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