Practice quiz Electrical characterization

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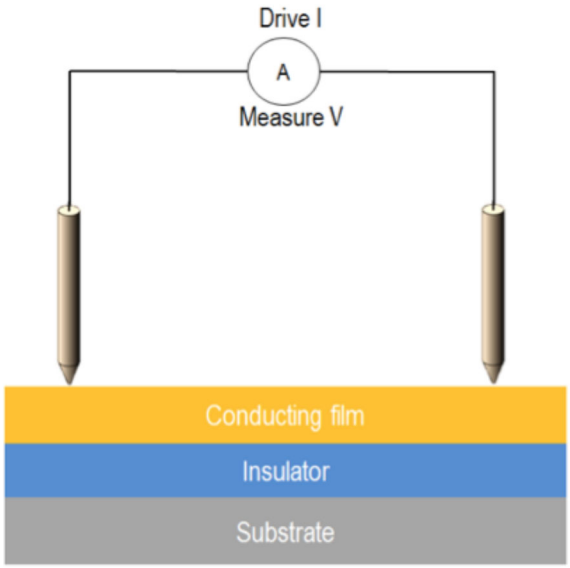
Questions:

0 points possible (ungraded)

1. Let us consider an electronic multimeter that has 1% accuracy and the possibility to work in both 2-point (see the following picture) and 4-point mode. Assuming the per-branch parasitic resistance is 1 Ohm, what is the minimum resistance you can measure with the 2-point approach? Consider a factor of 10 as error margin.



- ○ 1 mOhm
- ○ 10 mOhm
- ◉ 200 mOhm
- ○ 20 mOhm

✔

Explanation

As shown in the picture, at least two connections are required for the current to flow. Consequently, the overall parasitic resistance is equal to 2 Ohm. Such a value fixes the measurement range. Since the equipment has 1% accuracy, the target resistance cannot be lower than 1%*2 Ohm = 20 mOhm, otherwise the signal cannot be distinguished from the parasitic noise. By considering a factor of 10 for error margin, i.e. 10 % tolerance, the minimum measurable resistance turns out to be 200 mOhm. It is remarkable that the number of probes is limited, so setting the instrument to the 2-point mode may be useful to employ the other connections for multiple measurements at the same time.

2. Let us consider the metal connections in a bi-morph thermal actuator. Which of the following are good strategies to minimize the parasitic resistance and the capacitance of the metal connections?

- ☑ Increase the thickness of the metal connections.
- ☐ Maximize the square number of the metal connections.
- ☑ Reduce the overall area of the metal connections on the silicon substrate.
- ☐ Increase the sheet resistance of the metal connections.

✔

Explanation

Explanation

In order to minimize the parasitic resistance of the metal connections, one should increase the thickness since R=resistivity*L/w/t, where L is the length, w is the width and t is the thickness of the metal connections. Moreover, maximizing the square number is not a good strategy as the overall resistance is proportional to the sheet resistance times the square number. Finally, the overall area created by metal connections should be reduced to minimize the parasitic capacitance existing between the metal and the silicon substrate.

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Answers are displayed within the problem

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