



<u>Course</u> <u>Progress</u> <u>Dates</u> <u>Discussion</u> <u>Resources</u> <u>Search</u> <u>Course team</u>



| substra  | possible (ungraded)<br>h one is a useful step for fabricating a thin Si membrane by wet etching starting from a monolithic<br>ate?  | Si          |
|--|---|-------------|
|  | nstead of taking pure Si, take a wafer which is completely doped with boron at a concentration above 10 <sup>14</sup> atoms/cm <sup>3</sup>   |             |
|  | Placing the Si wafer in a KOH anisotropic bath  |             |
| 0 1  | mmersing the Si wafer in Piranha solution   |             |
| 0 1  | Dipping before etching the wafer in a concentrated acetone solution © All Rig   | nts Res     |
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| <b>E</b> ∳ <b>§</b> ∮avi   | Privacy Policy  |             |
| single of<br>put the<br>we pro<br>imposs<br>layer an<br>used to<br>"Anisot | opic etching baths can be used for making very thin Si membranes of the order of 1 µm thickness. crystalline Si substrate is normally around 500 µm thickness. If we have a mask opening structure a Si wafer in a KOH bath, the etching stops at certain planes of the crystal, usually the (111) planes. I ceed in time, the thickness of the Si substrate in the middle becomes always smaller, but it is ible to stop this process exactly when there is only 1 µm left. One can implant boron in a very thin nd, when the KOH etchant reaches the boron-implanted layer, the etching stops. This method that is structure micron-features into thick Si substrates is also named "bulk micromachining". See ropic and isotropic wet etching of Si and applications" video 7:05 to 8:45 for detailed explanations. rface micro-machining, a thin Si membrane can be fabricated by removing a SiO <sub>2</sub> sacrificial layer h a Si functional layer. Which of the following is true for this process? | nd<br>f     |
|  |   |             |
| 0  | No access holes are needed on the polySi to remove the SiO <sub>2</sub> layer by wet etching  |             |
|  | The SiO $_2$ layer can only be patterned by KOH etching   |             |
| 0  |   |             |
| 0 1  | The ${ m SiO_2}$ layer can only be patterned by KOH etching   |             |
| 0 1  | The $SiO_2$ layer can only be patterned by KOH etching  Wet etching of $SiO_2$ is performed by adding an electrical contact to the $Si$ wafer   |             |
| Explan Wet etc SiO <sub>2</sub> . TI the pat etching needed                | The SiO <sub>2</sub> layer can only be patterned by KOH etching  Wet etching of SiO <sub>2</sub> is performed by adding an electrical contact to the Si wafer  A polySi layer is deposited in the form of a thin film on top of a patterned SiO <sub>2</sub> layer  ation  thing permits to make thin membranes by first depositing and patterning of a sacrificial layer like his patterning can be made by dry or wet etching. The next step is the deposition of a polySi layer of terned SiO <sub>2</sub> layer. It can be deposited by LPCVD for example. The final step in the process is the weight SiO <sub>2</sub> in a HF bath forming fluorosilicic acid (H <sub>2</sub> SiF <sub>6</sub> ). Access holes through the polySi layer are at to remove the SiO <sub>2</sub> layer. This is an example of a "surface micromachining" process. See "Anisotro tropic wet etching of Si and applications" video from 11:10 to 13:00 for detailed explanations.  | t           |