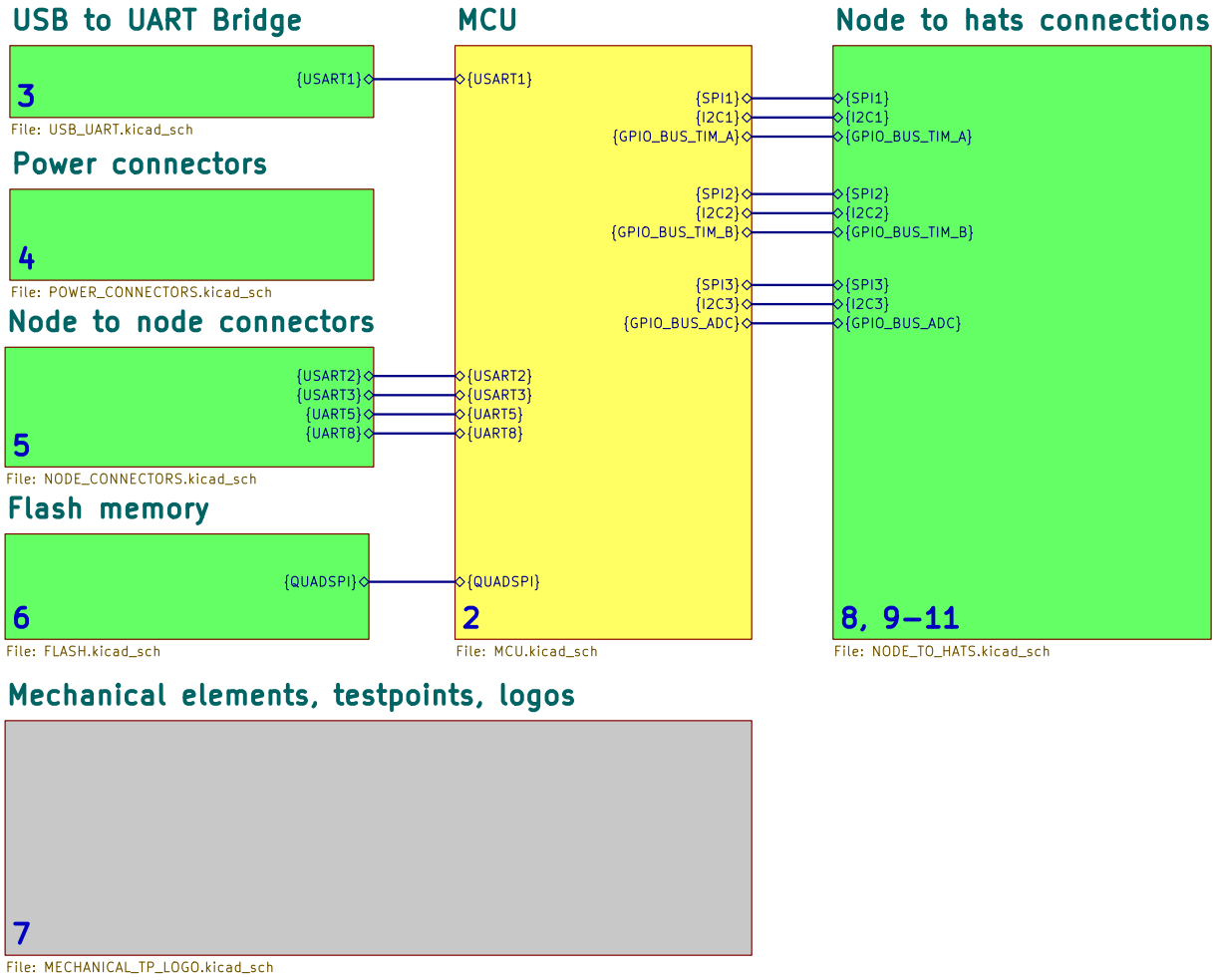
Orion PCB node overview



Author: Vincent Nguyen

EPFL Xplore

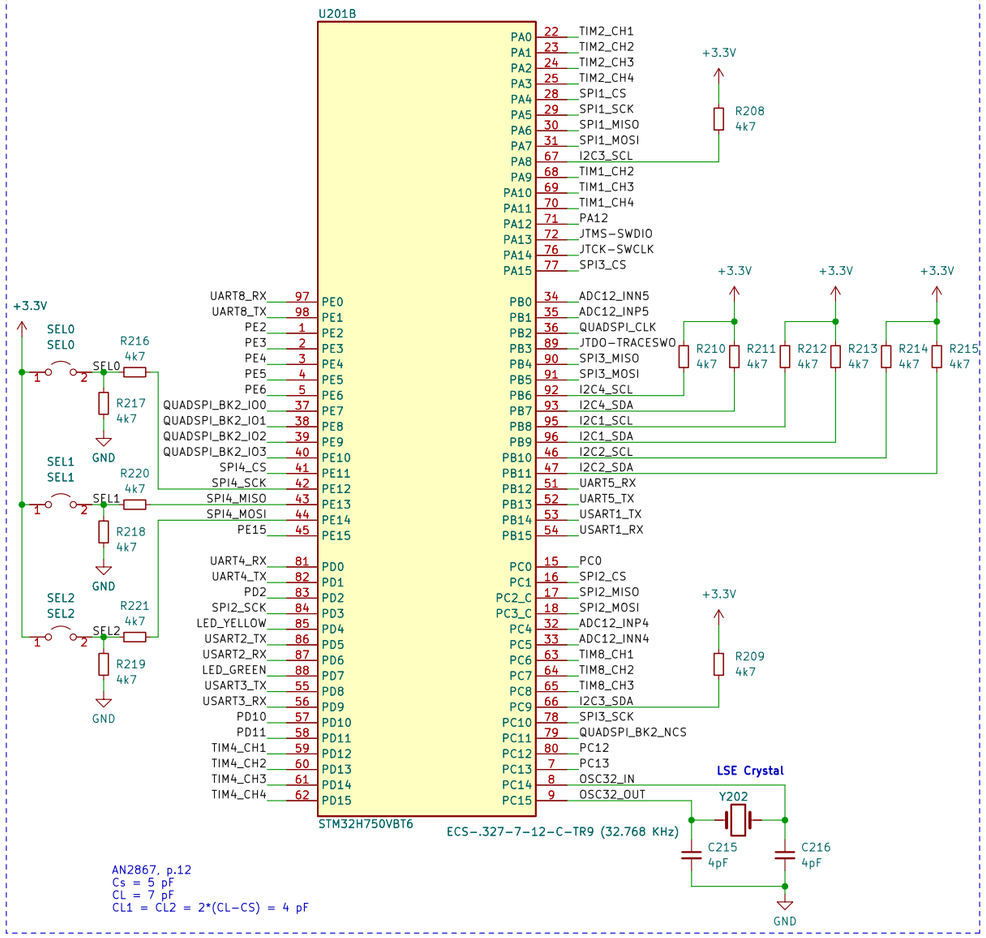
Sheet: /
File: orion_pcb.kicad_sch

Title: Orion PCB Node Overview

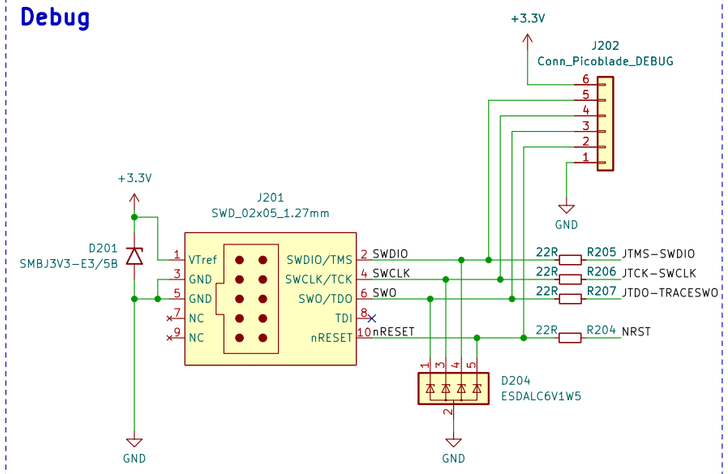
Size: A4	Date:	**Rev:**
KiCad E.D.A. eeschema (6.0.7)		Id: 1/11

MCU (STM32H750VBT6)

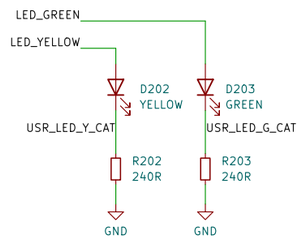
GPIO, UART, SPI, TIMERS, I2C, ADC



Debug

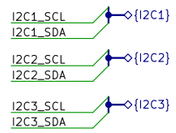


Status LEDs (user-controlled)

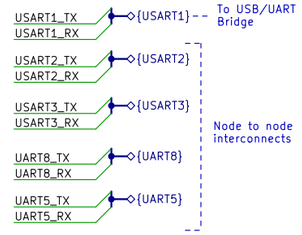


Buses

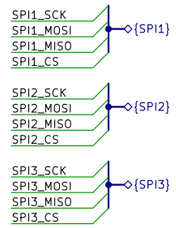
I2C



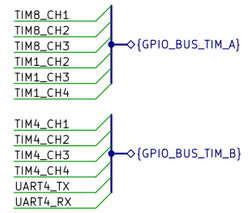
UART



SPI

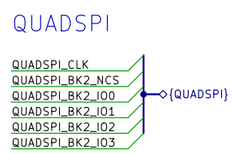


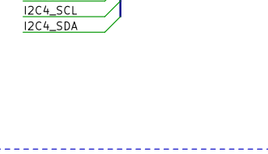
GPIO



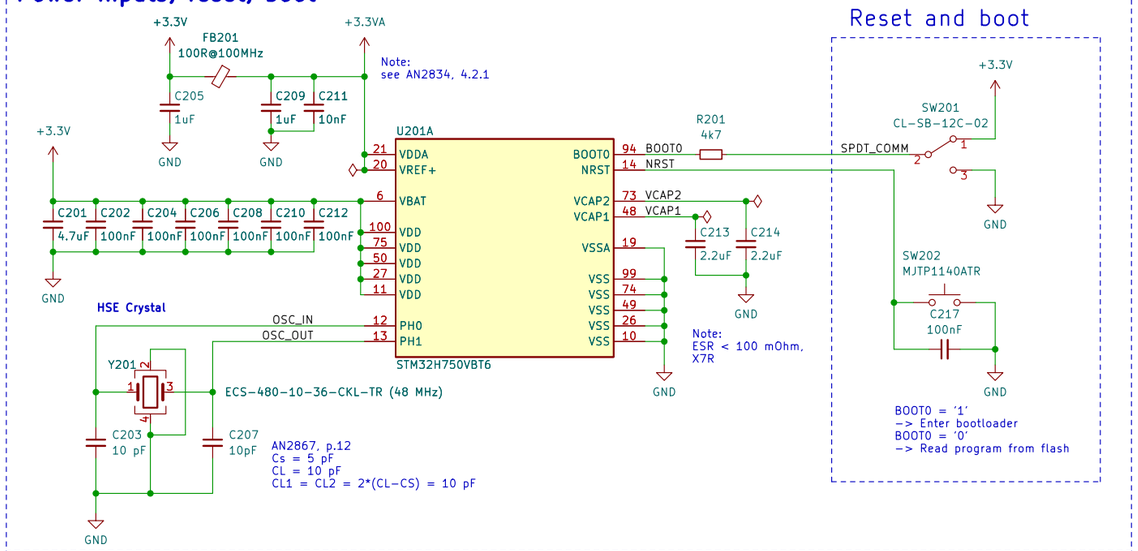
We only use one slave select pin per SPI bus. This means we are limited to one slave per SPI (unless a GPIO is reconfigured) which is enough.

QUADSPI





Power inputs, reset, boot



Reset and boot

Author: Vincent Nguyen

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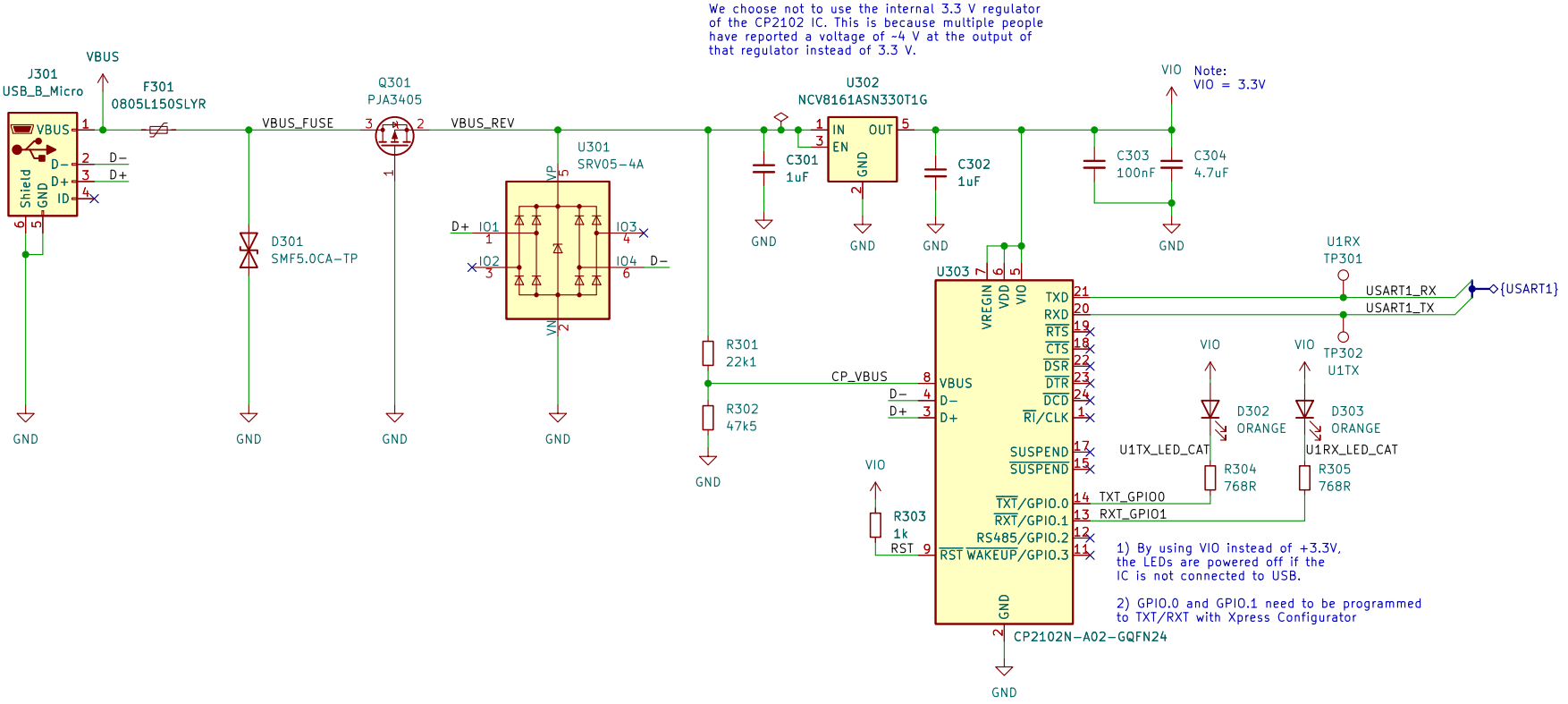
Sheet: /MCU/
File: MCU.kicad_sch

Title: MCU

Size: A3	Date:	Rev:
KiCad E.D.A. eeschema (6.0.7)		Id: 2/11

USB to UART bridge



Author: Vincent Nguyen

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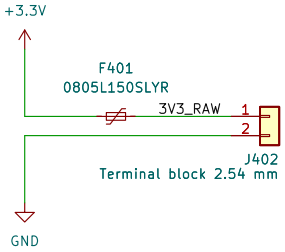
Sheet: /USB to UART Bridge/
File: USB_UART.kicad_sch

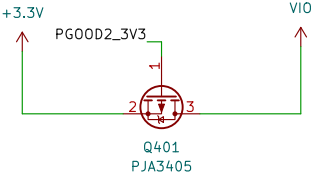
Title: USB to UART Bridge

Size: A4	Date:	**Rev:**
KiCad E.D.A. eeschema (6.0.7)		Id: 3/11

Raw power input



Power path



Diode forward voltage VDS = 1.2 V (VSD = −1.2 V)

1) External power is not connected (PGOOD2 = 0 V)

1a) USB is connected (VIO = 3.3 V)
Initially:
VS = VIO − VDS = 3.3 V − 1.2 V = 2.1 V
VGS = VG − VS = 0 V − 2.1 V = −2.1 V <= VGS(th) -> CLOSED
Then:
CLOSED -> VS = VD = VIO = 3.3 V
VGS = VG − VS = 0 V − 3.3 V < VGS(th) -> stays CLOSED

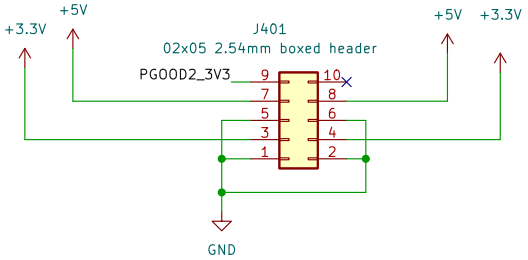
1b) USB is disconnected (VIO = 0 V)
No voltages, everything is at 0 V

2) External power is connected (PGOOD2 = 5 V, VS = 3.3 V)

2a) USB is connected (VIO = 3.3 V)
VGS = VG − VS = 5 V − 3.3 V = 1.7 V > VGS(th) -> OPEN

2b) USB is disconnected (VIO = 0 V)
VGS = VG − VS = 5 V − 3.3 V = 1.7 V > VGS(th) -> OPEN

Voltage regulator connector



Author: Vincent Nguyen

EPFL Xplore

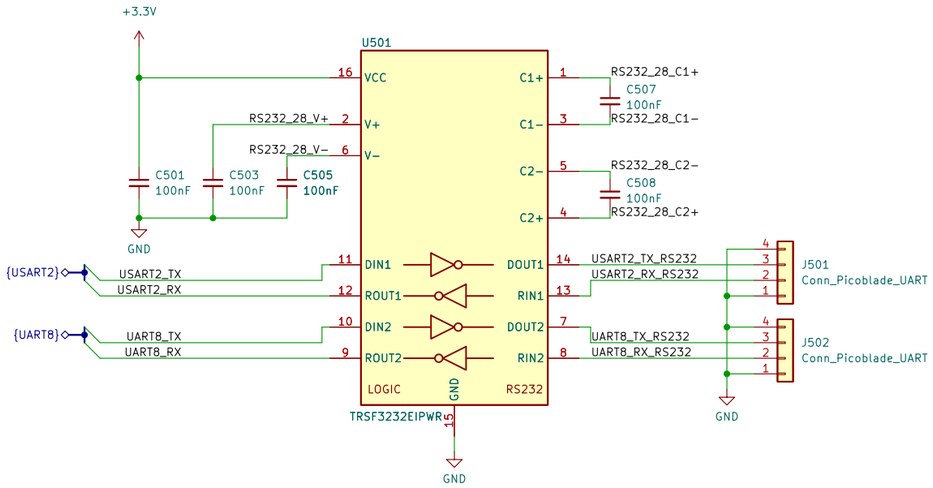
Sheet: /Power connectors/
File: POWER_CONNECTORS.kicad_sch

Title: External Connectors and Power Path

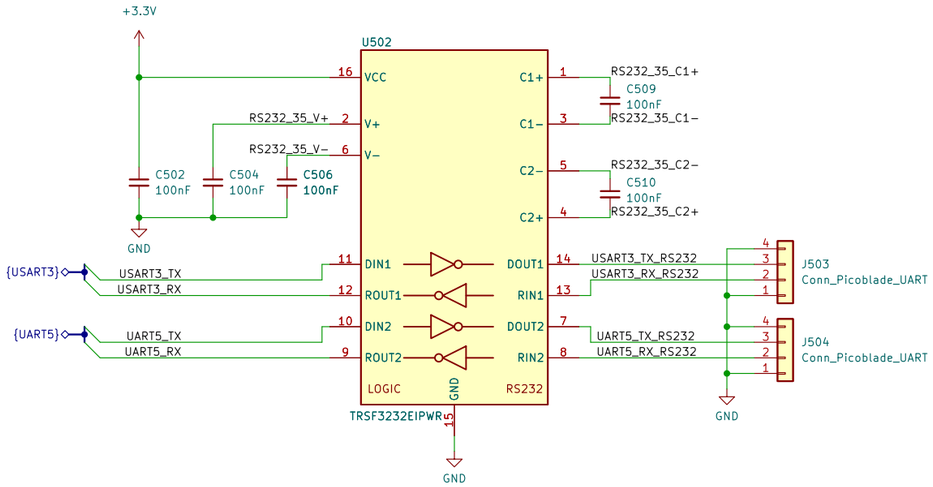
Size: A5	Date:	**Rev:**
KiCad E.D.A. eeschema (6.0.7)		Id: 4/11

RS232 Transceivers

USART2, USART8



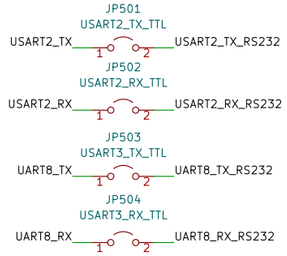
UART3, UART5



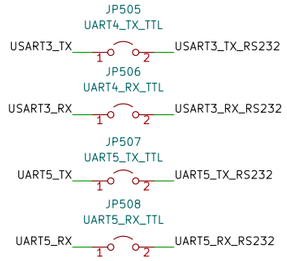
Maximum speed is 250 kb/s if using RS232 transceiver

Jumpers

USART2, USART8



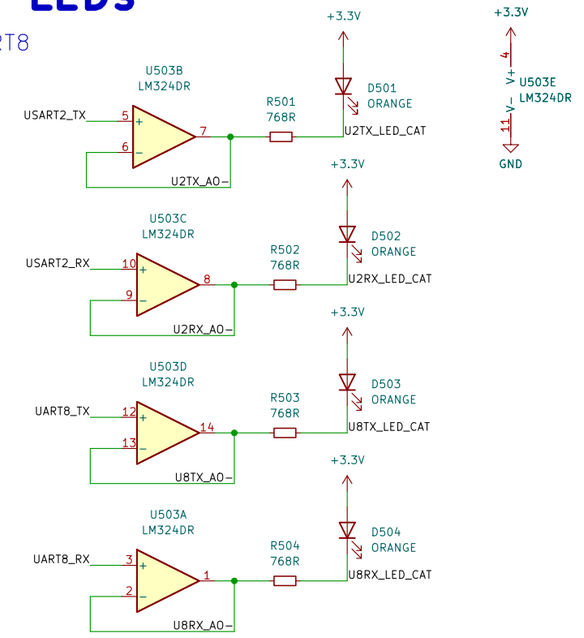
UART3, UART5



To use TTL voltage levels, short ALL of the jumpers
for both nodes, for the corresponding UART buses.

Activity LEDs

USART2, USART8



UART3, UART5

Activity LEDs don't need to be very bright.
We choose If = 1.7 mA
R = (3.3 V − 2 V)/(2 mA) = 765 Ohm
Closest standard resistor −> 768 Ohm

Author: Vincent Nguyen

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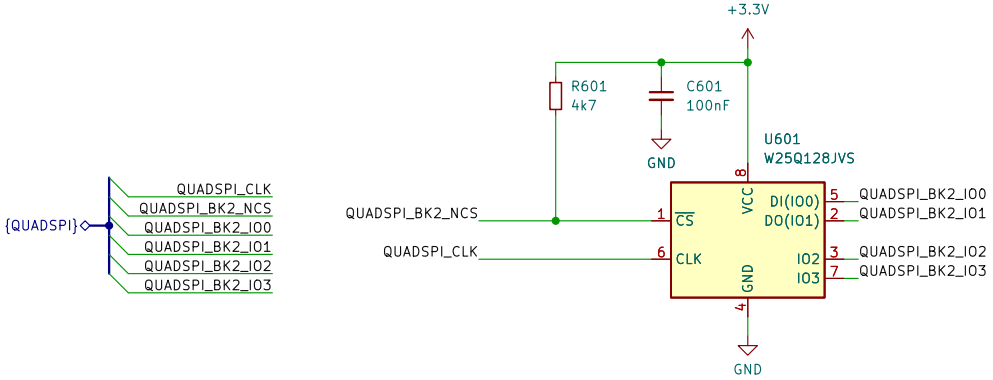
Sheet: /Node to node connectors/ File: NODE_CONNECTORS.kicad_sch		
Title: RS232 UART Node to Node Connectors		
Size: A3	Date:	**Rev:**
KiCad E.D.A. eeschema (6.0.7)		Id: 5/11

Quad-SPI external flash memory



Author: Vincent Nguyen

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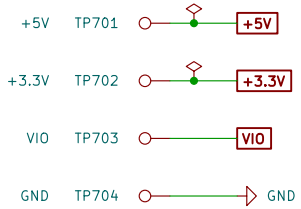
Sheet: /Flash memory/
File: FLASH.kicad_sch

Title: External Flash Memory

Size: A5	Date:	**Rev:**
KiCad E.D.A. eeschema (6.0.7)		Id: 6/11

Test points



Mounting holes

H701 MountingHole
H702 MountingHole
H703 MountingHole
H704 MountingHole
H705 MountingHole
H706 MountingHole
H707 MountingHole
H708 MountingHole

Logos

Xplore
EPFL
maxon
APCO TECHNOLOGIES
ELCA
astrocast

Author: Vincent Nguyen

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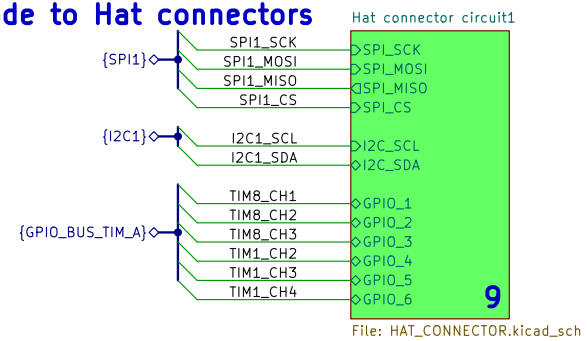
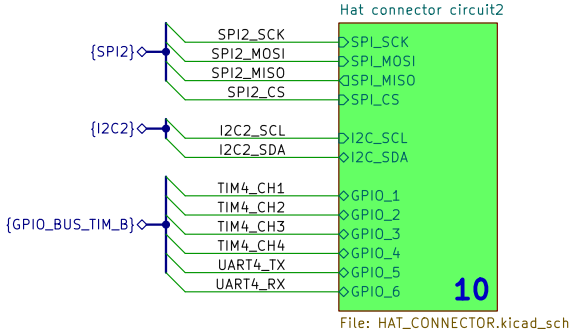
Sheet: /Mechanical elements, testpoints, logos/
File: MECHANICAL_TP_LOGO.kicad_sch

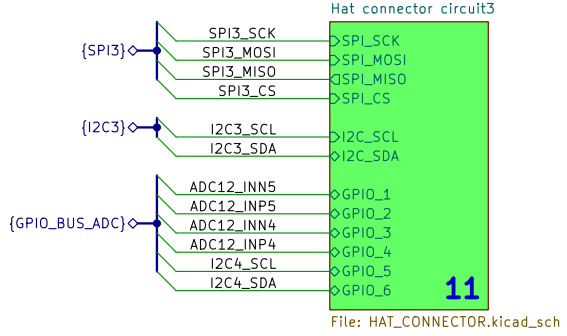
Title: Mechanical Elements and Test Points

Size: A5	Date:	**Rev:**
KiCad E.D.A. eeschema (6.0.7)		Id: 7/11

Node to Hat connectors







Author: Vincent Nguyen

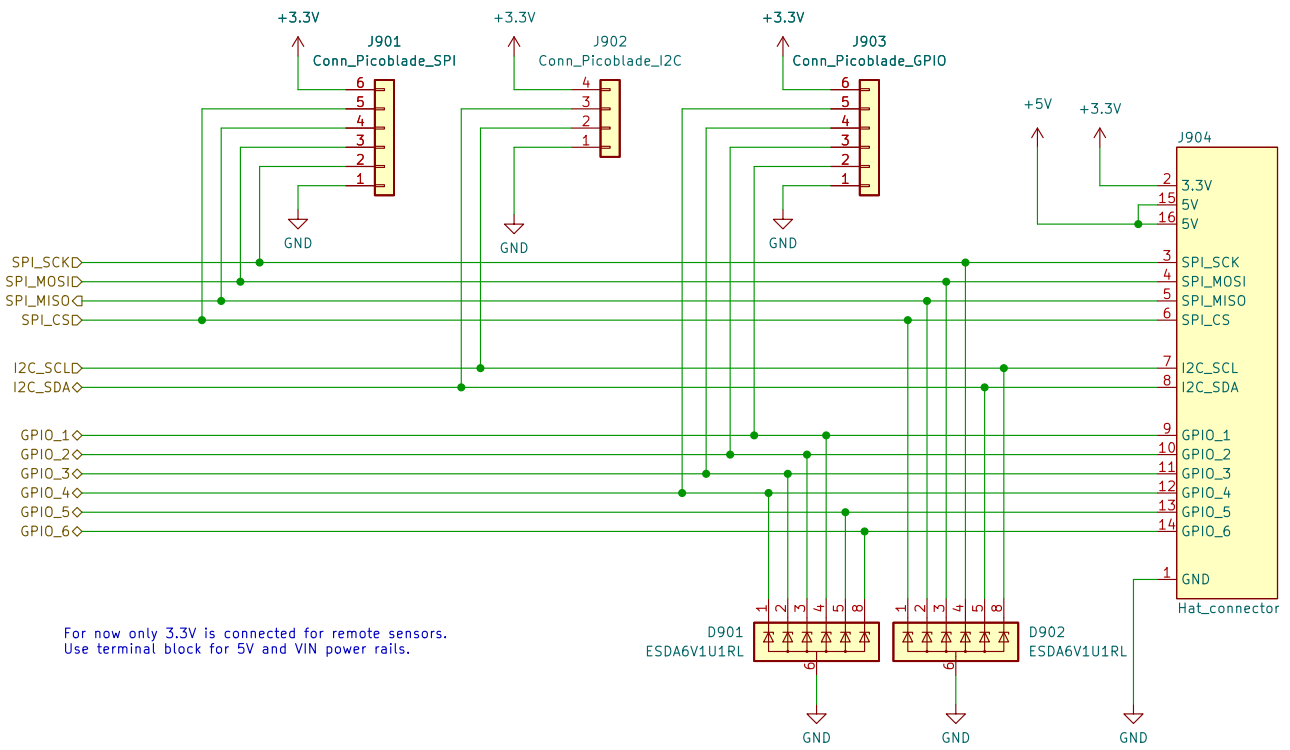
EPFL Xplore

Sheet: /Node to hats connections/
File: NODE_TO_HATS.kicad_sch

Title: Hat Connectors and Delocalized Connectors

Size: A5	Date:	**Rev:**
KiCad E.D.A. eeschema (6.0.7)		Id: 8/11

Hat connector



Author: Vincent Nguyen

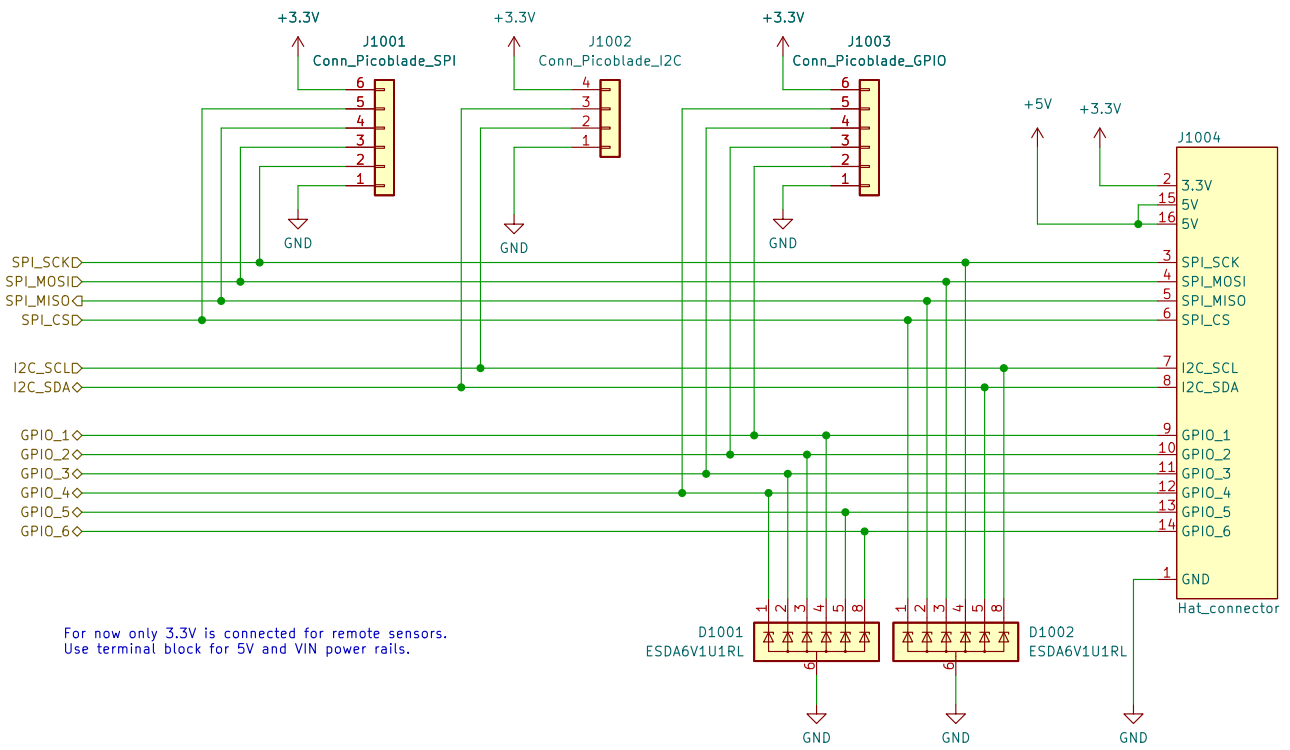
EPFL Xplore

Sheet: /Node to hats connections/Hat connector circuit1/
File: HAT_CONNECTOR.kicad_sch

Title: Hat Connector

Size: A4	Date:	**Rev:**
KiCad E.D.A. eeschema (6.0.7)		Id: 9/11

Hat connector



Author: Vincent Nguyen

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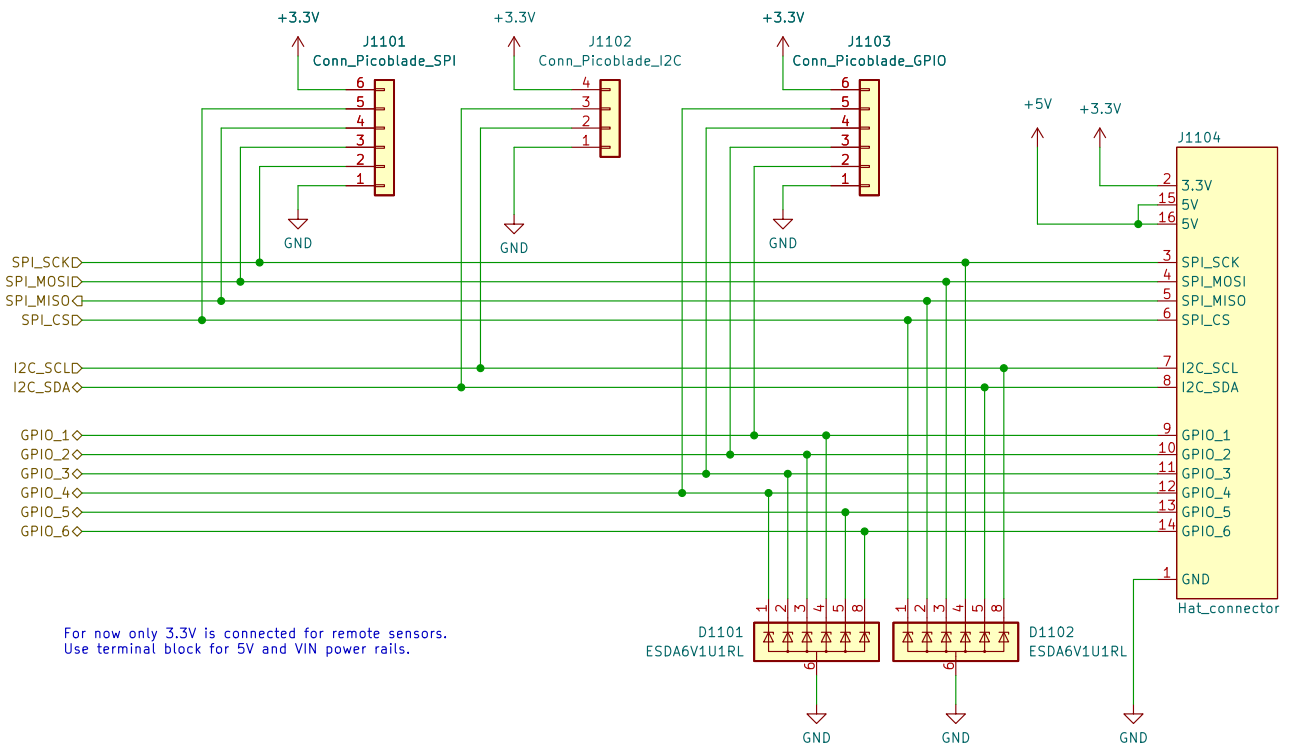
Sheet: /Node to hats connections/Hat connector circuit2/
File: HAT_CONNECTOR.kicad_sch

Title: Hat Connector

Size: A4	Date:	**Rev:**
KiCad E.D.A. eeschema (6.0.7)		Id: 10/11

Hat connector



Author: Vincent Nguyen

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Sheet: /Node to hats connections/Hat connector circuit3/
File: HAT_CONNECTOR.kicad_sch

Title: Hat Connector

Size: A4	Date:	**Rev:**
KiCad E.D.A. eeschema (6.0.7)		Id: 11/11