
STM32
CubeMX

1. Description

1.1. Project

Project Name	Orion_FW
Board Name	custom
Generated with:	STM32CubeMX 6.9.0
Date	09/01/2023

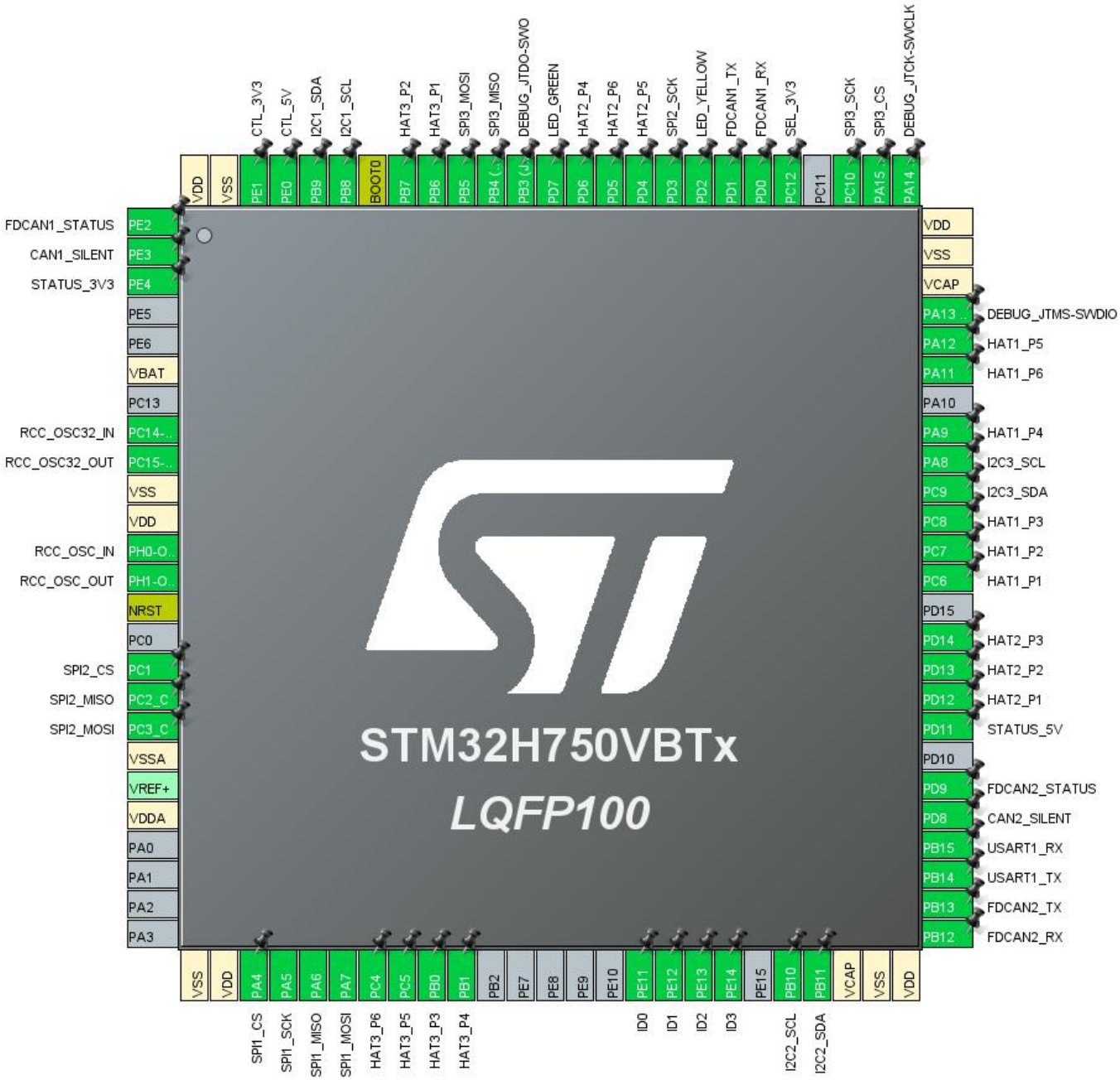
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H750 Value line
MCU name	STM32H750VBTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	ARM Cortex-M7

2. Pinout Configuration



3. Pins Configuration

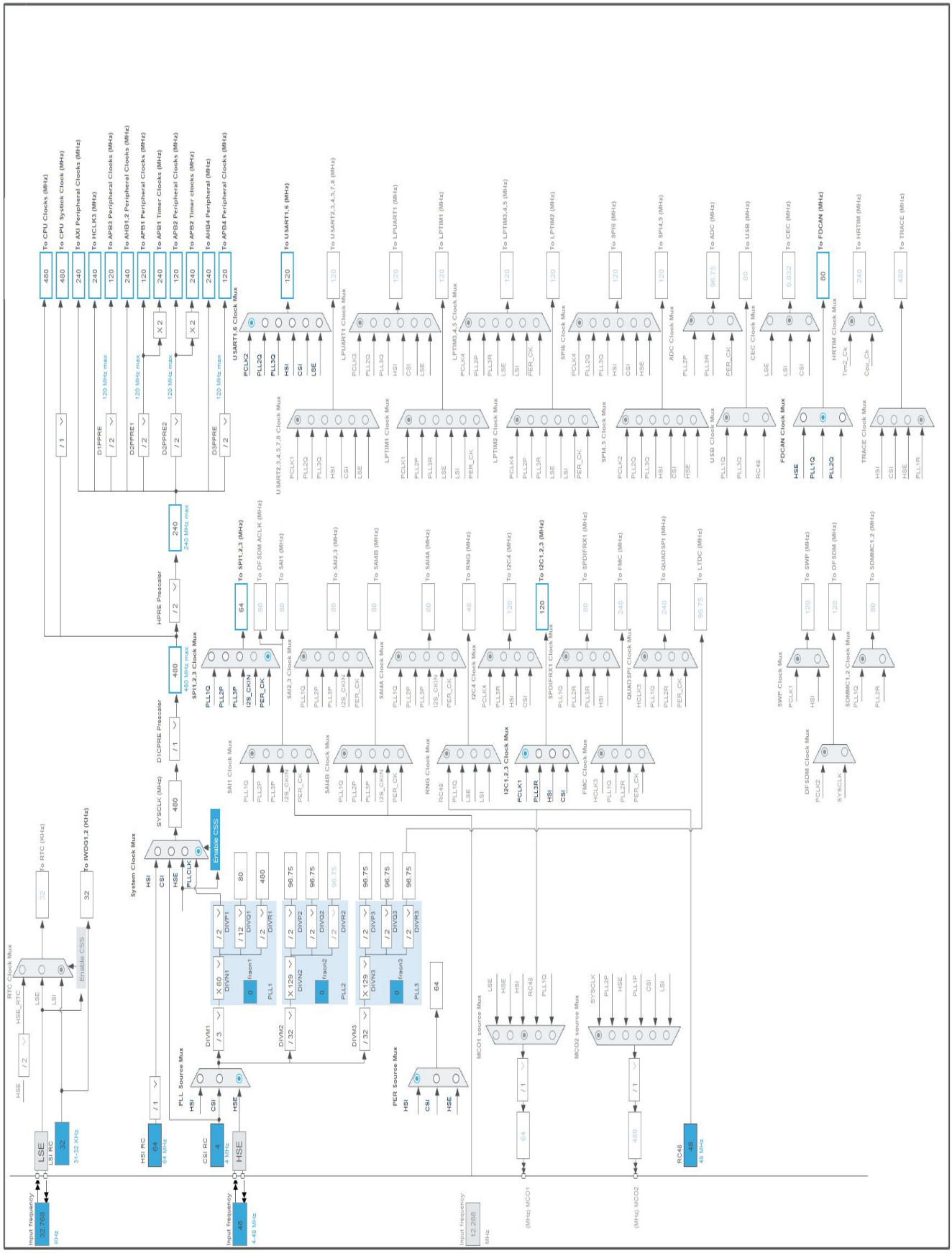
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	FDCAN1_STATUS
2	PE3 *	I/O	GPIO_Output	CAN1_SILENT
3	PE4 *	I/O	GPIO_Input	STATUS_3V3
6	VBAT	Power		
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
16	PC1 *	I/O	GPIO_Output	SPI2_CS
17	PC2_C	I/O	SPI2_MISO	
18	PC3_C	I/O	SPI2_MOSI	
19	VSSA	Power		
21	VDDA	Power		
26	VSS	Power		
27	VDD	Power		
28	PA4 *	I/O	GPIO_Output	SPI1_CS
29	PA5	I/O	SPI1_SCK	
30	PA6	I/O	SPI1_MISO	
31	PA7	I/O	SPI1_MOSI	
32	PC4 *	I/O	GPIO_Output	HAT3_P6
33	PC5 *	I/O	GPIO_Output	HAT3_P5
34	PB0 *	I/O	GPIO_Output	HAT3_P3
35	PB1 *	I/O	GPIO_Output	HAT3_P4
41	PE11 *	I/O	GPIO_Input	ID0
42	PE12 *	I/O	GPIO_Input	ID1
43	PE13 *	I/O	GPIO_Input	ID2
44	PE14 *	I/O	GPIO_Input	ID3
46	PB10	I/O	I2C2_SCL	
47	PB11	I/O	I2C2_SDA	
48	VCAP	Power		
49	VSS	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
50	VDD	Power		
51	PB12	I/O	FDCAN2_RX	
52	PB13	I/O	FDCAN2_TX	
53	PB14	I/O	USART1_TX	
54	PB15	I/O	USART1_RX	
55	PD8 *	I/O	GPIO_Output	CAN2_SILENT
56	PD9 *	I/O	GPIO_Output	FDCAN2_STATUS
58	PD11 *	I/O	GPIO_Input	STATUS_5V
59	PD12 *	I/O	GPIO_Output	HAT2_P1
60	PD13 *	I/O	GPIO_Output	HAT2_P2
61	PD14 *	I/O	GPIO_Output	HAT2_P3
63	PC6 *	I/O	GPIO_Output	HAT1_P1
64	PC7 *	I/O	GPIO_Output	HAT1_P2
65	PC8 *	I/O	GPIO_Output	HAT1_P3
66	PC9	I/O	I2C3_SDA	
67	PA8	I/O	I2C3_SCL	
68	PA9 *	I/O	GPIO_Output	HAT1_P4
70	PA11 *	I/O	GPIO_Output	HAT1_P6
71	PA12 *	I/O	GPIO_Output	HAT1_P5
72	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
77	PA15 (JTDI) *	I/O	GPIO_Output	SPI3_CS
78	PC10	I/O	SPI3_SCK	
80	PC12 *	I/O	GPIO_Output	SEL_3V3
81	PD0	I/O	FDCAN1_RX	
82	PD1	I/O	FDCAN1_TX	
83	PD2 *	I/O	GPIO_Output	LED_YELLOW
84	PD3	I/O	SPI2_SCK	
85	PD4 *	I/O	GPIO_Output	HAT2_P5
86	PD5 *	I/O	GPIO_Output	HAT2_P6
87	PD6 *	I/O	GPIO_Output	HAT2_P4
88	PD7 *	I/O	GPIO_Output	LED_GREEN
89	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	
90	PB4 (NJTRST)	I/O	SPI3_MISO	
91	PB5	I/O	SPI3_MOSI	
92	PB6 *	I/O	GPIO_Output	HAT3_P1

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
93	PB7 *	I/O	GPIO_Output	HAT3_P2
94	BOOT0	Boot		
95	PB8	I/O	I2C1_SCL	
96	PB9	I/O	I2C1_SDA	
97	PE0 *	I/O	GPIO_Output	CTL_5V
98	PE1 *	I/O	GPIO_Output	CTL_3V3
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Orion_FW
Project Folder	C:\Users\vince\STM32CubeIDE\workspace_1.13.0\AV_SW_workspace\Orion_F
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_I2C2_Init	I2C2
5	MX_I2C3_Init	I2C3
6	MX_SPI1_Init	SPI1
7	MX_SPI2_Init	SPI2
8	MX_SPI3_Init	SPI3
9	MX_TIM8_Init	TIM8
10	MX_USART1_UART_Init	USART1
11	MX_FDCAN1_Init	FDCAN1

Rank	Function Name	Peripheral Instance Name
12	MX_FDCAN2_Init	FDCAN2
13	MX_I2C1_Init	I2C1
14	MX_TIM5_Init	TIM5
15	MX_TIM1_Init	TIM1
16	MX_TIM3_Init	TIM3
17	MX_TIM4_Init	TIM4
18	MX_IWDG1_Init	IWDG1
19	MX_CRC_Init	CRC

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H750 Value line
MCU	STM32H750VBTx
Datasheet	DS12556_Rev6

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

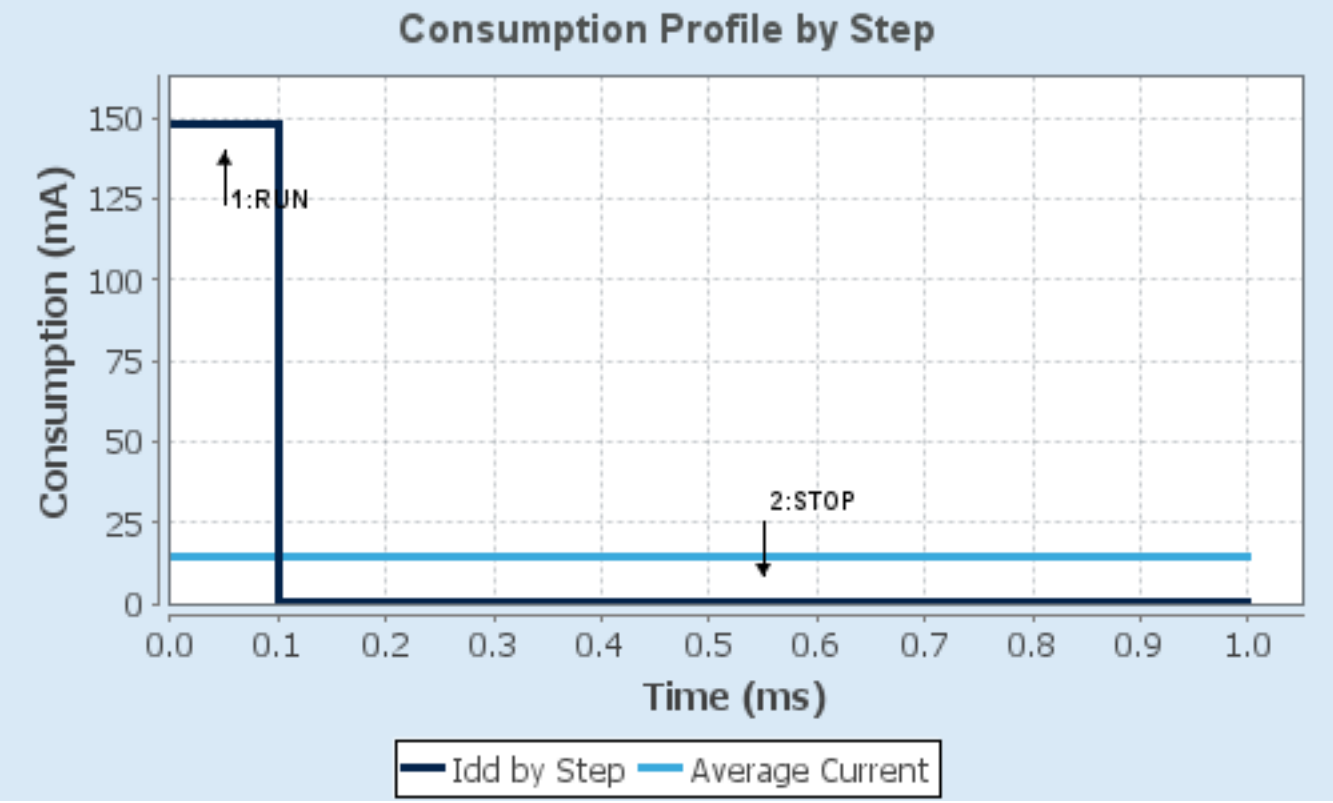
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	ITCM	NA
CPU Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL	Flash-OFF
Clock Source Frequency	24 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	148 mA	150 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Ta Max	105.02	124.98
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	14.94 mA
Battery Life	1 day, 17 hours	Average DMIPS	1027.2001 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
150
125
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Peripherals and Middlewares Configuration

2.1. CORTEX_M7

2.1.1. Parameter Settings:

Speculation default mode Settings:

Speculation default mode	Disabled

Cortex Interface Settings:

CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	**Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers ***

Cortex Memory Protection Unit Region 0 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x90000000 ***
MPU Region Size	**16MB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	level 0
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	**ENABLE ***
MPU Bufferable Permission	**ENABLE ***

Cortex Memory Protection Unit Region 1 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x90000000 ***
MPU Region Size	**1MB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	level 0
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	ENABLE
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	**ENABLE ***
MPU Bufferable Permission	**ENABLE ***

Cortex Memory Protection Unit Region 2 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 3 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 4 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region	Disabled

2.2. CRC

mode: Activated

2.2.1. Parameter Settings:

Basic Parameters:

Default Polynomial State	**Disable ***
CRC Length	**16-bit ***
CRC Generating Polynomial	**X12 + X5 + X0 ***
Default Init Value State	**Disable ***
Init Value For CRC computation	**0xFFFF ***

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

2.3. DEBUG

Debug: Trace Asynchronous Sw

2.4. FDCAN1

mode: Activated

2.4.1. Parameter Settings:

Basic Parameters:

Frame Format	**FD mode with BitRate Switching ***
Mode	Normal mode
Auto Retransmission	**Enable ***
Transmit Pause	**Enable ***
Protocol Exception	Disable
Nominal Sync Jump Width	**20 ***
Data Prescaler	**2 ***
Data Sync Jump Width	**2 ***
Data Time Seg1	**17 ***
Data Time Seg2	**2 ***
Message Ram Offset	0
Std Filters Nbr	**64 ***
Ext Filters Nbr	**32 ***
Rx Fifo0 Elmts Nbr	**32 ***
Rx Fifo0 Elmt Size	**64 bytes data field ***
Rx Fifo1 Elmts Nbr	0
Rx Fifo1 Elmt Size	**64 bytes data field ***
Rx Buffers Nbr	0
Rx Buffer Size	**64 bytes data field ***
Tx Events Nbr	0
Tx Buffers Nbr	0
Tx Fifo Queue Elmts Nbr	**16 ***
Tx Fifo Queue Mode	FIFO mode
Tx Elmt Size	**64 bytes data field ***

Clock Calibration Unit:

Clock Calibration	Disable

Bit Timings Parameters:

Nominal Prescaler	**1 ***
Nominal Time Quantum	**12.5 ***
Nominal Time Seg1	**139 ***
Nominal Time Seg2	**20 ***
Nominal Time for one Bit	**2000 ***
Nominal Baud Rate	**500000 ***

2.5. FDCAN2

mode: Activated

2.5.1. Parameter Settings:

Basic Parameters:

Frame Format	**FD mode with BitRate Switching ***
Mode	Normal mode
Auto Retransmission	**Enable ***
Transmit Pause	**Enable ***
Protocol Exception	Disable
Nominal Sync Jump Width	**20 ***
Data Prescaler	**2 ***
Data Sync Jump Width	**2 ***
Data Time Seg1	**17 ***
Data Time Seg2	**2 ***
Message Ram Offset	**993 ***
Std Filters Nbr	**64 ***
Ext Filters Nbr	**32 ***
Rx Fifo0 Elmts Nbr	**32 ***
Rx Fifo0 Elmt Size	**64 bytes data field ***
Rx Fifo1 Elmts Nbr	0
Rx Fifo1 Elmt Size	**64 bytes data field ***
Rx Buffers Nbr	0
Rx Buffer Size	**64 bytes data field ***
Tx Events Nbr	0
Tx Buffers Nbr	0
Tx Fifo Queue Elmts Nbr	**16 ***

Tx Fifo Queue Mode	FIFO mode
Tx Elmt Size	**64 bytes data field ***

Clock Calibration Unit:

Clock Calibration	Disable

Bit Timings Parameters:

Nominal Prescaler	**1 ***
Nominal Time Quantum	**12.5 ***
Nominal Time Seg1	**139 ***
Nominal Time Seg2	**20 ***
Nominal Time for one Bit	**2000 ***
Nominal Baud Rate	**500000 ***

2.6. I2C1

I2C: I2C

2.6.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00B03FDB ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

2.7. I2C2

I2C: I2C

2.7.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00B03FDB ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

2.8. I2C3

I2C: I2C

2.8.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00B03FDB ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

2.9. IWDG1

mode: Activated

2.9.1. Parameter Settings:

Watchdog Clocking:

IWDG counter clock prescaler	4
IWDG window value	4095
IWDG down-counter reload value	4095

2.10. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

2.10.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	32
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)
Product revision	**rev.V ***

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range

2.11. SPI1

Mode: Full-Duplex Master

2.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**32.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

2.12. SPI2

Mode: Full-Duplex Master

2.12.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**32.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

2.13. SPI3

Mode: Full-Duplex Master

2.13.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**32.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

2.14. SYS

Timebase Source: TIM6

2.15. TIM1

Clock Source : Internal Clock

2.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**240-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**DEFAULT_TIM_PERIOD ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

2.16. TIM3

Clock Source : Internal Clock

2.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**240-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**DEFAULT_TIM_PERIOD ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

2.17. TIM4

Clock Source : Internal Clock

2.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**240-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**DEFAULT_TIM_PERIOD ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

2.18. TIM5

Clock Source : Internal Clock

2.18.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**240-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

2.19. TIM8

Clock Source : Internal Clock

2.19.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**240-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**DEFAULT_TIM_PERIOD ***

Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

2.20. USART1

Mode: Asynchronous

2.20.1. Parameter Settings:

Basic Parameters:

Baud Rate	**921600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.21. FREERTOS

Interface: CMSIS_V2

2.21.1. Config parameters:

API:	
FreeRTOS API	CMSIS v2
Versions:	
FreeRTOS version	10.3.1
CMSIS-RTOS version	2.00
MPU/FPU:	
ENABLE_MPU	Disabled
ENABLE_FPU	**Enabled ***
Kernel settings:	
USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled
Memory management settings:	
Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	**61440 ***
Memory Management scheme	heap_4
Hook function related definitions:	
USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled
Run time and task stats gathering related definitions:	
GENERATE_RUN_TIME_STATS	Disabled

USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

CMSIS-RTOS V2 flags:

USE_OS2_THREAD_SUSPEND_RESUME	Enabled
USE_OS2_THREAD_ENUMERATE	Enabled
USE_OS2_EVENTFLAGS_FROM_ISR	Enabled
USE_OS2_THREAD_FLAGS	Enabled
USE_OS2_TIMER	Enabled
USE_OS2_MUTEX	Enabled

2.21.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled

eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

2.21.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	**Enabled ***

Project settings (see parameter description first):

Use FW pack heap file	Enabled

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
	PB3 (JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	
FDCAN1	PD0	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD1	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FDCAN2	PB12	FDCAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	FDCAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB9	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB11	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PA8	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
RCC	PC14-OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SPI2	PC2_C	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC3_C	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB4 (NJTRST)	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB14	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FDCAN1_STATUS
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CAN1_SILENT
	PE4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	STATUS_3V3
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI2_CS
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_CS
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT3_P6
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT3_P5
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT3_P3
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT3_P4
	PE11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID0
	PE12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID1
	PE13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID2
	PE14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID3
	PD8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CAN2_SILENT
	PD9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FDCAN2_STATUS
	PD11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	STATUS_5V
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT2_P1
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT2_P2
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT2_P3
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT1_P1
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT1_P2
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT1_P3
	PA9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT1_P4
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT1_P6
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT1_P5
	PA15 (JTDI)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI3_CS
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEL_3V3
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_YELLOW
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT2_P5
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT2_P6
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT2_P4
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GREEN

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT3_P1
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HAT3_P2
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CTL_5V
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CTL_3V3

3.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Stream0	Peripheral To Memory	Low
USART1_TX	DMA1_Stream1	Memory To Peripheral	Low

USART1_RX: DMA1_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA1_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

3.3. BDMA configuration

nothing configured in DMA service

3.4. MDMA configuration

nothing configured in DMA service

3.5. NVIC configuration

3.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	5	0
DMA1 stream1 global interrupt	true	5	0
FDCAN1 interrupt 0	true	5	0
FDCAN2 interrupt 0	true	5	0
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	true	15	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
FDCAN1 interrupt 1	unused		
FDCAN2 interrupt 1	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
USART1 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM5 global interrupt	unused		
SPI3 global interrupt	unused		
FDCAN calibration unit interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		

3.5.2. NVIC Code generation

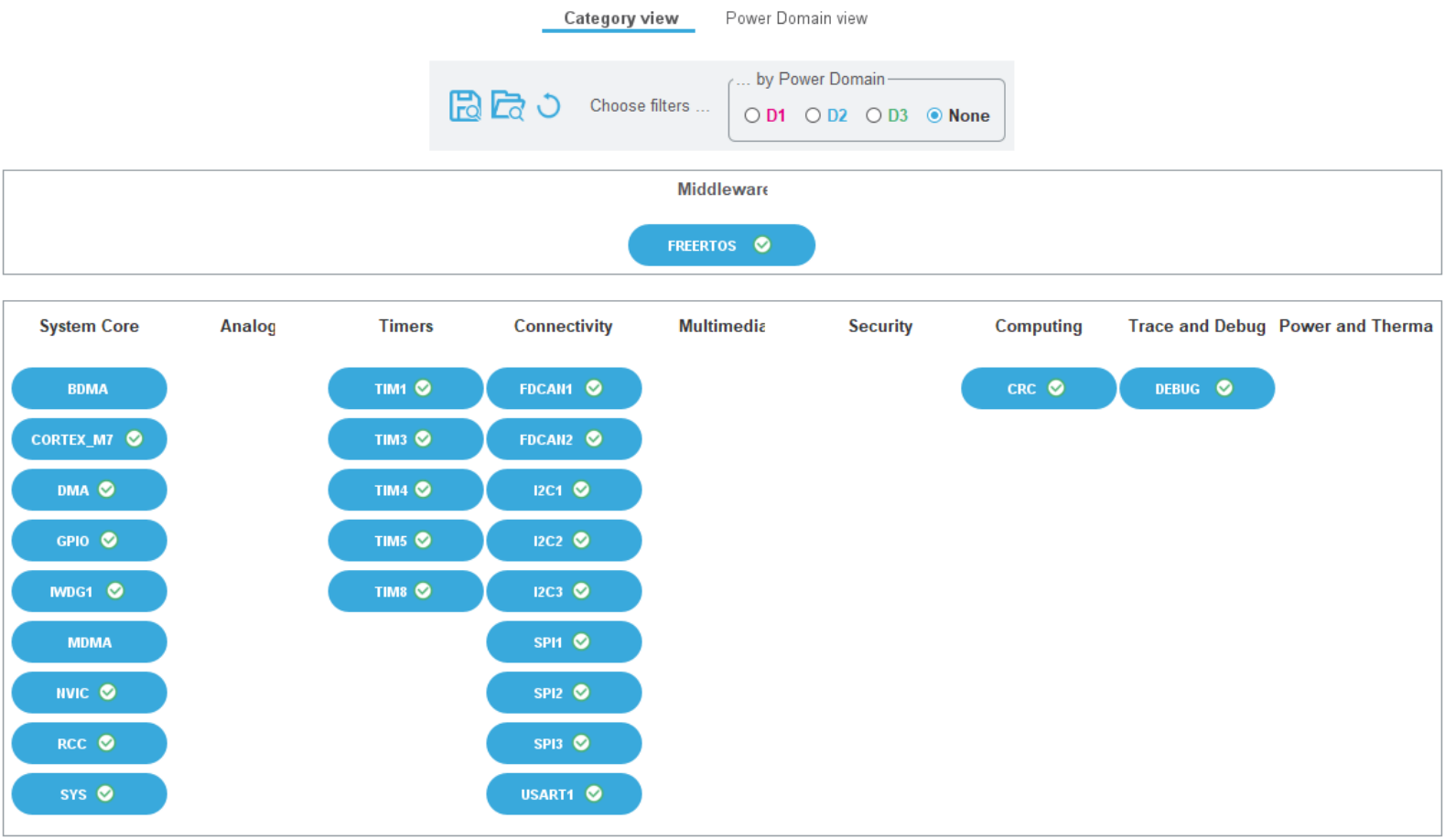
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
DMA1 stream0 global interrupt	false	true	true
DMA1 stream1 global interrupt	false	true	true
FDCAN1 interrupt 0	false	true	true
FDCAN2 interrupt 0	false	true	true
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	false	true	true

*** User modified value**

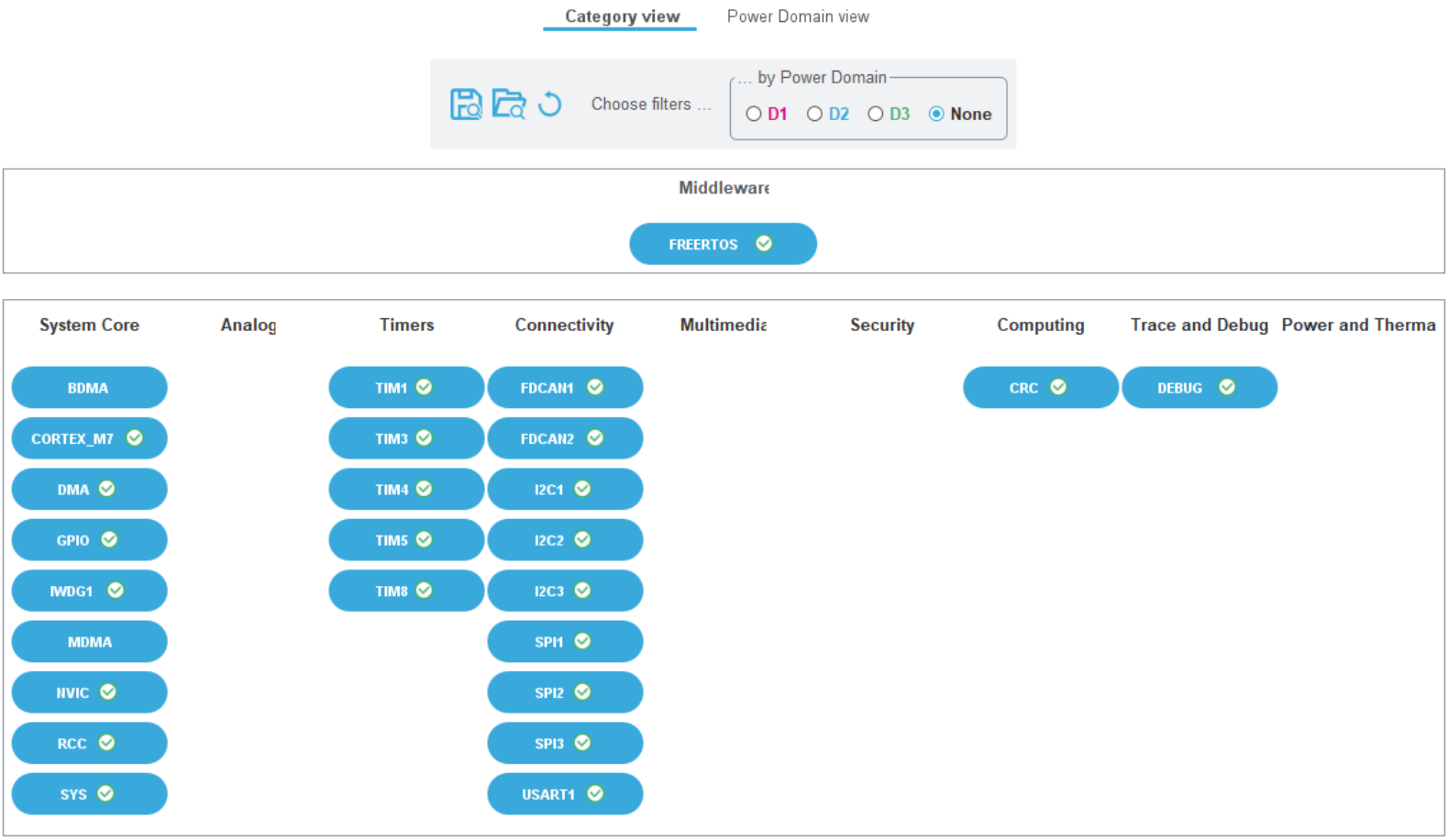
4. System Views

4.1. Category view

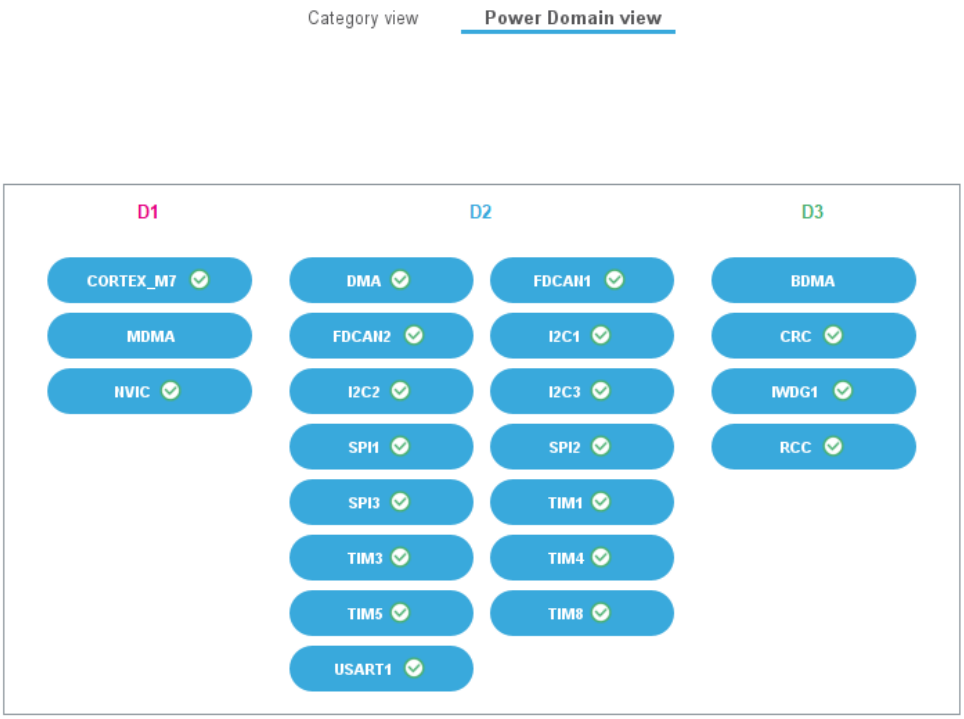
4.1.1. Current



4.1.2. Without filters



4.2. Power Domain view



5. Docs & Resources

Type	Link