outside those defined in the map, return 0xFF. The I²C interface supports standard mode (up to 100 kbits/s), fast mode (up to 400 kbits/s), and fast mode plus (up to 1 Mbit/s). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

System Note: All 16-bit registers are defined as Little Endian, with the most-significant byte allocated to the higher address. 16-bit register writes must be done sequentially and are recommended to be programmed using multi-write approach described in the Section 8.3.10.7.

8.3.10.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on SCL line is LOW. One clock pulse is generated for each data bit transferred.

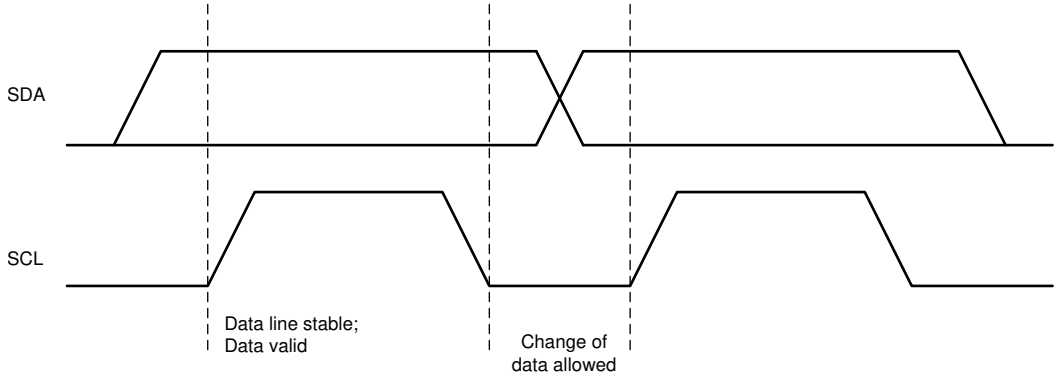

Figure 8-7. Bit Transfers on the I²C Bus

8.3.10.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the controller. The bus is considered busy after the START condition, and free after the STOP condition. When timeout condition is met, for example START condition is active for more than 2 seconds and there is no STOP condition triggered, the charger I²C communication will automatically reset and communication lines are free for another transmission.

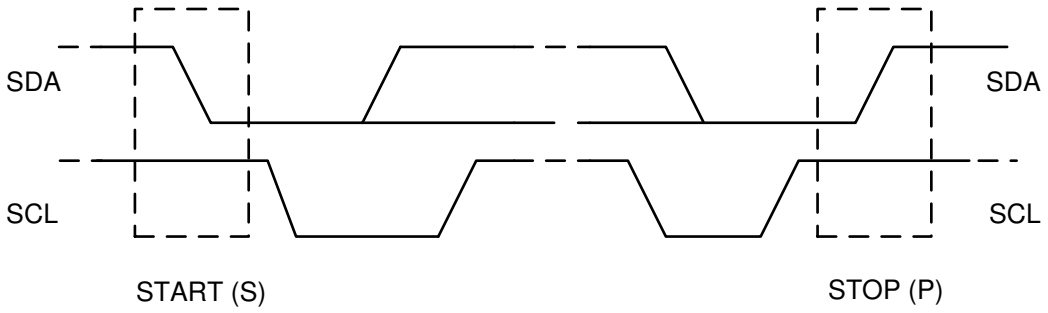

Figure 8-8. START and STOP Conditions on the I²C Bus

8.3.10.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the controller into a wait state (clock

stretching). Data transfer then continues when the target is ready for another byte of data and releases the SCL line.

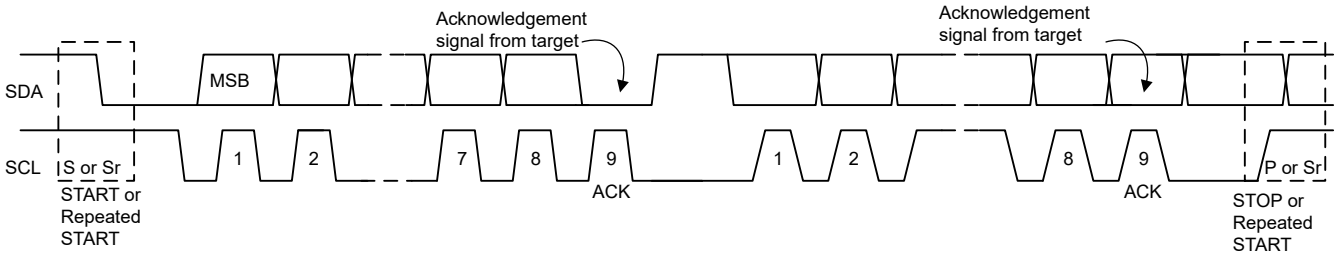

Figure 8-9. Data Transfer on the I²C Bus

8.3.10.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after byte. The ACK bit allows the target to signal the controller that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the controller.

The controller releases the SDA line during the acknowledge clock pulse so the target can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The controller can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

8.3.10.5 Target Address and Data Direction Bit

After the START signal, a target address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/ $\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The device 7-bit address is defined as 1101 011' (0x6A) by default.

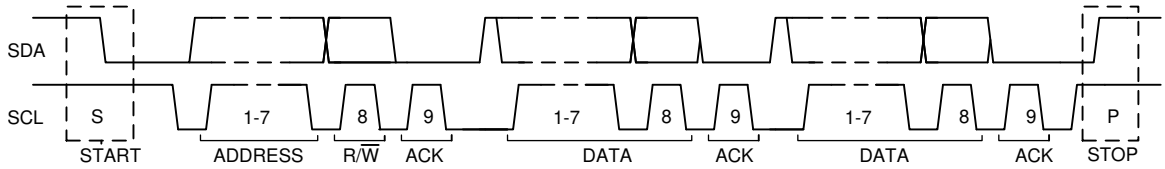

Figure 8-10. Complete Data Transfer on the I²C Bus

8.3.10.6 Single Write and Read

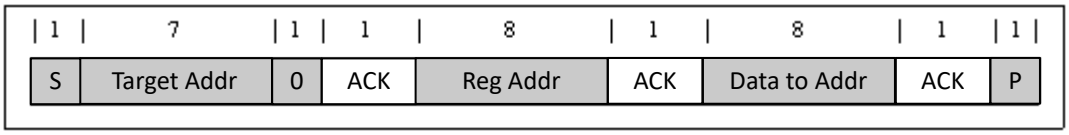

Figure 8-11. Single Write

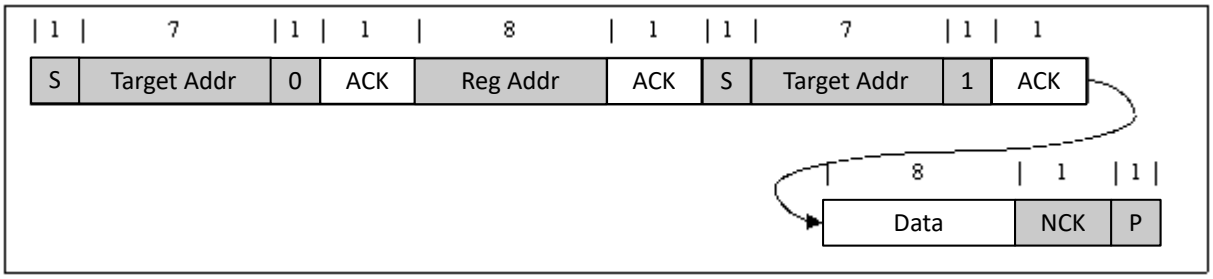

Figure 8-12. Single Read

If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

8.3.10.7 Multi-Write and Multi-Read

The charger device supports multi-read and multi-write of all registers.

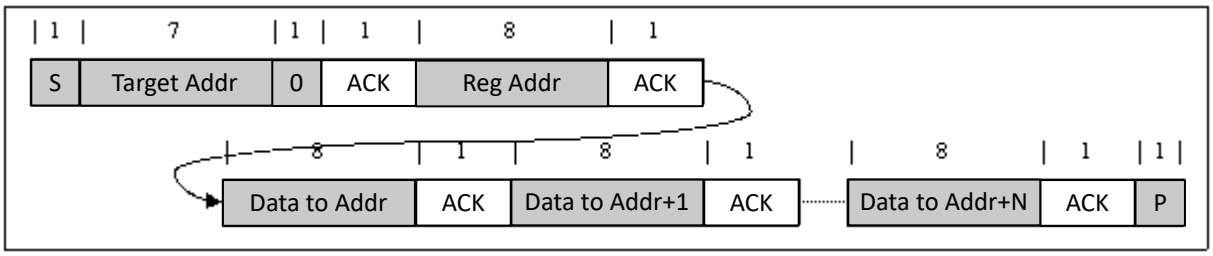

Figure 8-13. Multi-Write

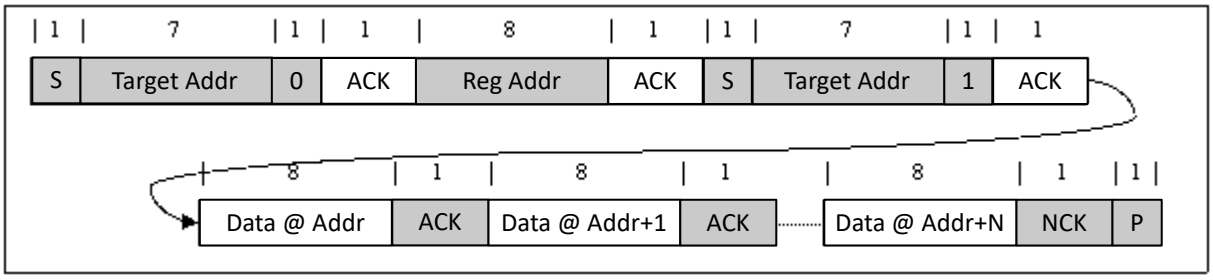

Figure 8-14. Multi-Read

8.4 Device Functional Modes

8.4.1 Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD_STAT bit becomes HIGH, WD_FLAG is set to 1, and a $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK). The WD_FLAG bit would read as a '1' upon the first read and then '0' upon subsequent reads. When the charger is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 2-hour pre-charging safety timer and the 12-hour fast charging safety timer. At the end of the 2-hour or 12-hour timer expiration, the charging is stopped if termination has not been detected.

A write to any I^2C register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer is expired, the device returns to default mode and select registers are reset to default values as detailed in the Register Map section. The Watchdog timer will be reset on any write if the watchdog timer has expired. When watchdog timer expires, WD_STAT and WD_FLAG is set to 1, and /INT is asserted low to alert the host (unless masked by WD_MASK).

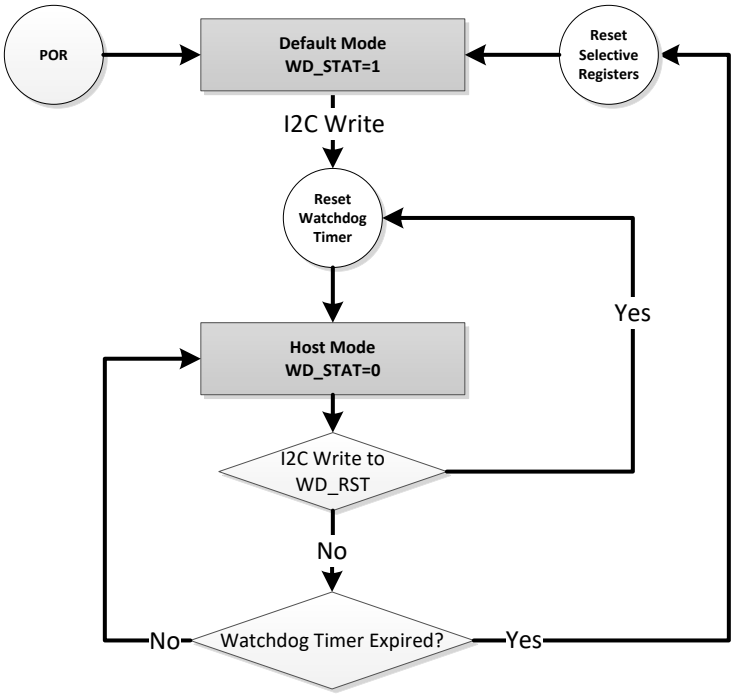

Figure 8-15. Watchdog Timer Flow Chart

8.4.2 Register Bit Reset

Beside the register reset by the watchdog timer in the default mode, the register and the timer could be reset to the default value by writing the REG_RST bit to 1. The register bits which can be reset by the REG_RST bit, are noted in the Register Map section. After the register reset, the REG_RST bit will go back from 1 to 0 automatically.

8.5 BQ25756E Registers

Table 8-7 lists the memory-mapped registers for the BQ25756E registers. All register offset addresses not listed in Table 8-7 should be considered as reserved locations and the register contents should not be modified.

Table 8-7. BQ25756E Registers

Address	Acronym	Register Name	Section
0x0	REG0x00_Charge_Voltage_Limit	Charge Voltage Limit	Go
0x2	REG0x02_Charge_Current_Limit	Charge Current Limit	Go
0x6	REG0x06_Input_Current_DPM_Limit	Input Current DPM Limit	Go
0x8	REG0x08_Input_Voltage_DPM_Limit	Input Voltage DPM Limit	Go
0xA	REG0x0A_Reverse_Mode_Input_Current_Limit	Reverse Mode Input Current Limit	Go
0xC	REG0x0C_Reverse_Mode_Input_Voltage_Limit	Reverse Mode Input Voltage Limit	Go
0x10	REG0x10_Precharge_Current_Limit	Precharge Current Limit	Go
0x12	REG0x12_Termination_Current_Limit	Termination Current Limit	Go
0x14	REG0x14_Precharge_and_Termination_Control	Precharge and Termination Control	Go
0x15	REG0x15_Timer_Control	Timer Control	Go
0x16	REG0x16_Three-Stage_Charge_Control	Three-Stage Charge Control	Go
0x17	REG0x17_Charger_Control	Charger Control	Go
0x18	REG0x18_Pin_Control	Pin Control	Go
0x19	REG0x19_Power_Path_and_Reverse_Mode_Control	Power Path and Reverse Mode Control	Go
0x1A	REG0x1A_MPPT_Control	MPPT Control	Go
0x1B	REG0x1B_TS_Charging_Threshold_Control	TS Charging Threshold Control	Go
0x1C	REG0x1C_TS_Charging_Region_Behavior_Control	TS Charging Region Behavior Control	Go
0x1D	REG0x1D_TS_Reverse_Mode_Threshold_Control	TS Reverse Mode Threshold Control	Go
0x1E	REG0x1E_Reverse_Undervoltage_Control	Reverse Undervoltage Control	Go
0x1F	REG0x1F_VAC_Max_Power_Point_Detected	VAC Max Power Point Detected	Go
0x21	REG0x21_Charger_Status_1	Charger Status 1	Go
0x22	REG0x22_Charger_Status_2	Charger Status 2	Go
0x23	REG0x23_Charger_Status_3	Charger Status 3	Go
0x24	REG0x24_Fault_Status	Fault Status	Go
0x25	REG0x25_Charger_Flag_1	Charger Flag 1	Go
0x26	REG0x26_Charger_Flag_2	Charger Flag 2	Go
0x27	REG0x27_Fault_Flag	Fault Flag	Go
0x28	REG0x28_Charger_Mask_1	Charger Mask 1	Go
0x29	REG0x29_Charger_Mask_2	Charger Mask 2	Go
0x2A	REG0x2A_Fault_Mask	Fault Mask	Go
0x2B	REG0x2B_ADC_Control	ADC Control	Go
0x2C	REG0x2C_ADC_Channel_Control	ADC Channel Control	Go
0x2D	REG0x2D_IAC_ADC	IAC ADC	Go
0x2F	REG0x2F_IBAT_ADC	IBAT ADC	Go
0x31	REG0x31_VAC_ADC	VAC ADC	Go

Table 8-7. BQ25756E Registers (continued)

Address	Acronym	Register Name	Section
0x33	REG0x33_VBAT_ADC	VBAT ADC	Go
0x37	REG0x37_TS_ADC	TS ADC	Go
0x39	REG0x39_VFB_ADC	VFB ADC	Go
0x3B	REG0x3B_Gate_Driver_Strength_Control	Gate Driver Strength Control	Go
0x3C	REG0x3C_Gate_Driver_Dead_Time_Control	Gate Driver Dead Time Control	Go
0x3D	REG0x3D_Part_Information	Part Information	Go
0x62	REG0x62_Reverse_Mode_Battery_Discharge_Current	Reverse Mode Battery Discharge Current	Go

Complex bit access types are encoded to fit into small table cells. Table 8-8 shows the codes that are used for access types in this section.

Table 8-8. BQ25756E Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.5.1 REG0x00_Charge_Voltage_Limit Register (Address = 0x0) [Reset = 0x0010]

REG0x00_Charge_Voltage_Limit is shown in Table 8-9.

Return to the Summary Table.

I2C REG0x01=[15:8], I2C REG0x00=[7:0]

Table 8-9. REG0x00_Charge_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:5	RESERVED	R	0x0		Reserved
4:0	VFB_REG	R/W	0x10	Reset by: REG_RESET	FB Voltage Regulation Limit: POR: 1536mV (10h) Range: 1504mV-1566mV (0h-1Fh) Bit Step: 2mV Offset: 1504mV

8.5.2 REG0x02_Charge_Current_Limit Register (Address = 0x2) [Reset = 0x0640]

REG0x02_Charge_Current_Limit is shown in Table 8-10.

Return to the Summary Table.

I2C REG0x03=[15:8], I2C REG0x02=[7:0]

Table 8-10. REG0x02_Charge_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:11	RESERVED	R	0x0		Reserved

Table 8-10. REG0x02_Charge_Current_Limit Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
10:2	ICHG_REG	R/W	0x190	Reset by: REG_RESET WATCHDOG	Fast Charge Current Regulation Limit with 5mΩ RBAT_SNS: Actual charge current is the lower of ICHG_REG and ICHG pin POR: 20000mA (190h) Range: 400mA-20000mA (8h-190h) Clamped Low Clamped High Bit Step: 50mA
1:0	RESERVED	R	0x0		Reserved

8.5.3 REG0x06_Input_Current_DPM_Limit Register (Address = 0x6) [Reset = 0x0640]

REG0x06_Input_Current_DPM_Limit is shown in Table 8-11.

Return to the Summary Table.

I2C REG0x07=[15:8], I2C REG0x06=[7:0]

Table 8-11. REG0x06_Input_Current_DPM_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:11	RESERVED	R	0x0		Reserved
10:2	IAC_DPM	R/W	0x190	Reset by: REG_RESET	Input Current DPM Regulation Limit with 5mΩ RAC_SNS: Actual input current limit is the lower of IAC_DPM and ILIM_HIZ pin POR: 20000mA (190h) Range: 400mA-20000mA (8h-190h) Clamped Low Clamped High Bit Step: 50mA
1:0	RESERVED	R	0x0		Reserved

8.5.4 REG0x08_Input_Voltage_DPM_Limit Register (Address = 0x8) [Reset = 0x0348]

REG0x08_Input_Voltage_DPM_Limit is shown in Table 8-12.

Return to the Summary Table.

I2C REG0x09=[15:8], I2C REG0x08=[7:0]

Table 8-12. REG0x08_Input_Voltage_DPM_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:14	RESERVED	R	0x0		Reserved
13:2	VAC_DPM	R/W	0xD2	Reset by: REG_RESET	Input Voltage Regulation Limit: Note if EN_MPPT = 1, the Full Sweep method will use this limit as the lower search window for Full Panel Sweep POR: 4200mV (D2h) Range: 4200mV-36000mV (D2h-708h) Clamped Low Clamped High Bit Step: 20mV
1:0	RESERVED	R	0x0		Reserved

8.5.5 REG0x0A_Reverse_Mode_Input_Current_Limit Register (Address = 0xA) [Reset = 0x0640]

REG0x0A_Reverse_Mode_Input_Current_Limit is shown in Table 8-13.

Return to the Summary Table.

I2C REG0x0B=[15:8], I2C REG0x0A=[7:0]

Table 8-13. REG0x0A_Reverse_Mode_Input_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:11	RESERVED	R	0x0		Reserved
10:2	IAC_REV	R/W	0x190	Reset by: REG_RESET	Input Current Regulation in Reverse Mode with 5mΩ RAC_SNS: POR: 20000mA (190h) Range: 400mA-20000mA (8h-190h) Clamped Low Clamped High Bit Step: 50mA
1:0	RESERVED	R	0x0		Reserved

8.5.6 REG0x0C_Reverse_Mode_Input_Voltage_Limit Register (Address = 0xC) [Reset = 0x03E8]

REG0x0C_Reverse_Mode_Input_Voltage_Limit is shown in Table 8-14.

Return to the Summary Table.

I2C REG0x0D=[15:8], I2C REG0x0C=[7:0]

Table 8-14. REG0x0C_Reverse_Mode_Input_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:14	RESERVED	R	0x0		Reserved
13:2	VAC_REV	R/W	0xFA	Reset by: REG_RESET	VAC Voltage Regulation in Reverse Mode: POR: 5000mV (FAh) Range: 3300mV-36000mV (A5h-708h) Clamped Low Clamped High Bit Step: 20mV
1:0	RESERVED	R	0x0		Reserved

8.5.7 REG0x10_Precharge_Current_Limit Register (Address = 0x10) [Reset = 0x0140]

REG0x10_Precharge_Current_Limit is shown in Table 8-15.

Return to the Summary Table.

I2C REG0x11=[15:8], I2C REG0x10=[7:0]

Table 8-15. REG0x10_Precharge_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:10	RESERVED	R	0x0		Reserved
9:2	IPRECHG	R/W	0x50	Actual pre-charge current is the lower of IPRECHG and ICHG pin Reset by: REG_RESET	Pre-charge current regulation limit with 5mΩ RBAT_SNS: POR: 4000mA (50h) Range: 250mA-10000mA (5h-C8h) Clamped Low Clamped High Bit Step: 50mA
1:0	RESERVED	R	0x0		Reserved

8.5.8 REG0x12_Termination_Current_Limit Register (Address = 0x12) [Reset = 0x00A0]

REG0x12_Termination_Current_Limit is shown in Table 8-16.

Return to the Summary Table.

I2C REG0x13=[15:8], I2C REG0x12=[7:0]

Table 8-16. REG0x12_Termination_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:10	RESERVED	R	0x0		Reserved
9:2	ITERM	R/W	0x28	Actual termination current is the lower of ITERM and ICHG pin if both functions enabled Reset by: REG_RESET	Termination Current Threshold with 5mΩ RBAT_SNS: POR: 2000mA (28h) Range: 250mA-10000mA (5h-C8h) Clamped Low Clamped High Bit Step: 50mA
1:0	RESERVED	R	0x0		Reserved

8.5.9 REG0x14_Precharge_and_Termination_Control Register (Address = 0x14) [Reset = 0x0F]

REG0x14_Precharge_and_Termination_Control is shown in Table 8-17.

Return to the Summary Table.

Table 8-17. REG0x14_Precharge_and_Termination_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:4	RESERVED	R	0x0		Reserved
3	EN_TERM	R/W	0x1	Reset by: REG_RESET	Enable termination control 0b = Disable 1b = Enable
2:1	VBAT_LOWV	R/W	0x3	Reset by: REG_RESET	Battery threshold for PRECHG to FASTCHG transition, as percentage of VFB_REG: 00b = 30% x VFB_REG 01b = 55% x VFB_REG 10b = 66.7% x VFB_REG 11b = 71.4% x VFB_REG
0	EN_PRECHG	R/W	0x1	Reset by: REG_RESET	Enable pre-charge and trickle charge functions: 0b = Disable 1b = Enable

8.5.10 REG0x15_Timer_Control Register (Address = 0x15) [Reset = 0x1D]

REG0x15_Timer_Control is shown in Table 8-18.

Return to the Summary Table.

Table 8-18. REG0x15_Timer_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	TOPOFF_TMR	R/W	0x0	Reset by: REG_RESET	Top-off timer control: 00b = Disable 01b = 15 mins 10b = 30 mins 11b = 45 mins

Table 8-18. REG0x15_Timer_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
5:4	WATCHDOG	R/W	0x1	Reset by: REG_RESET	Watchdog timer control: 00b = Disable 01b = 40s 10b = 80s 11b = 160s
3	EN_CHG_TMR	R/W	0x1	Reset by: REG_RESET WATCHDOG	Enable charge safety timer: 0b = Disable 1b = Enable
2:1	CHG_TMR	R/W	0x2	Reset by: REG_RESET	Charge safety timer setting: 00b = 5hr 01b = 8hr 10b = 12hr 11b = 24hr
0	EN_TMR2X	R/W	0x1	Reset by: REG_RESET	Charge safety timer speed in DPM: 0b = Timer always counts normally 1b = Timer slowed by 2x during input DPM

8.5.11 REG0x16_Three-Stage_Charge_Control Register (Address = 0x16) [Reset = 0x00]

REG0x16_Three-Stage_Charge_Control is shown in Table 8-19.

Return to the Summary Table.

Table 8-19. REG0x16_Three-Stage_Charge_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	RESERVED	R	0x0		Reserved
5	RESERVED	R	0x0		Reserved
4	RESERVED	R	0x0		Reserved
3:0	CV_TMR	R/W	0x0	Reset by: REG_RESET WATCHDOG	CV timer setting: 0000b = disable 0001b = 1hr 0010b = 2hr ... = ... 1110b = 14hr 1111b = 15hr

8.5.12 REG0x17_Charger_Control Register (Address = 0x17) [Reset = 0xC9]

REG0x17_Charger_Control is shown in Table 8-20.

Return to the Summary Table.

Table 8-20. REG0x17_Charger_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	VRECHG	R/W	0x3	Reset by: REG_RESET	Battery auto-recharge threshold, as percentage of VFB_REG: 00b = 93.0% x VFB_REG 01b = 94.3% x VFB_REG 10b = 95.2% x VFB_REG 11b = 97.6% x VFB_REG
5	WD_RST	R/W	0x0	Reset by: REG_RESET	I2C Watchdog timer reset control: 0b = Normal 1b = Reset (bit goes back to 0 after timer reset)

Table 8-20. REG0x17_Charger_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
4	DIS_CE_PIN	R/W	0x0	Reset by: REG_RESET	/CE pin function disable: 0b = /CE pin enabled 1b = /CE pin disabled
3	EN_CHG_BIT_RESET_BEHAVIOR	R/W	0x1	Reset by: REG_RESET	Controls the EN_CHG bit behavior when WATCHDOG expires: 0b = EN_CHG bit resets to 0 1b = EN_CHG bit resets to 1
2	EN_HIZ	R/W	0x0	Reset by: REG_RESET WATCHDOG Adapter Plug In	HIZ mode enable: 0b = Disable 1b = Enable
1	EN_IBAT_LOAD	R/W	0x0	Sinks current from SRN to GND. Recommend to disable IBAT ADC (IBAT_ADC_DIS = 1) while this bit is active. Reset by: REG_RESET WATCHDOG	Battery Load (IBAT_LOAD) Enable: 0b = Disabled 1b = Enabled
0	EN_CHG	R/W	0x1	Reset by: REG_RESET WATCHDOG	Charge enable control: 0b = Disable 1b = Enable

8.5.13 REG0x18_Pin_Control Register (Address = 0x18) [Reset = 0xC0]

REG0x18_Pin_Control is shown in Table 8-21.

Return to the Summary Table.

Table 8-21. REG0x18_Pin_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_ICHG_PIN	R/W	0x1	Reset by: REG_RESET WATCHDOG	ICHG pin function enable: 0b = ICHG pin disabled 1b = ICHG pin enabled
6	EN_ILIM_HIZ_PIN	R/W	0x1	Reset by: REG_RESET WATCHDOG	ILIM_HIZ pin function enable: 0b = ILIM_HIZ pin disabled 1b = ILIM_HIZ pin enabled
5	DIS_PG_PIN	R/W	0x0	Reset by: REG_RESET	PG pin function disable: 0b = PG pin enabled 1b = PG pin disabled
4	DIS_STAT_PINS	R/W	0x0	Reset by: REG_RESET	STAT1, STAT2 pin function disable: 0b = STAT pins enabled 1b = STAT pins disabled
3	FORCE_STAT4_ON	R/W	0x0	Reset by: REG_RESET	CE_STAT4 pin override: Can only be forced on if DIS_CE_PIN = 1 0b = CE_STAT4 open-drain off 1b = CE_STAT4 pulls LOW
2	FORCE_STAT3_ON	R/W	0x0	Reset by: REG_RESET	PG_STAT3 pin override: Can only be forced on if DIS_PG_PIN = 1 0b = PG_STAT3 open-drain off 1b = PG_STAT3 pulls LOW

Table 8-21. REG0x18_Pin_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
1	FORCE_STAT2_ON	R/W	0x0	Reset by: REG_RESET	STAT2 pin override: Can only be forced on if DIS_STAT_PINS = 1 0b = STAT2 open-drain off 1b = STAT2 pulls LOW
0	FORCE_STAT1_ON	R/W	0x0	Reset by: REG_RESET	STAT1 pin override: Can only be forced on if DIS_STAT_PINS = 1 0b = STAT1 open-drain off 1b = STAT1 pulls LOW

8.5.14 REG0x19_Power_Path_and_Reverse_Mode_Control Register (Address = 0x19) [Reset = 0x20]

REG0x19_Power_Path_and_Reverse_Mode_Control is shown in Table 8-22.

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Table 8-22. REG0x19_Power_Path_and_Reverse_Mode_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	REG_RST	R/W	0x0	Reset by: REG_RESET	Register reset to default values: 0b = Not reset 1b = Reset (bit goes back to 0 after register reset)
6	EN_IAC_LOAD	R/W	0x0	Reset by: REG_RESET WATCHDOG	VAC Load (IAC_LOAD) Enable: 0b = Disabled 1b = Enabled
5	EN_PFM	R/W	0x1	It is recommended to disable PFM when ITERM < 2A Reset by: REG_RESET	Enable PFM mode in light-load: Note this bit is reset upon a valid SYNC signal detection on FSW_SYNC pin. Host can set this bit back to 1 to force PFM operation even with a valid SYNC input 0b = Disable (Fixed-frequency DCM operation) 1b = Enable (PFM operation)
4	RESERVED	R	0x0		Reserved
3	RESERVED	R	0x0		Reserved
2	RESERVED	R	0x0		Reserved
1	RESERVED	R	0x0		Reserved
0	EN_REV	R/W	0x0	Reset by: REG_RESET WATCHDOG Adapter Plug In	Reverse Mode control: 0b = Disable 1b = Enable

8.5.15 REG0x1A_MPPT_Control Register (Address = 0x1A) [Reset = 0x20]

REG0x1A_MPPT_Control is shown in Table 8-23.

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Table 8-23. REG0x1A_MPPT_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	FORCE_SWEEP	R/W	0x0	Reset by: REG_RESET	Force Full Panel Sweep and reset MPPT timers: 0b = Normal 1b = Start Full Panel Sweep (bit goes back to 0 after Full Panel Sweep complete)
4:3	RESERVED	R	0x0		Reserved

Table 8-23. REG0x1A_MPPT_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
2:1	FULL_SWEEP_TMR	R/W	0x0	Reset by: REG_RESET	Full Panel Sweep timer control: 00b = 3 min 01b = 10 min 10b = 15 min 11b = 20 min
0	EN_MPPT	R/W	0x0	When MPPT is enabled, the ADC is controlled by the device, writes to REG2A are ignored Reset by: REG_RESET	MPPT algorithm control: 0b = Disable MPPT 1b = Enable MPPT

8.5.16 REG0x1B_TS_Charging_Threshold_Control Register (Address = 0x1B) [Reset = 0x96]

REG0x1B_TS_Charging_Threshold_Control is shown in Table 8-24.

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Table 8-24. REG0x1B_TS_Charging_Threshold_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	TS_T5	R/W	0x2	Reset by: REG_RESET	TS T5 (HOT) threshold control: 00b = 41.2% (50C) 01b = 37.7% (55C) 10b = 34.375% (60C) 11b = 31.25%(65C)
5:4	TS_T3	R/W	0x1	Reset by: REG_RESET	JEITA TS T3 (WARM) threshold control: 00b = 48.4% (40C) 01b = 44.8% (45C) 10b = 41.2% (50C) 11b = 37.7% (55C)
3:2	TS_T2	R/W	0x1	Reset by: REG_RESET	JEITA TS T2 (COOL) threshold control: 00b = 71.1% (5C) 01b = 68.4% (10C) 10b = 65.5% (15C) 11b = 62.4% (20C)
1:0	TS_T1	R/W	0x2	Reset by: REG_RESET	TS T1 (COLD) threshold control: 00b = 77.15% (-10C) 01b = 75.32% (-5C) 10b = 73.25% (0C) 11b = 71.1% (5C)

8.5.17 REG0x1C_TS_Charging_Region_Behavior_Control Register (Address = 0x1C) [Reset = 0x57]

REG0x1C_TS_Charging_Region_Behavior_Control is shown in Table 8-25.

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Table 8-25. REG0x1C_TS_Charging_Region_Behavior_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0x0		Reserved
6:5	JEITA_VSET	R/W	0x2	Reset by: REG_RESET	JEITA Warm (T3 < TS < T5) regulation voltage setting, as percentage of VFB_REG: 00b = Charge Suspend 01b = 94.3% x VFB_REG 10b = 97.6% x VFB_REG 11b = 100% x VFB_REG

Table 8-25. REG0x1C_TS_Charging_Region_Behavior_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
4	JEITA_ISETH	R/W	0x1	Reset by: REG_RESET	JEITA Warm (T3 < TS < T5) regulation current setting, as percentage of ICHG_REG: 0b = 40% x ICHG_REG 1b = 100% x ICHG_REG
3:2	JEITA_ISETC	R/W	0x1	Reset by: REG_RESET	JEITA Cool (T1 < TS < T2) regulation current setting, as percentage of ICHG_REG: 00b = Charge Suspend 01b = 20% x ICHG_REG 10b = 40% x ICHG_REG 11b = 100% x ICHG_REG
1	EN_JEITA	R/W	0x1	EN_VREG_TEMP_COMP and EN_JEITA cannot be set to 1 at the same time. Reset by: REG_RESET	JEITA profile control: 0b = Disabled (COLD/HOT control only) 1b = Enabled (COLD/COOL/WARM/HOT control)
0	EN_TS	R/W	0x1	Reset by: REG_RESET	TS pin function control (applies to forward charging and reverse discharging modes): 0b = Disabled (ignore TS pin) 1b = Enabled

8.5.18 REG0x1D_TS_Reverse_Mode_Threshold_Control Register (Address = 0x1D) [Reset = 0x40]

REG0x1D_TS_Reverse_Mode_Threshold_Control is shown in Table 8-26.

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Table 8-26. REG0x1D_TS_Reverse_Mode_Threshold_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	BHOT	R/W	0x1	Reset by: REG_RESET	Reverse Mode TS HOT temperature threshold control: 00b = 37.7% (55C) 01b = 34.2% (60C) 10b = 31.25%(65C) 11b = Disable
5	BCOLD	R/W	0x0	Reset by: REG_RESET	Reverse Mode TS COLD temperature threshold control: 0b = 77.15% (-10C) 1b = 80% (-20C)
4:0	RESERVED	R	0x0		Reserved

8.5.19 REG0x1E_Reverse_Undervoltage_Control Register (Address = 0x1E) [Reset = 0x00]

REG0x1E_Reverse_Undervoltage_Control is shown in Table 8-27.

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Table 8-27. REG0x1E_Reverse_Undervoltage_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0x0		Reserved
6	RESERVED	R	0x0		Reserved
5	SYSREV_UV	R/W	0x0	Reset by: REG_RESET	Reverse Mode System UVP: 0b = 80% of VSYS_REV target 1b = Fixed at 3.3V
4	RESERVED	R	0x0		Reserved
3	RESERVED	R	0x0		Reserved

Table 8-27. REG0x1E_Reverse_Undervoltage_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
2	RESERVED	R	0x0		Reserved
1	RESERVED	R	0x0		Reserved
0	RESERVED	R	0x0		Reserved

8.5.20 REG0x1F_VAC_Max_Power_Point_Detected Register (Address = 0x1F) [Reset = 0x0000]

REG0x1F_VAC_Max_Power_Point_Detected is shown in Table 8-28.

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I2C REG0x20=[15:8], I2C REG0x1F=[7:0]

Table 8-28. REG0x1F_VAC_Max_Power_Point_Detected Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:14	RESERVED	R	0x0		Reserved
13:2	VAC_MPP	R	0x0		Input Voltage for Max Power Point detected: POR: 0mV (0h) Range: 0mV-60000mV (0h-BB8h) Clamped High Bit Step: 20mV
1:0	RESERVED	R	0x0		Reserved

8.5.21 REG0x21_Charger_Status_1 Register (Address = 0x21) [Reset = 0x00]

REG0x21_Charger_Status_1 is shown in Table 8-29.

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Table 8-29. REG0x21_Charger_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	ADC_DONE_STAT	R	0x0		ADC conversion status (in one-shot mode only): 0b = Conversion not complete 1b = Conversion complete
6	IAC_DPM_STAT	R	0x0		Input Current regulation status: 0b = Normal 1b = In Input Current regulation (ILIM pin or IAC_DPM)
5	VAC_DPM_STAT	R	0x0		Input Voltage regulation status: 0b = Normal 1b = In Input Voltage regulation (VAC_DPM or VSYS_REV)
4	RESERVED	R	0x0		Reserved
3	WD_STAT	R	0x0		I2C Watchdog timer status: 0b = Normal 1b = WD timer expired
2:0	CHARGE_STAT	R	0x0		Charge cycle status: 000b = Not charging 001b = Trickle Charge (VBAT < VBAT_SHORT) 010b = Pre-Charge (VBAT < VBAT_LOWV) 011b = Fast Charge (CC mode) 100b = Taper Charge (CV mode) 101b = Reserved 110b = Top-off Timer Charge 111b = Charge Termination Done

8.5.22 REG0x22_Charger_Status_2 Register (Address = 0x22) [Reset = 0x00]

REG0x22_Charger_Status_2 is shown in Table 8-30.

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Table 8-30. REG0x22_Charger_Status_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	PG_STAT	R	0x0		Input Power Good status: 0b = Not Power Good 1b = Power Good
6:4	TS_STAT	R	0x0		TS (Battery NTC) status: 000b = Normal 001b = TS Warm 010b = TS Cool 011b = TS Cold 100b = TS Hot
3:2	RESERVED	R	0x0		Reserved
1:0	MPPT_STAT	R	0x0		Max Power Point Tracking Algorithm status: 00b = MPPT Disabled 01b = MPPT Enabled, But Not Running 10b = Full Panel Sweep In Progress 11b = Max Power Voltage Detected

8.5.23 REG0x23_Charger_Status_3 Register (Address = 0x23) [Reset = 0x00]

REG0x23_Charger_Status_3 is shown in Table 8-31.

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Table 8-31. REG0x23_Charger_Status_3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	RESERVED	R	0x0		Reserved
5:4	FSW_SYNC_STAT	R	0x0		FSW_SYNC pin status: 00b = Normal, no external clock detected 01b = Valid ext. clock detected 10b = Pin fault (frequency out-of-range) 11b = Reserved
3	CV_TMR_STAT	R	0x0		CV Timer status: 0b = Normal 1b = CV Timer Expired
2	REVERSE_STAT	R	0x0		Converter Reverse Mode status: 0b = Reverse Mode off 1b = Reverse Mode On
1	RESERVED	R	0x0		Reserved
0	RESERVED	R	0x0		Reserved

8.5.24 REG0x24_Fault_Status Register (Address = 0x24) [Reset = 0x00]

REG0x24_Fault_Status is shown in Table 8-32.

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Table 8-32. REG0x24_Fault_Status Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VAC_UV_STAT	R	0x0		Input under-voltage status: 0b = Input Normal 1b = Device in Input under-voltage protection
6	VAC_OV_STAT	R	0x0		Input over-voltage status: 0b = Input Normal 1b = Device in Input over-voltage protection
5	IBAT_OCP_STAT	R	0x0		Battery over-current status: 0b = Battery current normal 1b = Battery over-current detected
4	VBAT_OV_STAT	R	0x0		Battery over-voltage status: 0b = Normal 1b = Device in Battery over-voltage protection
3	TSHUT_STAT	R	0x0		Thermal shutdown status: 0b = Normal 1b = Device in thermal shutdown protection
2	CHG_TMR_STAT	R	0x0		Charge safety timer status: 0b = Normal 1b = Charge safety timer expired
1	DRV_OKZ_STAT	R	0x0	In battery-only mode with ADC disabled, this bit always reads '1'	DRV_SUP pin voltage status: 0b = Normal 1b = DRV_SUP pin voltage is out of valid range
0	RESERVED	R	0x0		Reserved

8.5.25 REG0x25_Charger_Flag_1 Register (Address = 0x25) [Reset = 0x00]

REG0x25_Charger_Flag_1 is shown in Table 8-33.

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Table 8-33. REG0x25_Charger_Flag_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	ADC_DONE_FLAG	R	0x0		ADC conversion INT flag (in one-shot mode only): Note: always reads 0 in continuous mode Access: R (ClearOnRead) 0b = Conversion not complete 1b = Conversion complete
6	IAC_DPM_FLAG	R	0x0		Input Current regulation INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Device entered Input Current regulation
5	VAC_DPM_FLAG	R	0x0		Input Voltage regulation INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Device entered Input Voltage regulation
4	RESERVED	R	0x0		Reserved
3	WD_FLAG	R	0x0		I2C Watchdog timer INT flag: Access: R (ClearOnRead) 0b = Normal 1b = WD_STAT rising edge detected
2	RESERVED	R	0x0		Reserved

Table 8-33. REG0x25_Charger_Flag_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
1	CV_TMR_FLAG	R	0x0		CV timer INT flag: Access: R (ClearOnRead) 0b = Normal 1b = CV timer expired rising edge detected
0	CHARGE_FLAG	R	0x0		Charge cycle INT flag: Access: R (ClearOnRead) 0b = Not charging 1b = CHARGE_STAT[2:0] bits changed (transition to any state)

8.5.26 REG0x26_Charger_Flag_2 Register (Address = 0x26) [Reset = 0x00]

REG0x26_Charger_Flag_2 is shown in Table 8-34.

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Table 8-34. REG0x26_Charger_Flag_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	PG_FLAG	R	0x0		Input Power Good INT flag: Access: R (ClearOnRead) 0b = Normal 1b = PG signal toggle detected
6	RESERVED	R	0x0		Reserved
5	RESERVED	R	0x0		Reserved
4	TS_FLAG	R	0x0		TS (Battery NTC) INT flag: Access: R (ClearOnRead) 0b = Normal 1b = TS_STAT[2:0] bits changed (transitioned to any state)
3	REVERSE_FLAG	R	0x0		Reverse Mode INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Reverse Mode toggle detected
2	RESERVED	R	0x0		Reserved
1	FSW_SYNC_FLAG	R	0x0		FSW_SYNC pin signal INT flag: Access: R (ClearOnRead) 0b = Normal 1b = FSW_SYNC status changed
0	MPPT_FLAG	R	0x0		Max Power Point Tracking INT flag: Access: R (ClearOnRead) 0b = Normal 1b = MPPT_STAT[1:0] bits changed (transitioned to any state)

8.5.27 REG0x27_Fault_Flag Register (Address = 0x27) [Reset = 0x00]

REG0x27_Fault_Flag is shown in Table 8-35.

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Table 8-35. REG0x27_Fault_Flag Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VAC_UV_FLAG	R	0x0		Input under-voltage INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Entered input under-voltage fault
6	VAC_OV_FLAG	R	0x0		Input over-voltage INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Entered Input over-voltage fault
5	IBAT_OCP_FLAG	R	0x0		Battery over-current INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Entered Battery over-current fault
4	VBAT_OV_FLAG	R	0x0		Battery over-voltage INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Entered battery over-voltage fault
3	TSHUT_FLAG	R	0x0		Thermal shutdown INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Entered TSHUT fault
2	CHG_TMR_FLAG	R	0x0		Charge safety timer INT flag: Access: R (ClearOnRead) 0b = Normal 1b = Charge Safety timer expired rising edge detected
1	DRV_OKZ_FLAG	R	0x0		DRV_SUP pin voltage INT flag: Access: R (ClearOnRead) 0b = Normal 1b = DRV_SUP pin fault detected
0	RESERVED	R	0x0		Reserved

8.5.28 REG0x28_Charger_Mask_1 Register (Address = 0x28) [Reset = 0x00]

REG0x28_Charger_Mask_1 is shown in Table 8-36.

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Table 8-36. REG0x28_Charger_Mask_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	ADC_DONE_MASK	R/W	0x0	Reset by: REG_RESET	ADC conversion INT mask (in one-shot mode only): 0b = ADC_DONE produces INT pulse 1b = ADC_DONE does not produce INT pulse
6	IAC_DPM_MASK	R/W	0x0	Reset by: REG_RESET	Input Current regulation INT mask: 0b = IAC_DPM_FLAG produces INT pulse 1b = IAC_DPM_FLAG does not produce INT pulse
5	VAC_DPM_MASK	R/W	0x0	Reset by: REG_RESET	Input Voltage regulation INT mask: 0b = VAC_DPM_FLAG produces INT pulse 1b = VAC_DPM_FLAG does not produce INT pulse
4	RESERVED	R	0x0		Reserved
3	WD_MASK	R/W	0x0	Reset by: REG_RESET	I2C Watchdog timer INT mask: 0b = WD expiration produces INT pulse 1b = WD expiration does not produce INT pulse
2	RESERVED	R	0x0		Reserved

Table 8-36. REG0x28_Charger_Mask_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
1	CV_TMR_MASK	R/W	0x0	Reset by: REG_RESET	CV timer INT mask: 0b = CV Timer expired rising edge produces INT pulse 1b = CV Timer expired rising edge does not produce INT pulse
0	CHARGE_MASK	R/W	0x0	Reset by: REG_RESET	Charge cycle INT mask: 0b = CHARGE_STAT change produces INT pulse 1b = CHARGE_STAT change does not produces INT pulse

8.5.29 REG0x29_Charger_Mask_2 Register (Address = 0x29) [Reset = 0x00]

REG0x29_Charger_Mask_2 is shown in Table 8-37.

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Table 8-37. REG0x29_Charger_Mask_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	PG_MASK	R/W	0x0	Reset by: REG_RESET	Input Power Good INT mask: 0b = PG toggle produces INT pulse 1b = PG toggle does not produce INT pulse
6	RESERVED	R	0x0		Reserved
5	RESERVED	R	0x0		Reserved
4	TS_MASK	R/W	0x0	Reset by: REG_RESET	TS (Battery NTC) INT mask: 0b = TS_STAT change produces INT pulse 1b = TS_STAT change does not produce INT pulse
3	REVERSE_MASK	R/W	0x0	Reset by: REG_RESET	Reverse Mode INT mask: 0b = REVERSE_STAT toggle produces INT pulse 1b = REVERSE_STAT toggle does no produce INT pulse
2	RESERVED	R	0x0		Reserved
1	FSW_SYNC_MASK	R/W	0x0	Reset by: REG_RESET	FSW_SYNC pin signal INT mask: 0b = FSW_SYNC status change produces INT pulse 1b = FSW_SYNC status change does not produce INT pulse
0	MPPT_MASK	R/W	0x0	Reset by: REG_RESET	Max Power Point Tracking INT mask: 0b = MPPT_STAT rising edge produces INT pulse 1b = MPPT_STAT rising edge does no produce INT pulse

8.5.30 REG0x2A_Fault_Mask Register (Address = 0x2A) [Reset = 0x00]

REG0x2A_Fault_Mask is shown in Table 8-38.

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Table 8-38. REG0x2A_Fault_Mask Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VAC_UV_MASK	R/W	0x0	Reset by: REG_RESET	Input under-voltage INT mask: 0b = Input under-voltage event produces INT pulse 1b = Input under-voltage event does not produce INT pulse

Table 8-38. REG0x2A_Fault_Mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
6	VAC_OV_MASK	R/W	0x0	Reset by: REG_RESET	Input over-voltage INT mask: 0b = Input over-voltage event produces INT pulse 1b = Input over-voltage event does not produce INT pulse
5	IBAT_OCP_MASK	R/W	0x0	Reset by: REG_RESET	Battery over-current INT mask: 0b = Battery over-current event produces INT pulse 1b = Battery over-current event does not produce INT pulse
4	VBAT_OV_MASK	R/W	0x0	Reset by: REG_RESET	Battery over-voltage INT mask: 0b = Battery over-voltage event produces INT pulse 1b = Battery over-voltage event does not produce INT pulse
3	TSHUT_MASK	R/W	0x0	Reset by: REG_RESET	Thermal shutdown INT mask: 0b = TSHUT event produces INT pulse 1b = TSHUT event does not produce INT pulse
2	CHG_TMR_MASK	R/W	0x0	Reset by: REG_RESET	Charge safety timer INT mask: 0b = Timer expired rising edge produces INT pulse 1b = Timer expired rising edge does not produce INT pulse
1	DRV_OKZ_MASK	R/W	0x0	Reset by: REG_RESET	DRV_SUP pin voltage INT mask: 0b = DRV_SUP pin fault produces INT pulse 1b = DRV_SUP pin fault does not produce INT pulse
0	RESERVED	R	0x0		Reserved

8.5.31 REG0x2B_ADC_Control Register (Address = 0x2B) [Reset = 0x60]

REG0x2B_ADC_Control is shown in Table 8-39.

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Table 8-39. REG0x2B_ADC_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	ADC_EN	R/W	0x0	When EN_VREG_TEMP_COMP = 1, the ADC will be automatically enabled, regardless of the status of ADC_EN Reset by: REG_RESET WATCHDOG	ADC control: 0b = Disable ADC 1b = Enable ADC
6	ADC_RATE	R/W	0x1	Reset by: REG_RESET	ADC conversion rate control: 0b = Continuous conversion 1b = One-shot conversion
5:4	ADC_SAMPLE	R/W	0x2	Reset by: REG_RESET	ADC sample speed: 00b = 15 bit effective resolution 01b = 14 bit effective resolution 10b = 13 bit effective resolution 11b = Reserved
3	ADC_AVG	R/W	0x0	Reset by: REG_RESET	ADC average control: 0b = Single value 1b = Running average

Table 8-39. REG0x2B_ADC_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
2	ADC_AVG_INIT	R/W	0x0	Reset by: REG_RESET	ADC average initial value control: 0b = Start average using existing register value 1b = Start average using new ADC conversion
1:0	RESERVED	R	0x0		Reserved

8.5.32 REG0x2C_ADC_Channel_Control Register (Address = 0x2C) [Reset = 0x0A]

REG0x2C_ADC_Channel_Control is shown in Table 8-40.

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Table 8-40. REG0x2C_ADC_Channel_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	IAC_ADC_DIS	R/W	0x0	Reset by: REG_RESET	IAC ADC control 0b = Enable 1b = Disable
6	IBAT_ADC_DIS	R/W	0x0	Recommend to disable IBAT ADC channel when EN_IBAT_LOAD bit is 1 Reset by: REG_RESET	IBAT ADC control 0b = Enable 1b = Disable
5	VAC_ADC_DIS	R/W	0x0	Reset by: REG_RESET	VAC ADC control 0b = Enable 1b = Disable
4	VBAT_ADC_DIS	R/W	0x0	Reset by: REG_RESET	VBAT ADC control 0b = Enable 1b = Disable
3	RESERVED	R	0x0		Reserved
2	TS_ADC_DIS	R/W	0x0	Reset by: REG_RESET	TS ADC control 0b = Enable 1b = Disable
1	VFB_ADC_DIS	R/W	0x1	Reset by: REG_RESET	VFB ADC control Recommend to disable this channel when charging is enabled 0b = Enable 1b = Disable
0	RESERVED	R	0x0		Reserved

8.5.33 REG0x2D_IAC_ADC Register (Address = 0x2D) [Reset = 0x0000]

REG0x2D_IAC_ADC is shown in Table 8-41.

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I2C REG0x2E=[15:8], I2C REG0x2D=[7:0]

Table 8-41. REG0x2D_IAC_ADC Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:0	IAC_ADC	R	0x0		IAC ADC reading with 5mΩ RAC_SNS: Reported as 2s complement POR: 0mA(0h) Format: 2s Complement Range: -20000mA - 20000mA (9E58h-61A8h) Clamped Low Clamped High Bit Step: 0.8mA

8.5.34 REG0x2F_IBAT_ADC Register (Address = 0x2F) [Reset = 0x0000]

REG0x2F_IBAT_ADC is shown in Table 8-42.

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I2C REG0x30=[15:8], I2C REG0x2F=[7:0]

Table 8-42. REG0x2F_IBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:0	IBAT_ADC	R	0x0		IBAT ADC reading with 5mΩ RBAT_SNS: Reported as 2s complement POR: 0mA (0h) Format: 2s Complement Range: -20000mA-20000mA (D8F0h-2710h) Clamped Low Clamped High Bit Step: 2mA

8.5.35 REG0x31_VAC_ADC Register (Address = 0x31) [Reset = 0x0000]

REG0x31_VAC_ADC is shown in Table 8-43.

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I2C REG0x32=[15:8], I2C REG0x31=[7:0]

Table 8-43. REG0x31_VAC_ADC Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:0	VAC_ADC	R	0x0		VAC ADC reading: Reported as unsigned integer POR: 0mV (0h) Format: 2s Complement Range: 0mV-60000mV (0h-7530h) Clamped Low Bit Step: 2mV

8.5.36 REG0x33_VBAT_ADC Register (Address = 0x33) [Reset = 0x0000]

REG0x33_VBAT_ADC is shown in Table 8-44.

Return to the Summary Table.

I2C REG0x34=[15:8], I2C REG0x33=[7:0]

Table 8-44. REG0x33_VBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:0	VBAT_ADC	R	0x0		VBAT ADC reading: Reported as unsigned integer POR: 0mV (0h) Format: 2s Complement Range: 0mV-60000mV (0h-7530h) Clamped Low Bit Step: 2mV

8.5.37 REG0x37_TS_ADC Register (Address = 0x37) [Reset = 0x0000]

REG0x37_TS_ADC is shown in Table 8-45.

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I2C REG0x38=[15:8], I2C REG0x37=[7:0]

Table 8-45. REG0x37_TS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:0	TS_ADC	R	0x0		TS ADC reading as percentage of REGN: Reported as unsigned integer POR: 0%(0h) Range: 0% - 99.90234375% (0h-3FFh) Clamped High Bit Step: 0.09765625%

8.5.38 REG0x39_VFB_ADC Register (Address = 0x39) [Reset = 0x0000]

REG0x39_VFB_ADC is shown in Table 8-46.

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I2C REG0x3A=[15:8], I2C REG0x39=[7:0]

Table 8-46. REG0x39_VFB_ADC Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15:0	VFB_ADC	R	0x0		VFB ADC reading: POR: 0mV (0h) Range: 0mV-2047mV (0h-7FFh) Clamped High Bit Step: 1mV

8.5.39 REG0x3B_Gate_Driver_Strength_Control Register (Address = 0x3B) [Reset = 0x00]

REG0x3B_Gate_Driver_Strength_Control is shown in Table 8-47.

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Table 8-47. REG0x3B_Gate_Driver_Strength_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	BOOST_HS_DRV	R/W	0x0	Reset by: REG_RESET	Boost High Side FET Gate Driver Strength: 00b = Fastest 01b = Faster 10b = Slower 11b = Slowest

Table 8-47. REG0x3B_Gate_Driver_Strength_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
5:4	BUCK_HS_DRV	R/W	0x0	Reset by: REG_RESET	Buck High Side FET Gate Driver Strength: 00b = Fastest 01b = Faster 10b = Slower 11b = Slowest
3:2	BOOST_LS_DRV	R/W	0x0	Reset by: REG_RESET	Boost Low Side FET Gate Driver Strength: 00b = Fastest 01b = Faster 10b = Slower 11b = Slowest
1:0	BUCK_LS_DRV	R/W	0x0	Reset by: REG_RESET	Buck Low Side FET Gate Driver Strength: 00b = Fastest 01b = Faster 10b = Slower 11b = Slowest

8.5.40 REG0x3C_Gate_Driver_Dead_Time_Control Register (Address = 0x3C) [Reset = 0x00]

REG0x3C_Gate_Driver_Dead_Time_Control is shown in Table 8-48.

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Table 8-48. REG0x3C_Gate_Driver_Dead_Time_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:4	RESERVED	R	0x0		Reserved
3:2	BOOST_DEAD_TIME	R/W	0x0	Reset by: REG_RESET	Boost Side FETs Dead Time Control: 00b = 45ns 01b = 75ns 10b = 105ns 11b = 135ns
1:0	BUCK_DEAD_TIME	R/W	0x0	Reset by: REG_RESET	Buck Side FETs Dead Time Control: 00b = 45ns 01b = 75ns 10b = 105ns 11b = 135ns

8.5.41 REG0x3D_Part_Information Register (Address = 0x3D) [Reset = 0x32]

REG0x3D_Part_Information is shown in Table 8-49.

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Table 8-49. REG0x3D_Part_Information Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0x0		Reserved
6:3	PART_NUM	R	0x6		Part Number: 0110 - BQ25756E
2:0	DEV_REV	R	0x2		Device Revision:

8.5.42 REG0x62_Reverse_Mode_Battery_Discharge_Current Register (Address = 0x62) [Reset = 0x02]

REG0x62_Reverse_Mode_Battery_Discharge_Current is shown in Table 8-50.

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Table 8-50. REG0x62_Reverse_Mode_Battery_Discharge_Current Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7:6	IBAT_REV	R/W	0x0	Reset by: REG_RESET	Reverse mode battery discharge current limit: 00b = 20A 01b = 15A 10b = 10A 11b = 5A
5:2	RESERVED	R	0x0		Reserved
1	EN_CONV_FAST_TRANSIENT	R/W	0x1	Reset by: REG_RESET	Enable converter fast transient response in reverse mode only - 0b = Disable 1b = Enable
0	RESERVED	R	0x0		Reserved