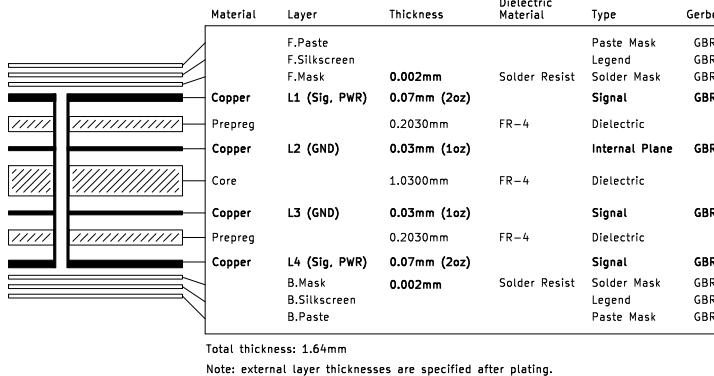


## Top Fabrication (Scale 1:1)

A

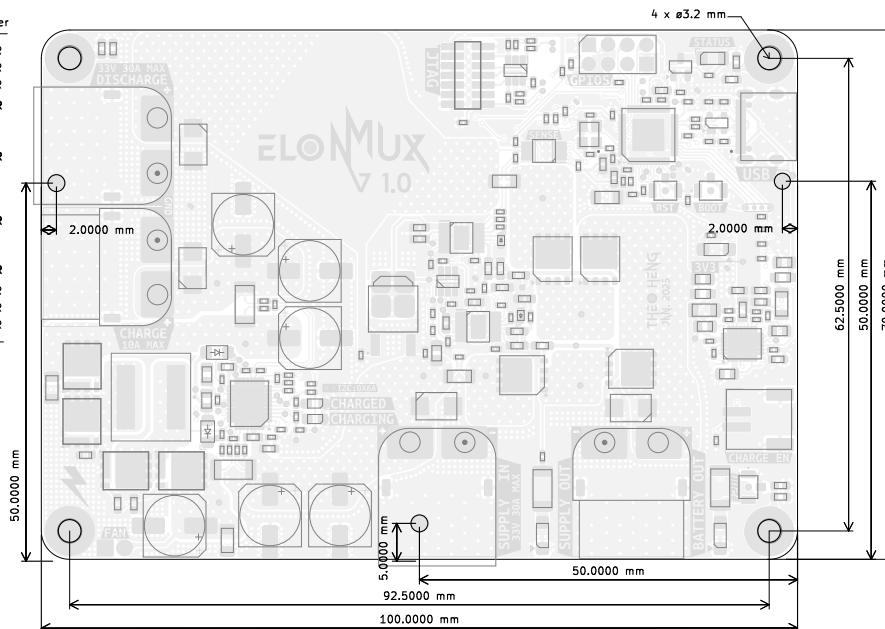
### Layer Stack Legend

JLC041621-7628(Standard/Finished thickness 1.64mm±10%)



B

L1 (Sig. PWR)(Scale 1:1)



### FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

- OUTLINE DEFINED IN SEPARATE GERBER FILE WITH "Edge\_Cuts.GBR" SUFFIX.  
DIMENSIONS OF CIRCUMSIZEZED RECTANGLE SHOWN ON THIS DWG FOR REF ONLY.
- SEE SEPARATE DRILL FILES WITH ".DRL" SUFFIX FOR HOLE LOCATIONS.  
SELECTED HOLE LOCATIONS SHOWN ON THIS DWG FOR REF ONLY.
- IMPEDANCE CONTROL REQUIRED.  
Microstrip 90-Ohm Differential (L1 ref. L2)  
0.2764mm width, 0.20mm spacing
- CONFIRM TRACE WIDTHS AND SPACINGS.
- DESIGN GEOMETRY MINIMUM FEATURE SIZES:  
TRACE WIDTH 0.20 mm  
TRACE TO TRACE 0.2 mm  
MIN. HOLE (PTH) ??? mm  
MIN. HOLE (NPTH) ??? mm  
ANNUAL RING 0.15 mm  
COPPER TO HOLE 0.254 mm  
COPPER TO EDGE 0.25 mm  
HOLE TO HOLE 0.254 mm

C

All dimensions are in millimeters unless otherwise specified.

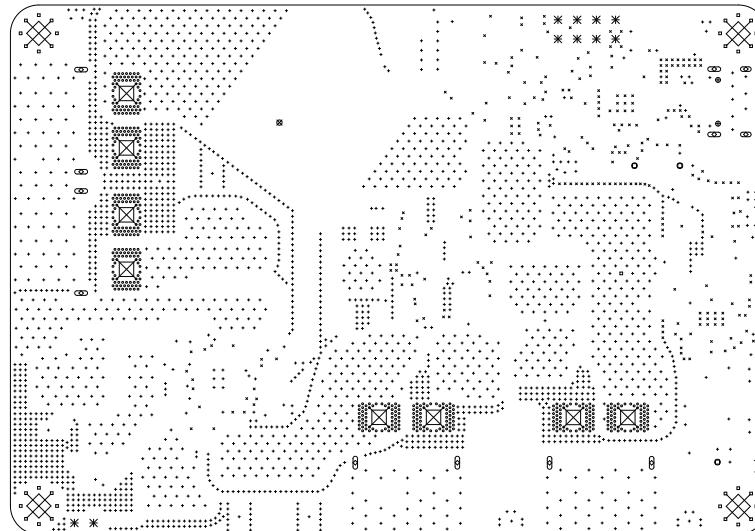
Comments:	Company: <b>EPFL Xplore</b> 	Variant: <b>Released</b>
Board Name: <b>ELOMUX</b> 		Project Name: <b>ERC</b>
Sheet Title: Assembly Document	File Name: ElonMux.kicad_pcb	Designer: Théo Heng
Sheet Path: FABRICATION_TOP	Reviewer: Federico Bise	Date: 2024-04-13
	Size: <b>A4</b>	Sheet: <b>of 1</b>

A

A

## Drill Drawing (Top View) (Scale 1:1)

Symbol	Count	Hole Size	Plated
·	264	0.25mm	Plated
·	480	0.25mm	Plated
·	2413	0.30mm	Plated
◦	33	0.50mm	Plated
◦	12 (slot)	0.60mm	Plated
☒	1	0.7mm	Plated
*	10	1.0mm	Plated
☒	8	2.7mm	Plated
☒	4	3.2mm	Plated
⊛	5	0.65–75mm	Unplated



B

B

C

C

D

D

Comments:	Company: EPFL Xplore		Variant: Released
	Board Name: <b>ELONMUX</b>		
Sheet Title: Assembly Document	File Name: ElonMux.kicad_pcb	Designer: Théo Heng	Date: 2024-04-13
Sheet Path: DRILL_DRAWING	Reviewer: Federico Bise	Size: <b>A4</b>	Sheet: of <b>1</b>

A

A

B

B

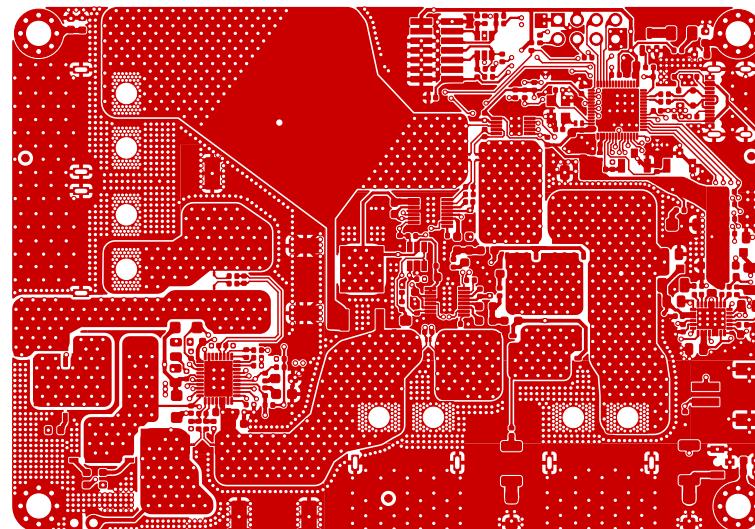
C

C

D

D

## L1 (Sig, PWR)(Scale 1:1)



Comments:	Company: EPFL Xplore	Variant: Released
Board Name: <b>ELONMUX</b>		Project Name: <b>ERC</b>
Sheet Title: Assembly Document	File Name: ElonMux.kicad_pcb	Designer: Théo Heng
Sheet Path: <b>L1</b>	Reviewer: Federico Bise	Date: 2024-04-13
	Size: <b>A4</b>	Sheet: <b>of 1</b>

A

A

B

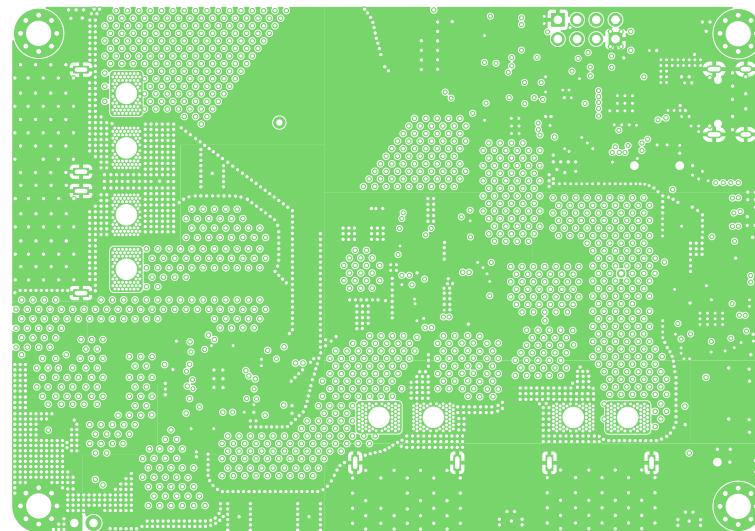
B

C

C

D

D

**L2 (GND)(Scale 1:1)**

Comments:	Company: EPFL Xplore	Variant: Released
Board Name: <b>ELONMUX</b>		Project Name: <b>ERC</b>
Sheet Title: Assembly Document	File Name: ElonMux.kicad_pcb	Designer: Théo Heng
Sheet Path: <b>L2</b>	Reviewer: Federico Bise	Date: 2024-04-13
	Size: <b>A4</b>	Sheet: <b>of 1</b>

A

A

B

B

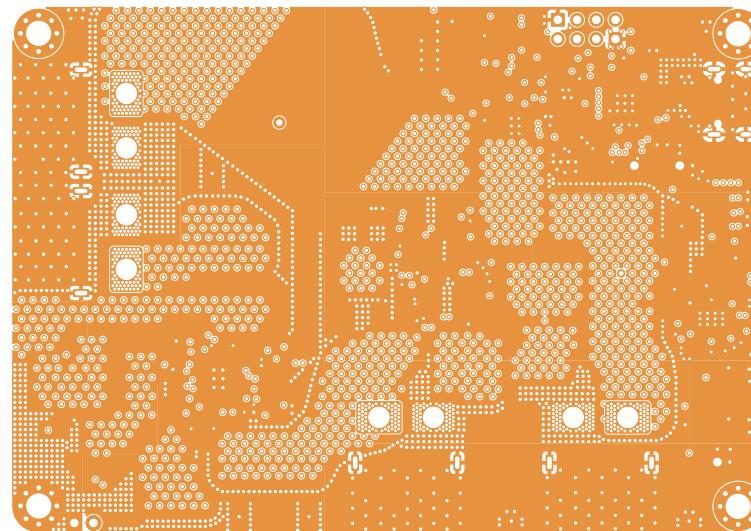
C

C

D

D

### L3 (GND)(Scale 1:1)



Comments:	Company: EPFL Xplore	Variant: Released		
Board Name: <b>ELONMUX</b>		Project Name: <b>ERC</b>		
Sheet Title: Assembly Document	File Name: ElonMux.kicad_pcb	Designer: Théo Heng	Date: 2024-04-13	Revision: 1.1
Sheet Path: <b>L3</b>	Reviewer: Federico Bise		Size: <b>A4</b>	Sheet: <b>of 1</b>

A

A

B

B

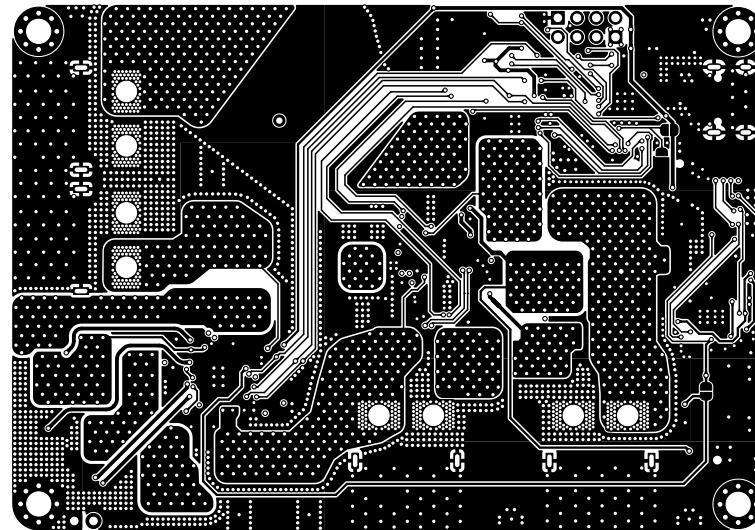
C

C

D

D

### L4 (Sig, PWR)(Scale 1:1)



Comments:	Company: EPFL Xplore	Variant: Released		
Board Name: <b>ELONMUX</b>		Project Name: <b>ERC</b>		
Sheet Title: Assembly Document	File Name: ElonMux.kicad_pcb	Designer: Théo Heng	Date: 2024-04-13	Revision: 1.1
Sheet Path: <b>L4</b>	Reviewer: Federico Bise	Size: <b>A4</b>	Sheet: <b>of 1</b>	