



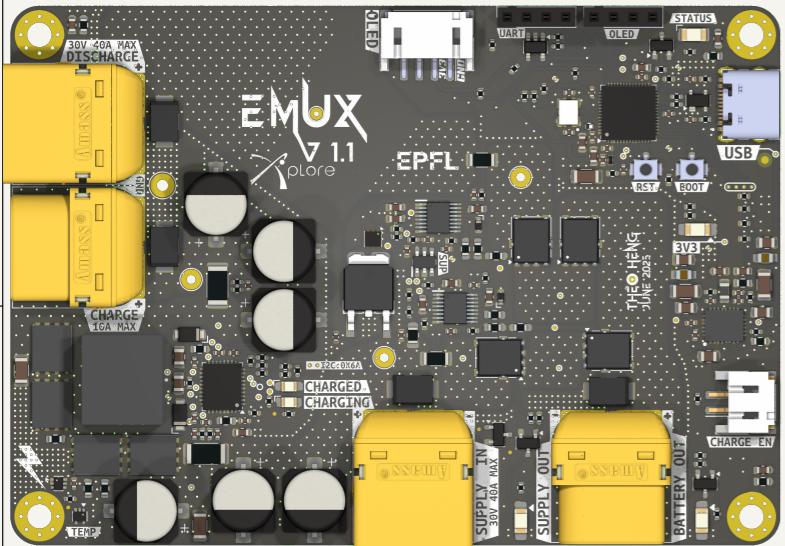
Variant: Released

2025-07-24

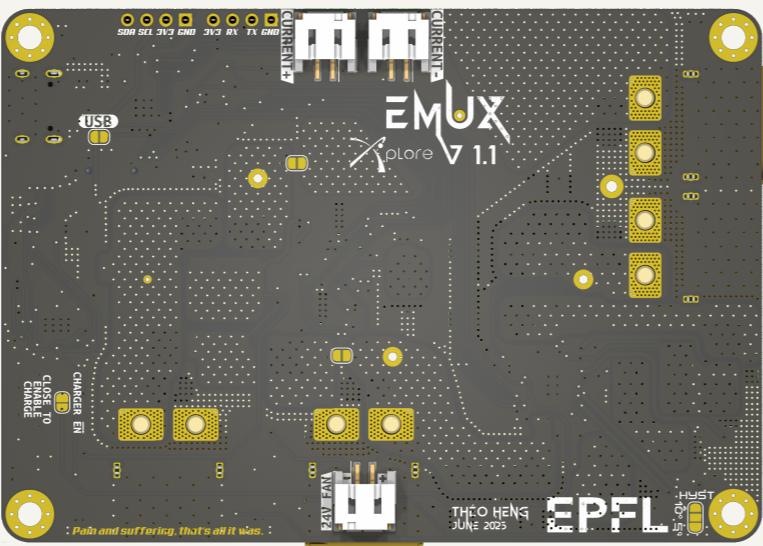
Rev 1.1

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TOP VIEW



BOTTOM VIEW



DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for debug notes.

DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

NOTES

Board designed for EPFL Xplore's rover in the context of the European Rover Challenge.
Schematic based on Vincent Nguyen's Template. Many thanks to him for making this public.

Not fitted components are marked as

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

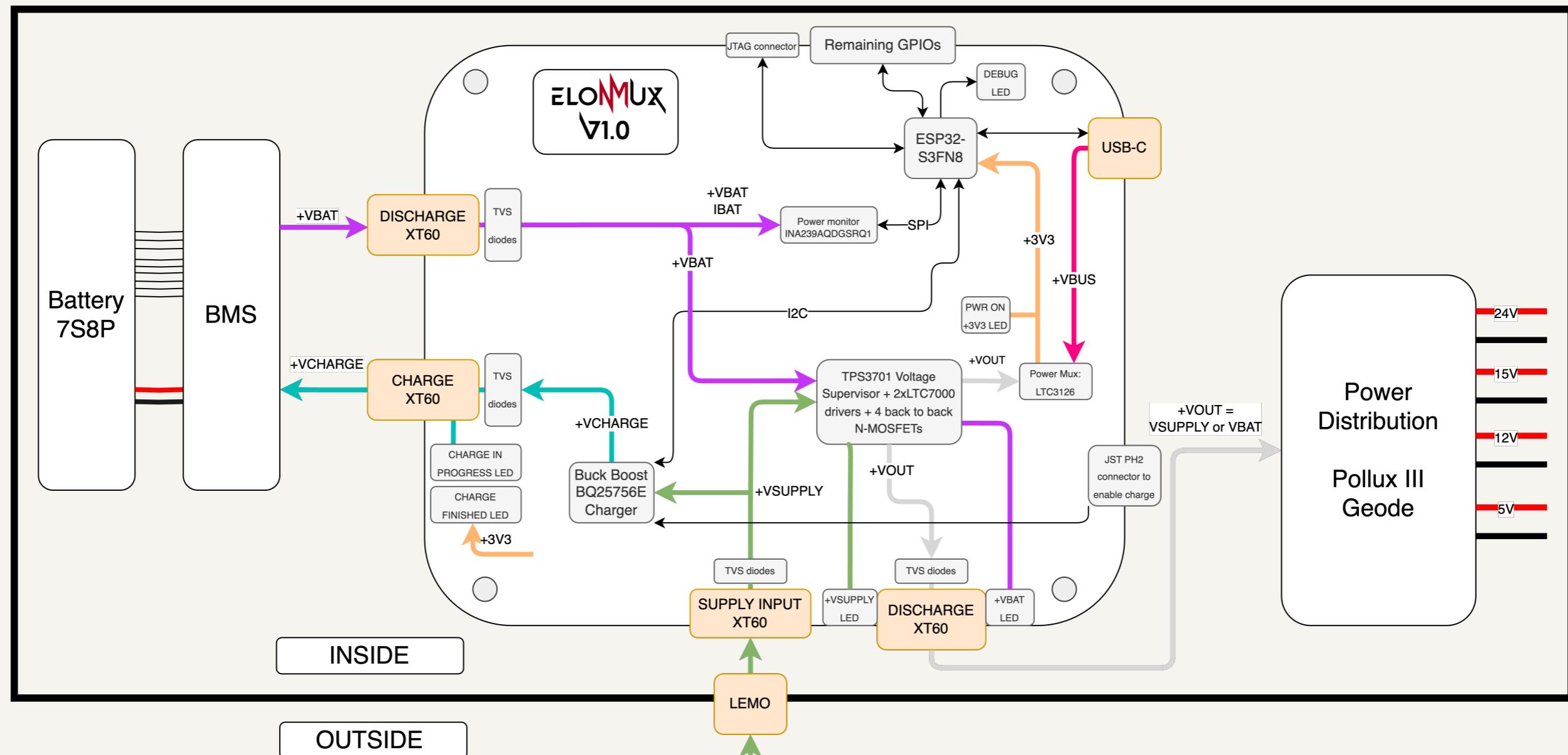
CHECKED - There shouldn't be any mistakes. Contact the engineer if you find any.

RELEASED - A board with this schematic has been sent to production.

Released 24-07-2025

Comments:	Company: EPFL Xplore	Variant: Released
Board Name: 	Project Name: ERC	
Sheet Title: Cover Page	File Name: ElonMux.kicad_sch	Designer: Théo Heng
Sheet Path: /	Reviewer: Federico B. - Eliot A. - Arion Z.	Date: 2025-07-24
	Size: A3	Revision: 1.1
	Sheet: 1 of 13	

[2] Block Diagram



The purpose of this board is to be able to charge a battery and power the main load simultaneously from the same external power supply. The user have to be able to plug and unplug the power supply from the rover without shutting down/rebooting the load, requiring fast switching times.

The system will always try to use the external power supply as the primary power source for the rover, but will default to the battery if it is not available.

Maximum rating:

Input voltage (battery&supply): 10V - 30V

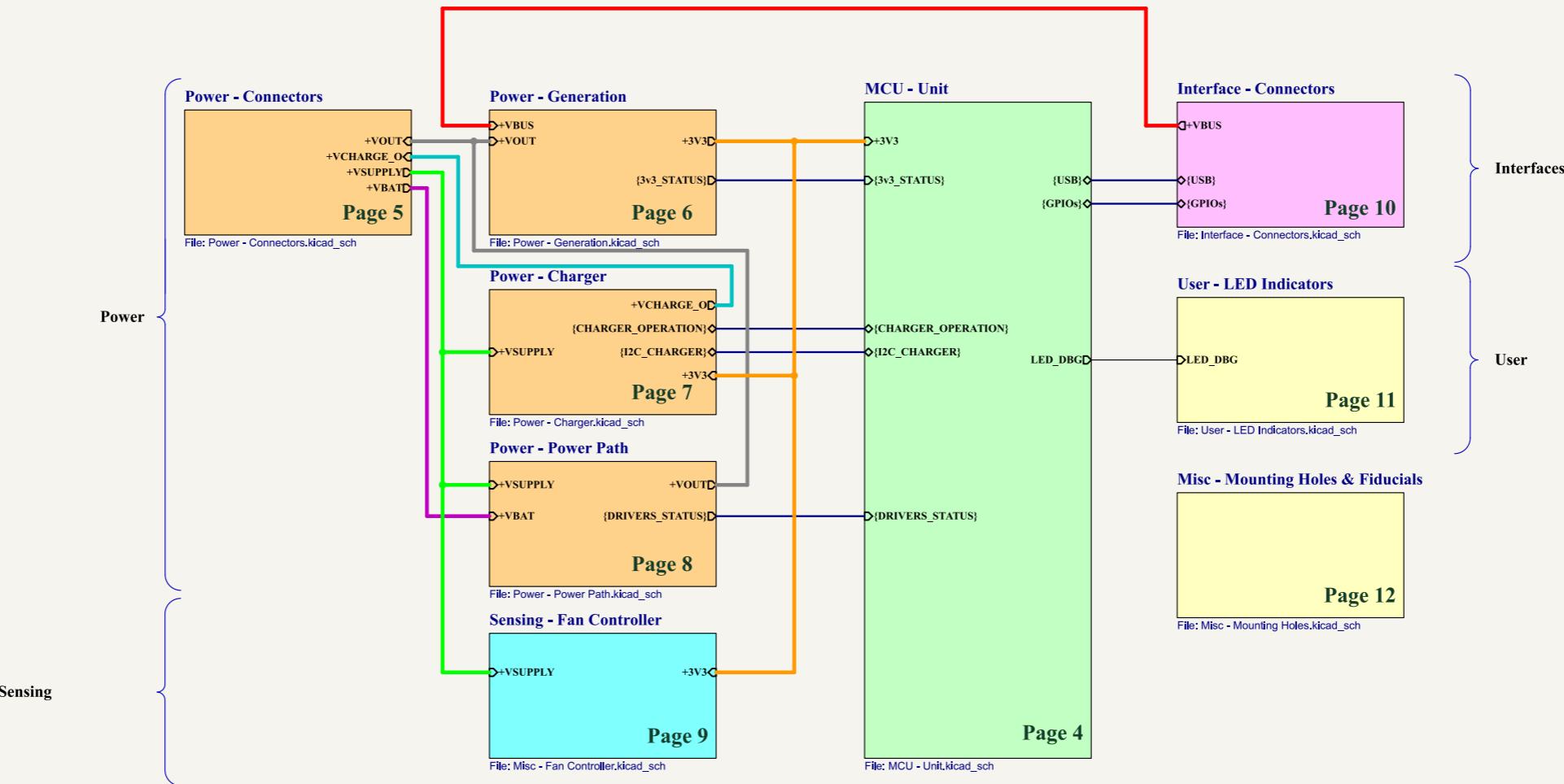
Continuous supply current: 40A

Continuous discharge current: 40A

Continuous charge current: 10A

Comments: Made in draw.io	Company: EPFL Xplore	Variant: Released
Board Name: EMUX		Project Name: ERC
Sheet Title: Block Diagram	File Name: Block Diagram.kicad_sch	Designer: Théo Heng
Sheet Path: /Block Diagram/	Reviewer: Federico B. - Eliot A. - Arion Z.	Date: 2025-07-24
	Size: A3	Revision: 1.1
		Sheet: 2 of 13

[3] Project Architecture



Comments:	Company: EPFL Xplore	Variant: Released
Board Name: EMUX		Project Name: ERC
Sheet Title: Project Architecture	File Name: Project Architecture.kicad_sch	Designer: Théo Heng
Sheet Path: /Project Architecture/	Reviewer: Federico B. - Eliot A. - Arion Z.	Date: 2025-07-24
		Revision: 1.1
	Size: A3	Sheet: 3 of 13

[4] MCU - Unit

Table 3-5. JTAG Signal Source Control				
JTAG Signal Source	EFUSE_DIS_PAD_JTAG	EFUSE_DIS_USB_JTAG	EFUSE_STRAP_JTAG_SEL	GPIO3
USB Serial/JTAG Controller	0	0	1	1
	1	0	Ignored	Ignored
JTAG pins 2	0	0	1	0
	0	1	Ignored	Ignored
JTAG is disabled	1	1	Ignored	Ignored

¹ Bold marks the default value and configuration.
² JTAG pins refer to MTDI, MTCK, MTMS, and MTDI.

DESIGN NOTE - I₂C pull-Up resistors:
R_{min} = (VDDmax - VOLmax) / I_{OL}
System I₂C voltage: VDD = 3.3V +/- 5% -> 3.47V
Low level output voltage (I₂C specs): VOLmax = 0.4V
Low level output current (I₂C specs): I_{OL} = 3mA
R_{min} = (3.47V - 0.4V) / 3mA ≈ 1k Ohm

R_{max} = (1.18 x trmax) / C_b
Standard mode (I₂C specs): trmax = 1000ns
C_{bmax} = 400pF (worst case)
⇒ R_{max} = (1.18 x 1000ns) / 400pF ≈ 3k Ohm
C_{bmin} = 50pF (only 1-2 devices on bus)
⇒ R_{max} = (1.18 x 1000ns) / 50pF ≈ 24k Ohm

Smaller resistors decrease rise time but increase power consumption.

USB flash: bridge to 3V3
JTAG flash: bridge to GND
SOLDER ONLY ONE AT A TIME
DO NOT LEAVE FLOATING

DESIGN NOTE - CLK caps:
C₁ = 10pF (load capacitance)
C_p = 5pF (stray capacitance)
C₁ = C₂ = C

C₁ = (C₁ x C₂)/(C₁+C₂) + C_p
10p C0G (NP0) 50V

C₁ = C₂ = 10pF

LAYOUT NOTE:
Place the 24nH inductor as close as the IC as possible. It is best not to route any signal trace under the crystal.

Ideally if space allows, add a 0.1uF capacitor on each ADC lines used to read values (IMON1 & 2)

MCU I/O

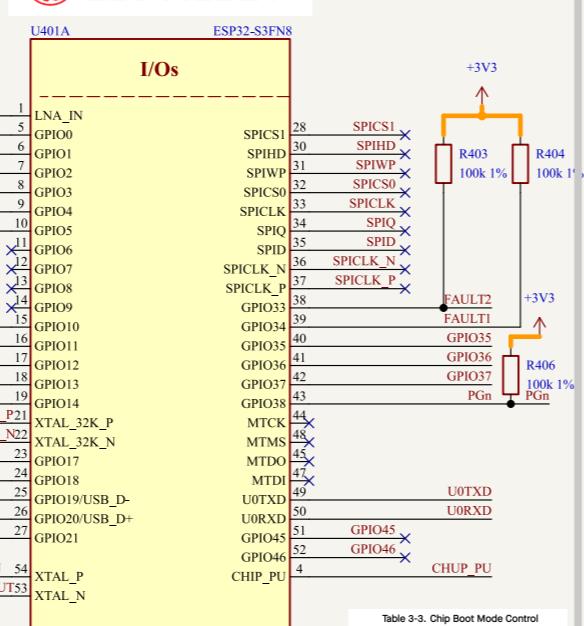
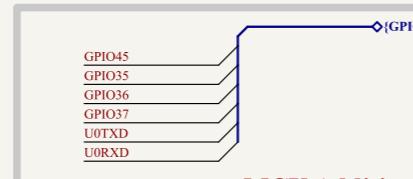


Table 3-1. Default Configuration of Strapping Pins		
Strapping Pin	Default Configuration	Bit Value
GPIO0	Weak pull-up	1
GPIO3	Floating	-
GPIO45	Weak pull-down	0
GPIO46	Weak pull-down	0

¹ Bold marks the default value and configuration.
² Joint Download Boot mode supports the following download methods:

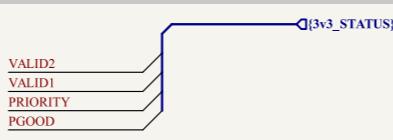
- USB Download Boot:
 - USB-Serial JTAG Download Boot
 - USB-OTG Download Boot
 - UART Download Boot

Removed JTAG in V1.1



DESIGN NOTE:
GPIO 35, 36 & 37 are available only because we are not using octal SPI for the internal 8MB FLASH.

MCU Additional I/Os



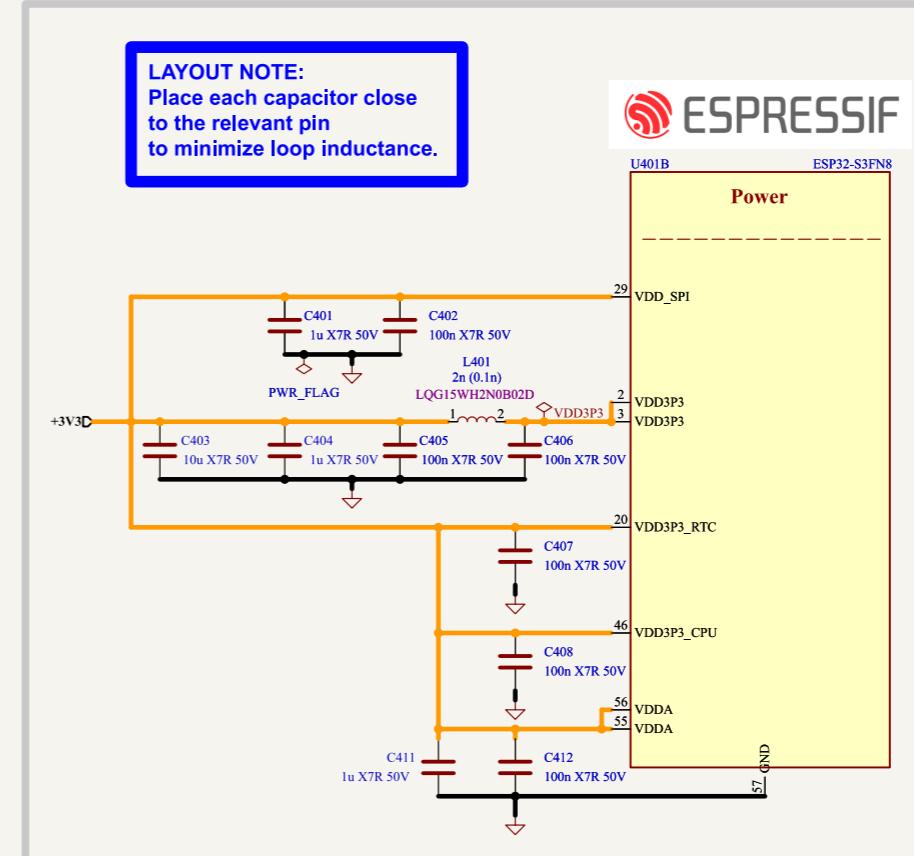
3V3 Buck Status



USB-C Interface

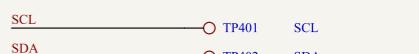


Drivers Status & Sensing



MCU POWER

I₂C - Charge



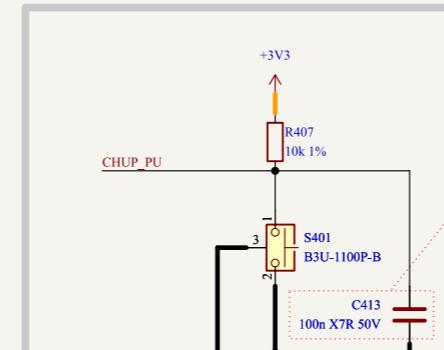
OTHER SIGNALS

INTn	TP403	CHARGER_STATUS
LED_DBG	TP404	LED_DBG
PRIORITY	TP405	PRIORITY
VALID1	TP406	VALID1
VALID2	TP407	VALID2
PGOOD	TP408	PGOOD
FAULT1	TP409	FAULT1
FAULT2	TP410	FAULT2
IMON1	TP411	IMON1
IMON2	TP412	IMON2
PGn	TP413	MODE

GND



Test Points

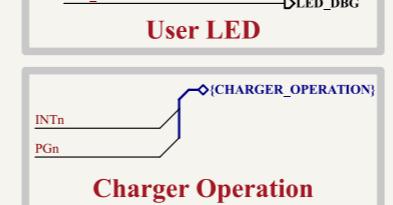
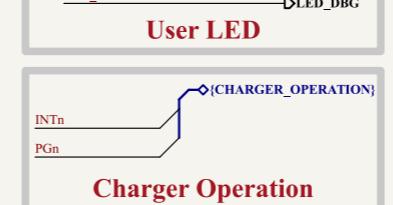


DESIGN NOTE - reset button capacitor:

Debouncing: It smooths out any quick, unintended changes in voltage due to mechanical bounce in the button switch. This ensures that when the reset button is pressed, it reliably resets without multiple unintended toggles.

Power Stabilization: It can also help stabilize the power when the chip resets, which may reduce potential issues during the reset process.

MCU Chip Reset



Comments:

Espressif Schematic Checklist
Espressif Datasheet p.25 (CHIP_PU)
Espressif Datasheet p.30 (GPIO0 boot)
Ph's Lab - SPI Hardware & PCB Design
Flashing ESP32-S3 with USB
ESP32-S3 BOOT selection

Company:
EPFL Xplore

Variant:

Released

Board Name:



Project Name:

ERC

Sheet Title:

MCU - Unit

File Name:

MCU - Unit.kicad_sch

Designer:

Théo Heng

Date:

2025-07-24

Revision:

1.1

Sheet Path:

/Project Architecture/MCU - Unit/

Reviewer:

Federico B. - Eliot A. - Arion Z.

Size:

A3

Sheet:

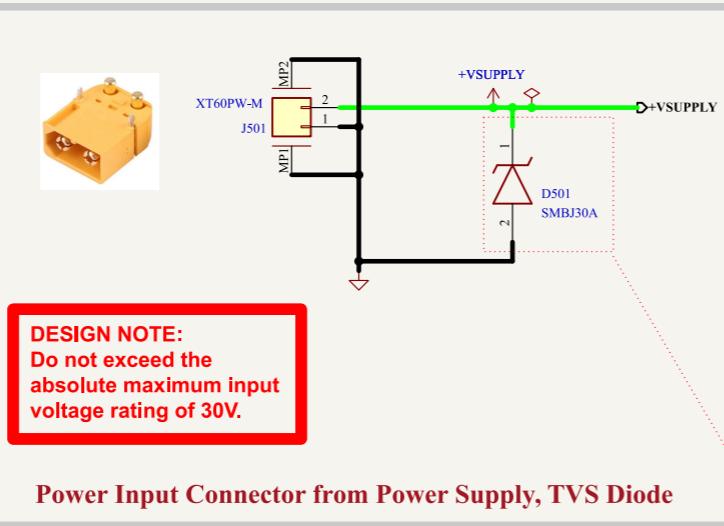
4 of 13

[5] Power - Connectors

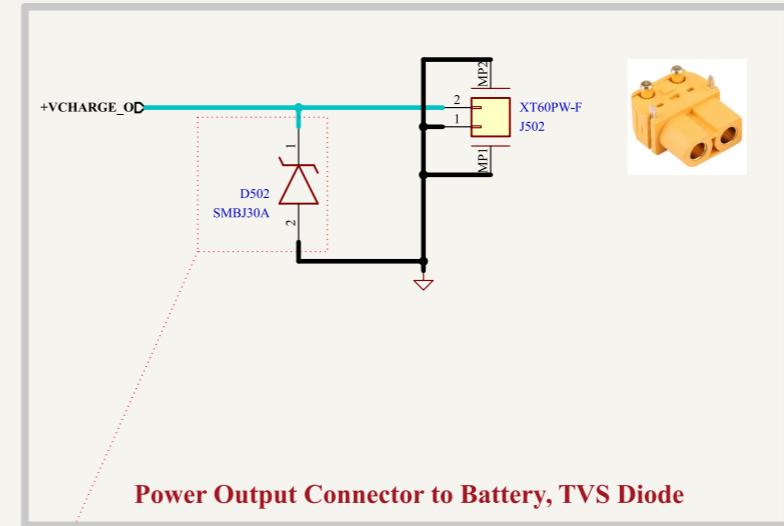
DESIGN NOTE:

No reverse polarity protection implemented. TVS diodes does not protect the PCB against reverse polarity.

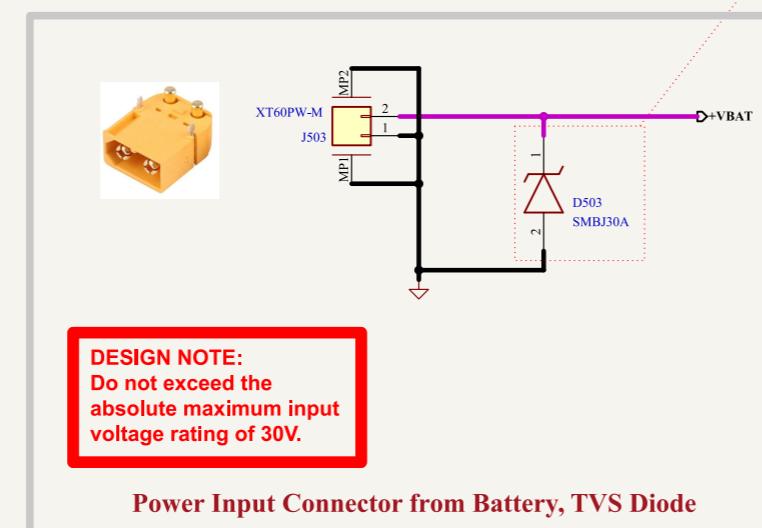
Always adhere to established industry conventions for connector polarity and gender to ensure compatibility and prevent reverse polarity connections. The female connector should always carry the power source with recessed contacts to minimize the risk of accidental short circuits. Polarity protection could be nice improvements for V1.1.



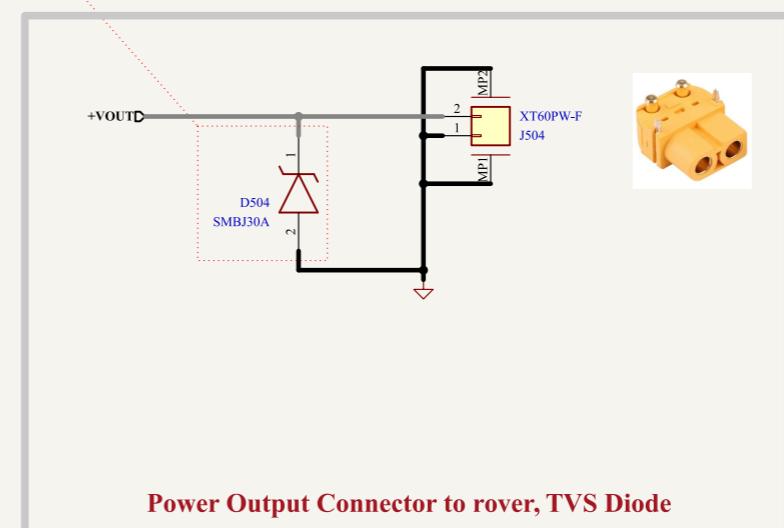
DESIGN NOTE:
Do not exceed the absolute maximum input voltage rating of 30V.



LAYOUT NOTE:
Place TVS diode near input power connectors, with an orientation minimizing the return path.



DESIGN NOTE:
Do not exceed the absolute maximum input voltage rating of 30V.



DESIGN NOTE:

TVS (Transient Voltage Suppression) are used to protect circuits from voltage spikes by clamping high voltages to a safe level.

Bidirectional diodes bring no additional benefits compared to unidirectional diodes and are in fact even a bit worse, as they will clamp later negative transients.

In situations like this, when the battery and power supply are always positive values, unidirectional diodes are better suited.

Bidirectional diodes are meant to be used to protect lines that usually go to negative values, like differential lines.

SMBJ33CA:

Reverse Stand off voltage (= working voltage): 30.0V (maximum continuous voltage that can be applied to the diode without it conducting current)
Min Breakdown Voltage: 33.30V
Max Breakdown Voltage: 36.8V
The breakdown voltage range (from 33.3V to 36.8V) ensures the diode begins to conduct in response to harmful spikes, not minor voltage changes.
Max Clamping Voltage: 48.40V (maximum voltage the protected circuit will experience for any spike of 53.3V or more)
Peak Pulse Power Dissipation: 600W
Peak Forward Surge Currents: 100A

Comments:
Inspired by Amulet controller Schematics by Vincent Nguyen
Uni or bi directional TVS diodes?

Company:
EPFL Xplore

Company:
EMUX

Variant:
Released

Board Name:
EMUX

Project Name:
ERC

Date:
2025-07-24

Revision:
1.1

Sheet Title:

Power - Connectors

File Name:
Power - Connectors.kicad_sch

Designer:
Théo Heng

Sheet Path:

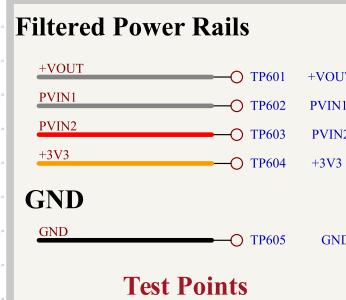
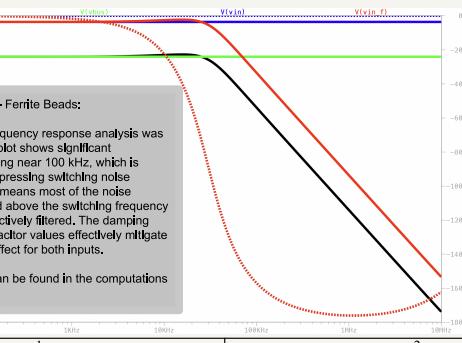
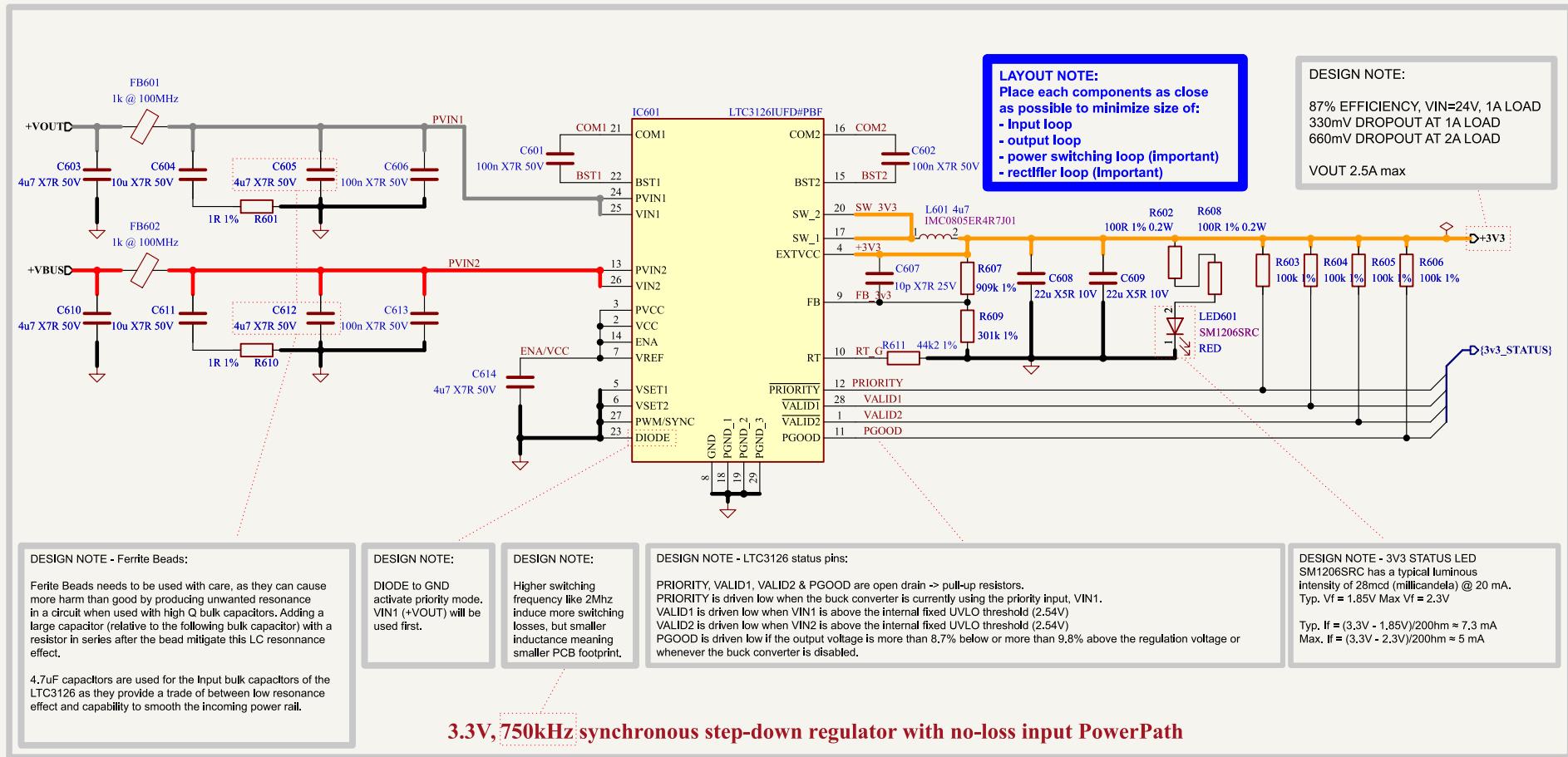
/Project Architecture/Power - Connectors/

Reviewer:
Federico B. - Eliot A. - Arion Z.

Size:
A3

Sheet:
5 of 13

[6] Power - Generation



Comments: LTC3126 Datasheet p.24 (schematic) LTC3126 Datasheet p.22 (layout) Ferrite Beads Demystified	Company: EPFL Xplore	Variant: Released
Board Name: EMUX		Project Name: ERC
Sheet Title: Power - Generation	File Name: Power - Generation.kicad_sch	Designer: Théo Heng
Sheet Path: /Project Architecture/Power - Generation/	Reviewer: Federico B. - Eliot A. - Arion Z.	Date: 2025-07-24 Revision: 1.1

[7] Power - Charger

Filtered Power Rails

+VCHARGE → TP701 +VCHARGE
+VCHARGE_O → TP702 +VCHARGE_O
+VSUPPLY_C → TP703 +VSUPPLY_C

Bridge Driver

HIDRV1 → TP704 HIDRV1
HIDRV2 → TP705 HIDRV2
LDRV1 → TP706 LDRV1
LDRV2 → TP707 LDRV2
SW1 → TP708 SW1
SW2 → TP709 SW2
STAT1 → TP710 STAT1
STAT2 → TP711 STAT2
CEn → TP712 CEn
DRV_SUP → TP713 DRV_SUP
REGN → TP714 REGN
BTST1 → TP715 BTST1
BTST2 → TP716 BTST2
+3V3 → TP717 +3V3

GND

GND → TP718 GND
GND → TP719 GND

Test Points

Under/over voltage input protection:
If unused, tie ACUV to VAC and ACOV to PGND in order to apply the internal VAC operating window (VVAC_OP: 4.2-36V)

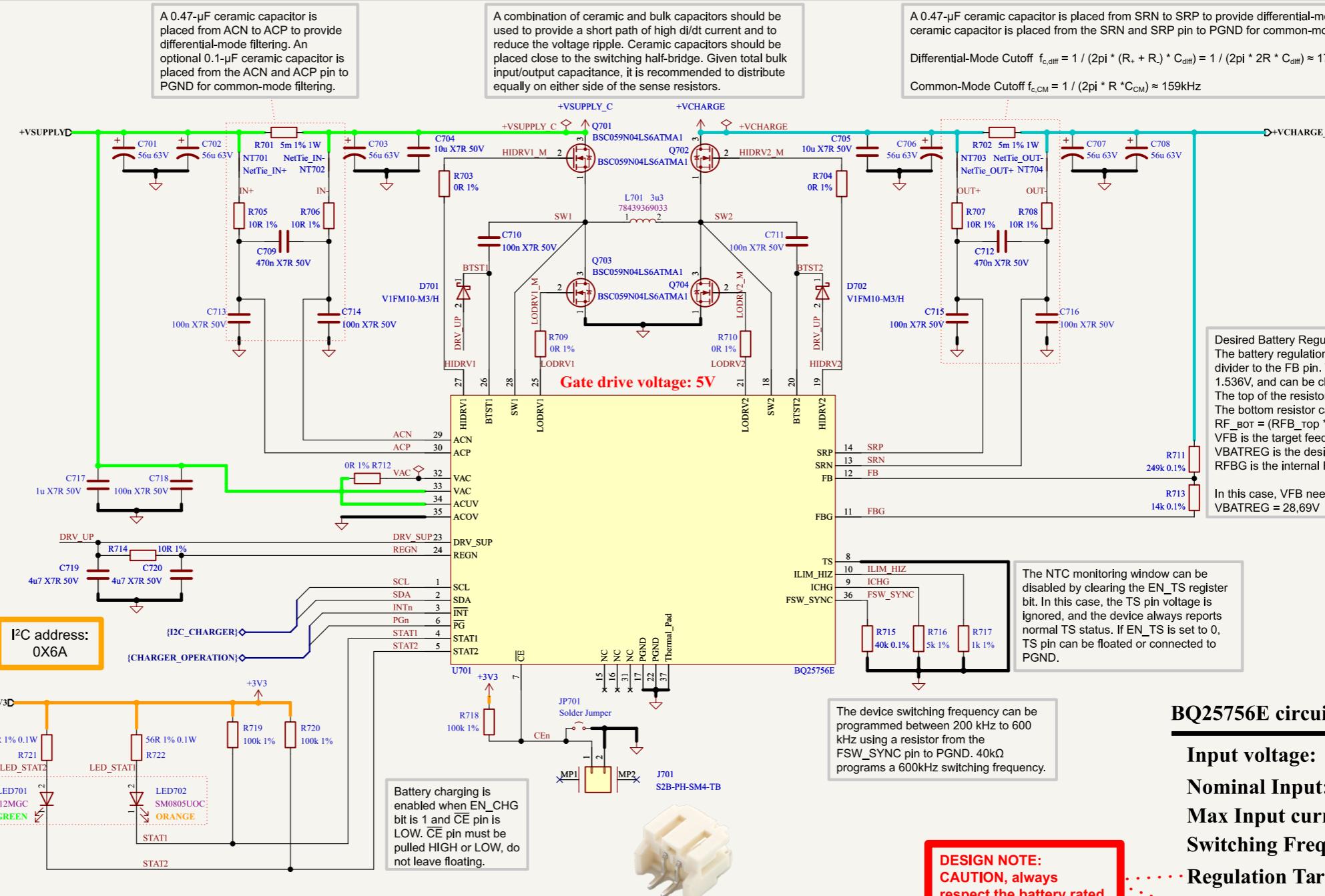
DESIGN NOTE - 3V3 STATUS LEDs

ORANGE LED:
SM0805UOC has a typical luminous intensity of 80 mcd (millicandela) @ 20 mA.
Typ. VF = 2.1V Max VF = 2.6V

Typ. If = (3.3V - 2.1V)/56Ω = 21 mA
Max. If = (3.3V - 2.6V)/56Ω = 13 mA
P = 2.1V×21mA = 44 mW < 78 mW (max rating)

GREEN LED:
AP2012MGC has a typical luminous intensity of 60 mcd (millicandela) @ 20 mA.
Typ. VF = 2.1V Max VF = 2.5V

Typ. If = (3.3V - 2.1V)/56Ω = 21 mA
Max. If = (3.3V - 2.5V)/56Ω = 14 mA
P = 2.1V×21mA = 44 mW < 75 mW (max rating)



BQ25756E: I2C Controlled, 1- to 7-Cell 600kHz Buck-Boost Battery Charge Controller

DESIGN NOTE - Charger Losses:

Switching losses:
 $P_{switch} = 0.5 * V_{ds} * I * (t_{rise} + t_{fall}) * f_{switch}$
 $P_{switch} = 0.5 * 28.8V * 7A * (1.2ns + 2 ns) * 600\text{kHz}$
 $P_{switch} = 0.19\text{ W}$

Conduction losses:
 $P_{cond} = I^2 * R_{ds}$
 $P_{cond} = 7^2 A * 5.9\text{ mOmh} = 0.29\text{ W}$

Gate drive losses:
 $P_{gate} = Q_g * V_{gs} * f_{switch}$
 $P_{gate} = 9.4nC * 28.8V * 600\text{ kHz}$
 $P_{gate} = 0.16\text{ W}$

Total pwr at 7A = $0.19\text{W} + 0.29\text{W} + 0.16\text{W} = 0.65\text{W}$
Total pwr at 10A = $0.27\text{W} + 0.6\text{W} + 0.16\text{W} = 1.03\text{W}$

DESIGN NOTE:

CAUTION: Charging the battery with more than 7A requires proper thermal management, such as adequate airflow or heatsinks, to prevent overheating of the MOSFETs.

DESIGN NOTE - Thermal MOS dissipation

Thermal resistance on PCB: 50°C/W

→ 0.65W * 50°C = 32,5 °C increase MOSFET @ ~55 °C

→ 1.03W * 50°C = 51,5 °C increase MOSFET @ ~75 °C

BSC059N04LS6ATMA1 40V N-Channel NexFET™ Power MOSFETs:

VDS(Drain-Source Breakdown Voltage) = 40V
Maximum voltage the MOSFET can handle between the drain and source when it's off.

RDS(on) (Drain-Source On-Resistance) = 6.8 mΩ @ 4.5V VGS

ID - Continuous Drain Current = 59A
Maximum continuous current the MOSFET can handle under specified conditions without overheating.

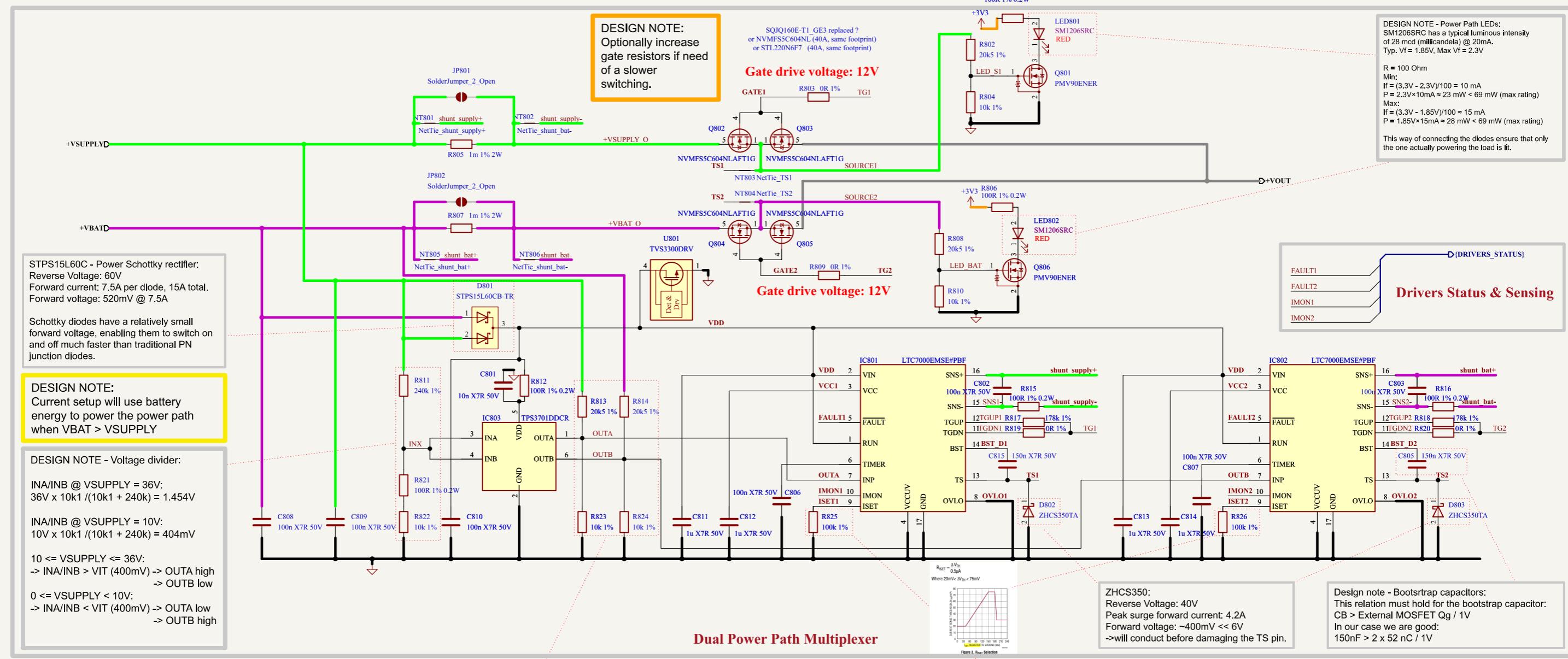
VGS(th) - Gate-Source Threshold Voltage = 1.3V - 2.3V

VGS - Gate-Source Voltage = ±20V
Maximum safe voltage between the gate and source terminals without damaging the gate.

CHARGING STATE	STAT1 ORANGE LED	STAT2 GREEN LED
Charge in progress (including recharge)	ON	OFF
Charge done	OFF	ON
Charging fault detected (TS out of range, safety timer fault, etc.)	ON	ON
Charge disabled (EN_CHG = 0, or CE pin high)	OFF	OFF

Comments: Detailed computations are available in the computations folder, using TI's provided tool.	Company: EPFL Xplore	Variant: Released
	Board Name: EMUX	Project Name: ERC
Sheet Title: Power - Charger	File Name: Power - Charger.kicad_sch	Designer: Théo Heng
Sheet Path: /Project Architecture/Power - Charger/	Reviewer: Federico B. - Eliot A. - Arion Z.	Date: 2025-07-24
		Revision: 1.1
	Size: A3	Sheet: 7 of 13

[8] Power - Power Path



DESIGN NOTE - Delay when switching between loads:

Battery Plugged (OUTA low, OUTB high) \rightarrow Plugging of Supply:
TPS3701: OUTA: low \rightarrow high 28.1us + 2.7us OUTB: high \rightarrow low 28.1us + 0.12us
LTC7000 TGDN1 low \rightarrow high worst case: 35ns + 13ns = 48ns
LTC7000 TGDN2 high \rightarrow low worst case: 70ns + 40ns = 110ns
CSD18540Q5B: low \rightarrow high: 6+9ns = 15ns high \rightarrow low: 20+3ns = 23ns
 \rightarrow fastest transition low \rightarrow high supply (worst case) = 30.8us + 63ns = 30.863us
 \rightarrow slowest transition high \rightarrow low battery (worst case) = 28.22us + 133ns = 28.353us
We have around 2.5 us of margin.

Supply Plugged (OUTA high, OUTB low) \rightarrow Plugging of Battery:
TPS3701: OUTA: high \rightarrow low 9.9us + 0.12us OUTB: low \rightarrow high 9.9us + 2.7us
LTC7000 TGDN1 high \rightarrow low worst case: 70ns + 40ns = 110ns
LTC7000 TGDN2 low \rightarrow high worst case: 35ns + 13ns = 48ns
CSD18540Q5B: low \rightarrow high 6+9ns = 15ns high \rightarrow low 20+3ns = 23ns
 \rightarrow fastest transition low \rightarrow high supply (worst case) = 12.6us + 63ns = 12.663us
 \rightarrow slowest transition high \rightarrow low battery (worst case) = 10.02us + 133ns = 10.153us
We have around 2.5 us of margin.

Battery & Supply Plugged (OUTA high, OUTB low) \rightarrow Unplugging of Supply:
 \rightarrow slowest transition low \rightarrow high battery (worst case) = 12.6us + 160ns = 12.760us
 \rightarrow fastest transition high \rightarrow low supply (worst case) = 10.2us + 48ns = 10.248us
 \rightarrow transition takes around 2.5us

The turn-off phase being faster than the turn-on phase for both scenario ensure that not both source will be activated at the same time while keeping the global down-time of the transition below the uS, ensuring continuous power to the rover.

DESIGN NOTE - Pull-up/Divider Resistors:

OUTA/B are open drain, so this design ensure a logic signal between 3.4V (10V input) and 12.4V (36V input). The INP pin of LTC7000 requires at least 2V but less than 15V to turn on the FETs, making this design a proper fit.

3V3 is not used for the pull up, as it is generated from VOUT, which itself needs first to be turned using OUTA/B, signals requiring 3V3 pull-up.

DESIGN NOTE - LTC7000 connections:

RUN: Connect to Vin to ensure normal operation of the IC
TIMER: Connect to VCC to disable the auto-restart feature.
IMON: Can be left floating if no need of current monitoring. The voltage on this pin with respect to GND represents the voltage across the sense resistor multiplied by 20.
ISET: Can be left floating if default 30mV threshold is ok, or connect a resistors to GND to set higher thresholds. Now @ 50mV
OVLO: Has to be connected to ground if not used.
BST: Has to be connected to the bootstrap capacitor.
TS: Need Schotky diode for complex loads.
FAULT: When timer is connected to VCC, this pin is driven low when the MOSFET is OFF.
Sense Resistor: $R = \Delta V/I_{max} = 50mV/50A = 1m\Omega$

DESIGN NOTE - Ensuring faster turn off time:

The load being large, complex and capacitive, inrush current must be limited, and the turn on time need to be slower than the turn off. The pull-up gate drive to the power MOSFET from TGUP is passed through an RC delay network, RG and CG, which greatly reduces the turn-on ramp rate of the MOSFET. Since the MOSFET source voltage follows the gate voltage, the load is powered smoothly from ground. This dramatically reduces the inrush current from the source supply and reduces the transient ramp rate of the load allowing for slower activation. The turn-off of the MOSFET is not affected by the RC delay network as the pull-down for the MOSFET gate is directly from the TGDN pin.

The values for RG and CG if we aim at at voltage ramp of 0.1V / us
 $RG * CG \approx 0.7V * 12V / (0.1V / us) = 84 \mu F$
If we fix CG to be 470pF, we calculate RG to be 178k Ω .

Power Path Logic

OUTA \rightarrow TP802 OUTA
OUTB \rightarrow TP804 OUTB
INX \rightarrow TP806 INX

Filtered Power Rails

+VSUPPLY \rightarrow TP809 +VSUPPLY
+VBAT \rightarrow TP811 +VBAT
+VBAT_O \rightarrow TP812 +VBAT_O
VDD \rightarrow TP814 VDD
+VSUPPLY_O \rightarrow TP816 +VSUPPLY_O

GND

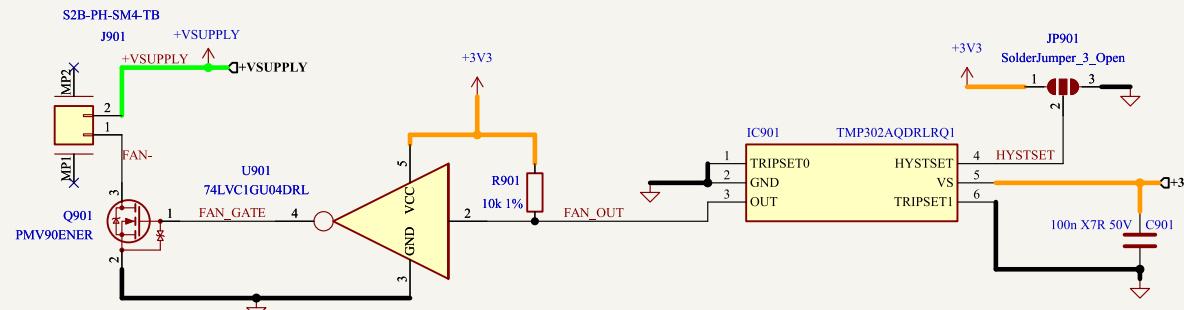
GND \rightarrow TP813 GND
GND \rightarrow TP815 GND

Test Points

Comments: Inspiration from TI Design: TIDA-00394 Dual Power Path Multiplexer Reference Design. External Gate Resistor Design Guide for Gate Drivers	Company: EPFL Xplore	Variant: Released
Board Name: EMUX		Project Name: ERC
Sheet Title: Power - Power Path	File Name: Power - Power Path.kicad_sch	Designer: Théo Heng
Sheet Path: /Project Architecture/Power - Power Path/	Reviewer: Federico B. - Eliot A. - Arion Z.	Date: 2025-07-24
	Size: A3	Sheet: 8 of 13

[9] Sensing - Fan Controller

HYSTSET	THRESHOLD HYSTERESIS
GND	5°C
V _S	10°C



TRIPSET1	TRIPSET0	TMP302A-Q1
GND	GND	50°C
GND	V _S	55°C
V _S	GND	60°C
V _S	V _S	65°C

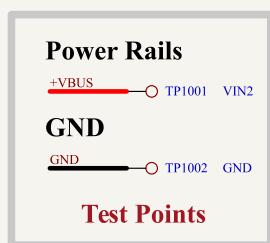
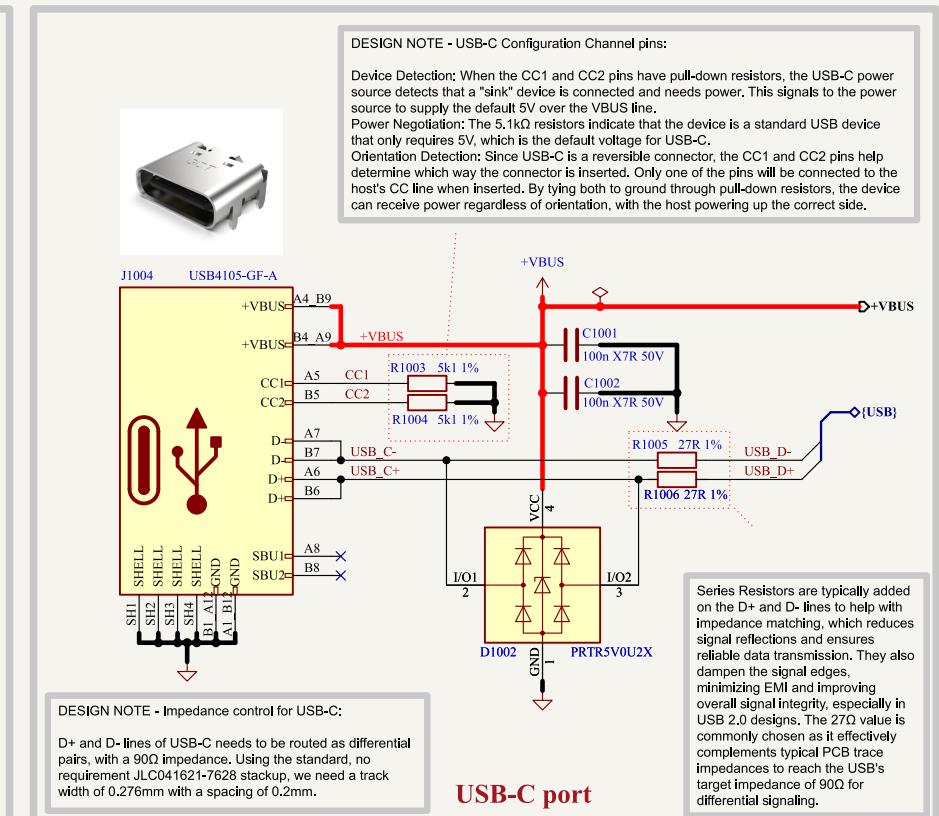
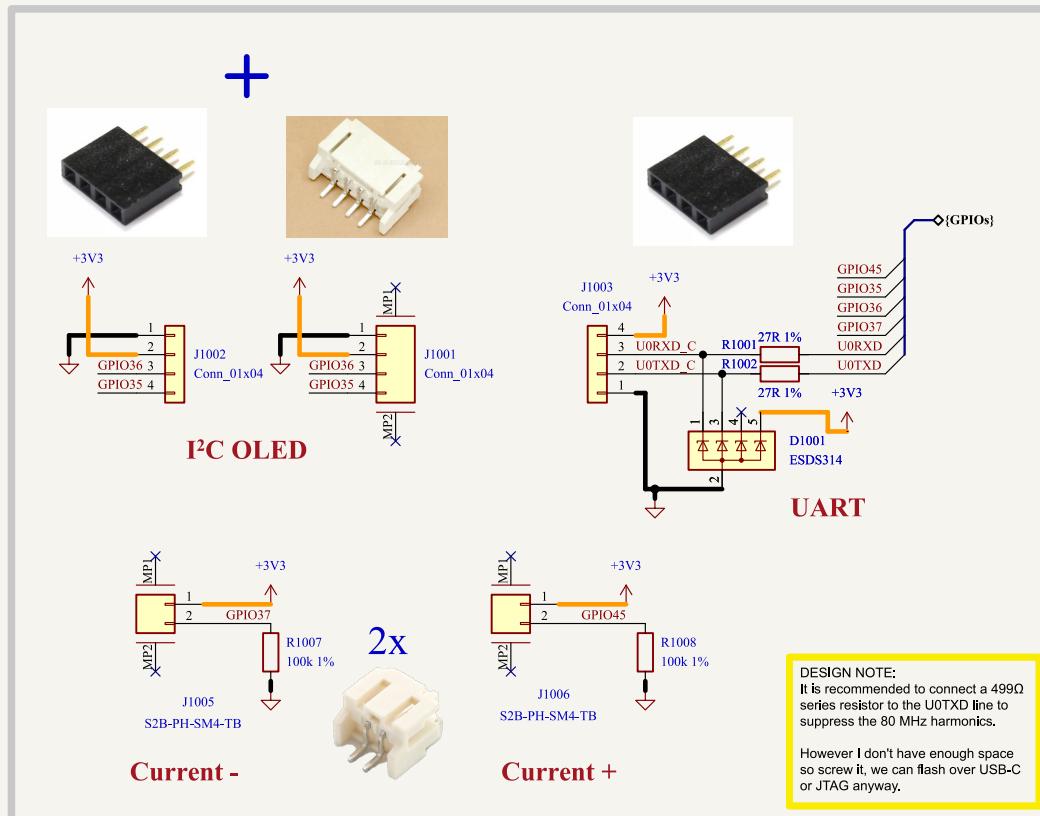
Basic standalone fan controller with over-temperature detection

FAN_OUT — TP1005 FAN_OUT
 FAN_GATE — TP1003 FAN_GATE
 FAN- — TP1004 FAN-

Test Points

Comments: Inspiration from TI Design: Basic fan controller reference design with over-temperature detection.	Company: EPFL Xplore	Variant:  Released
Board Name: 		Project Name: ERC
Sheet Title: Sensing - Fan Controller	File Name: Misc - Fan Controller.kicad_sch	Designer: Théo Heng
Sheet Path: /Project Architecture/Sensing - Fan Controller/	Reviewer: Federico B. - Eliot A. - Arion Z.	Date: 2025-07-24
		Size: A4
		Sheet: 9 of 13

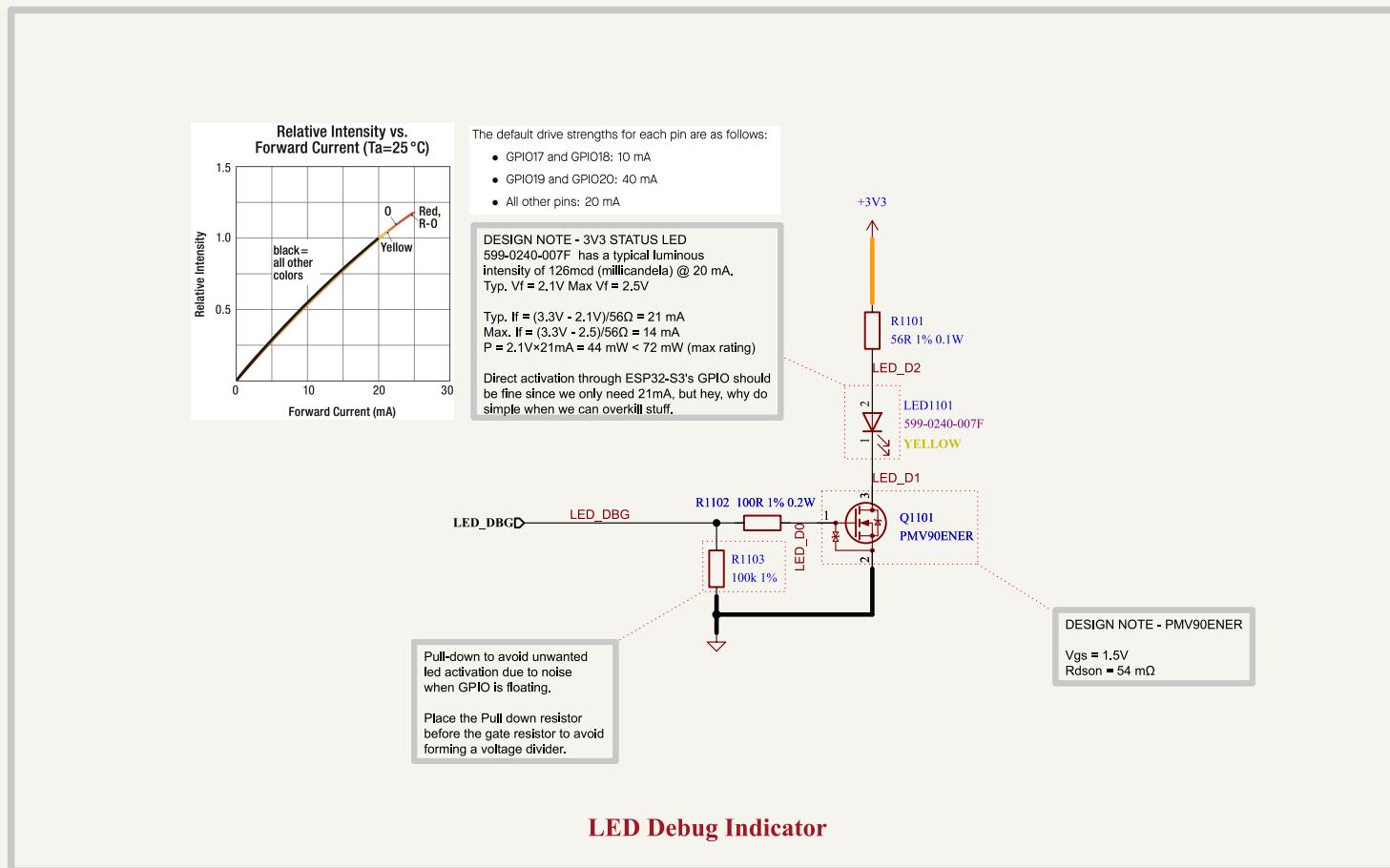
[10] Interface - Connectors



Removed JTAG in V1.1

Comments: Video for debugging ESP32 with JTAG & VSCode ESP-PROG Aliexpress link	Company: EPFL Xplore	Variant: Released
Board Name: EMUX		Project Name: ERC
Sheet Title: Interface - Connectors	File Name: Interface - Connectors.kicad_sch	Designer: Théo Heng
Sheet Path: /Project Architecture/Interface - Connectors/	Reviewer: Federico B. - Eliot A. - Arion Z.	Date: 2025-07-24 Revision: 1.1

[11] User - LED Indicators



Comments: Inspired by Amulet controller Schematics by Vincent Nguyen	Company: EPFL Xplore	Variant: Released
Board Name: EMUX		Project Name: ERC
Sheet Title: User - LED Indicators	File Name: User - LED Indicators.kicad_sch	Designer: Théo Heng
Sheet Path: /Project Architecture/User - LED Indicators/	Reviewer: Federico B. - Eliot A. - Arion Z.	Date: 2025-07-24
	Size: A4	Revision: 1.1
	Sheet: 11	of 13

[12] Misc - Mouting Holes & Fiducials

A

A

B

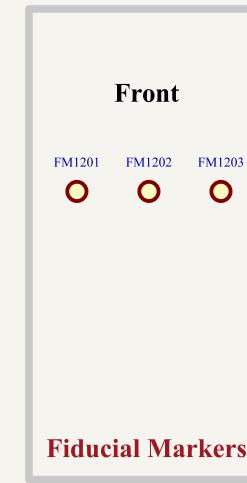
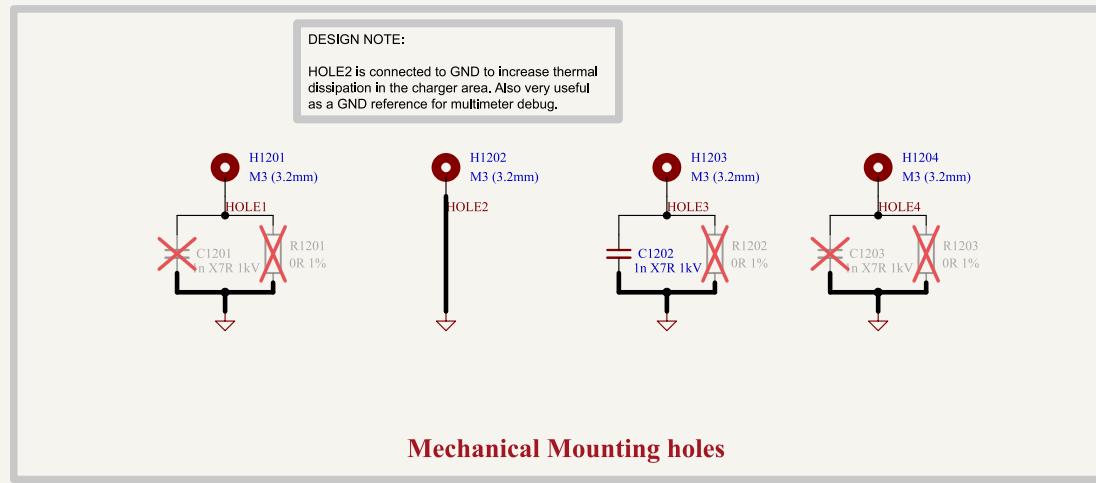
B

C

C

D

D



DESIGN NOTE:
In general, do not ground mounting holes that are connected to chassis if there is a risk that the chassis sends current into the PCB and damages it or if the PCB works with high voltage and there is a risk for the user which is in contact with the chassis.

For a PCB in a metallic enclosure, the enclosure can act like a big antenna. The cavities (space between the ground plane on the PCB and the bottom metallic plane of the enclosure) cause capacitive coupling. This is because we have two metallic planes separated by a dielectric, at a separated potential, causing common mode noise, and result in the noise being amplified by the metal enclosure.
Ideally, in this case, the case should be grounded. But the grounding will cause multiple return paths if multiple mounting holes are connected to GND. In that case, some current will flow in the enclosure and can give a little choc when the user touch it. This can be fine for small battery operated devices.

The best option is therefore to ground only one mounting hole.

Comments: Inspired by Amulet controller Schematics by Vincent Nguyen How to connect mounting holes, PCB Mounting Holes	Company: EPFL Xplore 	Variant: Released	
Board Name: EMUX		Project Name: ERC	
Sheet Title: Misc - Mouting Holes & Fiducials	File Name: Misc - Mounting Holes.kicad_sch	Designer: Théo Heng	
Sheet Path: /Project Architecture/Misc - Mounting Holes & Fiducials/	Reviewer: Federico B. - Eliot A. - Arion Z.	Date: 2025-07-24	Revision: 1.1
Size: A4		Sheet: 12 of 13	

[14] Revision History

A	<p>15.10.2024 - Xplore Schematic Review Variant: V1.0 Draft > V1.0 Preliminary</p> <ul style="list-style-type: none"> - Added the pin 29 on the ESP32 that was missing. - Added test points for the status pins of the other ICs. - Improved brightness of debug LED 30->130 mcd. - Switch to differential pairs for shunt resistors. - Connecting some debug GPIO to Ics (ex: VALID1/2). - Found board name, added Logo. - Added bulk capacitors and refined their value from dev board of LM51772. - Change the source of power generation from VSUPPLY to VOUT to constantly enable the MCU. - Added jumpers and larger footprint resistors for easy test of gate resistors values. - Added fault and current sensing from LTC7000 to ESP32. - Increased spacing between high voltage copper pours and GND to provide more isolation. - Reduced power-path diode size. - Increased via spacing to avoid ground splitting - Re-arranged TVS diodes placement. - Added series inductance on the XTAL_P line. 	<p>31.10.2024 - Xplore IDR Variant: V1.0 Preliminary > V1.0 Checked</p> <ul style="list-style-type: none"> - Added polarity to the XT60 connectors. - Completely re-rooted the charger section with the following improvements: wider gate traces, switched to 2 layer for the power planes, greatly improved the overall rooting especially the diff pairs. - Added thermal reliefs. - Simulated then added ferrite bead EMI filtering at the inputs of the 3v3 buck. - Improved Branding. - Fixed fiducials placement. - Added 4th mounting hole. - Increased board lenght by 5mm (95->100) - _____ - _____ - _____ - _____ - _____ - _____ 	<p>10.02.2025 - Xplore Final Review Variant: V1.0 Checked > V1.0 Released</p> <ul style="list-style-type: none"> - Added solder jumpers for GPIO3, to be able to choose between USB or JTAG lines flashing. - Changed charger's MOSFETs to reduce losses, therefore reducing heat to an acceptable level. Old: CSD18540Q5B New: BSC059N04LS6 - Added UART programming support. - Placed TVS diodes before the 27Ω resistors for the JTAG lines. - Improved documentation for Connectors & LED schematic. - Fixed TS connection of drivers for power path. 	<p>08.06.2025 - After test revision Variant: V1.0 > V1.1</p> <ul style="list-style-type: none"> ● - Fixed charger's LED schematic & layout ● - Added autom. Fan control from temperature ● - Use larger MOSFETs for powerpath ● - Remove the RC delay network for the LTC7000, or connect it to TS and not GND. ● - Add protection to the TPS3701 ● - Inverser capa/resistor pour filtre passe bas dans LTC7000 ● - Utiliser via 0.3 avec smaller annular width to reduce costs (0.3/0.55) or (0.3/0.50). ● - added capa to timer pin of the LTC7000 for power path to avoid false inrush triggers ● - use transistors rather than just resistor for the OUT LEDs ● - changed power tvs diode from SMBJ33A to SMBJ30A -> max input voltage 33 -> 30V ● - integrated connectors for current buttons ● - removed JTAG ● - inverted charge enable button use ● - Removed INA current/voltage sensor
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Comments:	Company: EPFL Xplore	Variant:  Released
Board Name: EMUX		Project Name: ERC
Sheet Title: Revision History	File Name: Revision History.kicad_sch	Designer: Théo Heng
Sheet Path: /Revision History/	Reviewer: Federico B. - Eliot A. - Arion Z.	Date: 2025-07-24
	Size: A4	Sheet: 14 of 13