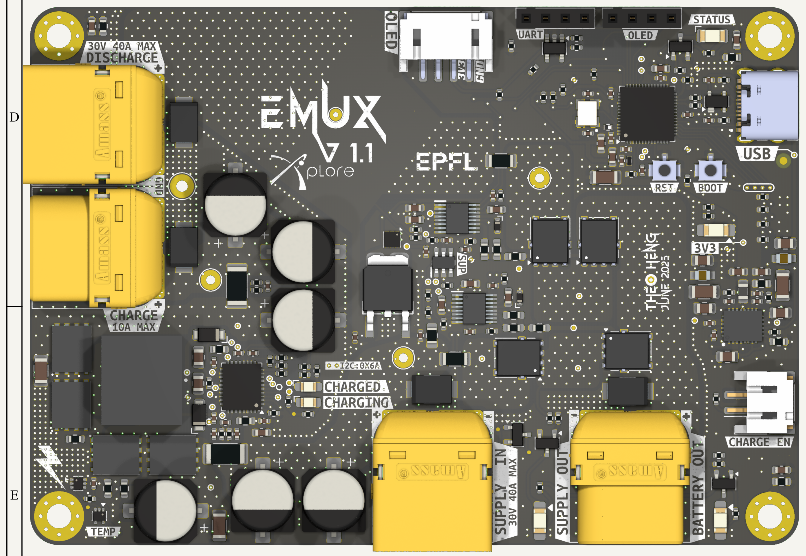
Variant: Released

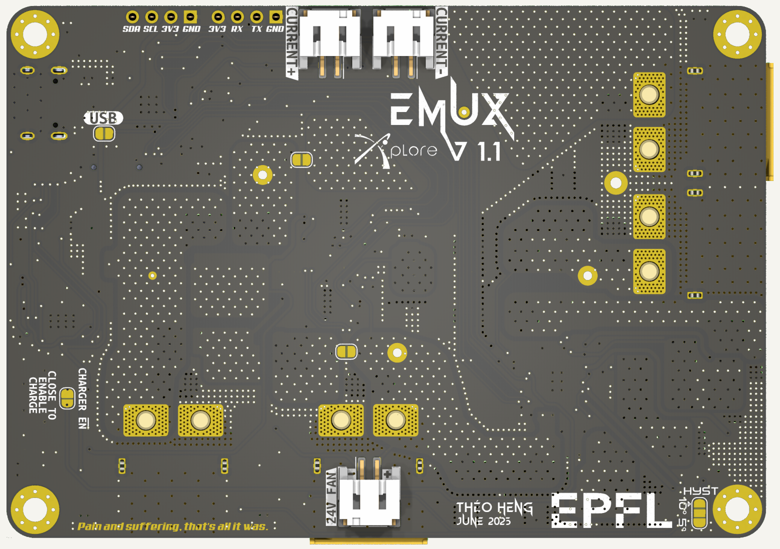
2025-09-04

Rev 1.1

TOP VIEW



BOTTOM VIEW



NOTES

Board designed for EPFL Xplore's rover in the context of the European Rover Challenge.
Schematic based on Vincent Nguyen's Template. Many thanks to him for making this public.

Not fitted components are marked as X

DRAFT - Very early stage of schematic, ignore details.
PRELIMINARY - Close to final schematic.
CHECKED - There shouldn't be any mistakes. Contact the engineer if you find any.
RELEASED - A board with this schematic has been sent to production.

Released 24-07-2025

DESIGN CONSIDERATIONS

DESIGN NOTE: Example text for informational design notes.

DESIGN NOTE: Example text for debug notes.

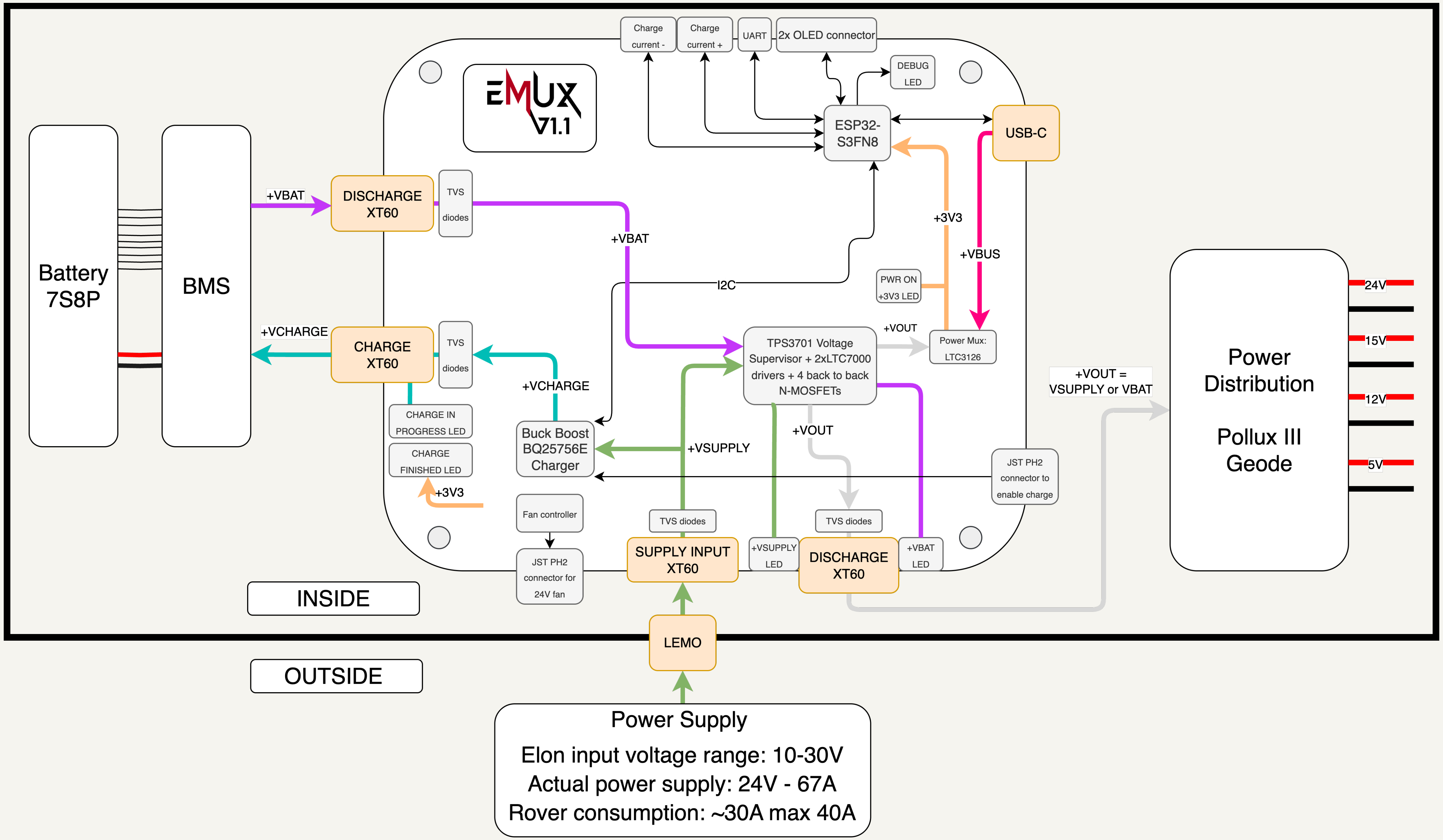
DESIGN NOTE: Example text for cautionary design notes.

DESIGN NOTE: Example text for critical design notes.

LAYOUT NOTE: Example text for critical layout guidelines.

Comments:	Company: EPFL Xplore		Variant: Released	
	Board Name: EMUX		Project Name: ERC	
Sheet Title: Cover Page	File Name: ElonMux.kicad_sch	Designer: Théo Heng	Date: 2025-09-04	Revision: 1.1
Sheet Path: /		Reviewer: Federico B. - Eliot A. - Arion Z.	Size: A3	Sheet: 1 of 13

[2] Block Diagram



The purpose of this board is to be able to charge a battery and power the main load simultaneously from the same external power supply. The user have to be able to plug and unplug the power supply from the rover without shuting down/rebooting the load, requiring fast switching times.

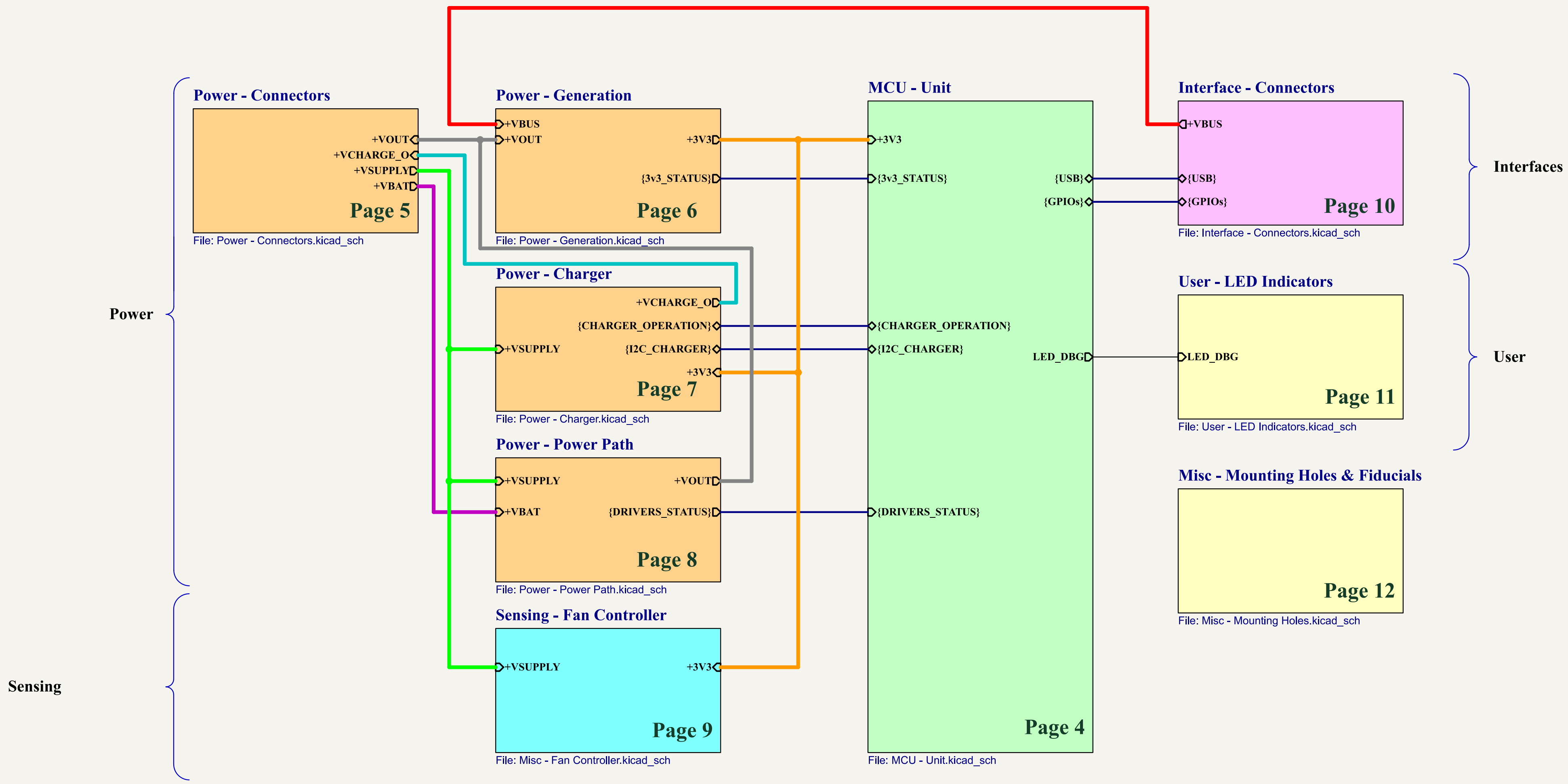
The system will always try to use the external power supply as the primary power source for the rover, but will default to the battery if it is not availaible.

Maximum rating:

Input voltage (battery&supply):	10V - 30V
Continuous supply current:	40A
Continuous discharge current:	40A
Continuous charge current:	10A

Comments: Made in draw.io	Company: EPFL Xplore		Variant: Released	
	Board Name: EMUX		Project Name: ERC	
Sheet Title: Block Diagram	File Name: Block Diagram.kicad_sch	Designer: Théo Heng	Date: 2025-09-04	Revision: 1.1
Sheet Path: /Block Diagram/		Reviewer: Federico B. - Eliot A. - Arion Z.	Size: A3	Sheet: 2 of 13

[3] Project Architecture



Comments:	Company: EPFL Xplore		Variant: Released	
	Board Name: EMUX		Project Name: ERC	
Sheet Title: Project Architecture	File Name: Project Architecture.kicad_sch	Designer: Théo Heng	Date: 2025-09-04	Revision: 1.1
Sheet Path: /Project Architecture/		Reviewer: Federico B. - Eliot A. - Arion Z.	Size: A3	Sheet: 3 of 13

[4] MCU - Unit

Table 3-5. JTAG Signal Source Control

JTAG Signal Source	EFUSE_DIS_PAD_JTAG	EFUSE_DIS_USB_JTAG	EFUSE_STRAP_JTAG_SEL	GPIO3
USB Serial/JTAG Controller	**0**	**0**	**0**	Ignored
	0	0	1	1
	1	0	Ignored	Ignored
JTAG pins [2]	0	0	1	0
	0	1	Ignored	Ignored
JTAG is disabled	1	1	Ignored	Ignored

[1] **Bold** marks the default value and configuration.
[2] JTAG pins refer to MTDI, MTCK, MTMS, and MTDO.

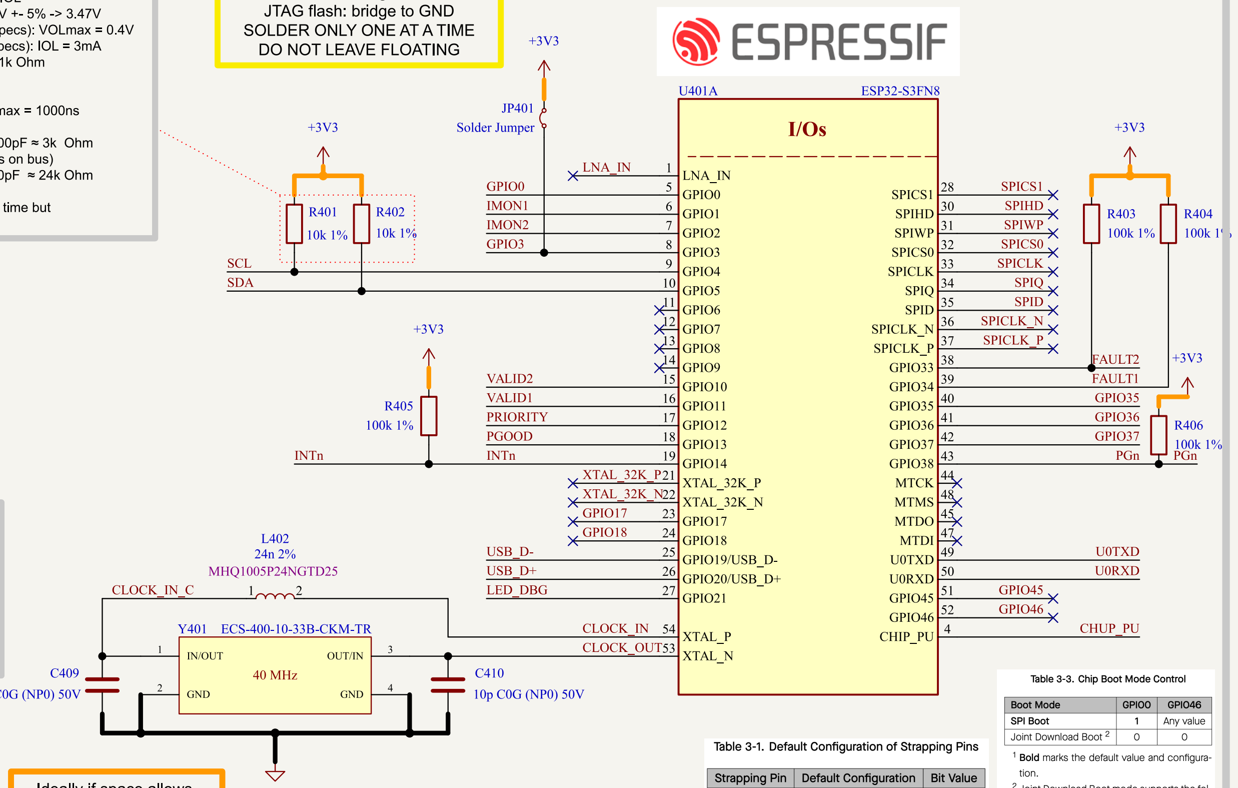
DESIGN NOTE - I2C pull-Up resistors:

Rmin = (VDDmax - VOLmax) / IOL
System I/O voltage: VDD = 3.3V +- 5% -> 3.47V
Low level output volatge (I2C specs): VOLmax = 0.4V
Low level output current (I2C specs): IOL = 3mA
Rmin = (3.47V - 0.4V) / 3mA ≈ 1k Ohm

Rmax ≈ (1.18 x trmax) / Cb
Standard mode (I2C specs): trmax = 1000ns
Cbmax = 400pF (worst case)
-> Rmax ≈ (1.18 x 1000ns) / 400pF ≈ 3k Ohm
Cbmin = 50pF (only 1-2 devices on bus)
-> Rmax ≈ (1.18 x 1000ns) / 50pF ≈ 24k Ohm

Smaller resistors decrease rise time but increase power consumption.

USB flash: bridge to 3V3
JTAG flash: bridge to GND
SOLDER ONLY ONE AT A TIME
DO NOT LEAVE FLOATING



DESIGN NOTE - CLK caps:

Cl = 10pF (load capacitance)
Cp = 5pF (stray capacitance)
C1 = C2 = C

Cl = (C1 x C2)/(C1+C2) + Cp
10pF = C/2 + Cp

C1 = C2 = 10pF

LAYOUT NOTE:
Place the 24nH inductor as close as the IC as possible. It is best not to route any signal trace under the crystal.

Ideally if space allows, add a 0.1uF capacitor on each of the ADC lines used to read values (IMON 1 & 2)

Table 3-1. Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO0	Weak pull-up	1
GPIO3	Floating	–
GPIO45	Weak pull-down	0
GPIO46	Weak pull-down	0

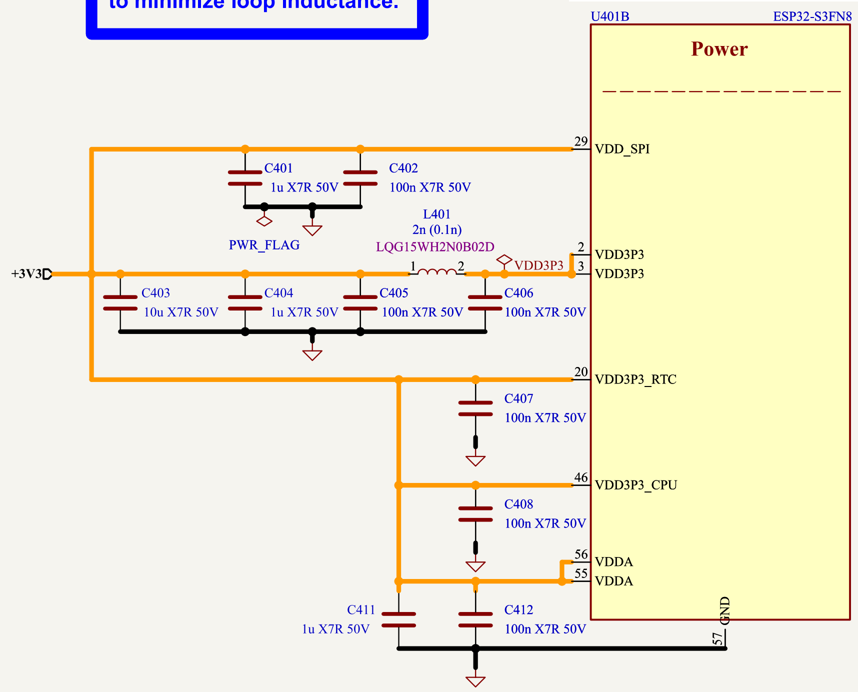
Table 3-3. Chip Boot Mode Control

Boot Mode	GPIO0	GPIO46
SPI Boot	**1**	Any value
Joint Download Boot [2]	0	0

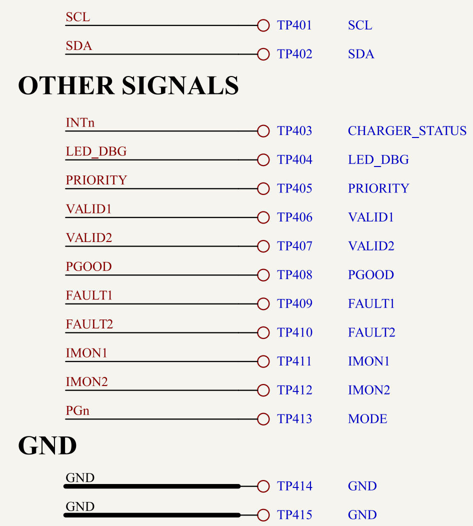
[1] **Bold** marks the default value and configuration.
[2] Joint Download Boot mode supports the following download methods:
- USB Download Boot:
  - USB-Serial-JTAG Download Boot
  - USB-OTG Download Boot
- UART Download Boot

MCU I/O

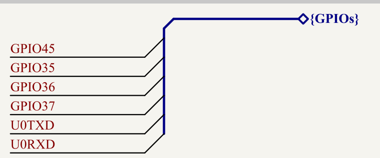
LAYOUT NOTE:
Place each capacitor close to the relevant pin to minimize loop inductance.



MCU POWER



Test Points

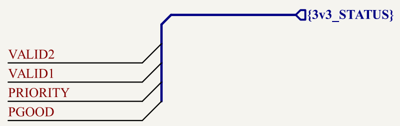


DESIGN NOTE:

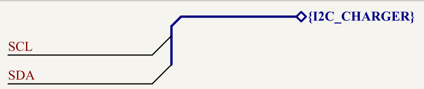
GPIO 35, 36 & 37 are availaible only because we are not using octal SPI for the internal 8MB FLASH.

MCU Additional I/Os

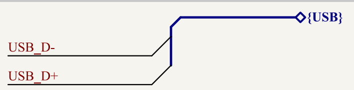
Removed JTAG in V1.1



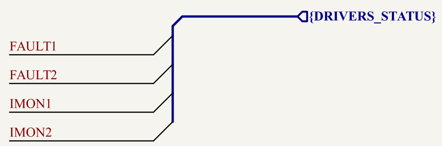
3V3 Buck Status



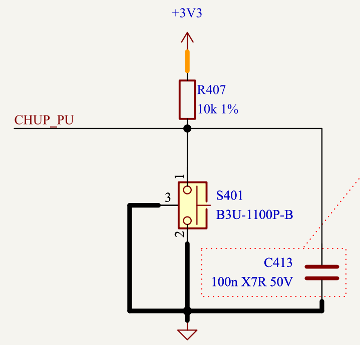
I2C Bus to Battery Charger



USB-C Interface



Drivers Status & Sensing



MCU Chip Reset

DESIGN NOTE - reset button capacitor:

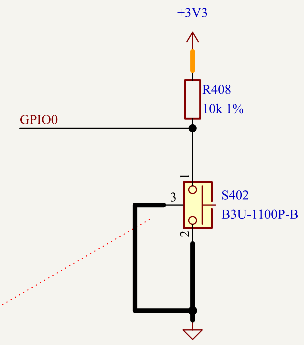
Debouncing: It smooths out any quick, unintended changes in voltage due to mechanical bounce in the button switch. This ensures that when the reset button is pressed, it reliably resets without multiple unintended toggles.

Power Stabilization: It can also help stabilize the power when the chip resets, which may reduce potential issues during the reset process.

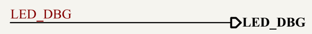
DESIGN NOTE:

USB flashing is fully automated because of its ability to reset the ESP32 directly, while JTAG debugging operates through distinct dedicated pins that do not handle the board's power state automatically. Therefore, the BOOT button is necessary to enable flash mode when using JTAG for programming or debugging.

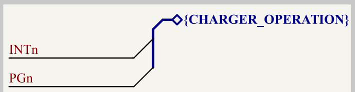
The ESP32-S3 will enter the serial bootloader when GPIO0 is held low on reset. Otherwise it will run the program in flash.



MCU JTAG Boot



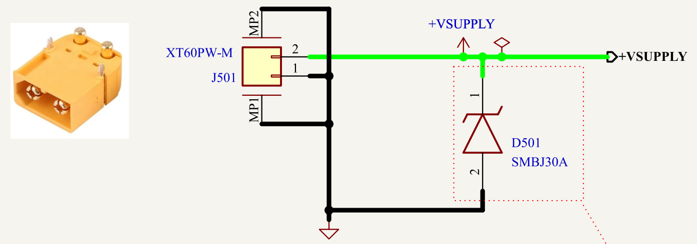
User LED



Charger Operation

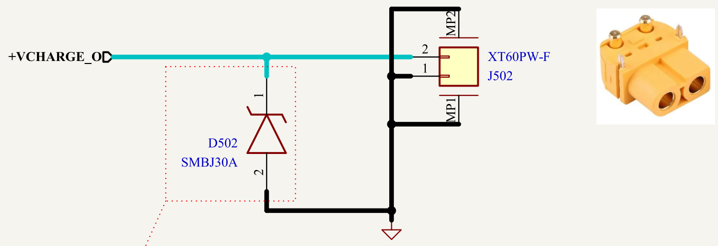
Comments: Espressif Scematic Checklist; Espressif Datasheet p.25 (CHIP_PU); Espressif Datasheet p.30 (GPIO0 boot); Phil's Lab - SPI Hardware & PCB Design; Flashing ESP32-s3 with USB; ESP32-s3 BOOT selection	Company: EPFL Xplore		Variant: Released
	Board Name: EMUX		Project Name: ERC
Sheet Title: MCU - Unit	File Name: MCU - Unit.kicad_sch	Designer: Théo Heng	Date: 2025-09-04 / Revision: 1.1
Sheet Path: /Project Architecture/MCU - Unit/		Reviewer: Federico B. - Eliot A. - Arion Z.	Size: A3 / Sheet: 4 of 13

[5] Power - Connectors



DESIGN NOTE:
Do not exceed the absolute maximum input voltage rating of 30V.

Power Input Connector from Power Supply, TVS Diode



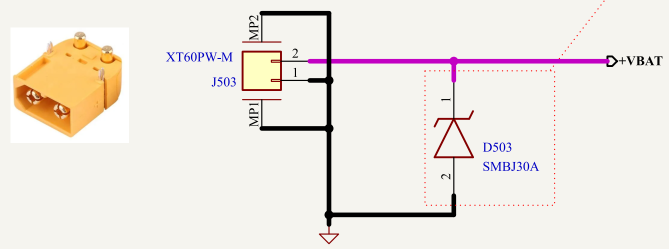
Power Output Connector to Battery, TVS Diode

DESIGN NOTE:

No reverse polarity protection implemented. TVS diodes does not protect the PCB against reverse polarity.

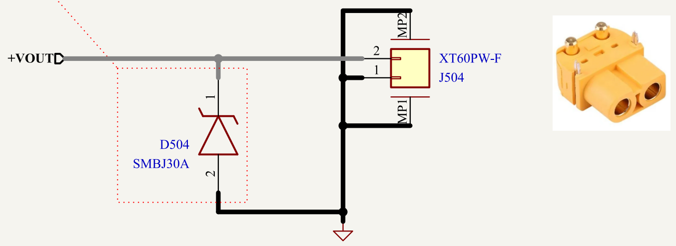
Always adhere to established industry conventions for connector polarity and gender to ensure compatibility and prevent reverse polarity connections. The female connector should always carry the power source with recessed contacts to minimize the risk of accidental short circuits. Polarity protection could be nice improvements for V1.1.

LAYOUT NOTE:
Place TVS diode near input power connectors, with an orientation minimizing the return path.



DESIGN NOTE:
Do not exceed the absolute maximum input voltage rating of 30V.

Power Input Connector from Battery, TVS Diode



Power Output Connector to rover, TVS Diode

DESIGN NOTE:

TVS (Transient Voltage Suppresion) are used to protect circuits from voltage spikes by clamping high voltages to a safe level.

Bidirectional diodes brings no additional benefits compared to unidirectional diodes and are in fact even a bit worse, as they will clamp later negative transients.

In sintuations like this, when the battery and power supply are always positive values, unidirectional diodes are better suitted.

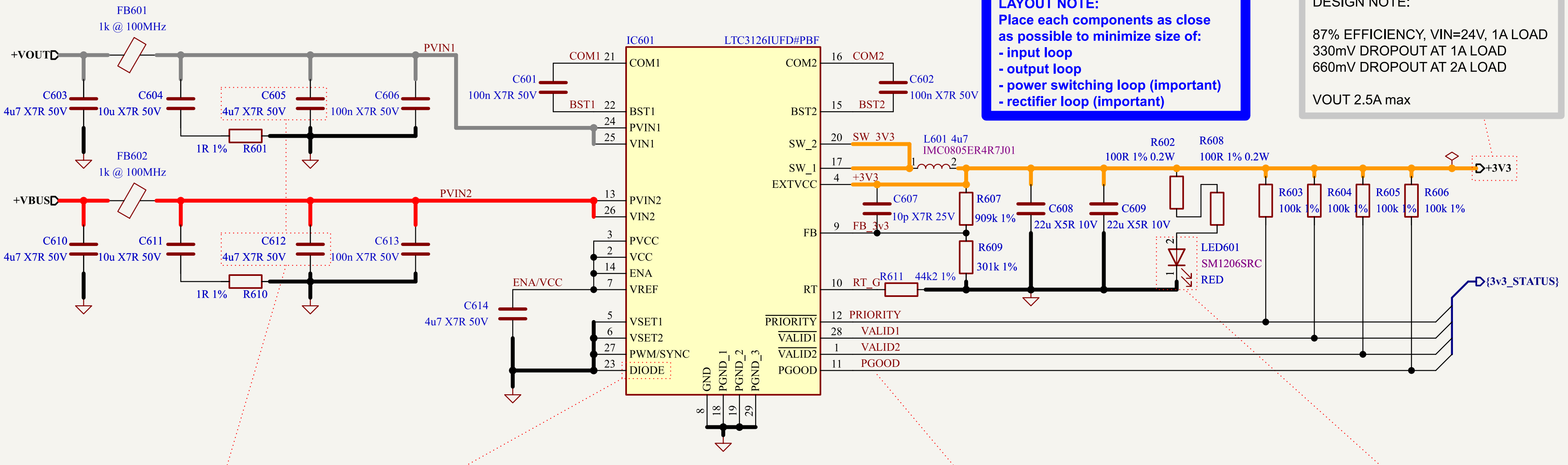
Bidirectional diodes are meant to be use to proetct lines that usually goes to negative values, like differential lines.

SMBJ33CA:

Reverse Stand off voltage (= working voltage): 30.0V (maximum continuous voltage that can be applied to the diode without it conducting current)
Min Breakdown Voltage: 33.30V
Max Breakdown Voltage: 36.8V
The breakdown voltage range (from 33.3V to 36.8V) ensures the diode begins to conduct in response to harmful spikes, not minor voltage changes.
Max Clamping Voltage: 48.40V (maximun voltage the protected circuit will experience for any spike of 53.3V or more)
Peak Pulse Power Dissipation: 600W
Peak Forward Surge Currents: 100A

Comments: Inspired by Amulet controller Schematics by Vincent Nguyen. Uni or bi directional TVS diodes?	Company: EPFL Xplore		Variant: Released	
	Board Name: EMUX		Project Name: ERC	
Sheet Title: Power - Connectors	File Name: Power - Connectors.kicad_sch	Designer: Théo Heng	Date: 2025-09-04	Revision: 1.1
Sheet Path: /Project Architecture/Power - Connectors/		Reviewer: Federico B. - Eliot A. - Arion Z.	Size: A3	Sheet: 5 of 13

[6] Power - Generation



LAYOUT NOTE:
Place each components as close as possible to minimize size of:
- **input loop**
- **output loop**
- **power switching loop (important)**
- **rectifier loop (important)**

DESIGN NOTE:

87% EFFICIENCY, VIN=24V, 1A LOAD
330mV DROPOUT AT 1A LOAD
660mV DROPOUT AT 2A LOAD

VOUT 2.5A max

DESIGN NOTE - Ferrite Beads:

Ferite Beads needs to be used with care, as they can cause more harm than good by producing unwanted resonance in a circuit when used with high Q bulk capacitors. Adding a large capacitor (relative to the following bulk capacitor) with a resistor in series after the bead mitigate this LC resonnance effect.

4.7uF capacitors are used for the input bulk capacitors of the LTC3126 as they provide a trade of between low resonance effect and capability to smooth the incoming power rail.

DESIGN NOTE:

DIODE to GND activate priority mode. VIN1 (+VOUT) will be used first.

DESIGN NOTE:

Higher switching frequency like 2Mhz induce more switching losses, but smaller inductance meaning smaller PCB footprint.

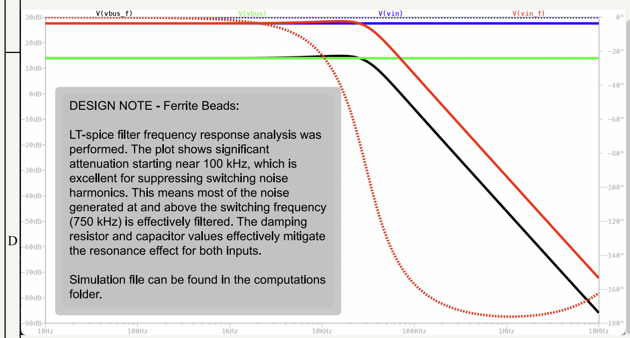
DESIGN NOTE - LTC3126 status pins:

PRIORITY, VALID1, VALID2 & PGOOD are open drain -> pull-up resistors.
PRIORITY is driven low when the buck converter is currently using the priority input, VIN1.
VALID1 is driven low when VIN1 is above the internal fixed UVLO threshold (2.54V)
VALID2 is driven low when VIN2 is above the internal fixed UVLO threshold (2.54V)
PGOOD is driven low if the output voltage is more than 8.7% below or more than 9.8% above the regulation voltage or whenever the buck converter is disabled.

DESIGN NOTE - 3V3 STATUS LED
SM1206SRC has a typical luminous intensity of 28mcd (millicandela) @ 20 mA.
Typ. Vf = 1.85V Max Vf = 2.3V

Typ. If = (3.3V - 1.85V)/200hm ≈ 7.3 mA
Max. If = (3.3V - 2.3V)/200hm ≈ 5 mA

3.3V, 750kHz synchronous step-down regulator with no-loss input PowerPath

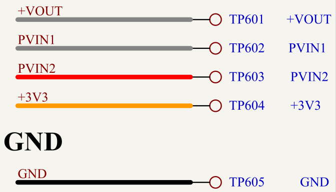


DESIGN NOTE - Ferrite Beads:

LT-spice filter frequency response analysis was performed. The plot shows significant attenuation starting near 100 kHz, which is excellent for suppressing switching noise harmonics. This means most of the noise generated at and above the switching frequency (750 kHz) is effectively filtered. The damping resistor and capacitor values effectively mitigate the resonance effect for both inputs.

Simulation file can be found in the computations folder.

Filtered Power Rails



Test Points

Comments:
LTC3126 Datasheet p.24 (schematic)
LTC3126 Datasheet p.22 (layout)
Ferrite Beads Demystified

Company: EPFL Xplore

Board Name: EMUX

Variant: Released

Project Name: ERC

Sheet Title:	File Name:	Designer:	Date:	Revision:
Power - Generation	Power - Generation.kicad_sch	Théo Heng	2025-09-04	1.1

Sheet Path:	Reviewer:	Size:	Sheet:
/Project Architecture/Power - Generation/	Federico B. - Eliot A. - Arion Z.	A4	6 of 13

[7] Power - Charger

Under/over voltage input protection:
If unused, tie ACUV to VAC and ACOV to PGND in order to apply the internal VAC operating window (VVAC_OP: 4.2-36V)

DESIGN NOTE - 3V3 STATUS LEDs

ORANGE LED:
SM0805UOC has a typical luminous intensity of 80 mcd (millicandela) @ 20 mA.
Typ. Vf = 2.1V Max Vf = 2.6V

Typ. If = (3.3V - 2.1V)/56Ω = 21 mA
Max. If = (3.3V - 2.6)/56Ω = 13 mA
P = 2.1V×21mA = 44 mW < 78 mW (max rating)

GREEN LED:
AP2012MGC has a typical luminous intensity of 60mcd (millicandela) @ 20 mA.
Typ. Vf = 2.1V Max Vf = 2.5V

Typ. If = (3.3V - 2.1V)/56Ω = 21 mA
Max. If = (3.3V - 2.5)/56Ω = 14 mA
P = 2.1V×21mA = 44 mW < 75 mW (max rating)

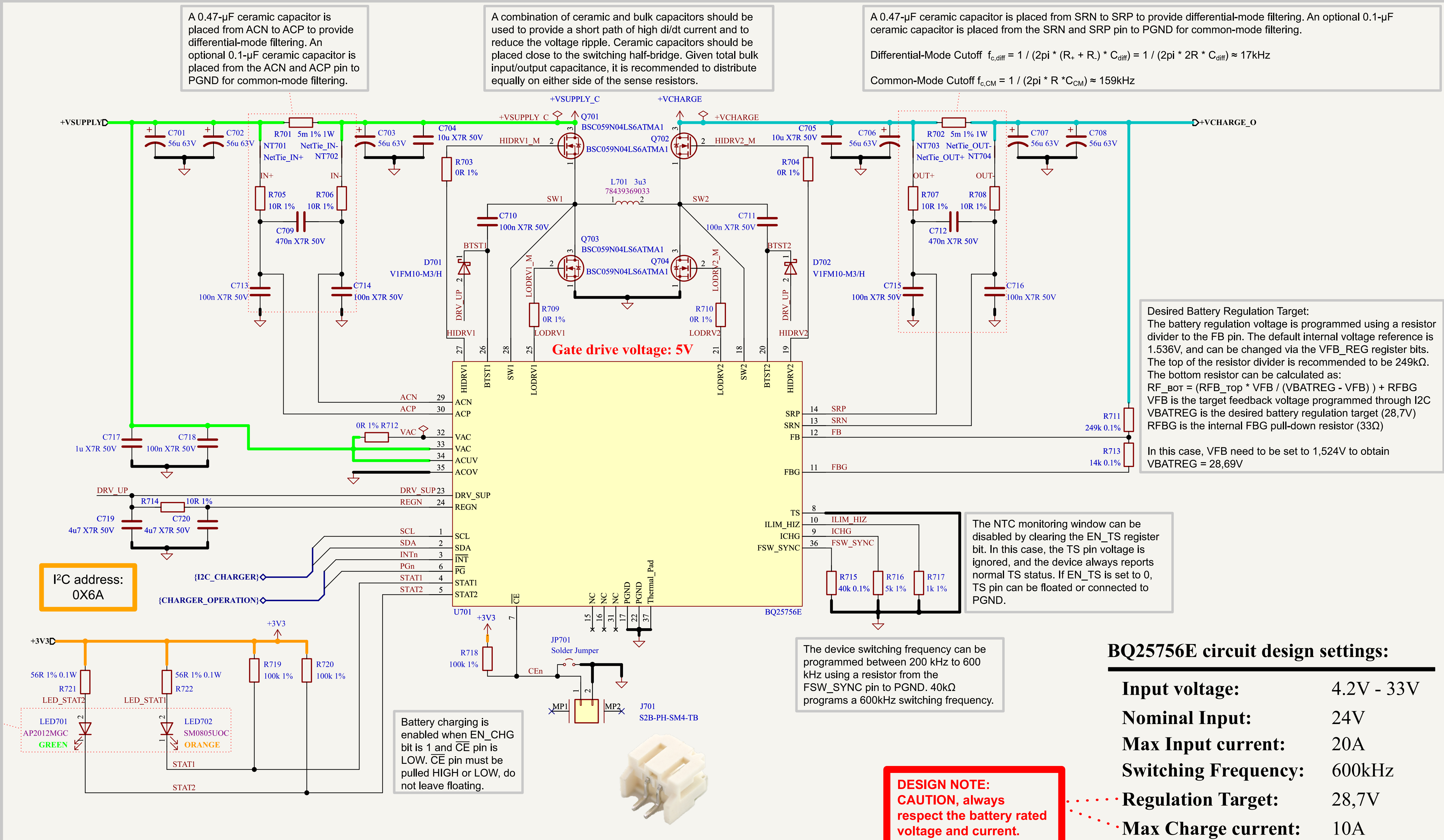
A 0.47-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. An optional 0.1-µF ceramic capacitor is placed from the ACN and ACP pin to PGND for common-mode filtering.

A combination of ceramic and bulk capacitors should be used to provide a short path of high di/dt current and to reduce the voltage ripple. Ceramic capacitors should be placed close to the switching half-bridge. Given total bulk input/output capacitance, it is recommended to distribute equally on either side of the sense resistors.

A 0.47-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. An optional 0.1-µF ceramic capacitor is placed from the SRN and SRP pin to PGND for common-mode filtering.

Differential-Mode Cutoff $f_{c,diff} = 1 / (2\pi * (R_+ + R_-) * C_{diff}) = 1 / (2\pi * 2R * C_{diff}) \approx 17kHz$

Common-Mode Cutoff $f_{c,CM} = 1 / (2\pi * R * C_{CM}) \approx 159kHz$



I²C address: 0X6A

Battery charging is enabled when EN_CHG bit is 1 and $\overline{CE}$ pin is LOW. $\overline{CE}$ pin must be pulled HIGH or LOW, do not leave floating.

Desired Battery Regulation Target:
The battery regulation voltage is programmed using a resistor divider to the FB pin. The default internal voltage reference is 1.536V, and can be changed via the VFB_REG register bits. The top of the resistor divider is recommended to be 249kΩ.
The bottom resistor can be calculated as:
$RF_{BOT} = (RFB_{TOP} * VFB / (VBATREG - VFB)) + RFBG$
VFB is the target feedback voltage programmed through I2C
VBATREG is the desired battery regulation target (28,7V)
RFBG is the internal FBG pull-down resistor (33Ω)

In this case, VFB need to be set to 1,524V to obtain VBATREG = 28,69V

The NTC monitoring window can be disabled by clearing the EN_TS register bit. In this case, the TS pin voltage is ignored, and the device always reports normal TS status. If EN_TS is set to 0, TS pin can be floated or connected to PGND.

The device switching frequency can be programmed between 200 kHz to 600 kHz using a resistor from the FSW_SYNC pin to PGND. 40kΩ programs a 600kHz switching frequency.

BQ25756E circuit design settings:

Input voltage:	4.2V - 33V
Nominal Input:	24V
Max Input current:	20A
Switching Frequency:	600kHz
Regulation Target:	28,7V
Max Charge current:	10A

DESIGN NOTE: CAUTION, always respect the battery rated voltage and current.

BQ25756E: I2C Controlled, 1- to 7-Cell 600kHz Buck-Boost Battery Charge Controller

DESIGN NOTE - Charger Losses:

Switching losses:
Pswitch = 0.5 * Vds * I * (trise + tfall) * fswitch
Pswitch = 0.5 * 28.8V * 7A * (1.2ns + 2 ns) * 600kHz
Pswitch = 0.19 W

Conduction losses:
Pcond = I^2 * Rds
Pcond = 7^2 A * 5.9 mOmh = 0.29 W

Gate drive losses:
Pgate = Qg * Vgs * fswitch
Pgate = 9.4nC * 28.8V * 600 kHz
Pgate = 0.16 W

Total pwr at 7A = 0.19W + 0.29W + 0.16W = 0.65W
Total pwr at 10A = 0.27W + 0.6W + 0.16W = 1.03W

DESIGN NOTE:

CAUTION: Charging the battery with more than 7A requires proper thermal management, such as adequate airflow or heatsinks, to prevent overheating of the MOSFETs.

DESIGN NOTE - Thermal MOS dissipation

Thermal resistance on PCB: 50°C/W

-> 0.65W * 50°C = 32,5 °C increase
MOSFET @ ~55 °C

-> 1.03W * 50°C = 51,5 °C increase
MOSFET @ ~75 °C

BSC059N04LS6ATMA1 40V N-Channel NexFET™ Power MOSFETs:

VDS(Drain-Source Breakdown Voltage) = 40V
Maximum voltage the MOSFET can handle between the drain and source when it's off.

RDS(on) (Drain-Source On-Resistance) = 6.8 mΩ @ 4.5V VGS

ID - Continuous Drain Current = 59A
Maximum continuous current the MOSFET can handle under specified conditions without overheating.

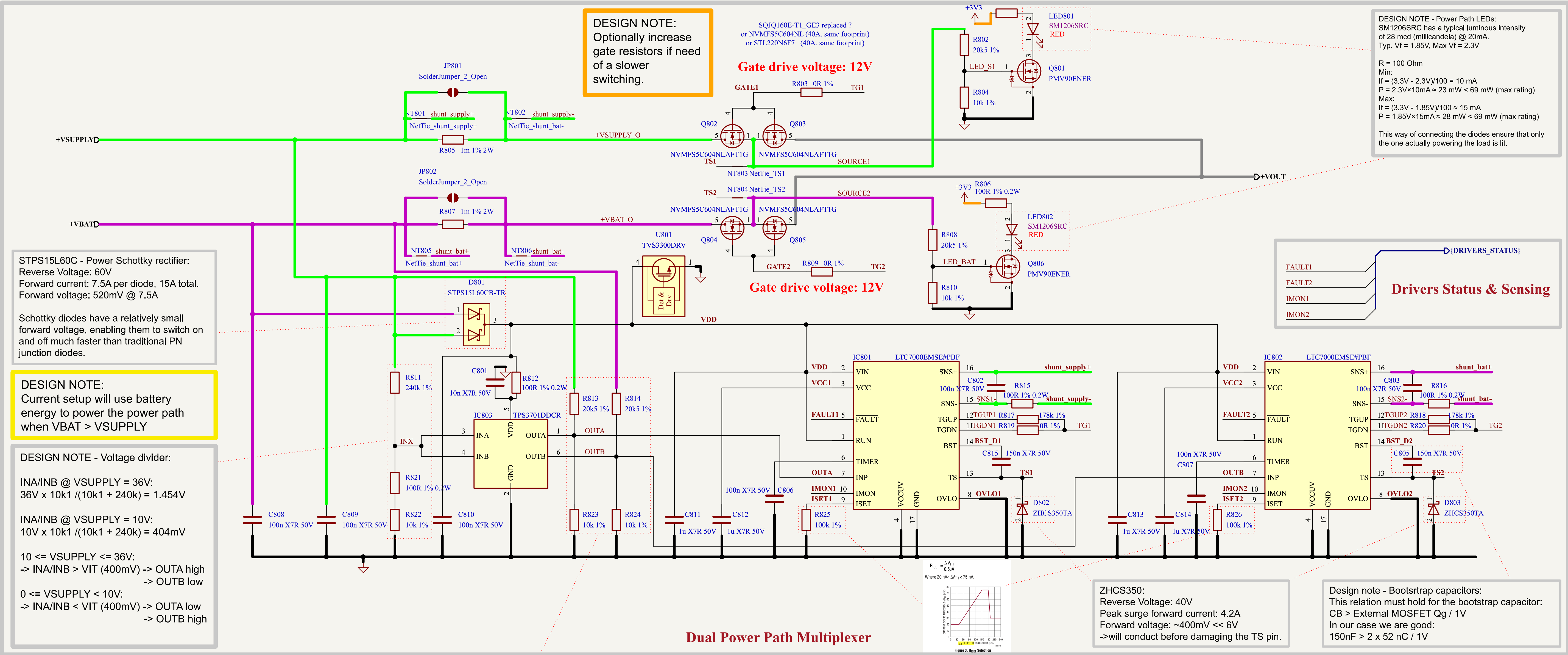
VGS(th) - Gate-Source Threshold Voltage = 1.3V - 2.3V

VGS - Gate-Source Voltage = ±20V
Maximum safe voltage between the gate and source terminals without damaging the gate.

CHARGING STATE	STAT1 ORANGE LED	STAT2 GREEN LED
Charge in progress (including recharge)	ON	OFF
Charge done	OFF	ON
Charging fault detected (TS out of range, safety timer fault, etc.)	ON	ON
Charge disabled (EN_CHG = 0, or $\overline{CE}$ pin high)	OFF	OFF

Comments: Detailled computations are availaible in the computations folder, using TI's provided tool.	Company: EPFL Xplore		Variant: Released	
	Board Name: EMUX		Project Name: ERC	
Sheet Title: Power - Charger	File Name: Power - Charger.kicad_sch	Designer: Théo Heng	Date: 2025-09-04	Revision: 1.1
Sheet Path: /Project Architecture/Power - Charger/		Reviewer: Federico B. - Eliot A. - Arion Z.	Size: A3	Sheet: 7 of 13

[8] Power - Power Path



DESIGN NOTE:
Optionally increase gate resistors if need of a slower switching.

DESIGN NOTE - Power Path LEDs:
SM1206SRC has a typical luminous intensity of 28 mcd (millicandela) @ 20mA.
Typ. Vf = 1.85V, Max Vf = 2.3V

R = 100 Ohm
Min:
If = (3.3V - 2.3V)/100 = 10 mA
P = 2.3V×10mA ≈ 23 mW < 69 mW (max rating)
Max:
If = (3.3V - 1.85V)/100 ≈ 15 mA
P = 1.85V×15mA ≈ 28 mW < 69 mW (max rating)

This way of connecting the diodes ensure that only the one actually powering the load is lit.

STPS15L60C - Power Schottky rectifier:
Reverse Voltage: 60V
Forward current: 7.5A per diode, 15A total.
Forward voltage: 520mV @ 7.5A

Schottky diodes have a relatively small forward voltage, enabling them to switch on and off much faster than traditional PN junction diodes.

DESIGN NOTE:
Current setup will use battery energy to power the power path when VBAT > VSUPPLY

DESIGN NOTE - Voltage divider:

INA/INB @ VSUPPLY = 36V:
36V x 10k1 /(10k1 + 240k) = 1.454V

INA/INB @ VSUPPLY = 10V:
10V x 10k1 /(10k1 + 240k) = 404mV

10 <= VSUPPLY <= 36V:
-> INA/INB > VIT (400mV) -> OUTA high
-> OUTB low
0 <= VSUPPLY < 10V:
-> INA/INB < VIT (400mV) -> OUTA low
-> OUTB high

ZHCS350:
Reverse Voltage: 40V
Peak surge forward current: 4.2A
Forward voltage: ~400mV << 6V
->will conduct before damaging the TS pin.

Design note - Bootstrap capacitors:
This relation must hold for the bootstrap capacitor:
CB > External MOSFET Qg / 1V
In our case we are good:
150nF > 2 x 52 nC / 1V

DESIGN NOTE - Delay when switching between loads:

Battery Plugged (OUTA low, OUTB high) -> Plugging of Supply:
TPS3701: OUTA: low -> high 28.1us + 2.7us OUTB: high -> low 28.1us + 0.12us
LTC7000 TGDN1 low -> high worst case: 35ns + 13ns = 48ns
LTC7000 TGDN2 high -> low worst case: 70ns + 40ns = 110ns
CSD18540Q5B: low -> high: 6+9ns = 15ns high -> low: 20+3ns = 23ns
-> fastest transition low -> high supply (worst case) = 30.8us + 63ns = 30.863us
-> slowest transition high -> low battery (worst case) = 28.22us + 133ns = 28.353us
We have arround 2.5 us of margin.

Supply Plugged (OUTA high, OUTB low) -> Plugging of Battery:
TPS3701: OUTA: high -> low 9.9us + 0.12us OUTB: low -> high 9.9us + 2.7us
LTC7000 TGDN1 high -> low worst case: 70ns + 40ns = 110ns
LTC7000 TGDN2 low -> high worst case: 35ns + 13ns = 48ns
CSD18540Q5B: low -> high 6+9ns = 15ns high -> low 20+3ns = 23ns
-> fastest transition low -> high supply (worst case) = 12.6us + 63ns = 12.663us
-> slowest transition high -> low battery (worst case) = 10.02us + 133ns = 10.153us
We have arround 2.5 us of margin.

Battery & Supply Plugged (OUTA high, OUTB low) -> Unplugging of Supply:
-> slowest transition low -> high battery (worst case) = 12.6us + 160ns = 12.760us
-> fastest transition high -> low supply (worst case) = 10.2us + 48ns = 10.248us
-> transition takes around 2.5us

The turn-off phase being faster than the turn-on phase for both scnenario ensure that not both source will be activated at the same time while keeping the global down-time of the transition below the uS, ensuring continuous power to the rover.

DESIGN NOTE - Pull-up/Divider Resistors:

OUTA/B are open drain, so this design ensure a logic signal between 3.4V (10V input) and 12.4V (36V input). The INP pin of LTC7000 requires at least 2V but less than 15V to turn on the FETs, making this design a proper fit.

3V3 is not used for the pull up, as it is generated from VOUT, which itself needs first to be turned using OUTA/B, signals requiring 3V3 pull-up.

DESIGN NOTE - LTC7000 connections:

RUN: Connect to Vin to ensure normal operation of the IC
TIMER: Connect to VCC to disable the auto-restart feature.
IMON: Can be left floating if no need of current monitoring. The voltage on this pin with respect to GND represents the voltage across the sense resistor multiplied by 20.
ISET: Can be left floating if default 30mV threshold is ok, or connect a resitors to GND to set higher thresholds. Now @ 50mV
OVLO: Has to be connected to ground if not used.
BSST: Has to be connected to the bootstrap capacitor.
TS: Need Schotky diode for complex loads.
FAULT: When timer is connected to VCC, this pin is driven low when the MOSFET is OFF.
Sense Resistor: R = DeltaV/Imax = 50mV/50A = 1mOhm

DESIGN NOTE - Ensuring faster turn off time:

The load being large, complex and capacitive, inrush current must be limited, and the turn on time need to be slower than the turn off. The pull-up gate drive to the power MOSFET from TGUP is passed through an RC delay network, RG and CG, which greatly reduces the turn-on ramp rate of the MOSFET. Since the MOSFET source voltage follows the gate voltage, the load is powered smoothly from ground. This dramatically reduces the inrush current from the source supply and reduces the transient ramp rate of the load allowing for slower activation. The turn-off of the MOSFET is not affected by the RC delay network as the pull-down for the MOSFET gate is directly from the TGDN pin.

The values for RG and CG if we aim at at voltage ramp of 0.1V / us
RG * CG ≈ 0.7V * 12V / (0.1V / us) = 84 us
If we fix CG to be 470pF, we calculate RG to be 178kΩ.

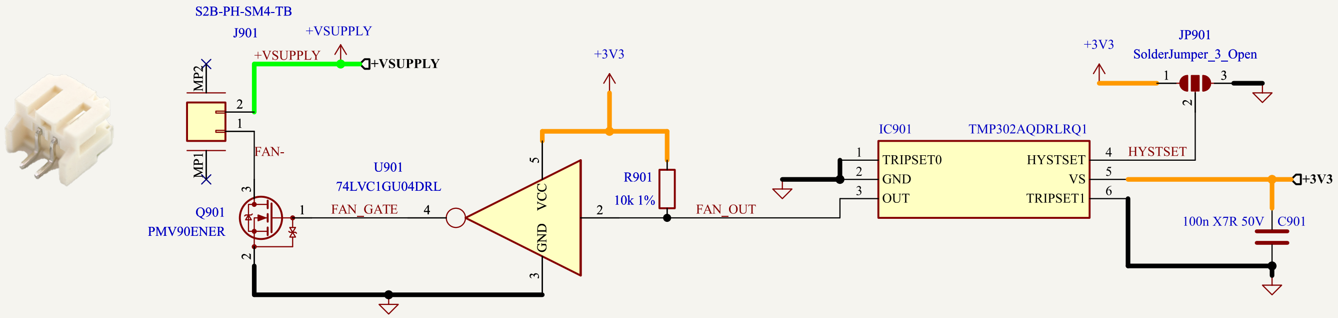
Test Points

Power Path Logic	OUTA → TP802	OUTA
	OUTB → TP804	OUTB
	INX → TP806	INX
Filtered Power Rails	+VSUPPLY → TP809	+VSUPPLY
	+VBAT → TP811	+VBAT
	+VBAT_O → TP812	+VBAT_O
	VDD → TP814	VDD
	+VSUPPLY_O → TP816	+VSUPPLY_O
Drivers	SOURCE1 → TP801	SOURCE1
	SOURCE2 → TP803	SOURCE2
	GATE1 → TP805	GATE1
	GATE2 → TP807	GATE2
	VCC1 → TP808	VCC1
	VCC2 → TP810	VCC2
GND	GND → TP813	GND
	GND → TP815	GND

Comments: Inspiration from TI Design: TIDA-00394 Dual Power Path Multiplexer Reference Design. External Gate Resistor Design Guide for Gate Drivers	Company: EPFL Xplore		Variant: Released
	Board Name: EMUX		Project Name: ERC
Sheet Title: Power - Power Path	File Name: Power - Power Path.kicad_sch	Designer: Théo Heng	Date: 2025-09-04 — Revision: 1.1
Sheet Path: /Project Architecture/Power - Power Path/		Reviewer: Federico B. - Eliot A. - Arion Z.	Size: A3 — Sheet: 8 of 13

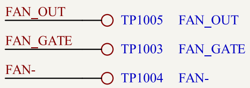
[9] Sensing - Fan Controller

HYSTSET	THRESHOLD HYSTERESIS
GND	5°C
V_S	10°C



TRIPSET1	TRIPSET0	TMP302A-Q1
GND	GND	50°C
GND	V_S	55°C
V_S	GND	60°C
V_S	V_S	65°C

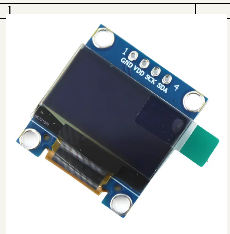
Basic standalone fan controller with over-temperature detection

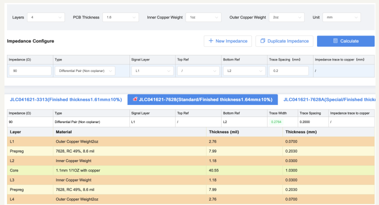


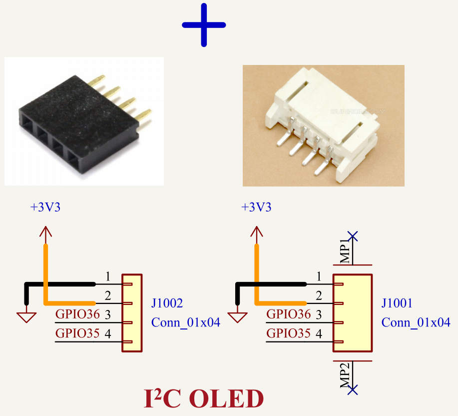
Test Points

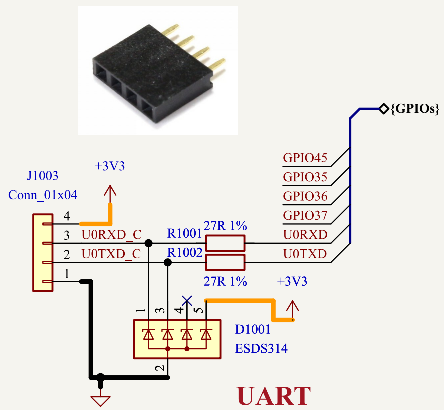
Comments: Inspiration from TI Design: Basic fan controller reference design with over-temperature detection.	Company: EPFL Xplore		Variant: Released	
	Board Name: EMUX		Project Name: ERC	
Sheet Title: Sensing - Fan Controller	File Name: Misc - Fan Controller.kicad_sch	Designer: Théo Heng	Date: 2025-09-04	Revision: 1.1
Sheet Path: /Project Architecture/Sensing - Fan Controller/		Reviewer: Federico B. - Eliot A. - Arion Z.	Size: A4	Sheet: 9 of 13

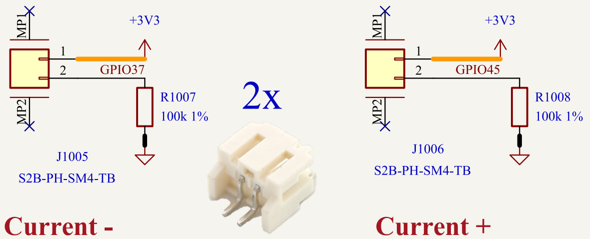
[10] Interface - Connectors









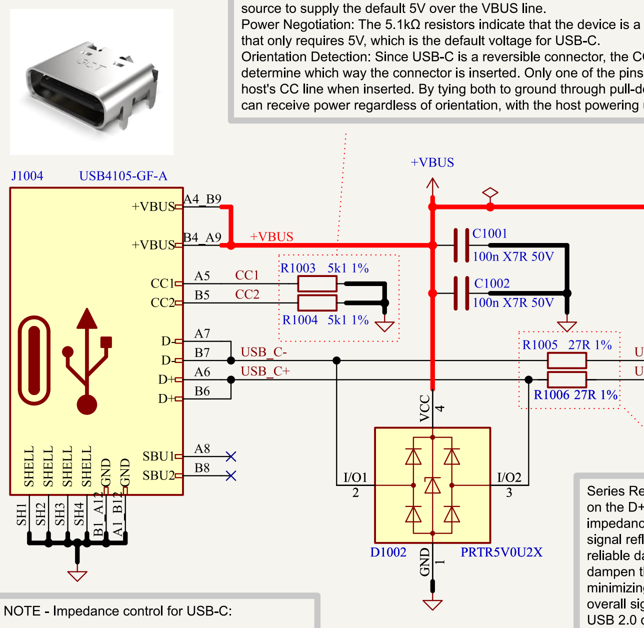


DESIGN NOTE:
It is recommended to connect a 499Ω series resistor to the U0TXD line to suppress the 80 MHz harmonics.

However I don't have enough space so screw it, we can flash over USB-C or JTAG anyway.

DESIGN NOTE - USB-C Configuration Channel pins:

Device Detection: When the CC1 and CC2 pins have pull-down resistors, the USB-C power source detects that a "sink" device is connected and needs power. This signals to the power source to supply the default 5V over the VBUS line.
Power Negotiation: The 5.1kΩ resistors indicate that the device is a standard USB device that only requires 5V, which is the default voltage for USB-C.
Orientation Detection: Since USB-C is a reversible connector, the CC1 and CC2 pins help determine which way the connector is inserted. Only one of the pins will be connected to the host's CC line when inserted. By tying both to ground through pull-down resistors, the device can receive power regardless of orientation, with the host powering up the correct side.



DESIGN NOTE - Impedance control for USB-C:

D+ and D- lines of USB-C needs to be routed as differential pairs, with a 90Ω impedance. Using the standard, no requirement JLC041621-7628 stackup, we need a track width of 0.276mm with a spacing of 0.2mm.

USB-C port

Series Resistors are typically added on the D+ and D- lines to help with impedance matching, which reduces signal reflections and ensures reliable data transmission. They also dampen the signal edges, minimizing EMI and improving overall signal integrity, especially in USB 2.0 designs. The 27Ω value is commonly chosen as it effectively complements typical PCB trace impedances to reach the USB's target impedance of 90Ω for differential signaling.

Power Rails

+VBUS — TP1001 VIN2

GND

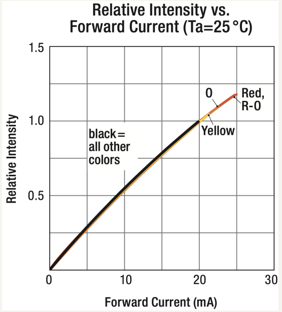
GND — TP1002 GND

Test Points

Removed JTAG in V1.1

Comments: Video for debugging ESP32 with JTAG & VSCODE ESP-PROG Aliexpress link	Company: EPFL Xplore		Variant: Released	
	Board Name: EMUX		Project Name: ERC	
Sheet Title: Interface - Connectors	File Name: Interface - Connectors.kicad_sch	Designer: Théo Heng	Date: 2025-09-04	Revision: 1.1
Sheet Path: /Project Architecture/Interface - Connectors/		Reviewer: Federico B. - Eliot A. - Arion Z.	Size: A4	Sheet: 10 of 13

[11] User - LED Indicators



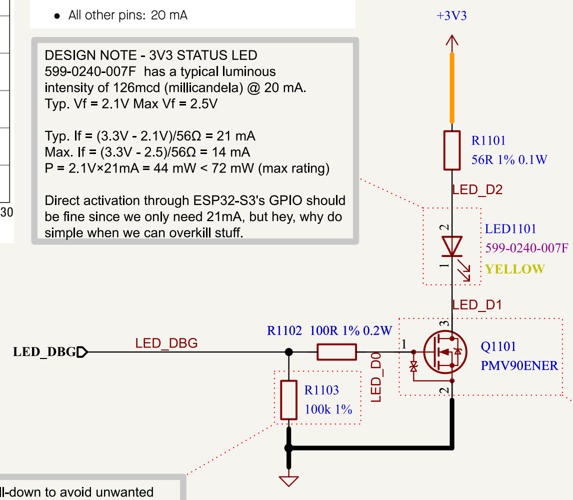
The default drive strengths for each pin are as follows:

- GPIO17 and GPIO18: 10 mA
- GPIO19 and GPIO20: 40 mA
- All other pins: 20 mA

DESIGN NOTE - 3V3 STATUS LED
599-0240-007F has a typical luminous intensity of 126mcd (millicandela) @ 20 mA.
Typ. Vf = 2.1V Max Vf = 2.5V

Typ. If = (3.3V - 2.1V)/56Ω = 21 mA
Max. If = (3.3V - 2.5)/56Ω = 14 mA
P = 2.1V×21mA = 44 mW < 72 mW (max rating)

Direct activation through ESP32-S3's GPIO should be fine since we only need 21mA, but hey, why do simple when we can overkill stuff.



DESIGN NOTE - PMV90ENER

Vgs = 1.5V
Rdson = 54 mΩ

Pull-down to avoid unwanted led activation due to noise when GPIO is floating.

Place the Pull down resistor before the gate resistor to avoid forming a voltage divider.

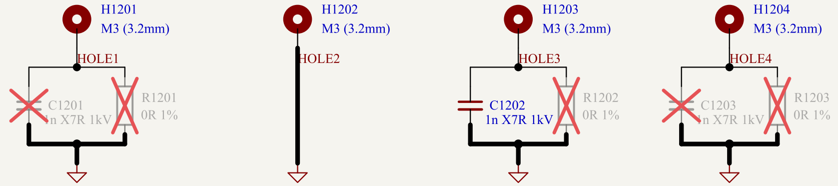
LED Debug Indicator

Comments: Inspired by Amulet controller Schematics by Vincent Nguyen	Company: EPFL Xplore		Variant: Released	
	Board Name: EMUX		Project Name: ERC	
Sheet Title: User - LED Indicators	File Name: User - LED Indicators.kicad_sch	Designer: Théo Heng	Date: 2025-09-04	Revision: 1.1
Sheet Path: /Project Architecture/User - LED Indicators/		Reviewer: Federico B. - Eliot A. - Arion Z.	Size: A4	Sheet: 11 of 13

[12] Misc - Mouting Holes & Fiducials

DESIGN NOTE:

HOLE2 is connected to GND to increase thermal dissipation in the charger area. Also very useful as a GND reference for multimeter debug.



Mechanical Mounting holes

Front

Fiducial Markers

DESIGN NOTE:

In general, do not ground mounting holes that are connected to chassis if there is a risk that the chassis sends current into the PCB and dammages it or if the PCB works with high voltage and there is a risk for the user which is in contact with the chassis.

For a PCB in a metallic enclosure, the enclosure can act like a big antenna. The cavities (space between the ground plane on the pcb and the bottom metallic plane of the enclosure) cause capacitive coupling. This is because we have two metallic planes separated by a dielectric, at a separated potential, causing common mode noise. and result in the noise being amplified by the metal enclosure.
Ideally, in this case, the case should be grounded. But the grounding will cause multiple return paths if multiples mounting holes are connected to GND. In that case, some current will flow in the enclosure and can give a little choc when the user touch it. This can be fine for small battery operated devices.

The best option is therefore to ground only one mounting hole.

Comments: Inspired by Amulet controller Schematics by Vincent Nguyen. How to connect mounting holes. PCB Mounting Holes	Company: EPFL Xplore		Variant: Released	
	Board Name: EMUX		Project Name: ERC	
Sheet Title: Misc - Mouting Holes & Fiducials	File Name: Misc - Mounting Holes.kicad_sch	Designer: Théo Heng	Date: 2025-09-04	Revision: 1.1
Sheet Path: /Project Architecture/Misc - Mounting Holes & Fiducials/		Reviewer: Federico B. - Eliot A. - Arion Z.	Size: A4	Sheet: 12 of 13

[14] Revision History

15.10.2024 - Xplore Schematic Review
Variant: V1.0 Draft -> V1.0 Preliminary

- Added the pin 29 on the ESP32 that was missing.
- Added test points for the status pins of the other ICs.
- Improved brightness of debug LED 30->130 mcd.
- Switch to differential pairs for shunt resistors.
- Connecting some debug GPIO to Ics (ex: VALID1/2).
- Found board name, added Logo.
- Added bulk capacitors and refined their value from dev board of LM51772.
- Change the source of power generation from VSUPPLY to VOUT to constantly enable the MCU.
- Added jumpers and larger footprint resistors for easy test of gate resistors values.
- Added fault and current sensing from LTC7000 to ESP32.
- Increased spacing between high voltage copper pours and GND to provide more isolation.
- Reduced power-path diode size.
- Increased via spacing to avoid ground splitting
- Re-arranged TVS diodes placement.
- Added series inductance on the XTAL_P line.

31.10.2024 - Xplore IDR
Variant: V1.0 Preliminary -> V1.0 Checked

- Added polarity to the XT60 connectors.
- Completely re-rooted the charger section with the following improvements: wider gate traces, switched to 2 layer for the power planes, greatly improved the overall rooting especially the diff pairs.
- Added thermal reliefs.
- Simulated then added feritte bead EMI filtering at the inputs of the 3v3 buck.
- Improved Branding.
- Fixed fiducials placement.
- Added 4th mounting hole.
- Increased board lenght by 5mm (95->100)
- ________________________________
- ________________________________
- ________________________________
- ________________________________
- ________________________________
- ________________________________

10.02.2025 - Xplore Final Review
Variant: V1.0 Checked -> V1.0 Released

- Added solder jumpers for GPIO3, to be able to choose between USB or JTAG lines flashing.
- Changed charger's MOSFETs to reduce losses, therefore reducing heat to an acceptable level. Old: CSD18540Q5B New: BSC059N04LS6
- Added UART programming support.
- Placed TVS diodes before the 27Ω resistors for the JTAG lines.
- Improved documentation for Connectors & LED schematic.
- Fixed TS connection of drivers for power path.

- Reduced current in 3V3 ON LED (56->200Ω)
- Increase Pull-up resistor values to reduce power consumption
- Rebranded PCB to Emux

08.06.2025 - After test revision
Variant: V1.0 -> V1.1

- Fixed charger's LED schematic & layout
- Added autom. Fan control from temperature
- Use larger MOSFETs for powerpath
- Remove the RC delay network for the LTC7000, or connect it to TS and not GND.
- Add protection to the TPS3701
- Inverser capa/resistor pour filtre passe bas dans LTC7000
- Utiliser via 0.3 avec smaller annular width to reduce costs (0.3/0.55) or (0.3/0.50).
- added capa to timer pin of the LTC7000 for power path to avoid false inrush triggers
- use transistors rather than just resistor for the OUT LEDs
- changed power tvs diode from SMBJ33A to SMBJ30A -> max input voltage 33 -> 30V
- integrated connectors for current buttons
- removed JTAG
- inverted charge enable button use
- Removed INA current/voltage sensor

Future Improvements:
- Route the feedback signal for 3V3 away from switching elements, and use this trace only for this purpose
- Instead of a TVS flat clamp that is overkill and expensive (and wrongly placed (should be after RC filter), use a zener didode instead, cheaper and simpler.
- you can route power on layer 3
- weird coper pours shape, especially for vbat, also put solder jumper on top, to be able to route signals in straight line on L4

Comments:	Company: EPFL Xplore		Variant: Released	
	Board Name: EMUX		Project Name: ERC	
Sheet Title: Revision History	File Name: Revision History.kicad_sch	Designer: Théo Heng	Date: 2025-09-04	Revision: 1.1
Sheet Path: /Revision History/		Reviewer: Federico B. - Eliot A. - Arion Z.	Size: A4	Sheet: 14 of 13