DIGITAL DESIGN

ASSIGNMENT REPORT

ASSIGNMENT ID : 1

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PART 1: DIGITAL DESIGN THEORY

Provide your answers here:

1.

(a)64*1024=65536 bytes

(b)128*1024*1024=134217728 bytes

(c)6.4*1024*1024*1024=6871947674 bytes

2.

(a)11111111111111

(b) $2^{13}+2^{12}+2^{11}+2^{10}+2^{9}+2^{8}+2^{7}+2^{6}+2^{5}+2^{4}+2^{3}+2^{2}+2^{1}+2^{0}=16383$ (decimal),

3fff(hexadecimal)

3.

(a)10111000

(b)b8, 10111000

Method (b) is faster

4.

(a)27904836: (9 减去各位加一) 72095164

(b)63325006: (9 减去各位加一) 36674994

5.0123456789ABCDEF

(a)3911

(b)1100011011101111

(b)0011100100010001

(c)3911

(d)equivalent

6.

(a)19.625 转成 10011.101

(b)4/3 不断乘二后取整数部分，8 次后得到 1.01010101, $(341/256=1.33203125)_D$, difference:(1/768=0.00130208333)

(c)$(1.55)_H$, $(1.33203125)_D$, equivalent, because conversion of binary and hexadecimal doesn't change precision.

7.

6:0110, 5:0101, 0:0000, 3:0011

(a)(0110010100000011)BCD

(b)(1001100000110110)excess-3 code

(c)(1010101100000101)8,4,-2,-1 code

(d)(1000011100000100)6311 code

8.(binary: hexadecimal)

(a)00000000: 0

(b)10111111: BF

(c)10111111: BF

(d)01011010: 5A

(e)11100101: E5

(f)11111111: FF

(g)01000000: 40

PART 2: DIGITAL DESIGN LAB (TASK1)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design (provide the Verilog code)*

```
module lab2(addend, augend, addend_led, augend_led, sum_led);
    input signed [1:0] addend;
    input signed [1:0] augend;
    output [1:0] addend_led;
    output [1:0] augend_led;
    output [2:0] sum_led;

    assign addend_led = addend;
    assign augend_led = augend;
    assign sum_led = addend + augend;
endmodule
```

- *Truth-table*

	addend		augend			addend_led		augend_led		sum_led		
位数	1	0	1	0		1	0	1	0	2	1	0
	0	0	0	0		0	0	0	0	0	0	0
	0	0	0	1		0	0	0	1	0	0	1
	0	0	1	0		0	0	1	0	1	1	0
	0	0	1	1		0	0	1	1	1	1	1
	0	1	0	0		0	1	0	0	0	0	1
	0	1	0	1		0	1	0	1	0	1	0
	0	1	1	0		0	1	1	0	1	1	1
	0	1	1	1		0	1	1	1	0	0	0
	1	0	0	0		1	0	0	0	1	1	0
	1	0	0	1		1	0	0	1	1	1	1
	1	0	1	0		1	0	1	0	1	0	0

	1	0	1	1		1	0	1	1	1	0	1
	1	1	0	0		1	1	0	0	1	1	1
	1	1	0	1		1	1	0	1	0	0	0
	1	1	1	0		1	1	1	0	1	0	1
	1	1	1	1		1	1	1	1	1	1	0

SIMULATION

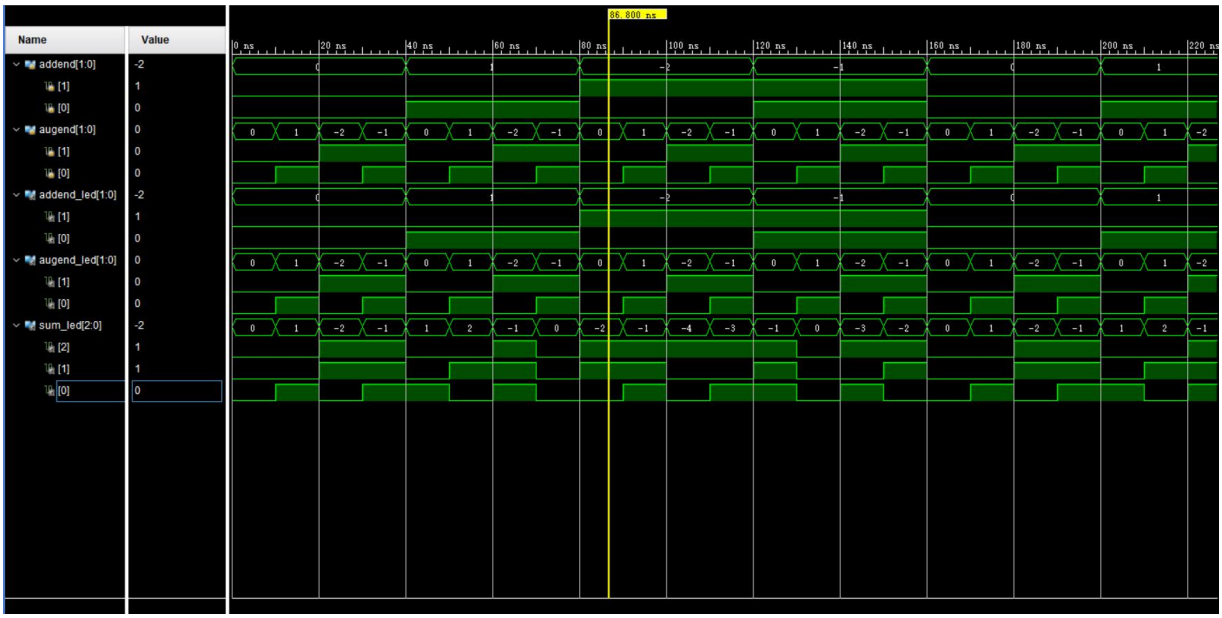
Describe how you build the test bench and do the simulation.

- *Using Verilog(provide the Verilog code)*

```
module lab2_sim();

    reg signed [1:0]addend;

    reg signed [1:0]augend;

    wire signed [1:0]addend_led;

    wire signed [1:0]augend_led;

    wire signed [2:0]sum_led;

    lab2 xc(addend, augend, addend_led, augend_led, sum_led);

    initial
```

```
    begin
                {addend,  augend}=4'b0000;
    end


    always
    begin
        #10      {addend,  augend}  =  {addend,  augend}  +  1;
    end
endmodule
```

- *Wave form of simulation result (provide screen shots)*



- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

	addend		augend			addend_led		augend_led		sum_led		
位数	1	0	1	0		1	0	1	0	2	1	0
	0	0	0	0		0	0	0	0	0	0	0
	0	0	0	1		0	0	0	1	0	0	1
	0	0	1	0		0	0	1	0	1	1	0
	0	0	1	1		0	0	1	1	1	1	1
	0	1	0	0		0	1	0	0	0	0	1
	0	1	0	1		0	1	0	1	0	1	0
	0	1	1	0		0	1	1	0	1	1	1
	0	1	1	1		0	1	1	1	0	0	0
	1	0	0	0		1	0	0	0	1	1	0
	1	0	0	1		1	0	0	1	1	1	1
	1	0	1	0		1	0	1	0	1	0	0
	1	0	1	1		1	0	1	1	1	0	1

	1	1	0	0		1	1	0	0	1	1	1
	1	1	0	1		1	1	0	1	0	0	0
	1	1	1	0		1	1	1	0	1	0	1
	1	1	1	1		1	1	1	1	1	1	0

Yes.

THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

- *Problems and solutions*

PART 2: DIGITAL DESIGN LAB (TASK2)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design while using data flow (provide the Verilog code)*
- *Verilog design while using structured design (provide the Verilog code)*
- *Truth-table*

x	y		(x+y)’	x'y'	(xy)'	x'+y'
0	0		1	1	1	1
0	1		0	0	1	1
1	0		0	0	1	1
1	1		0	0	0	0

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog (provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

CONSTRAINT FILE AND THE TESTING

Describe how you test your design on the Minisys Practice platform.

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene)) to show state of inputs and outputs along with the related descriptions.*

THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

- *Problems and solutions*