



DIGITAL DESIGN

ASSIGNMENT 4

Deadline: 22:30, Thursday 24 December 2020

Lab sessions & Location:

- 1. Lychee Garden 6, Room 402 (Wednesday 14:00-15:50 pm)**
- 2. Lychee Garden 6, Room 402 (Wednesday 16:20-18:10 pm)**
- 3. Lychee Garden 6, Room 402 (Thursday 08:00-09:50 am)**
- 4. Lychee Garden 6, Room 402 (Thursday 10:10-12:10 am)**

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PART 1: DIGITAL DESIGN THEORY

Provide answers to the following questions:

1. Write A sequential circuit has two JK flip-flops A and B and one input x . The circuit is described by the following flip-flop input equations:

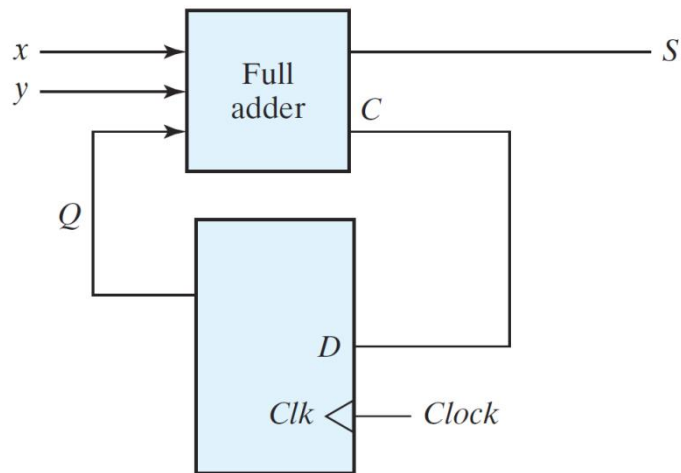
$$J_A = x \quad K_A = B$$

$$J_B = x \quad K_B = A'$$

(a) Derive the state equations $A(t+1)$ and $B(t+1)$ by substituting the input equations for the J and K variables.

(b) Draw the state diagram of the circuit.

2. Design a counter with T flip-flops that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. Show that when binary states 010 and 101 are considered as don't care conditions, the counter may not operate properly. Find a way to correct the design.
3. A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in figure. Derive the state table and state diagram of the sequential circuit.



4. Design a serial 2's complementer with a shift register and a flip-flop. The binary number is shifted out from one side and it's 2's complement shifted into the other side of the shift register.

PART 2: DIGITAL DESIGN LAB

INTRODUCTION

In this lab, you are required to use Vivado 2017.4 and Minisys Practice platform (xilinx FPGA chip artix 7 inside) to design sequential circuits and test them.

PREAMBLE

Before working on the coursework itself, you should master the following material.

1. 'CH5-Synchronous Sequential Logic-SUSTC.ppt' in Sakai site.
2. 'Digital design lab10', 'Digital design lab11', 'Digital design lab12', 'Digital design lab13' in Sakai site.
3. Verilog: <http://www.verilog.com>

EXERCISE SPECIFICATION

TASK1: A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z. The input and output equations are:

$$\begin{aligned} J_A &= Bx + B'y' & K_A &= B'xy' & J_B &= A'x & K_B &= A + xy' \\ z &= Ax'y' + Bx'y' \end{aligned}$$

Implement the sequential circuit in verilog.

- Do the design.
 - i. Implement the JK flip-flop (sensitive to positive edge of clock. an asynchronous reset signal)
 - ii. Implement the sequential circuit which is asked at the 1 st step.
- Write testbench to verify the function of your design.
 - i. Verify the function of JK flip-flop
 - ii. Verify the function of the sequential circuit in Task1

TASK2:

Use two 74194 to implement a 8-bits serial-parallel Converter.

Implement the sequential circuit in verilog.

- Do the design.
 - i. Implement 74194 which is described in lab13 slides.
 - ii. Implement a four-bit ring counter with 74194 which is asked at the 1st step.
- Write testbench to verify the function of your design.
 - i. Verify the function of 74194
 - ii. Verify the function of the sequential circuit in Task2

TASK3:

Implement a subtitles showing 'CSE' on the tubes of Minisys board.

- Do the design, Structure design is expected:
 - There should be 3 modules: 1st one is used to generate a special clock(frequency divider), 2nd one which using the clock generated

by the 1nd module to control the showing on the tubes. 3rd is the top module which instance two modules and do the connection.

- Write testbench to verify the function of the 1st module(frequency divider).
- Create the constraint file about task2.
- Do the synthetic and implementation, generate the bitstream file and program the device, then test on Minisys the develop board

SUBMISSION

Submit your assignment report to the Sakai on *Corresponding site* “CS207-Prof.G” by the deadline.

ASSESSMENT

The full marks for this exercise is 100 and they are distributed as follows:

Theory: 40%

Question 1	10
Question 2	10
Question 3	10
Question 4	10
Total	40 marks

Lab: 60%

Task 1: Design of JK flip-flop in Verilog	5 marks
Task 1: Design of task1 in Verilog(using JK flip-flop is asked)	5 marks
Task 1: Test bench in Verilog, simulation result and its description on JK flip-flop and task1.	5*2 marks
Task 2: Design of 74194 in Verilog	5 marks
Task 2: Design of task2 in Verilog(using 74194 is asked)	5 marks

Task 2: Test bench in Verilog, simulation result and its description on 74194 and task2.	5*2 marks
Task 3: Design of module 1, 2 and 3 in task2 of this assignment.	5*3 marks
Task 3: Constrains file, the photos and description of the test result on Minisys practice board.	5 marks
Total	60 marks

The template for the report could be found on sakai site “CS207-Prof.G”.