DIGITAL DESIGN

ASSIGNMENTREPORT

ASSIGNMENT ID : 4

Student Name: 徐驰 (Xu Chi)

Student ID: 11912224

PART 1: DIGITAL DESIGN THEORY

Provide your answers here：

1.

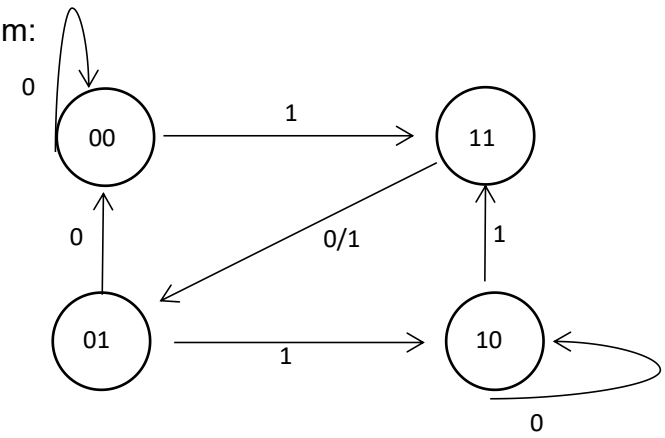
(a) $A(t+1) = J_A A_t' + K_A' A_t = xA_t' + B_t' A_t$

$B(t+1) = J_B B_t' + K_B' B_t = xB_t' + A_t B_t$

(b) state-table:

present state		input	next state		filp-flop input			
At	Bt	x	A(t+1)	B(t+1)	JA	KA	JB	KB
0	0	0	0	0	0	0	0	1
0	0	1	1	1	1	0	1	1
0	1	0	0	0	0	1	0	1
0	1	1	1	0	1	1	1	1
1	0	0	1	0	0	0	0	0
1	0	1	1	1	1	0	1	0
1	1	0	0	1	0	1	0	0
1	1	1	0	1	1	1	1	0

state-diagram:



2.

Here is the state transition table: three bits are denoted by $Q_2Q_1Q_0$

0	1	3	7	6	4	0	1	...
000	001	011	111	110	100	000	001	...

Hence, we need 3 T-flip-flop to control every bit's change:

present state			next state			T-flip-flop		
Q2	Q1	Q0	Q2(t+1)	Q1(t+1)	Q0(t+1)	T2	T1	T0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	X	X	X	X	X	X
0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	0
1	0	1	X	X	X	X	X	X
1	1	0	1	0	0	0	1	0
1	1	1	1	1	0	0	0	1

K-map will be shown below:

T2:

Q2 \ Q1Q0	00	01	11	10
0	0	0	1	X
1	1	X	0	0

So: T2 = Q2'Q1 + Q2Q1' = Q2 ⊕ Q1

T1:

Q2 Q1Q0	00	01	11	10
0	0	1	0	X
1	0	X	0	1

So: T1 = Q1'Q0 + Q1Q0' = Q1 ⊕ Q0

T0:

Q2 Q1Q0	00	01	11	10
0	1	0	0	X
1	0	X	1	0

So: T0 = Q2'Q1' + Q2Q0 = Q2 ⊙ Q0

However,since we got its expressions, we discover that, as it is described in the text above, when binary states 010 and 101 are considered as don't care conditions, the counter may not operate properly.

The remedy is shown below:

When Q2Q1Q0 = 010, Q2(t+1)Q1(t+1)Q0(t+1) = 100;

Q2Q1Q0 = 101, Q2(t+1)Q1(t+1)Q0(t+1) = 010

present state			next state			T-flip-flop		
Q2	Q1	Q0	Q2(t+1)	Q1(t+1)	Q0(t+1)	T2	T1	T0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	1	0	0	1	1	0
0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	0
1	0	1	0	1	0	1	1	1
1	1	0	1	0	0	0	1	0
1	1	1	1	1	0	0	0	1

K-map will be shown below:

T2:

Q2 \ Q1Q0	00	01	11	10
0	0	0	1	1
1	1	1	0	0

So: T2 = Q2Q1' + Q2'Q1 = Q2 ⊕ Q1

T1:

Q2 \ Q1Q0	00	01	11	10
0	0	1	0	1

1	0	1	0	1

So: T1 = Q1'Q0 + Q1Q0' = Q1 ⊕ Q0

T0:

Q2 Q1Q0	00	01	11	10
0	1	0	0	0
1	0	1	1	0

So: T0 = Q2'Q1'Q0' + Q2Q0

3.

The FA equation will be given as

S = x ⊕ y ⊕ Q

C = xy + xQ + yQ

The input equation will be given as

DQ = C = xy + xQ + yQ

The characteristic equation will be given as

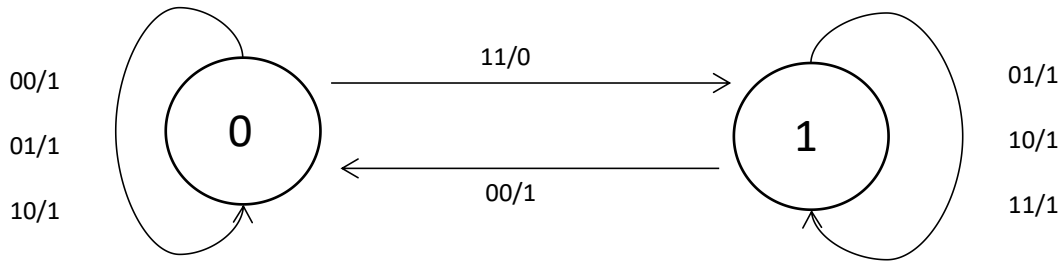
Q(t+1) = D = xy + xQ + yQ

State equation will be Q(t+1) = C

Here is the state table:

present state	input		next state	output
Q(t)	x	y	Q(t+1)	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Here is the state diagram:



4.

We will show the principle by truth table:

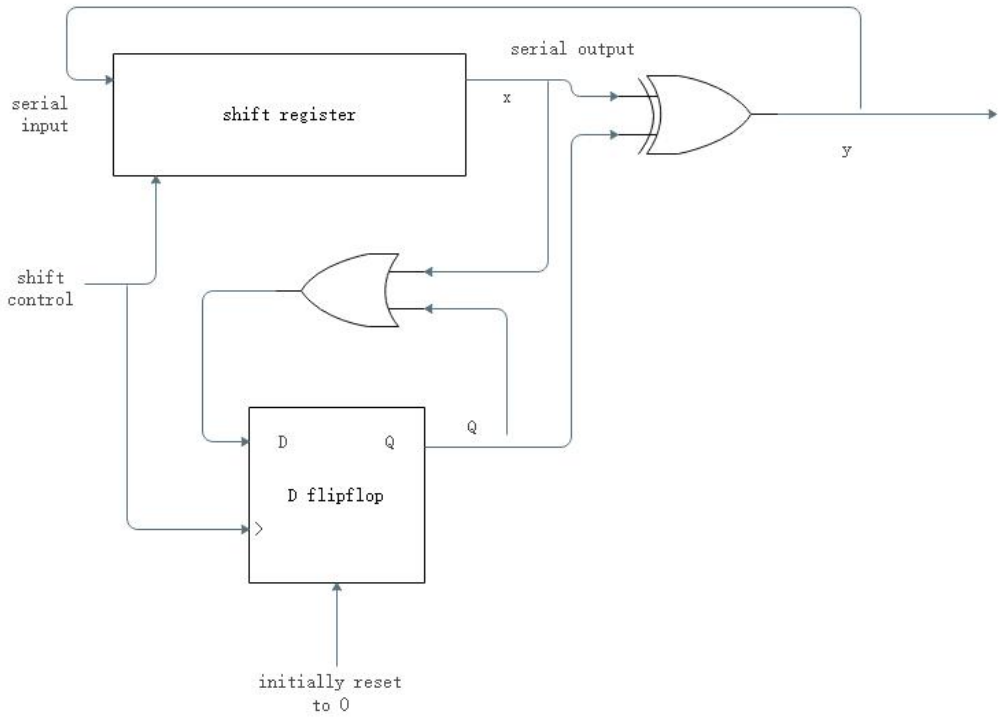
Q	output of shift register	input of shift register
0	0	0
0	1	1
1	0	1
1	1	0

Q(n)	output of shift register	Q(n+1)
0	0	0
0	1	1
1	0	1
1	1	1

Therefore, we can get these conclusion: input = Q ⊕ output,

and Q(n+1) = Q(n) or output.

The diagram is shown as below:



PART 2: DIGITAL DESIGN LAB (TASK1) (CHECKED)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design (provide the Verilog code)*
- *Truth-table*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog(provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

CONSTRAINT FILE AND THE TESTING

Describe how you test your design on the Minisys Practice platform.

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene) to show state of inputs and outputs along with the related descriptions.*

THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

- *Problems and solutions*

PART 2: DIGITAL DESIGN LAB (TASK2) (CHECKED)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design while using data flow (provide the Verilog code)*
- *Verilog design while using structured design (provide the Verilog code)*
- *Block design (provide screen shots)*
- *Truth-table*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog (provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

CONSTRAINT FILE AND THE TESTING

Describe how you test your design on the Minisys Practice platform.

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