DIGITAL DESIGN

ASSIGNMENTREPORT

ASSIGNMENT ID : 2

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PART 1: DIGITAL DESIGN THEORY

Provide your answers here:

1. (a) Suppose F1 = ∑ai, F2 = ∑bi, E = F1 + F2 = ∑ai + ∑bi, so given the Boolean function E=F1+F2, if F1 and F2 can be expressed by the sum of minterms, then E=F1+F2 is the sum of the minterms of F1 and the sum of the minterims of F2. Such that, the Boolean function E=F1+F2 contains the sum of the minterms of F1 and F2.

(b) Given the Boolean function G=F1*F2, and F1 and F2 can be expressed by the sum of minterms. Then as F1*F2 going on, each minterm of F1 will multiply by each minterm of F2. If the minterm of F1 is different from the minterm of F2, this will result the minterm disappear since AA'=0. On the other hand, if the minterm of F1 is same as the minterm of F2, the minterm will reserve since AA=A. Such that, the Boolean function G=F1*F2 contains only the minterms that are common to F1 and F2.

2. Here we give the maps:

(a)

x	y	z	SOP		POS	
0	0	0	x'y'z'	m0	x+y+z	M0
0	0	1	x'y'z	m1	x+y+z'	M1
0	1	0	x'yz'	m2	x+y'+z	M2
0	1	1	x'yz	m3	x+y'+z'	M3
1	0	0	xy'z'	m4	x'+y+z	M4
1	0	1	xy'z	m5	x'+y+z'	M5
1	1	0	xyz'	m6	x'+y'+z	M6
1	1	1	xyz	m7	x'+y'+z'	M7

So F(x, y, z) = ∑(1, 3, 7) = x'y'z + x'yz + xyz

= ∏(0, 2, 4, 5, 6) = (x + y + z)(x + y' + z)(x' + y + z)(x' + y + z')(x' + y' + z)

(b)

A	B	C	D	SOP		POS	
0	0	0	0	A'B'C'D'	m0	A+B+C+D	M0
0	0	0	1	A'B'C'D	m1	A+B+C+D'	M1
0	0	1	0	A'B'CD'	m2	A+B+C'+D	M2
0	0	1	1	A'B'CD	m3	A+B+C'+D'	M3
0	1	0	0	A'BC'D'	m4	A+B'+C+D	M4
0	1	0	1	A'BC'D	m5	A+B'+C+D'	M5
0	1	1	0	A'BCD'	m6	A+B'+C'+D	M6
0	1	1	1	A'BCD	m7	A+B'+C'+D'	M7
1	0	0	0	AB'C'D'	m8	A'+B+C+D	M8
1	0	0	1	AB'C'D	m9	A'+B+C+D'	M9
1	0	1	0	AB'CD'	m10	A'+B+C'+D	M10
1	0	1	1	AB'CD	m11	A'+B+C'+D'	M11
1	1	0	0	ABC'D'	m12	A'+B'+C+D	M12
1	1	0	1	ABC'D	m13	A'+B'+C+D'	M13
1	1	1	0	ABCD'	m14	A'+B'+C'+D	M14
1	1	1	1	ABCD	m15	A'+B'+C'+D'	M15

So F(A, B, C, D) = $\prod$(1, 3, 5, 8, 11, 13, 15)

=(A+B+C+D')(A+B+C'+D')(A+B'+C+D')(A'+B+C+D)(A'+B+C'+D')(A'+B'+C+D')(A'+B'+C'+D')

=$\sum$(0, 2, 4, 6, 7, 9, 10, 12, 14)

= A'B'C'D' + A'B'CD' + A'BC'D' + A'BCD' + A'BCD + AB'C'D + AB'CD' + ABC'D' + ABCD'

3.

(a) F1 = (b’ + d)(a’+ b’+ c)(a + c)

a	b	c	d	F1	SOP	
0	0	0	0	0	a'b'c'd'	m0
0	0	0	1	0	a'b'c'd	m1
0	0	1	0	1	a'b'cd'	m2
0	0	1	1	1	a'b'cd	m3
0	1	0	0	0	a'bc'd'	m4
0	1	0	1	0	a'bc'd	m5
0	1	1	0	0	a'bcd'	m6
0	1	1	1	1	a'bcd	m7
1	0	0	0	1	ab'c'd'	m8
1	0	0	1	1	ab'c'd	m9
1	0	1	0	1	ab'cd'	m10
1	0	1	1	1	ab'cd	m11
1	1	0	0	0	abc'd'	m12
1	1	0	1	0	abc'd	m13
1	1	1	0	0	abcd'	m14
1	1	1	1	1	abcd	m15

So F1 = a'b'cd' + a'b'cd + a'bcd + ab'c'd' + ab'c'd + ab'cd' + ab'cd + abcd

= ∑(2, 3, 7, 8, 9, 10, 11, 15)

(b) F2 = ab + a'c'+ bc

a	b	c	F2	POS	
0	0	0	1	a+b+c	M0
0	0	1	0	a+b+c'	M1
0	1	0	1	a+b'+c	M2
0	1	1	1	a+b'+c'	M3
1	0	0	0	a'+b+c	M4
1	0	1	0	a'+b+c'	M5
1	1	0	1	a'+b'+c	M6
1	1	1	1	a'+b'+c'	M7

So F2 = (a + b + c')(a' + b + c)(a' + b + c') = ∏(1, 4, 5)

4.

(a) y'z' + yz' + x'z = z' + x'z = x'z' + xz' + x'z, ∵ xz' + x'z does not equal 0 all the time, so y'z' + yz' + x'z ≠ x'z'

(b) x'y'+ x'z'+ yz = x'(y' + z') + yz = x' + yz = x'(y + z) + x'(y'z') + yz, and the right section = x'y + x'z = x'(y + z) ∵ x'(y'z') + yz does not equal 0 all the time, so x'y'+ x'z'+ yz ≠ x'(y + z)

5.

(a)

CD \ AB	00	01	11	10
00	1	0	0	1
01	0	1	1	0

11	0	1	1	0
10	1	0	0	1

So F (A, B, C, D) = ∑ (0, 2, 5, 7, 8, 10, 13, 15)

=(A'B'C'D' + A'B'CD') + (AB'C'D' + AB'CD') + (A'BC'D + A'BCD) + (ABC'D + ABCD)

= B'D' + BD

(b)

yz \ wx	00	01	11	10
00	0	1	0	0
01	1	1	1	1
11	1	1	1	1
10	0	1	0	0

So F (w, x, y, z) = ∑ (1, 3, 4, 5, 6, 7, 9, 11, 13, 15 = z + w'x

(c)

CD \ AB	00	01	11	10
00	0	0	0	0
01	1	0	0	1
11	1	1	1	1
10	0	0	1	0

A'BCD + ABC + CD + B'D = A'BCD + ABC + CD + B'D = CD + B'D + ABC

(d)

CD \ AB	00	01	11	10
00	1	0	0	0
01	1	1	1	0
11	0	1	1	1
10	0	0	0	0

A’B’C’D’ + BC’D + A’C’D + A’BCD + ACD = BD + A’B’C’ + ACD

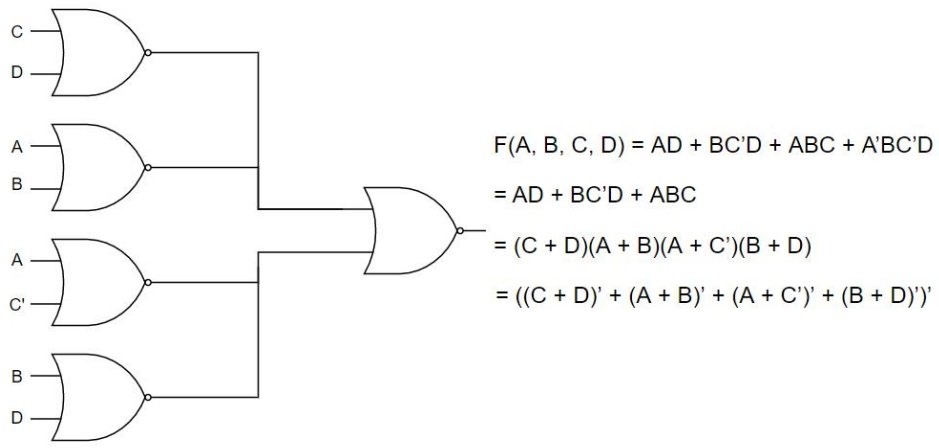
6.

(a) F(A, B, C, D) = AD + BC’D + ABC + A’BC’D

= AD + BC’D + ABC

= (C + D)(A + B)(A + C’)(B + D)

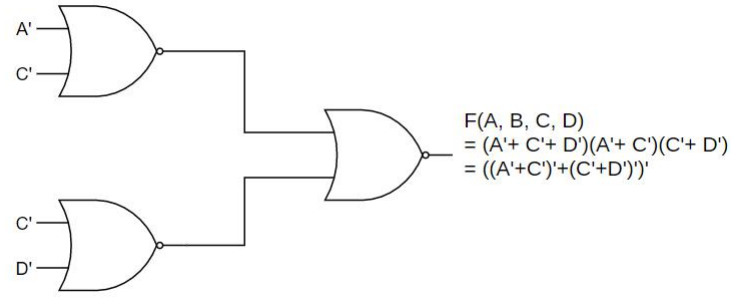
= ((C + D)’ + (A + B)’ + (A + C’)’ + (B + D)’)’



(b) F(A, B, C, D)= (A’ + C’+ D’)(A’ + C’)(C’ + D’)

=(A’ + C’)(C’ + D’)

= ((A’ + C’)’ + (C’ + D’)’)’



7.

(a) F(x, y, z) = ∑(0, 1, 4, 5, 6) with d(x, y, z)= ∑(2, 3, 7)

F(x, y, z) = x'y'z' + x'y'z + xy'z' + xy'z + xyz'

d(x, y, z) = x'yz' + x'yz + xyz

F(x, y, z) = 1

(b) F(A, B, C, D) = ∑(5, 6, 7, 12, 14) with d(x, y, z)= ∑(3, 9, 11)

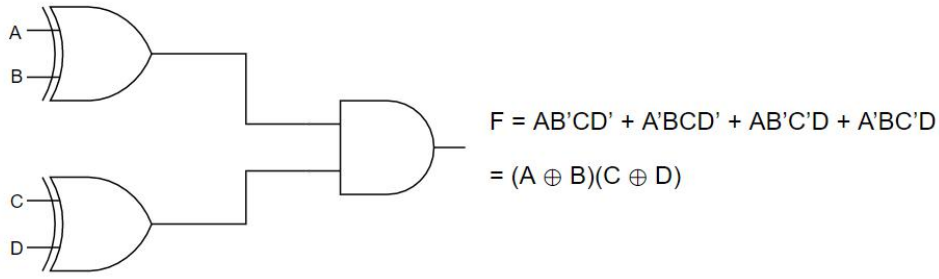
F(A, B, C, D) = ∑(5, 6, 7, 12, 14) = A'BC'D + A'BCD' + A'BCD + ABC'D' + ABCD'

= A'BD + BCD' + ABD'

8. F = AB'CD' + A'BCD' + AB'C'D + A'BC'D

= (AB' + A'B)(CD' + C'D)

= (A ⊕ B)(C ⊕ D)



PART 2: DIGITAL DESIGN LAB (TASK1) (CHECKED)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design (provide the Verilog code)*
- *Truth-table*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog(provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

CONSTRAINT FILE AND THE TESTING

Describe how you test your design on the Minisys Practice platform.

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene) to show state of inputs and outputs along with the related descriptions.*

THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

- *Problems and solutions*

PART 2: DIGITAL DESIGN LAB (TASK2) (CHECKED)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design while using data flow (provide the Verilog code)*
- *Verilog design while using structured design (provide the Verilog code)*
- *Block design (provide screen shots)*
- *Truth-table*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog (provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

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Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

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