DIGITAL DESIGN

ASSIGNMENT 3

Deadline: *22:30, Wednesday 2 December 2020*

Lab sessions & Location:

1. **Lychee Garden 6, Room 406 (Wednesday 16:20-18:10 pm)**

2. **Lychee Garden 6, Room 408 (Wednesday 19:00-20:50 pm)**

3. **Lychee Garden 6, Room 402 (Thursday 8:00-9:50 am)**

4. **Lychee Garden 6, Room 402 (Thursday 10:10~12:10 am)**

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Provide answers to the following questions:

1. Implement the following Boolean function F, using the two-level forms of logic:(a)AND-OR, (b) OR-AND (c) NOR-OR, (d) NOR-NOR (e) NAND-NAND, and (f) NAND-AND: $F(A, B, C, D) = \sum (1, 3, 5, 8, 9, 10, 11, 13, 15)$Please note that you only need to write the logic equation, no drawing needed.

2. Derive the circuits for a parity generator and a parity checker using an even parity bit. Write the truth table, simplify your logic equation and draw circuit diagram using minimal number of gates. The parity generator has 4 inputs, A, B, C, and D. The parity checker has also 4 inputs, A, B, C and P.

3. Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B , and C. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. When the binary input is 0, 1, 2 or 3, the binary output is one greater than the input. Write the logic formula and draw circuit diagram. Tip: You may use adders together with gates.

4. For a binary multiplier that multiplies two unsigned four-bit numbers, use AND gates and adders, design the circuit. Briefly describe your design and list the logic formulas. Draw the circuit diagram. For adders, you can just use a block diagram with ports to represent them. Tip: You can write the signal name next to ports of gates/adders, to avoid drawing long wires.

5. Implement the following Boolean function with a multiplexer. No drawings needed.

    (a) $F(A, B, C, D) = \sum (1, 2, 5, 8, 10, 14)$

    (b) $F(A, B, C, D) = \prod (4, 5, 11)$

6. Implement a full subtractor with two 4x1 multiplexers or an 8x1 multiplexer. Write down your process and draw the circuit diagram.

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PART 2: DIGITAL DESIGN LAB

INTRODUCTION

In this lab, you are required to use Vivado 2017.4 and Minisys Practice platform (xilinx FPGA chip artix 7 inside) to design combinational logic circuits and test them.

PREAMBLE

Before working on the coursework itself, you should master the following material.

1.'CH3-Minimisation-SUSTC-new.ppt' and 'CH4-COMBINATIONAL LOGiC.ppt' in Sakai site.

2. 'Digital design lab8', 'Digital design lab9' in Sakai site.

3. Verilog: http://www.verilog.com

EXERCISE SPECIFICATION

TASK1:

Implement a 4-16 decoder by two 3-8 decoders. You can either modify the provided 3-8 decoder or design 74138 decoder.

- Do the design.
    - i. Implement a 3-8 decoder 1st
    - ii. implement a 4-16 decoder using the 3-8 decoder which is asked at the 1st step
- Write testbench to verify the function of your design.
    - i. Verify the function of 3-8 decoder
    - ii. Verify the function of 4-16 decoder
- Create the constraint file about 4-16 decoder.
- Do the synthetic and implementation, generate the bitstream file and program the device, then test on the Minisys develop board.

TASK2:

Use 74151(8-to-1-line multiplexer) realize the following logic function "Y = A'B'C'D' + BC'D + A'C'D + A'BCD + ACD".

- Do the design.
  - Implement 74151
  - Realize the logic function:

    "Y = A'B'C'D' + BC'D + A'C'D + A'BCD + ACD" in two ways:
    a) Using data flow
    b) Using 74151
- Write testbench to verify the function of your design.
  - Verify the function of 74151
  - Verify the function of "Y = A'B'C'D' + BC'D + A'C'D + A'BCD + ACD"
- Create the constraint file about "Y = A'B'C'D' + BC'D + A'C'D + A'BCD + ACD"
- Do the synthetic and implementation, generate the bitstream file and program the device, then test on Minisys the develop board

SUBMISSION

Submit your assignment report to the Sakai on *Corresponding site* "CS207-Prof.G" by the deadline.

ASSESSEMENT

The full marks for this exercise is 100 and they are distributed as follows:

Theory: 40%

Question 1	12
Question 2	8
Question 3	4
Question 4	8
Question 5	4

Question 6	4
Total	40 marks

Lab: 60%

Task 1: Design of 3-8 decoder in Verilog, the truth-table of 3-8 decoder	5 marks
Task 1: Design of 4-16 decoder in Verilog(using 3-8 decoder is asked), the truth-table of 4-16 decoder.	10 marks
Task 1: Test bench in Verilog, simulation result and its description on both 3-8 decoder and 4-16 decoder.	5 marks
Task 1: Constrains file, the photos and description of the test result on Minisys practice board.(3 test scenarios at least)	10 marks
Task 2: Design of 74151 in Verilog, the truth-table of 74151	5 marks
Task 2: Design of digital logic "Y = A'B'C'D' + BC'D + A'C'D + A'BCD + ACD" by using 74151 and by data-flow respectively.	10 marks
Task 2: Test bench in Verilog, simulation result and its description on both data-flow design and structure design of logic function.	5 marks
Task 2: Constrains file, the photos and description of the test result on Minisys practice board.(3 test scenarios at least)	10 marks
Total	60 marks

The template for the report could be found on sakai site "CS207-Prof.G".