Test Case 1

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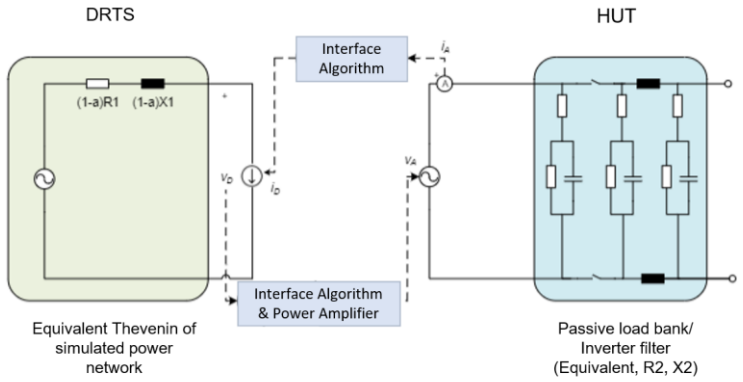
Name of the Test Case	Virtual Shifting Impedance with Delay Compensation & Sensitivity Framework
Narrative	An advanced method for improving stability and accuracy of PHIL experiments is considered. It was developed based on existing proven ones, namely the shifting impedance and the time delay compensation, aiming to combine and take advantage of their properties. At the same time, the method expanded to overcome some limitations, like the need for availability of actual hardware impedance. This method while increasing stability of the PHIL setup, also improves the accuracy. This TC aims to verify and validate the properties of VSIDC interface algorithm in simple and more complex scenarios. Moreover, the sensitivity framework will be employed to precisely estimate the PHIL system properties prior to experimental testing.
Function(s) under Investigation (*FuI*) "the referenced specification of a function realized (operationalized) by the object under investigation"	• Applicability of VSIDC interface algorithm • Accuracy and stability assessment of VSIDC
Object under Investigation (*OuI*) "the component(s) (1..n) that are to be qualified by the test"	• VSIDC interface algorithm • The tested HUT
Domain under Investigation (*DuI*): "the relevant domains or sub-domains of test parameters and connectivity."	Electrical Domain
Purpose of Investigation *(PoI)* The test purpose in terms of Characterization, Verification, or Validation	• Characterization and validation of the System under Test (SuT) • Verification and validation of the OuI • Verification and validation of the FuI
System under Test (*SuT*): Systems, subsystems, components included in the test case or test setup.	PHIL setup with passive or active load.
Functions under Test (*FuT*) Functions relevant to the operation of the system under test, including FuI and relevant interactions btw. OuI and SuT.	• Applicability of VSIDC interface algorithm • Accuracy and stability assessment of VSIDC

Test criteria: Formulation of criteria for each PoI based on properties of SuT; encompasses properties of test signals and output measures.	Evaluation of the stability and accuracy of the setups realized through the incorporation of the VSIDC
target metrics Measures required to quantify each identified test criteria	• Current and voltage measurements • Error in active and reactive power exchange at point of common coupling. • Time delay • Sensitivity functions
variability attributes controllable or uncontrollable factors and the required variability; ref. to PoI.	Variability factors include: • Varying cut-off frequency of feedback filter • Varying ratio of software and hardware impedance
quality attributes threshold levels for test result quality as well as pass/fail criteria.	Proper stability margins and accuracy metrics (e.g. Phw=Psw, etc)

Qualification Strategy

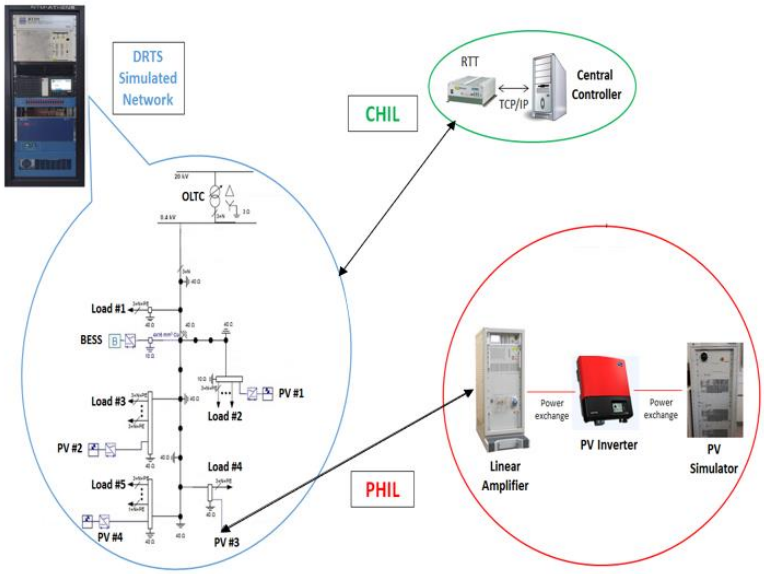
i.e. how are the PoI to be met by the different tests and how will the test results be combined to yield the desired PoI outcomes (see guideline)

Test Specification D1.1

Reference to Test Case	*TC D1*
Title of Test	***Validation of Virtual Shifting Impedance with Delay Compensation (VSIDC)***
Test Rationale	*This test aims to validate the developed VSIDC method in a PHIL setup with passive/active HUT.*
Specific Test System (graphical)	Simple voltage divider circuit. 
Target measures	• *Stability assessment* • *Active power and reactive power at the point of common coupling and accuracy assessment* • *Sensitivity functions* • *Signal to Noise Ratio (SNR) and Total Harmonic Distortion (THD) measurements*
Input and output parameters	*Input:*

	• Load/Hardware device *• Grid condition* *Output:* *• Voltage, current and power measurements, during steady and transient states*
Test Design	*• The simulation at DRTS starts first* *• The voltage is applied to the amplifier and measured* *• The voltage of the amplifier is output to the HUT and current and voltage measurements are taken* *• Finally, the loop closes, and the accuracy of the system is estimated*
Initial system state	*The system is initialised and synchronized at nominal values of voltage (230 V) and frequency (50 Hz).*
Evolution of system state and test signals	*Use of different sets of Zs, Zh and LPF (feedback filters) to compare experimental results with theoretical stability margins.*
Other parameters	*n/a*
Temporal resolution	*16 kHz, 50 µs.*
Source of uncertainty	*Amplifier's response (delay, amplification), sensors imperfections, HUT's behavior in case of active component, etc.*
Suspension criteria / Stopping criteria	*Suspension – Instability* *Stopping: Successful evolution of system states and recording of target measures.*

Test Specification D1.2

Reference to Test Case	*TC D1*
Title of Test	***PHIL setup for testing the compliance with FRT requirements and other ancillary services provided by DERs***
Test Rationale	*A microgrid application is considered, in which DERs feed the load and achieve power sharing. At the same time, the voltage and frequency of the microgrid are regulated close to their nominal values (droop control operation). Furthermore, when a fault occurs, the inverters inject power according to international standards to provide grid support. Advanced interface algorithms, like delay compensation and VSIDC which was developed in the frame of ERIGrid 2.0, will be utilized to make the PHIL setup stable and to provide more accurate results of testing.*
Specific Test System (graphical)	
Target measures	*• Inverter power injection, load voltage and frequency, inverter currents*

	• Active power and reactive power at the point of common coupling *and accuracy assessment* *• Stability assessment* *• Sensitivity functions* *• SNR and THD measurements*
Input and output parameters	*Input:* *• Load* *• Inverter power injection set-points* *• Grid condition* *Output:* *• Voltage, current and power measurements, during steady and transient states*
Test Design	*• Operate a set of inverters in parallel* *• Perform a network fault when the microgrid operates either in islanded (non-interconnected) mode or in grid-connected mode* *• Save the experimental results*
Initial system state	*The system is initialised and synchronized at nominal values of voltage (230 V) and frequency (50 Hz).*
Evolution of system state and test signals	*The system goes from normal operation (operation close to nominal voltage and frequency) to operation under fault, to test the inverter behavior*
Other parameters	*n/a*
Temporal resolution	*16 kHz (in case a switched-type amplifier is used), 50 µs.*
Source of uncertainty	*Hardware inverter's response, amplifier's response (delay, amplification), sensors imperfections, etc.*
Suspension criteria / Stopping criteria	*Suspension: Abnormal current, Instability* *Stopping: Successful evolution of system states and recording of target measures.*

Mapping to Research Infrastructure

i.e. how is it planned to distribute (map) and execute the specified test system in a given research infrastructure (free text); this section can be used to list the intended Experiment specifications.

Experiment Specification ES.D1.1

Reference to Test Specification	*TS D2.1*
Title of Experiment	*Validation of VSIDC method in PHIL setup with passive load*
Research Infrastructure	EESL (ICCS-NTUA) and DPSL (Strathclyde)
Experiment Realisation	• Designing the interface topology in the real-time simulator, and the proposed interface algorithm • Designing of the appropriate software protection • Hardware interfaces
Experiment Setup (concrete lab equipment)	• Real-Time Digital Simulator (RTDS) • Interfacing I/O cards • PC for RSCAD (UI of RTDS) • Switching Amplifier (Triphase) • Hardware passive load • Metering devices
Experimental Design and Justification	*In RSCAD the simulated part will be designed based on known interface topologies (Voltage-Type Ideal Transformer Model (V-ITM), etc). Then the VSIDC will be designed in the controller of the power amplifier and finally, the HUT will be interfaced to RTDS through the amplifier.*
Precision of equipment and measurement uncertainty	• 50 μs time step • precision of the used ammeter • Delay introduced for the D/A and A/D conversions • Delay introduced and non-ideal output response of the amplifier
Storage of experiment data	*RTDS – Various formats (excel, dat, cfg, etc).*

Experiment Specification ES.D1.2

Reference to Test Specification	*TS D1.1*
Title of Experiment	*PHIL for analysing inverter's response in real condition*
Research Infrastructure	DPSL (Strathclyde) or EESL (ICCS-NTUA)
Experiment Realisation	• Microgrid design in RSCAD • Designing of the appropriate software protection • Hardware interfaces
Experiment Setup (concrete lab equipment)	• Real Time Digital Simulator (RTDS) • Interfacing I/O cards • PC for RSCAD (UI of RTDS) • Switching Amplifier (Triphase) • Hardware solar inverter • Metering devices
Experimental Design and Justification	*• In RSCAD an inverter-based microgrid will be designed. The inverters will be simulated as controlled voltage sources to facilitate testing under various grid conditions.* *• FRT curve according to Grid Codes, will be used.* *• A hardware inverter will be connected to RTDS to perform PHIL experiments and validate the performance under real conditions.*
Precision of equipment and measurement uncertainty	• 50 μs time step • precision of the used ammeter • Delay introduced for the D/A and A/D conversions • Delay introduced and non-ideal output response of the amplifier
Storage of experiment data	*RTDS – Various formats (excel, dat, cfg, etc).*