Test Case 2

Author M. Syed (UoS), Z. Feng (UoS), S. Vogel (RWTH), A. Kontou (ICCS), A. Paspatis (ICCS), T.The Hoang (CEA)
Version 0.1
Project ERIGrid 2.0 Date 17.02.2023

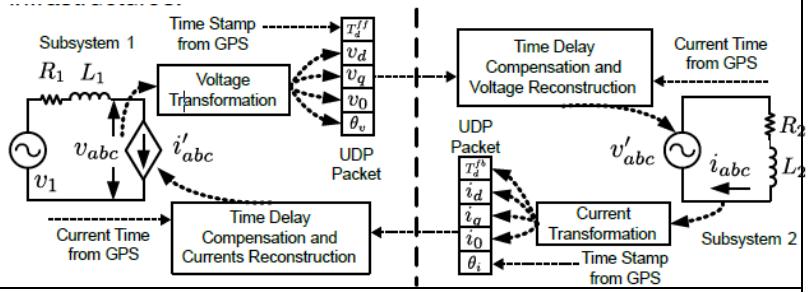
Name of the Test Case	Time Delay Compensation
Narrative	Time delay is an inherent characteristic of any closed-loop power hardware in the loop (PHIL) setup affecting both accuracy and stability of the setup. High fidelity PHIL set-ups are conventionally realized through the compensation of time delay, that is variable yet deterministic for such setups. The renewed challenge is presented through the emergence of geographically distributed simulations where two or more digital real-time simulators (DRTS) are interconnected over the Internet through a similar interface algorithm as utilised in PHIL setups. The indeterministic nature of the exchange of data through the Internet presents a challenge for the determination of the time delay and its consequent compensation to realise high fidelity simulations. While GPS time-stamped signals exchange presents a viable approach to development of accurate time-delay compensation method, two* additional time delay compensation methods have been realized within the ERIGRID 2.0 project. The objective of this test case is to characterize the performance of the two methods against the GPS based time delay compensation.
Function(s) under Investigation (*FuI*) "the referenced specification of a function realized (operationalized) by the object under investigation"	The time delay compensation methods developed: • GPS based time delay compensation. • Probabilistic time delay compensation. • Data-driven time delay compensation.
Object under Investigation (*OuI*) "the component(s) (1..n) that are to be qualified by the test"	The two DRTS at the two research infrastructures.
Domain under Investigation (*DuI*): "the relevant domains or sub-domains of test parameters and connectivity."	Electrical Domain ICT Domain
Purpose of Investigation *(PoI)* The test purpose in terms of Characterization, Verification, or Validation	PoI 1: To validate the developed time delay compensation methods PoI 2: To characterize the accuracy of the setups realized through the integration of the three* time delay compensation methods.
System under Test (*SuT*): Systems, subsystems, components included in the test case or test setup.	Voltage divider circuit split for simulation across the two DRTS.

Functions under Test (*FuT*) Functions relevant to the operation of the system under test, including FuI and relevant interactions btw. OuI and SuT.	For all compensation methods: • Interface signals reconstruction (the function de-pends on the transformation chosen) For GPS based time delay compensation: • GPS time-stamp signal
Test criteria: Formulation of criteria for each PoI based on properties of SuT; encompasses properties of test signals and output measures.	Evaluation of accuracy of the setups realized through the incorporation of the time-delay compensation methods
target metrics Measures required to quantify each identified test criteria	The measure required: • Time delay • Error in active and reactive power exchange at point of common coupling.
variability attributes controllable or uncontrollable factors and the required variability; ref. to PoI.	Variability factors include: • Time of day of experiment • Size of data packet
quality attributes threshold levels for test result quality as well as pass/fail criteria.	Successful (stable) realization of the voltage divider circuit synchronization over the two DRTS with incorporation of the time-delay compensation methods.

Qualification Strategy

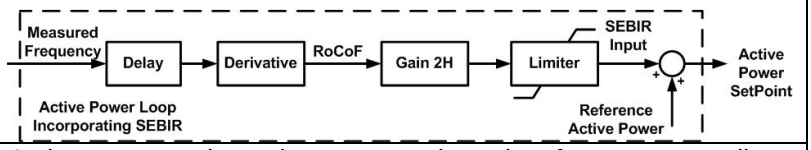
i.e. how are the PoI to be met by the different tests and how will the test results be combined to yield the desired PoI outcomes (see guideline)

Test Specification D2.1

Reference to Test Case	*TC D2*
Title of Test	***Validation of Time Delay Compensation***
Test Rationale	*This test aims to validate the developed time delay compensation methods.*
Specific Test System (graphical)	A voltage divider circuit split for simulation in DRTS at two research infrastructures. 
Target measures	*Active power and reactive power at the point of common coupling.*
Input and output parameters	*n/a*
Test Design	*The simulation at either end is started and the two systems synchronized without time delay compensation.* *Voltage and frequency step up and down are emulated to evaluate*

	the accuracy of the time delay compensation method during dynamics. Target metrics are recorded for each event. *The above events are repeated when time delay compensation method is turned on.*
Initial system state	*The system is initialised and synchronized at nominal values of voltage (230 V) and frequency (50 Hz).*
Evolution of system state and test signals	*A positive 23 V (0.1 pu) step is initiated, followed by a negative 23 V step to bring the system back to nominal values. A negative 23V step is initiated followed by a positive step to bring the voltage back to nominal values.* *The frequency is changed from 50 Hz to 51 Hz and is then brought back to nominal value of 50 Hz.* *The frequency is changed from 50 Hz to 49 Hz and is then brought back to 50 Hz*
Other parameters	*All other parameters are kept constant.*
Temporal resolution	*20 kHz, 50 µs.*
Source of uncertainty	*Time of Day.*
Suspension criteria / Stopping criteria	*Suspension – Instability* *Stopping: Successful evolution of system states and recording of target measures.*

Test Specification D2.2

Reference to Test Case	*TC D2*
Title of Test	***Characterization of Time Delay Compensation Methods in Smart Grid Application***
Test Rationale	*This test aims to characterize the performance of the developed time delay compensation methods against the time delay compensation method using GPS. The test is performed within the context of a smart grid application, i.e., inertia provision, to demonstrate the effectiveness of the approaches.*
Specific Test System (graphical)	The reduced model of the Great Britain (GB) power system is utilized. The system is split for simulation in two research infrastructures. Implementation of inertial control: 
Target measures	*Active power and reactive power at the point of common coupling and the frequency of the system.*
Input and output parameters	
Test Design	*The simulation at either end is started and the two systems synchronized without time delay compensation.* *Voltage and frequency step up and down are emulated to evaluate the accuracy of the time delay compensation method during dynamics. Target metrics are recorded for each event.* *The above events are repeated when time delay compensation method is turned on.*
Initial system state	*The system is initialised and synchronized at nominal values of voltage (230 V) and frequency (50 Hz).*
Evolution of system state and test signals	*To initiate a frequency event, a 1GW load is added on to the network to emulate a generator loss.*
Other parameters	*All other parameters are kept constant.*
Temporal resolution	*20 kHz*
Source of uncertainty	*Time of Day* *Size of data packet*

Suspension criteria / Stopping criteria	*Suspension –Instability* *Stopping: Successful evolution of system states and recording of target measures.*

Mapping to Research Infrastructure

i.e. how is it planned to distribute (map) and execute the specified test system in a given research infrastructure (free text); this section can be used to list the intended Experiment specifications.

Experiment Specification ES.D2.1

Reference to Test Specification	*TS D2.1*
Title of Experiment	*Validation of Time Delay Compensation*
Research Infrastructure	DPSL (Strathclyde) and RWTH Aachen?
Experiment Realisation	The subsystem with voltage source and controlled current source is simulated in the DRTS at DPSL and the subsystem with load and controlled voltage source is simulated at RWTH Aachen. The GT-NET cards communicate over the internet (reference case) establishing the performance of the GPS based time delay compensation method.
Experiment Setup (concrete lab equipment)	• DRTS with GT-Sync and GT-NET (x2) cards at each RI • DRTS Host PC at each RI • Mobile units at each RI • GPS clock for time synchronization at each RI
Experimental Design and Justification	*The simulation at either end is started and the two systems synchronized without time delay compensation.* *Voltage and frequency step up and down are emulated to evaluate the accuracy of the time delay compensation method during dynamics. Target metrics are recorded for each event. The above events are repeated when time delay compensation method is turned on.*
Precision of equipment and measurement uncertainty	50 µs time step GPS Time Synchronization
Storage of experiment data	*RSCAD – Various formats*

Experiment Specification ES.D2.2

Reference to Test Specification	*TS D2.2*
Title of Experiment	*Characterization of Time Delay Compensation Methods in Smart Grid Application*
Research Infrastructure	DPSL (Strathclyde) and RWTH Aachen?
Experiment Realisation	The use of the reduced Great Britain Power System is proposed. Three of the 5 areas of the power system will be simulated within DRTS at DPSL with remainder two at RWTH.
Experiment Setup (concrete lab equipment)	• DRTS with GT-Sync and GT-NET (x2) cards at each RI • DRTS Host PC at each RI • Mobile units at each RI • GPS clock for time synchronization at each RI
Experimental Design and Justification	*The simulation at either end is started and the two systems synchronized with GPS based time delay compensation.* *A frequency event is initiated and the target measures are recorded. The above events are repeated for different time delay compensation methods.*
Precision of equipment and measurement uncertainty	50 µs time step GPS Tyme Synchronization
Storage of experiment data	*RSCAD – Various formats.*