Design of MUX

Experiment no. 8   **Date:**

Aim:

To design and implement multiplexer using logic gates.

SOFTWARE REQUIRED: LTspice software

THEORY:

MULTIPLEXER:

Multiplexer doe the function of transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2n input line and n selection lines whose bit combination determine which input is selected.
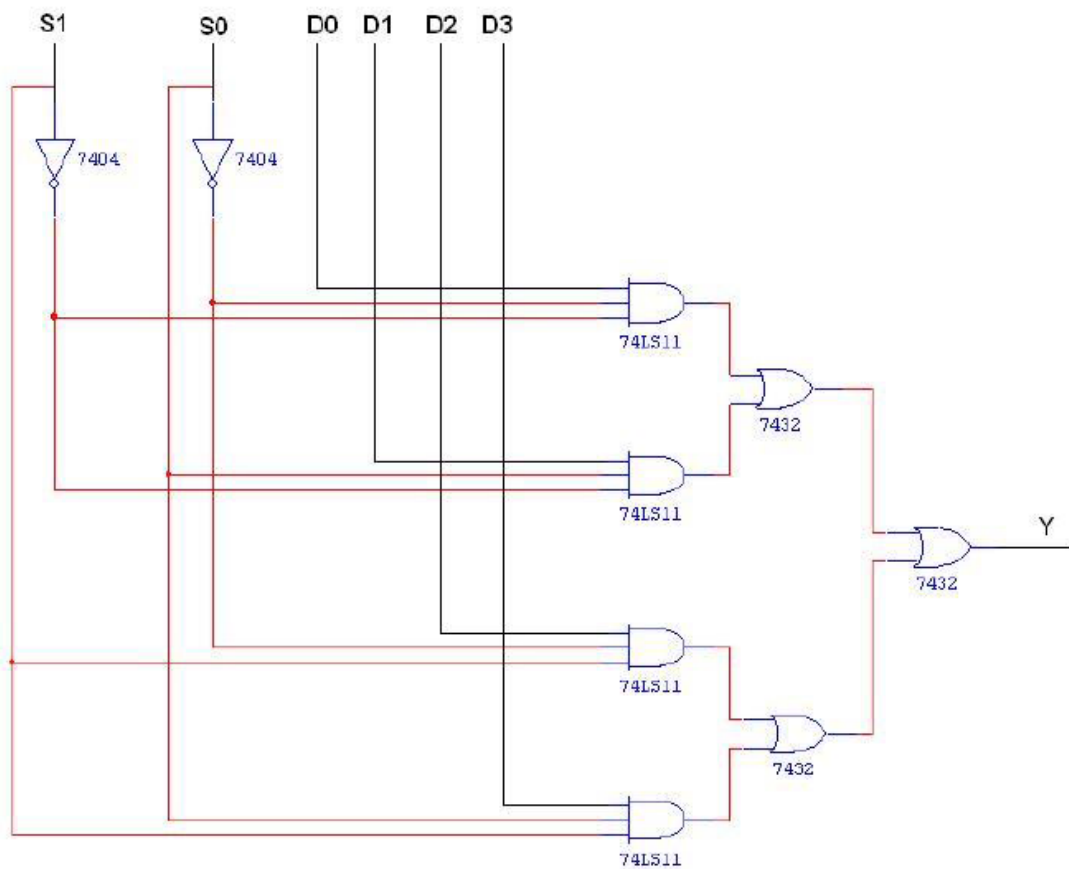
BLOCK DIAGRAM FOR 4:1 MULTIPLEXER
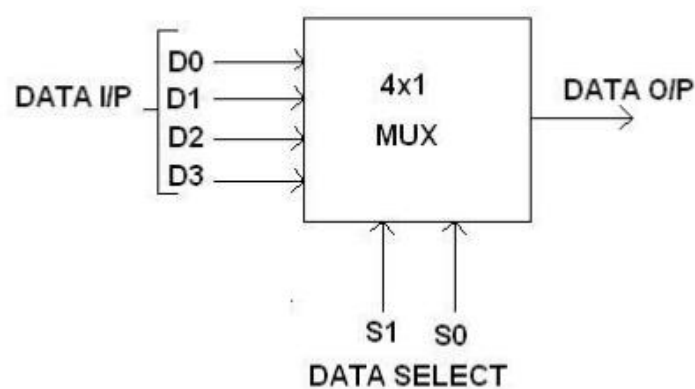
FUNCTION TABLE:

S1	S0	INPUTS Y
0	0	D0 → D0 S1' S0'
0	1	D1 → D1 S1' S0
1	0	D2 → D2 S1 S0'
1	1	D3 → D3 S1 S0

$$Y = D0\ S1'\ S0' + D1\ S1'\ S0 + D2\ S1\ S0' + D3\ S1\ S0$$

CIRCUIT DIAGRAM FOR MULTIPLEXER:

TRUTH TABLE

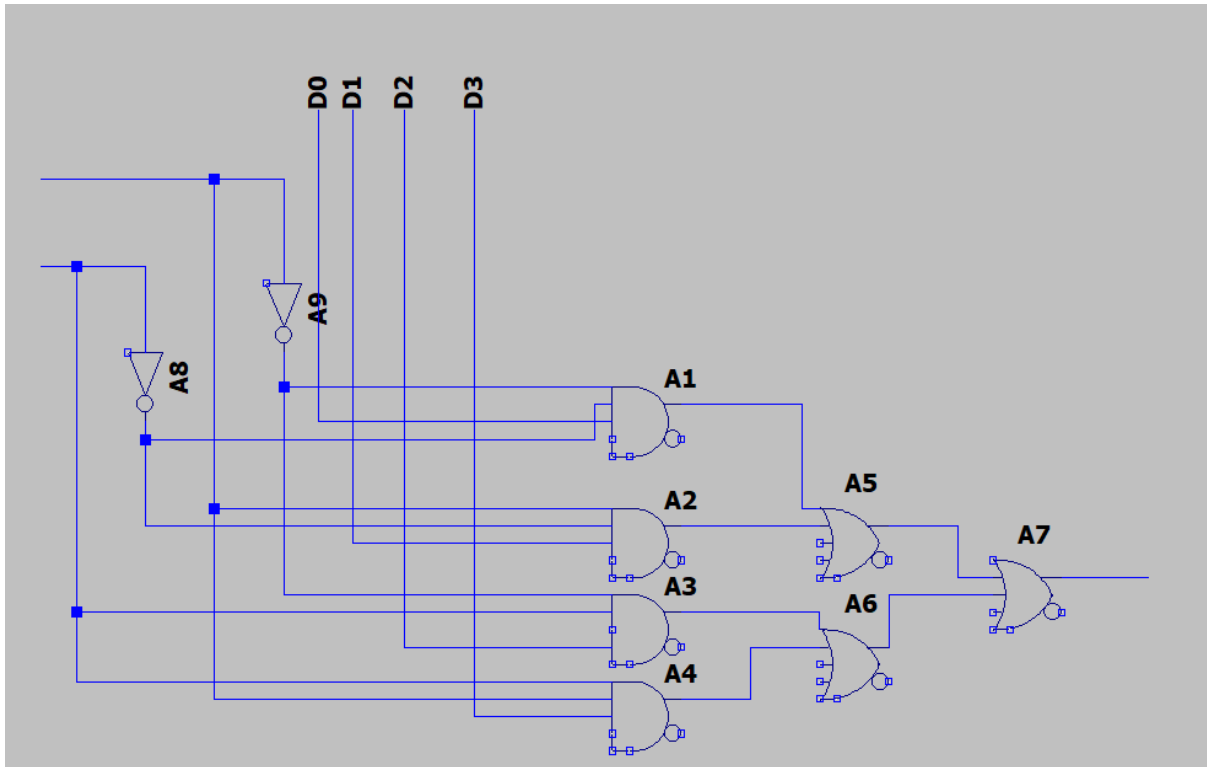| S1	S0	Y = OUTPUT
0	0	D0
0	1	D1
1	0	D2
1	1	D3

SIMULATION PROCEDURE:
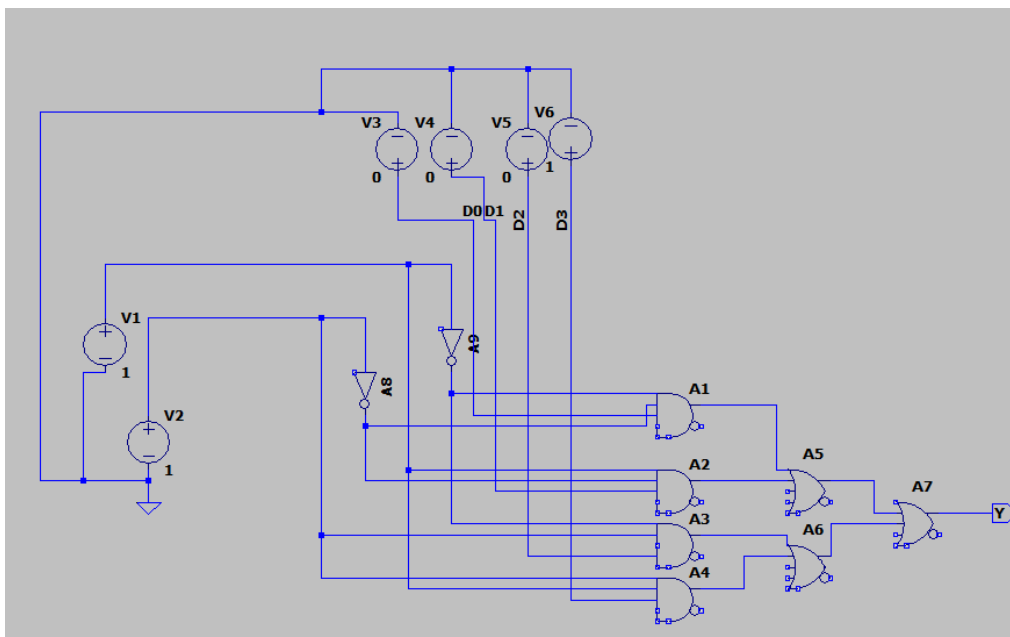
1. Open LTspice. Go to File⌐ New Schematic.
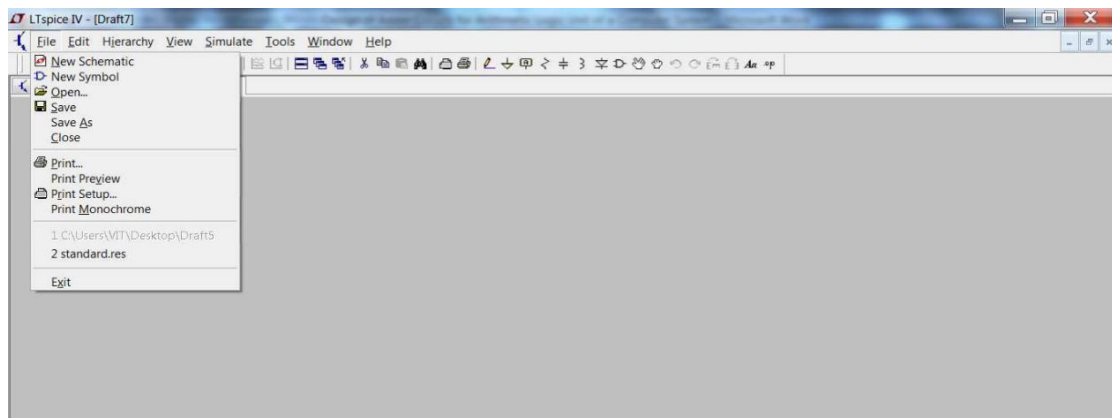
2. On the File Menu, click on Edit⌐ Component.
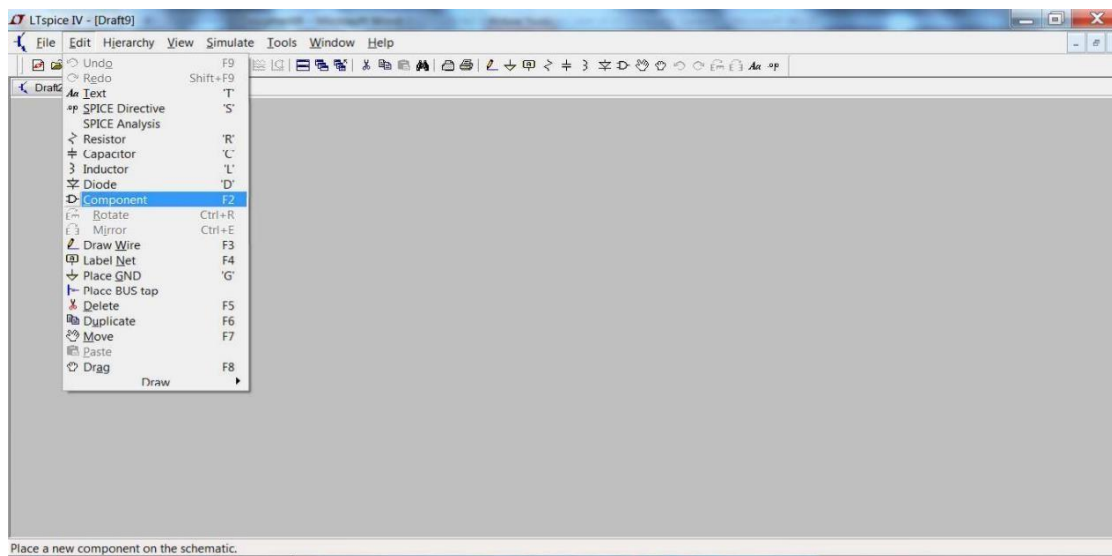
3. **a. For Multiplexer**: Place the voltage sources, NOT gate, AND gate, and OR gate on to schematic and make necessary connections as shown in the Figure.


4.a. Connect the voltage sources as shown Figure for multiplexer.

5.**For Multiplexer**:
Right click on the voltage sources V6 and then Enter DC Value 1 and then click OK option.
Right click on the voltage sources V5 and then Enter DC Value 0 and then click OK option.
Right click on the voltage sources V4 and then Enter DC Value 0 and then click OK option.
Right click on the voltage sources V3 and then Enter DC Value 0 and then click OK option.
Right click on the voltage sources V2 and then Enter DC Value 1 and then click OK option.
Right click on the voltage sources V1 and then Enter DC Value 1 and then click OK option
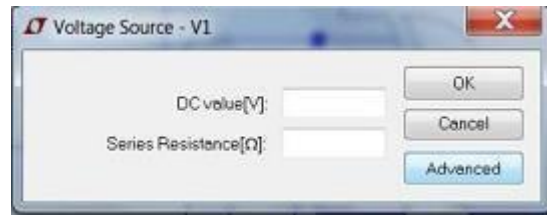
6. Go to Edit → SPICE analysis.

For both Decoder and Encoder: Select "DC op pnt" tab and Click "OK" and Press run symbol on menu bar.
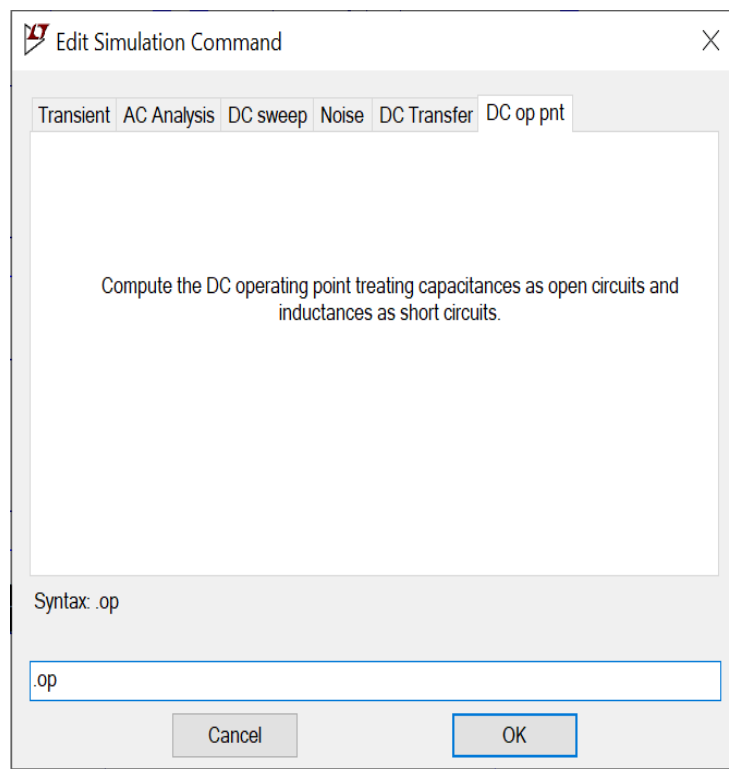
Result for Multiplexer:

```
* C:\Users\gkani\Documents\LTspiceXVII\Draft11.asc

      --- Operating Point ---

V(n003):        0              voltage
V(n004):        0              voltage
V(d0):          0              voltage
V(n005):        0              voltage
V(n001):        1              voltage
V(d1):          0              voltage
V(n006):        0              voltage
V(n002):        1              voltage
V(d2):          0              voltage
V(n009):        0              voltage
V(d3):          1              voltage
V(n010):        1              voltage
V(n007):        0              voltage
V(n008):        1              voltage
V(y):           1              voltage
I(V4):          0              device_current
I(V6):          0              device_current
I(V5):          0              device_current
I(V3):          0              device_current
I(V2):          0              device_current
I(V1):          0              device_current
I8(A9):        -0              device_current
I6(A9):         0              device_current
I8(A8):        -0              device_current
I6(A8):         0              device_current
I8(A7):        -0              device_current
I7(A7):         0              device_current
I8(A6):        -0              device_current
```

Result

Thus, the multiplexer was implemented and verified using logic gates in LT spice software.