Expt. No. 6	Design and Implementation of Magnitude Comparator, Parity Generator & Checker

AIM:

(a). Design a control unit for a sea salt packing machine to pack a salt bag of 2kg each. Current weight of the bag is measured and represented in 2-bit binary number then compared with the reference value. If the salt bag is less/greater than 2kg control signal generated to add/remove excess salt to/from salt bag. If the salt bag weight is exactly 2kg then control signal generated to make a pack. Design and Implement an appropriate digital circuit using basic logic gates to meet this requirement. (Hint: 2-Bit Magnitude comparator)

(b). Bluetooth module is interfaced with Arduino Uno board and transmitting its 4-bit data continuously to the receiver section. This 4-bit data comprises of 3-bit temperature sensor data and 1-bit for parity (even). Since this system operating under a noisy environment, there is a possibility of error prone into the actual values of transmitting data. Design a suitable combinational logic circuit in the transmitter and receiver section to detect the data is valid or not. (Hint: Parity or and Checker)

COMPONENTS REQUIRED:

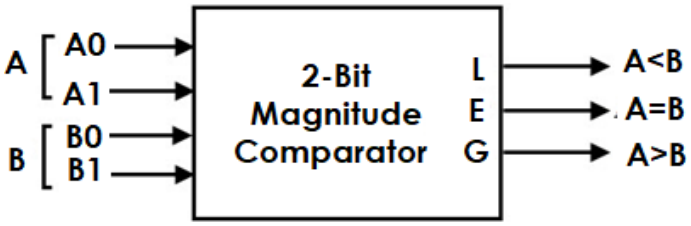
S. No.	COMPONENT	SPECIFICATION	QUANTITY
1.	2-INPUT AND GATE	IC 7408	2
2.	2-INPUT OR GATE	IC 7432	1
3.	1-INPUT NOT GATE	IC 7404	1
4.	2-INPUT XOR GATE	IC7486	1
5.	DIGITAL TRAINER KIT	-	1
6.	Connecting wires	-	few

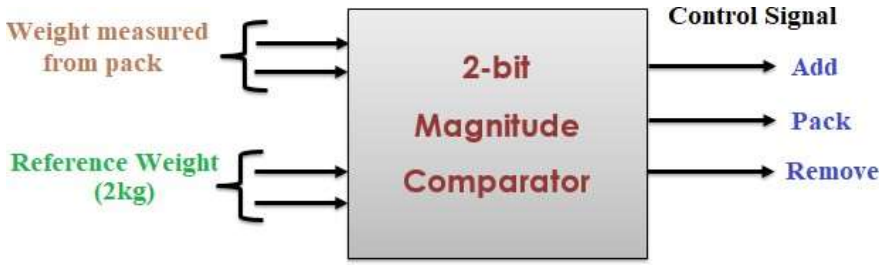
(a). 2-BIT MAGNITUDE COMPARATOR:

THEORY:

Data comparison is needed in digital systems while performing arithmetic or logical operations. The purpose of a Digital Comparator is to compare a set of variables or unknown numbers, for example A (A1, A2, A3, …An, etc) against that of a constant or unknown value such as B (B1, B2, B3, …. Bn, etc) and produce an output condition or flag depending upon the result of the comparison. A Magnitude Comparator is a digital comparator which has three output terminals, one each for equality, A = B greater than, A > B and less than A < B. A 2-bit comparator compares two binary numbers, each of two bits and produces their relation such as one number is equal or greater than or less than the other. The first number A is designated as A = A1A0 and the second number is designated as B = B1B0. This comparator produces three outputs as G (G = 1 if A>B), E (E = 1, if A = B) and L (L = 1 if A<B).

BLOCK DIAGRAM:

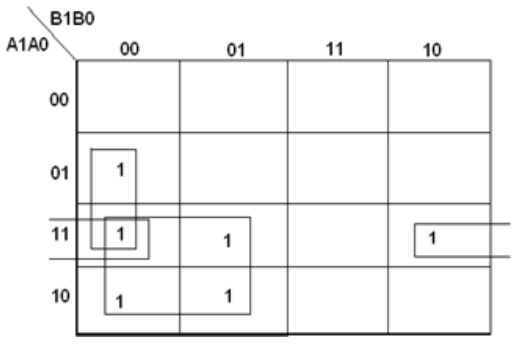




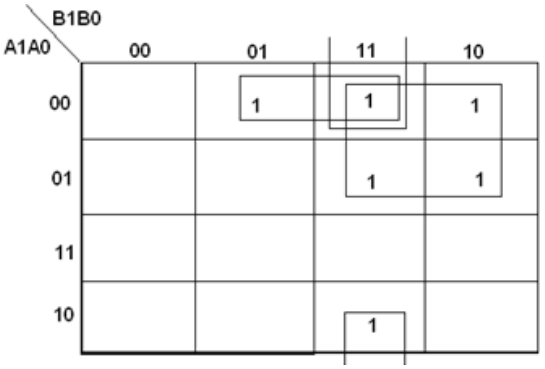
TRUTH TABLE:

INPUTS				OUTPUT		
A1	**A0**	**B1**	**B0**	**A>B**	**A=B**	**A<B**
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

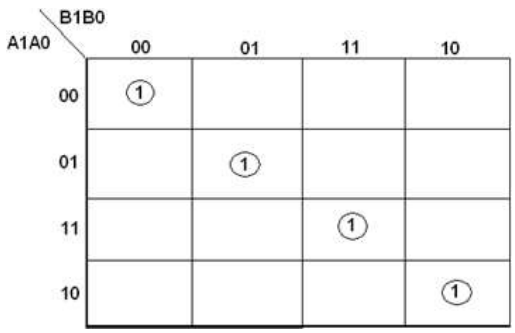
K-MAP:



A>B = A1B1′ + A0B1′B0′ + A1A0B0′



A<B = A1′B1 + A0′B1B0 + A1′A0′B0



A=B = A1′A0′B1′B0′ + A1′A0B1′B0 + A1A0B1B0 + A1A0′B1B0′

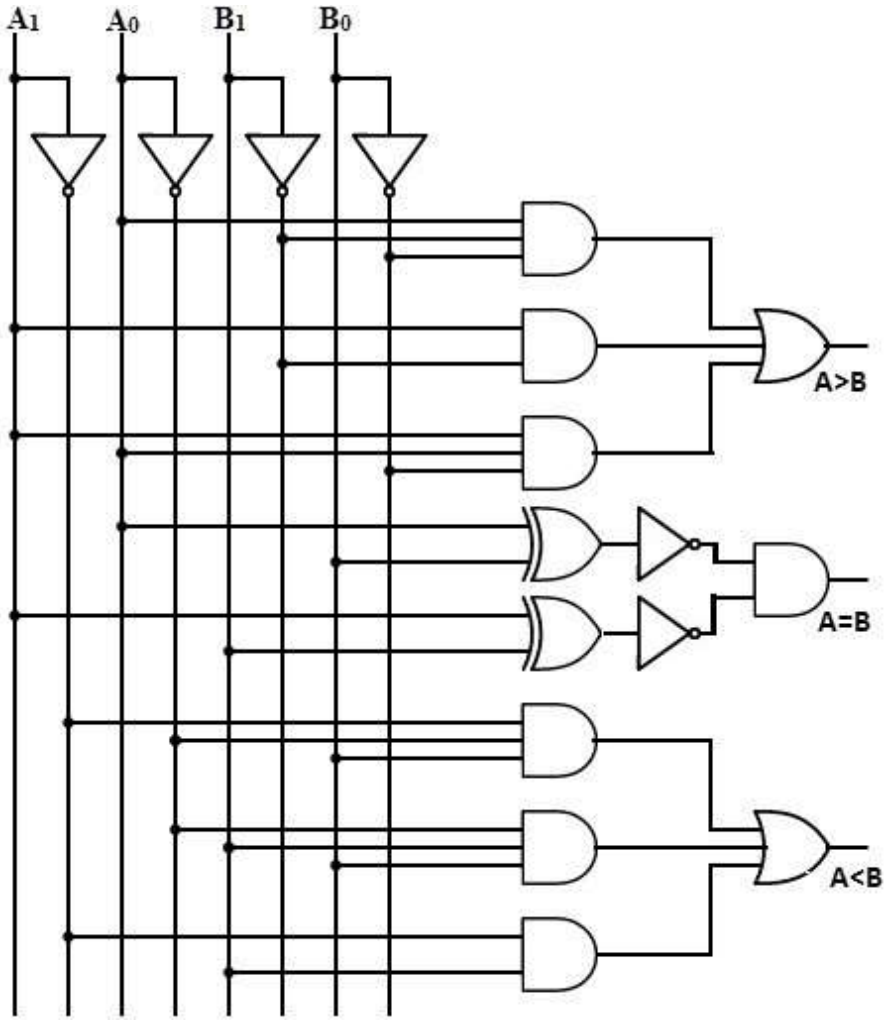
= A1′B1′ (A0′B0′ + A0B0) + A1B1 (A0B0 + A0′B0′)

= (A0B0 + A0′B0′) (A1B1 + A1′B1′)

= (A0 ⊖ B0) (A1 ⊖ B1)

A=B = (A0 ⊕ B0)′ (A1 ⊕ B1)′

LOGIC DIAGRAM:



(b). PARITY (EVEN) GENERATOR & CHECKER:

THEORY:

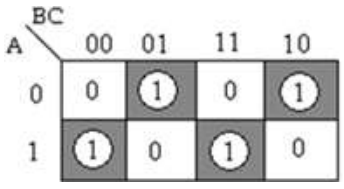
A Parity is a very useful tool in information processing in digital computers to indicate any presence of error in bit information. External noise and loss of signal strength causes loss of data bit information while transporting data from one device to other device, located inside the computer or externally. To indicate any occurrence of error, an extra bit is included with the message according to the total number of 1s in a set of data, which is called parity. If the extra bit is considered 0 if the total number of 1s is even and 1 for odd quantities of 1s in a set of data, then it is called even parity. On the other hand, if the extra bit is 1 for even quantities of 1s and 0 for an odd number of 1s, then it is called odd parity. The message including the parity is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not correspond with the one transmitted. The circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called a parity checker. The message bits with the parity bit are transmitted to their destination, where they are applied to a parity checker circuit. The parity checker circuit produces a check bit and is very similar to the parity generator circuit. If the check bit is 1, then it is assumed that the received data is incorrect. The check bit will be 0 if the received data is correct.

3- BIT EVEN PARITY GENERATOR:

TRUTH TABLE:

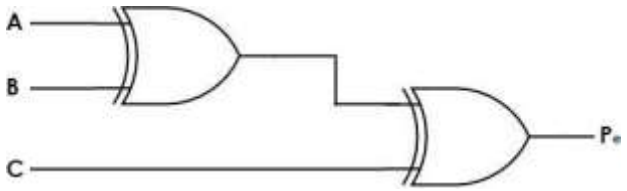
3-BIT MESSAGE INPUT			EVEN PARITY BIT
A	B	C	P_e
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

K-MAP:



$$P_e = A'B'C + A'BC' + A'B'C' + ABC$$
$$= A'(B'C + BC') + A(B'C' + BC)$$
$$= A'(B \oplus C) + A(B \oplus C)'$$
$$P_e = (A \oplus B \oplus C)$$

LOGIC DIAGRAM:

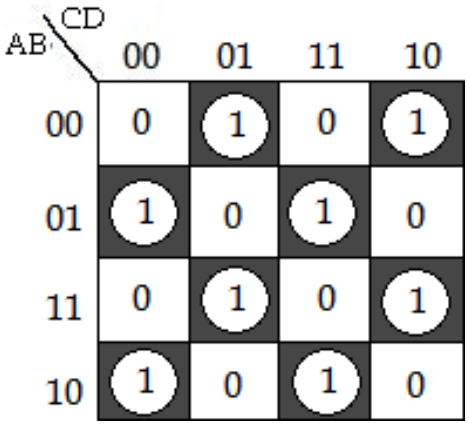


4- BIT EVEN PARITY CHECKER:

TRUTH TABLE:

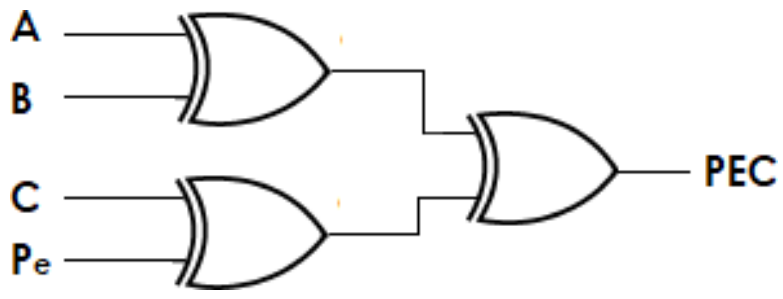
4-BIT RECEIVED MESSAGE				PARITY ERROR CHECK (PEC)
A	B	C	P_e	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

K-MAP:



PEC = A'B' (C'D+ CD') + A'B (C'D'+ CD) + AB (C'D+ CD') + AB' (C'D'+ CD)
= A'B' (C ⊕ D) + A'B (C ⊕ D)' + AB (C ⊕ D) + AB' (C ⊕ D)'
= (A'B'+ AB) (C ⊕ D) + (A'B+ AB') (C ⊕ D)'
= (A ⊕ B)' (C ⊕ D) + (A ⊕ B) (C ⊕ D)'
PEC = (A ⊕ B) ⊕ (C ⊕ D)

LOGIC DIAGRAM:



PROCEDURE:

1. Place the IC on IC trainer kit
2. Connect the Vcc and ground to respective pins of IC trainer kit
3. Connections are given as per logic diagram.
4. Connect the inputs to the input switches provided in the IC trainer kit
5. Connect the outputs to the switches of output LED's
6. Apply various combinations of input according to the truth table
7. Observe the condition of output LED's and verify the truth table

RESULT:

Thus combinational logic circuits such as 2-bit magnitude comparator, 3-bit even parity checker and 4-bit even parity checker are constructed using basic logic gates and their truth tables are verified.

VIVA QUESTIONS WITH ANSWERS:

1. **What is the difference between identity comparator and magnitude comparator?** Identity Comparator is a digital comparator with only one output terminal for when A = B, either A = B = 1 (HIGH) or A = B = 0 (LOW). Magnitude Comparator is a digital comparator which has three output terminals, one each for equality, A = B greater than, A > B and less than A < B.
2. **Magnitude comparator always produces only output (s) as HIGH among itspossible_number of outputs.**
   1, 3
3. **Number of inputs required for magnitude comparator is?**
   Two inputs are required to perform comparison operation by magnitudecomparator
4. **Which combination of logic gates are ideal realizing "equal" condition in 2-bit magnitude comparator?**
   XNOR, AND
5. **State atleast 2 application of Magnitude comparator**
   - In CPU and microcontrollers
   - Used in password verification and biometric applications
6. **What is a parity bit?**
   A simple form of error detection is achieved by adding an extra bit to thetransmitted word. The additional bit is known as parity bits.
7. **The even parity output of binary number (1101010111) is?**
   1
8. **Which logic gate is most appropriate to modify the even parity generator logiccircuit into odd parity generator logic circuit?**
   Adding NOT gate at the output end of even parity generator
9. **State main drawback of parity checker based error detection method.**
   Parity checker is capable of identifying only one bit change. If there is more thanone bit change on the message signal, then it can't be detected by parity checker
10. **List atleast three application of Parity Checker / Generator.**
    - SCSI and PCI buses use parity to detect transmission errors
    - many microprocessor instruction caches include parity protection
    - In serial communication contexts, parity is usually generated and checkedby interface hardware (e.g., a UART)