Design of Half Adder circuit for Arithmetic Logic Unit of a Computer System

Experiment no.

Date:

Aim:

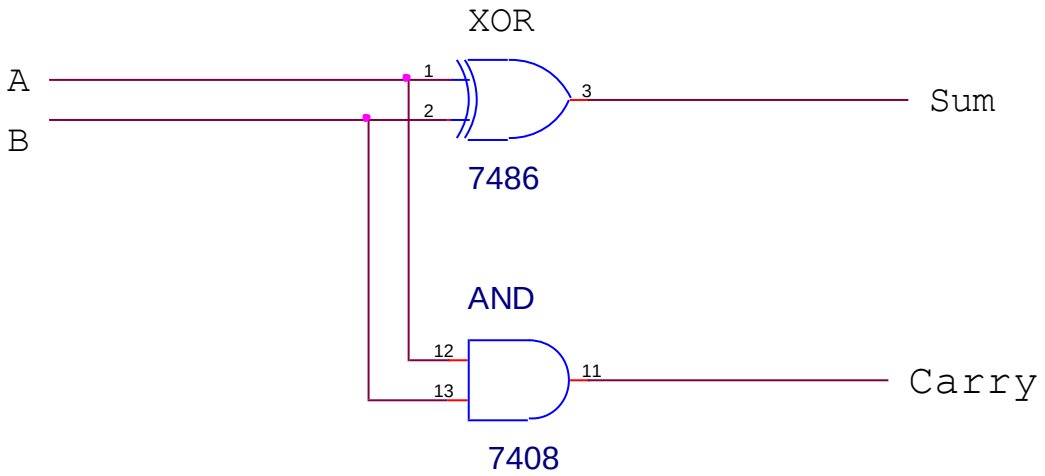
1) An arithmetic circuit has two selection signals, S_0 and S_1. After addition of the two signals, Sum 'S' and Carry 'C' are generated. Design a half adder circuit to implement the addition operation using Exclusive-OR and AND gates.

Apparatus Required:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	AND GATE	IC 7408	1
2.	X-OR GATE	IC 7486	1
3.	IC TRAINER KIT	-	1
4.	PATCH CORDS	-	

Circuit Diagram:

Half Adder using EX-OR and AND logic gates



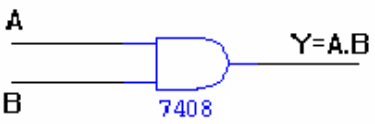
Formulae:

Half Adder

$$\text{SUM} = \bar{A}B + A\bar{B}$$
$$\text{CARRY} = AB$$

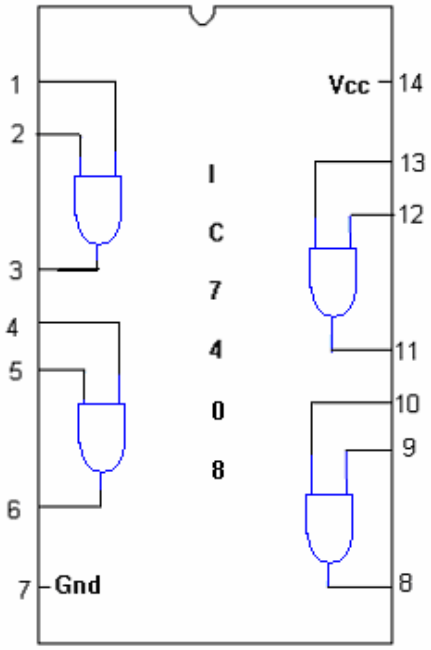
AND GATE:

SYMBOL: **PIN DIAGRAM:**



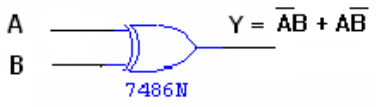
TRUTH TABLE

A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1



X-OR GATE :

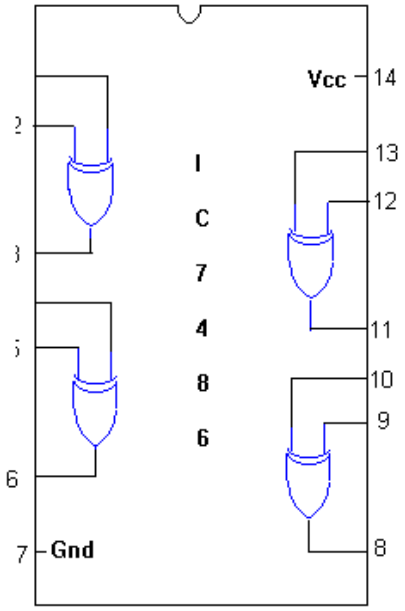
SYMBOL :



TRUTH TABLE :

A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

PIN DIAGRAM :



Theory:

Adders form a core component of the Arithmetic Logic Unit (ALU) and play a major role in calculating memory addresses, table indices etc.

A half adder is the simplest digital adder. It is combinational circuit that performs addition of two binary digits. It takes in two input bits, A (addend) and B (augend) and produces two output bits, the sum and the carry. A half adder lacks provision for carries from preceding bits.
The truth table for adding two binary digits A and B is shown below:

Truth Table for Half Adder

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Procedure:

1. Give the connections as per the logic diagram for half adder.
2. Use RPS to provide necessary input signals (High (5 V) or Low (0 V)).
3. Connect a LED across the output terminals (Sum and Ground or Carry and Ground).
4. Check the output (LED: either ON or OFF) for various combinations of input from the truth table.

Observation:

Verify the truth table for Half Adder Circuits using the output obtained at terminals Sum and Carry

Result

Thus, a half adder circuit to implement addition operation and ALU circuit with a 1-bit is designed, implemented and verified.

Design of Full Adder circuit for Arithmetic Logic Unit of a Computer System

Experiment no.2
Date:

Aim:

To design a full adder circuit and verify the same for the given problem statement.

Problem Statement:

1. An arithmetic circuit has two input signals A, B and a third carry-in bit C_{in}. The circuit is required to output the Sum 'S' and carry-out bit 'C_{out}'. Design the ALU circuit with a 1-bit full adder using Exclusive-OR, OR and AND gates.

Software Required: LTspice software

Theory:

The Full adder takes in three input bits, an addend (A), an augend (B) and carry input (C_{in}) generated by the previous stage addition. It has two outputs, sum (S) and carry out (C_{out}). The truth table for full adder is shown below:

Truth Table for Full Adder

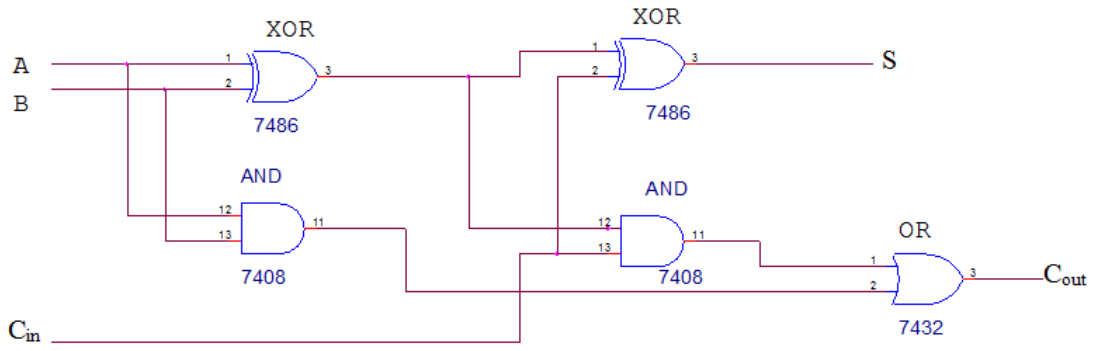
C_{in}	A	B	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The simplified Boolean functions from the truth table are:

$$S = A \oplus B \oplus C$$
$$Carry = (A \oplus B)C + AB$$

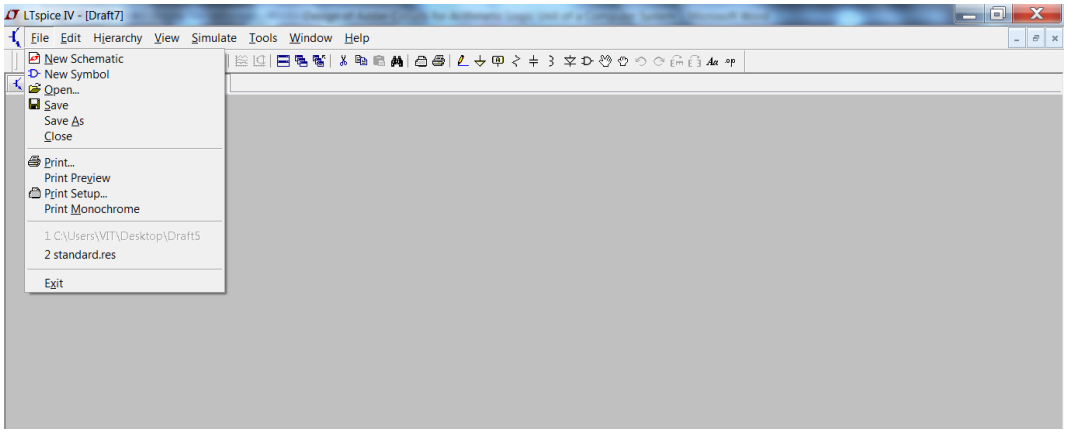
The boolean expressions can be implemented in different ways. Below example shows the implementation of Full Adder using EX-OR, AND and OR logic gates.

Implementation of Full Adder using EX-OR, OR and AND logic gates

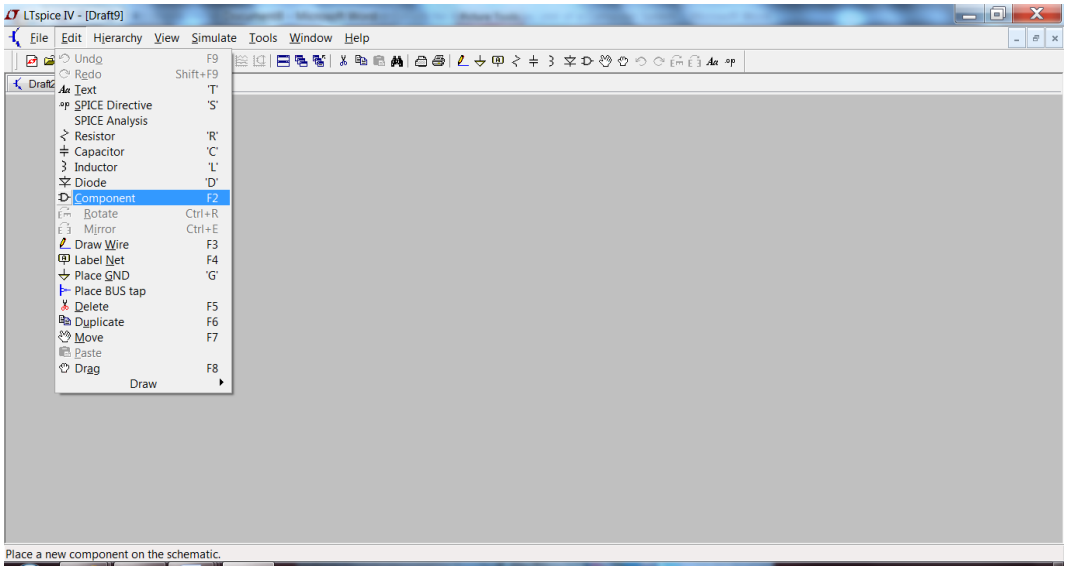


Procedure for Simulation:

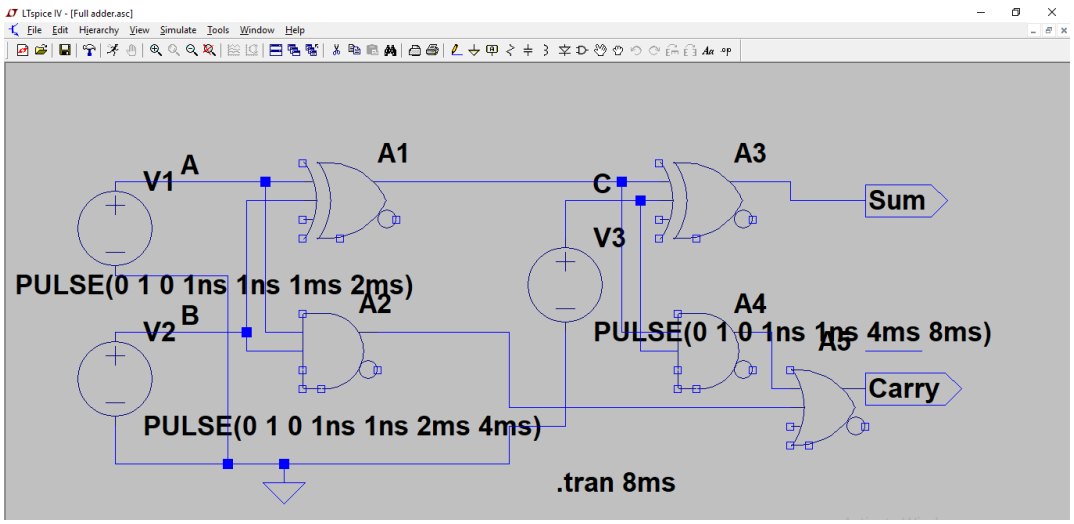
1. Open LTspice. Go to File – New Schematic.



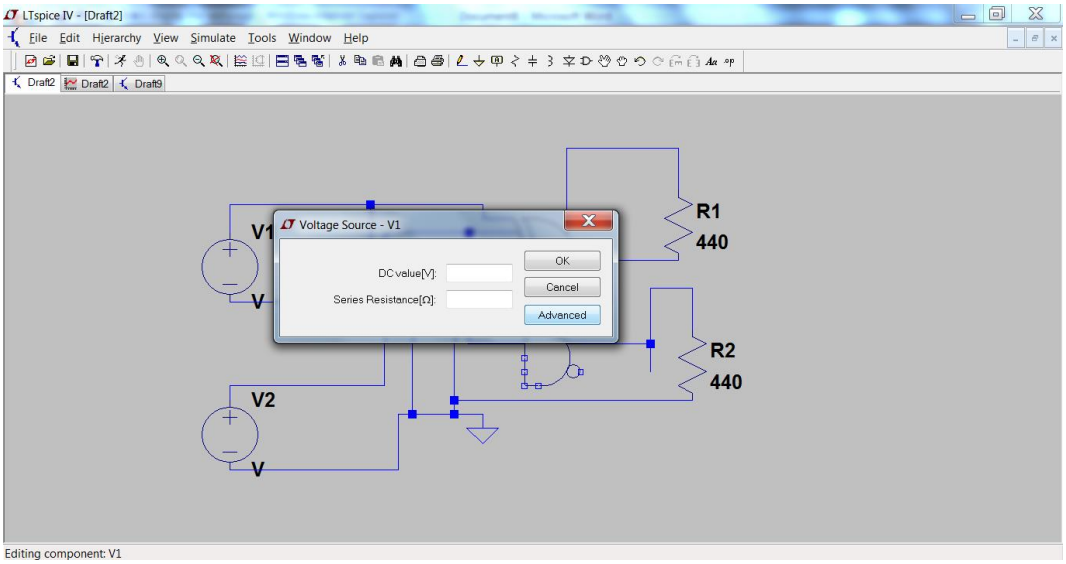
2. On the File Menu, click on Edit – Component.

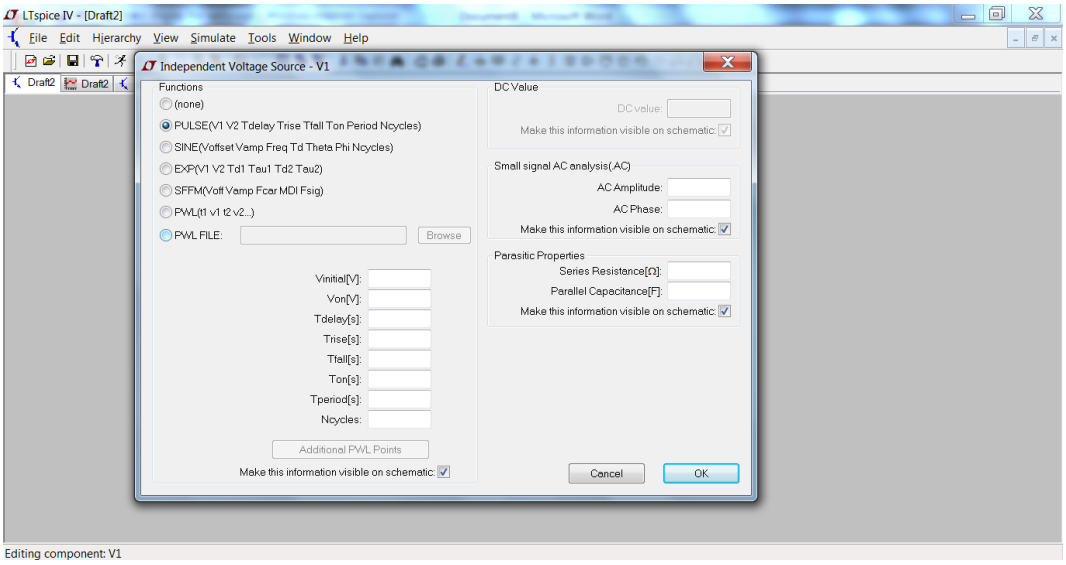


3. Place the voltage sources, XOR gate, AND gate, OR gate and ground on to schematic and make necessary connections as shown in the Figure.

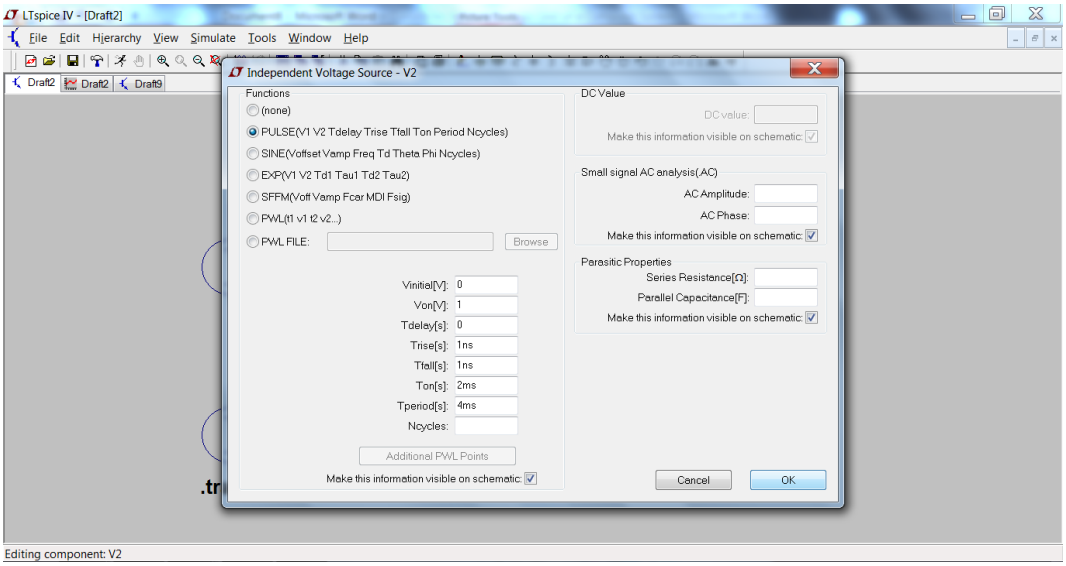


4. As shown in the figures below, Right click on the voltage sources and click Advanced option and then Select PULSE (V1 V2 Tdelay Trise Tfall Ton Period Ncycles).



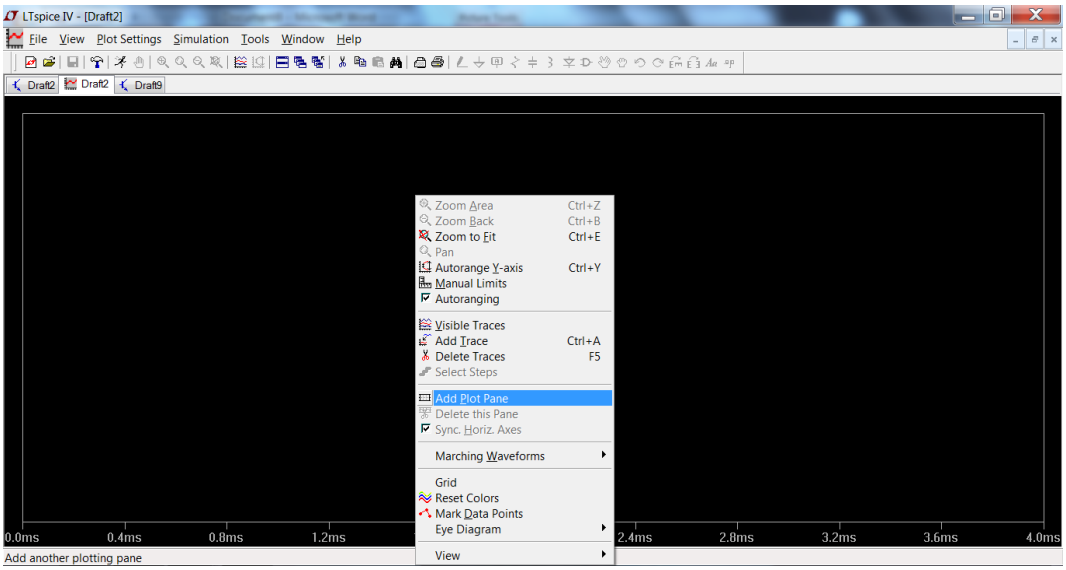


5. Set the values as (0, 1, 0, 1ns, 1ns, 1ms, 2 ms) for A, (0, 1, 0, 1ns, 1ns, 2ms, 4 ms) for B, as (0, 1, 0, 1ns, 1ns, 4 ms, 8 ms) for C

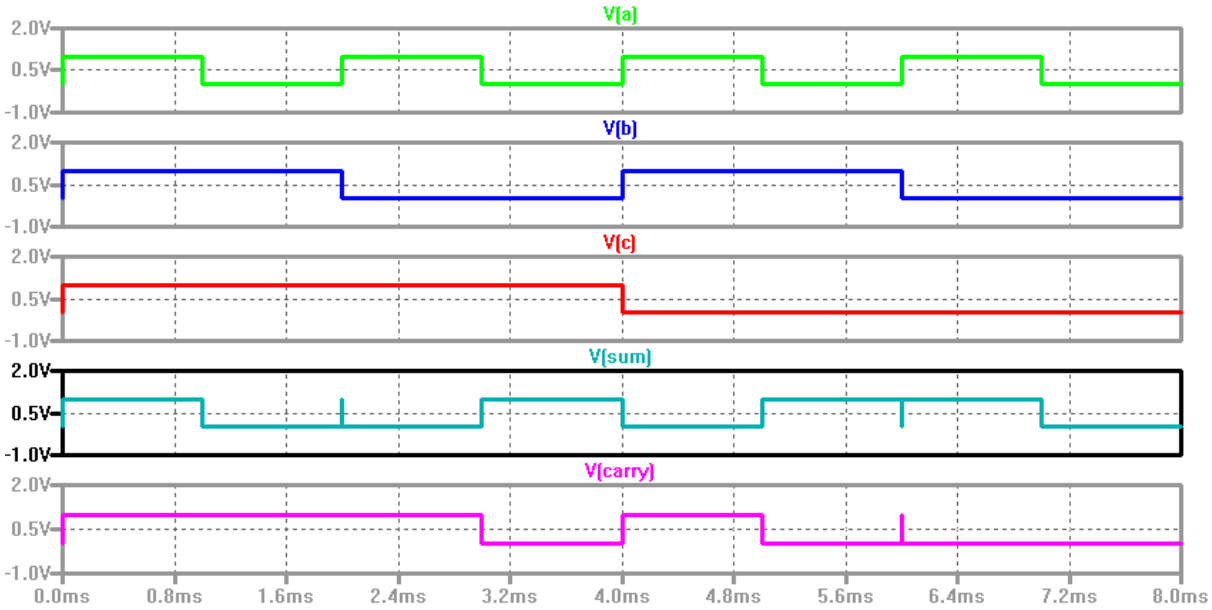


6. Go to Edit – SPICE analysis. Set the stop time to 8 ms in Transient command and run the simulation (run symbol on menu bar).

7. To view the results, right click – Add Plot Pane (add 5 plot panes to view the three inputs, sum and carry). For each pane, right click – Add Trace – Select V (<<respective node>>). (nodes correspond to input 1, input 2, input 3, sum and carry)



8. Observe the waveforms and verify the truth table.



Result:

Thus, an ALU circuit with a 1-bit full adder is designed, implemented and verified.