Expt. No.10	Design and Implementation of 4-Bit Shift Registers (SISO, SIPO, PIPO)

AIM:

(a). In modern computer system, it is essential to operating the computing unit in optimized manner. Especially, shift registers are extensively used to perform optimized binary multiplication and division. This is due to the fact that the shift of data bit by one position towards right causes the number to be divided by 2 while the left-shift of the data bit by one place in the shift register multiplies the number by 2. For example, consider a 4-bit shift register with the content 0110, which is equal to 6 in decimal. If the number shifts left by one-bit, then one gets 1100, which is 12 (= 6 × 2) in decimal. Similarly is the number shifts towards right by one bit, then the register contents will become 0011, which is nothing but 3 (=6/2) in decimal. Design and implement the suitable 4-bit shift register logic circuit for the given requirement using appropriate flip flop.(Hint: SISO)

(b). In general, many microprocessors/microcontrollers handle data as bytes (8 bits) or words (16 bit, 32 bit) as a preferred format. However, many external interfacing device prefer to operate on serial format instead of parallel. Whenever any external serial device communicate with microprocessor/microcontrollers, there should be a serial-to-parallel converter unit to convert the serial data into parallel data. Design and implement the suitable 4-bit serial to parallel converter logic circuit for the given requirement using appropriate flip-flop. (Hint: SIPO)

(c). A free-running analog-to-digital converter is one that updates its digital output(for the given analog signal) as often as it can, not waiting for any prompting from another device. If we were to connect a free-running ADC to a computer (microprocessor or microcontroller), we would need some way to sample the ADC's output at times specified by the computer, and hold that binary number long enough for the computer to register it. Otherwise, the ADC may update its output in the middle of one of the computer's "input" cycles, possibly resulting in corrupted data. We could build such a sample-and-hold circuit out of flip-flops, which could shift register inputs multiple bits of data all at once, and transfers that data to its output lines all at once, at the command of a clock pulse. Design and implement the suitable 4-bit shift register to serve for the sample and hold circuit requirement using appropriate flip-flop. (Hint: PIPO)

COMPONENTS REQUIRED:

S. No.	COMPONENT	SPECIFICATION	QUANTITY
1.	D-FLIP FLOP	IC7474	2
2.	DIGITAL TRAINER KIT	-	1
3.	Connecting wires	-	few

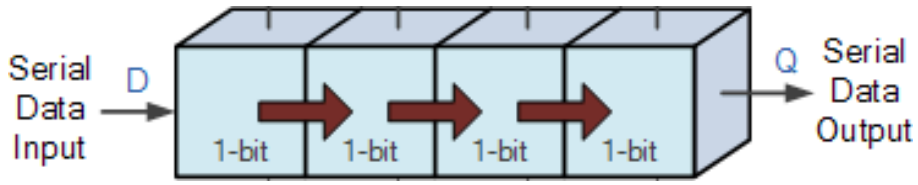
(a). SERIAL-IN SERIAL-OUT (SISO):

THEORY:

Shift Registers are sequential logic circuits, capable of storage and transfer of data. Shift Register is a group of flip flops used to store multiple bits of data. Shift registers are basically a type of register which have the ability to transfer ("shift") data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses. An n-bit shift register can be formed by connecting n flip-flops where each flip flop stores a single bit of data. Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format.

The shift register, which allows serial input (one bit per clock cycle) and produces a serial output is known as Serial-In Serial-Out shift register. In this shift register, we can send the bits serially from the input of left most D flip-flop. Hence, this input is also called as serial input. For every positive edge triggering of clock signal, the data shifts from one stage to the next. So, we can receive the bits serially from the output of right most D flip-flop. Hence, this output is also called as serial output. The circuit consists of four D flip-flops which are connected in a serial manner. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop. This type of Shift Register also acts as a temporary storage device or it can act as a time delay device for the data, with the amount of time delay being controlled by the number of stages in the register, 4, 8, 16 etc., or by varying the application of the clock pulses.

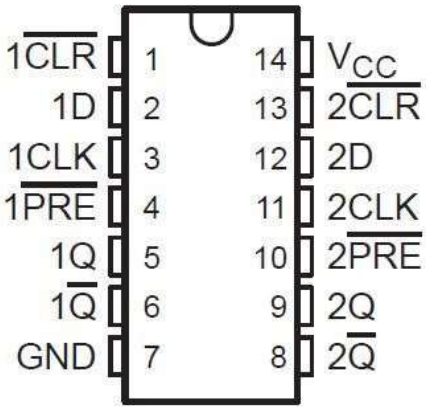
BLOCK DIAGRAM:



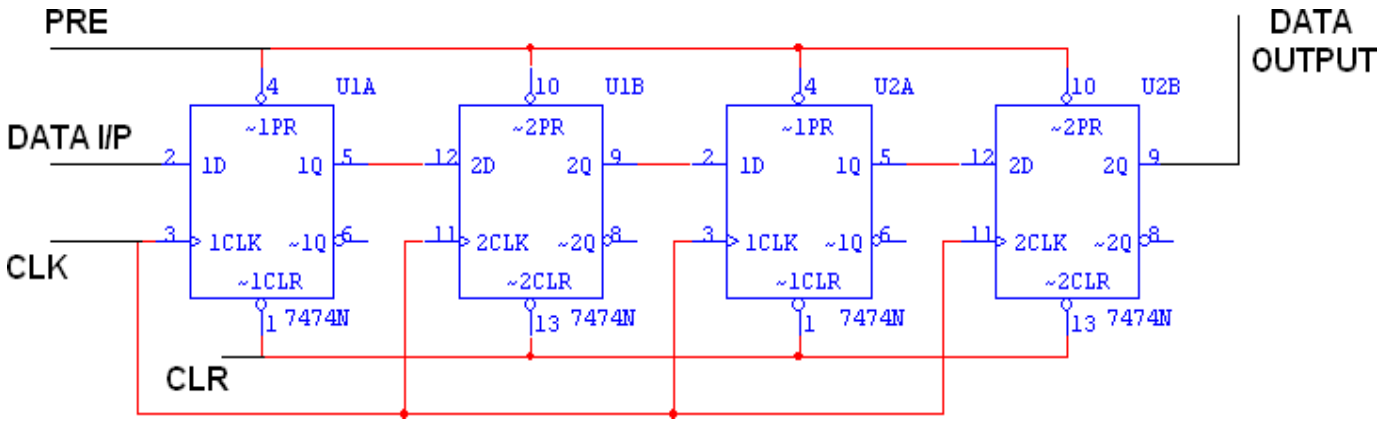
TRUTH TABLE:

CLOCK PULSE NO.	SERIAL DATA INPUT (D)	EACH FLIP FLOP STATE AT Q				SERIAL DATA OUTPUT (Q)
		Q3	Q2	Q1	Q0	
0	0	0	0	0	0	0
1	1	1	0	0	0	0
2	1	1	1	0	0	0
3	0	0	1	1	0	0
4	1	1	0	1	1	1
5	0	0	1	0	1	1
6	0	0	0	1	0	0
7	0	0	0	0	1	1
8	0	0	0	0	0	0

IC7474 PIN DIAGRAM:



LOGIC DIAGRAM:

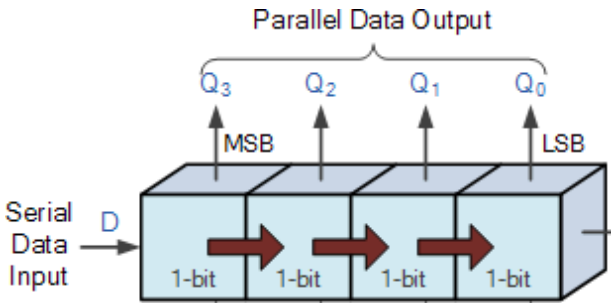


(b). SERIAL-IN PARALLEL-OUT (SIPO):

THEORY:

In the serial in-parallel out shift register, the data is input serially one bit at a time and output in a parallel form. The effect of each clock pulse is to shift the data contents of each stage one place to the right. This data value can now be read directly from the outputs of Q0 to Q3. This means when the data is read in, each read in bit becomes available simultaneously on their respective output line. Then the data has been converted from a serial data input signal to a parallel data output. They are used in communication lines where demultiplexing of a data line into several parallel lines is required because the main use of SIPO register is to convert serial data into parallel data.

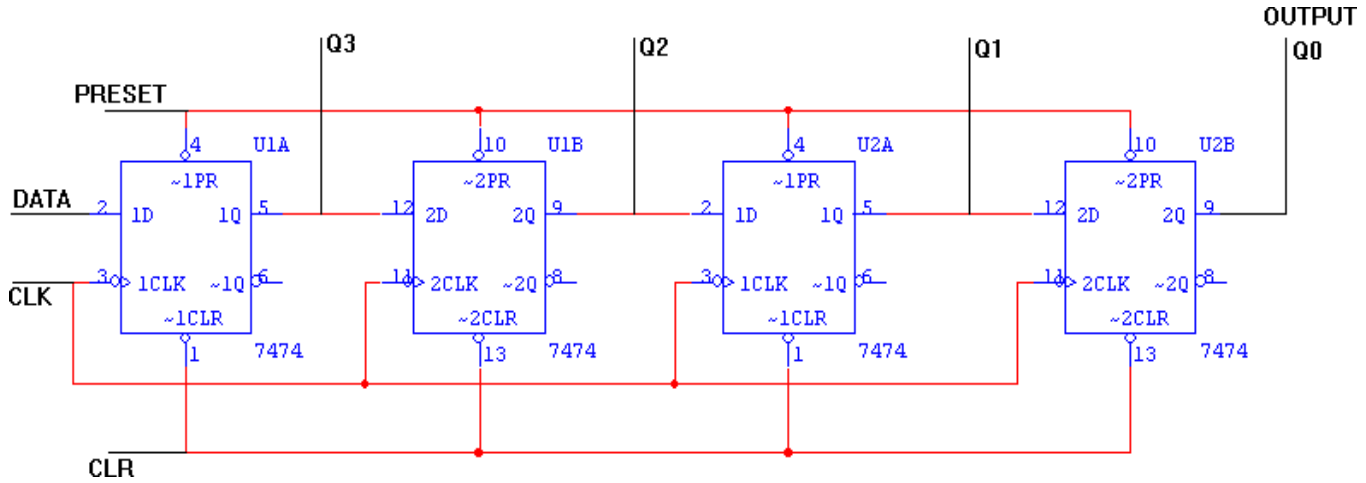
BLOCK DIAGRAM:



TRUTH TABLE:

CLOCK PULSE NO.	SERIAL DATA INPUT (D)	PARALLEL DATA OUTPUT			
		Q3	Q2	Q1	Q0
0	0	0	0	0	0
1	1	1	0	0	0
2	1	1	1	0	0
3	0	0	1	1	0
4	1	1	0	1	1
5	0	0	1	0	1
6	0	0	0	1	0
7	0	0	0	0	1
8	0	0	0	0	0

LOGIC DIAGRAM:

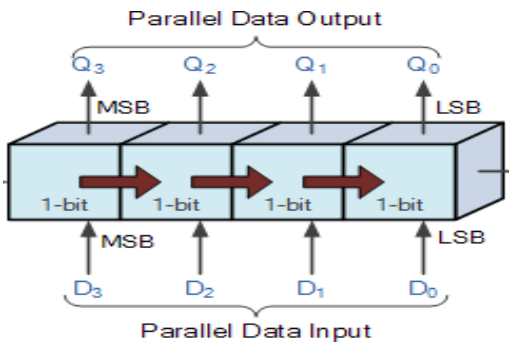


(c). PARALLEL-IN PARALLEL-OUT (PIPO):

THEORY:

The parallel-in parallel-out shift register receives the data input in parallel batches on every clock pulse and the data is shifted and output in parallel. In this type of register, there are no interconnections between the individual flip-flops since no serial shifting of the data is required. Data is given as input separately for each flip-flop and in the same way, output also collected individually from each flip-flop. The data is presented in a parallel format to the parallel input pins D0 to D3 and then transferred together directlyto their respective output pins Q0 to Q3 by the same clock pulse. This type of shift registeralso acts as a temporary storage device or as a time delay device similar to the SISO.

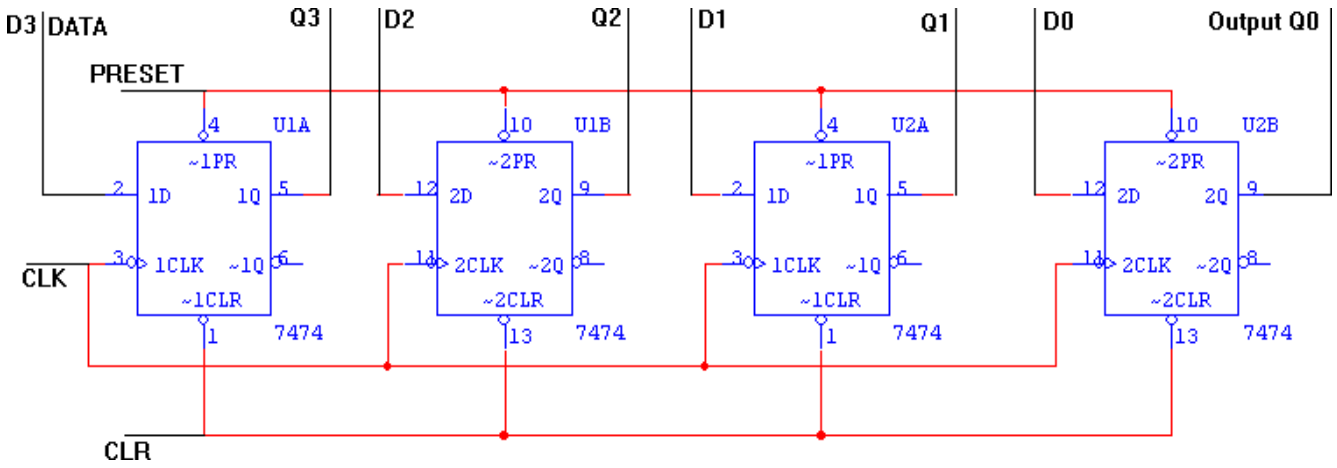
BLOCK DIAGRAM:



TRUTH TABLE:

CLOCK PULSE NO.	PARALLEL DATA INPUT				PARALLEL DATA OUTPUT			
	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	1	1
2	1	0	1	0	1	0	1	0
3	1	1	0	0	1	1	0	0
4	1	0	0	1	1	0	0	1

LOGIC DIAGRAM:



PROCEDURE:

1. Place the IC on IC trainer kit
2. Connect the Vcc and ground to respective pins of IC trainer kit
3. Connections are given as per logic diagram.
4. Connect the inputs to the input switches provided in the IC trainer kit
5. Connect the outputs to the switches of output LED's
6. Apply various combinations of input according to the truth table
7. Observe the condition of output LED's and verify the truth table

RESULT:

Thus, 4-bit shift registers such as SISO, SIPO and PIPO are constructed using D-flip flop (IC7474), and their truth tables are verified.

VIVA QUESTIONS WITH ANSWERS:

1. **List out different type shift registers.**
   SISO, SIPO, PIPO, PISO

2. **Which flip-flop is most commonly used to design shift registers?**
   D Flip-flop

3. **How much storage capacity (in bit(s)) does each stage in a shift register represent?**
   1-bit

4. **Number of flip-flops required to construct 8-Bit serial-in parallel-out shift register?**
   8

5. **How can parallel data be taken out of a shift register simultaneously?**
   Use the Q output of each FF

6. **How many clock pulses will be required to completely load serially a 5-bit shiftregister?**
   5

7. **The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains___.**
   00101

8. **A serial in parallel out, 4-bit shift register initially contains all 1s. The data nibble0111 is waiting to enter. After three clock pulses, the register contains_____** 111

9. **An 8-bit serial in/serial out shift register is used with a clock frequency of 2 MHz toachieve a time delay (t_d) of_.**
   4 µs

10. **List atleast 3 applications of shift registers.**
    - Used for data transfer, manipulation and data storage
    - PISO shift register is used for converting parallel to serial data
    - SIPO used for converting serial to parallel data in communication lines
    - SISO & PIPO shift registers are used for generating time delay in digital circuit