

ECE 351 - Lab 5 - Step and Impulse Response of a RLC Bandpass Filter

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1 Purpose

The purpose of this lab was to use Laplace transformations to find the time-domain response of an RLC bandpass filter to both impulse and step inputs.

2 Procedure

This lab began with a prelab calculating the transfer function and the impulse response of the circuit shown in Figure 1.

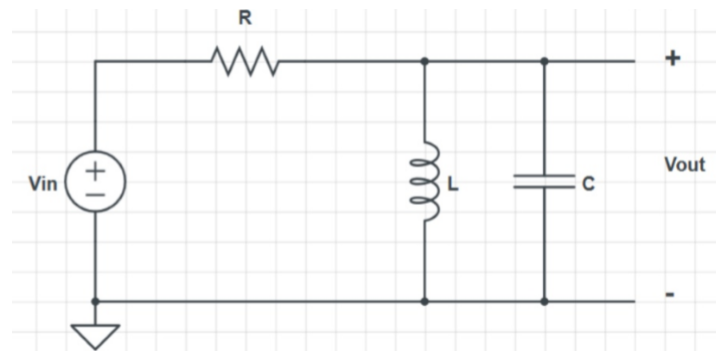


Figure 1: Prelab Schematic

Then, for the lab, there were two parts. The first was graphing the derived equation for the impulse response from the prelab together with the impulse function contained in the scipy library on the same plot and comparing them. These are shown in Figure 2 in the Results section. Then the scipy library command to find the step response, as shown graphed in Figure 3 in the Results section.

Finally, the Final Value Theorem was applied to the step response, as shown in Equation 1 in the Results section.

3 Results

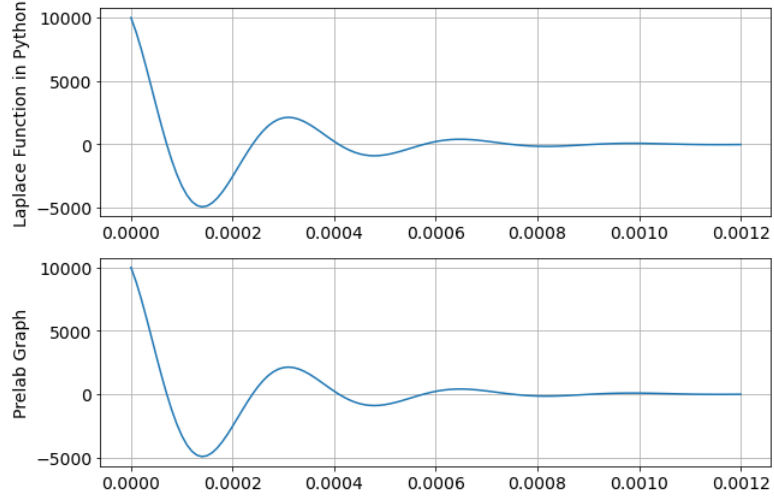


Figure 2: Plots of Hand-Derived and Computer-Calculated Impulse Response

This figure shows that the hand-calculated transfer function from the prelab was identical to the impulse response done by the python command.

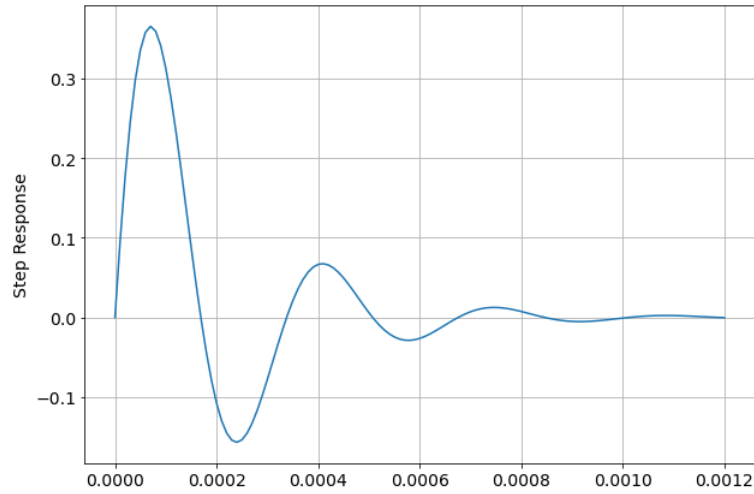


Figure 3: Plot of Computer-Calculated Step Response

This figure shows that the step response has a very similar shape to the impulse response, but instead of starting at the high value, it increases from 0 to the peak before following the same trend as the impulse response.

$$\lim_{s \rightarrow 0} \frac{s * \frac{1}{RC} * s}{s^2 + \frac{1}{RC} * s + \frac{1}{LC}} = \frac{0}{0 + 0 + \frac{1}{LC}} = 0 \quad (1)$$

4 Questions

Explain the result of the Final Value Theorem from Part 2 Task 2 in terms of the physical circuit components.

The Final Value Theorem shows the steady-state value of the transfer function as the time goes to infinity, due to the following property:

$$\lim_{s \rightarrow 0} s * F(s) = \lim_{t \rightarrow \infty} f(t) \quad (2)$$

Because of this, as s goes to 0, or as t goes to infinity, the transfer function of the output voltage over the input voltage reduces to 0. This makes sense because in a steady-state circuit, a capacitor is an open circuit and an inductor is a short circuit. The voltage drop across a short circuit, especially in series with a resistor, will be 0, this the FVT confirms what simple circuit analysis hypothesizes.

Leave any feedback on the clarity of lab tasks, expectations, and deliverables.

The lab was clear and the expectations were understood.

5 GitHub Link

<https://github.com/EReeder35>

6 Conclusion

In conclusion, this was another educational lab. The best part about it for me was getting practice making my own function to implement the sine method, which taught me a lot more about how to format code in Python.