Faculty Of Computers and Information
Mansoura University

Hardware of Real-time Systems

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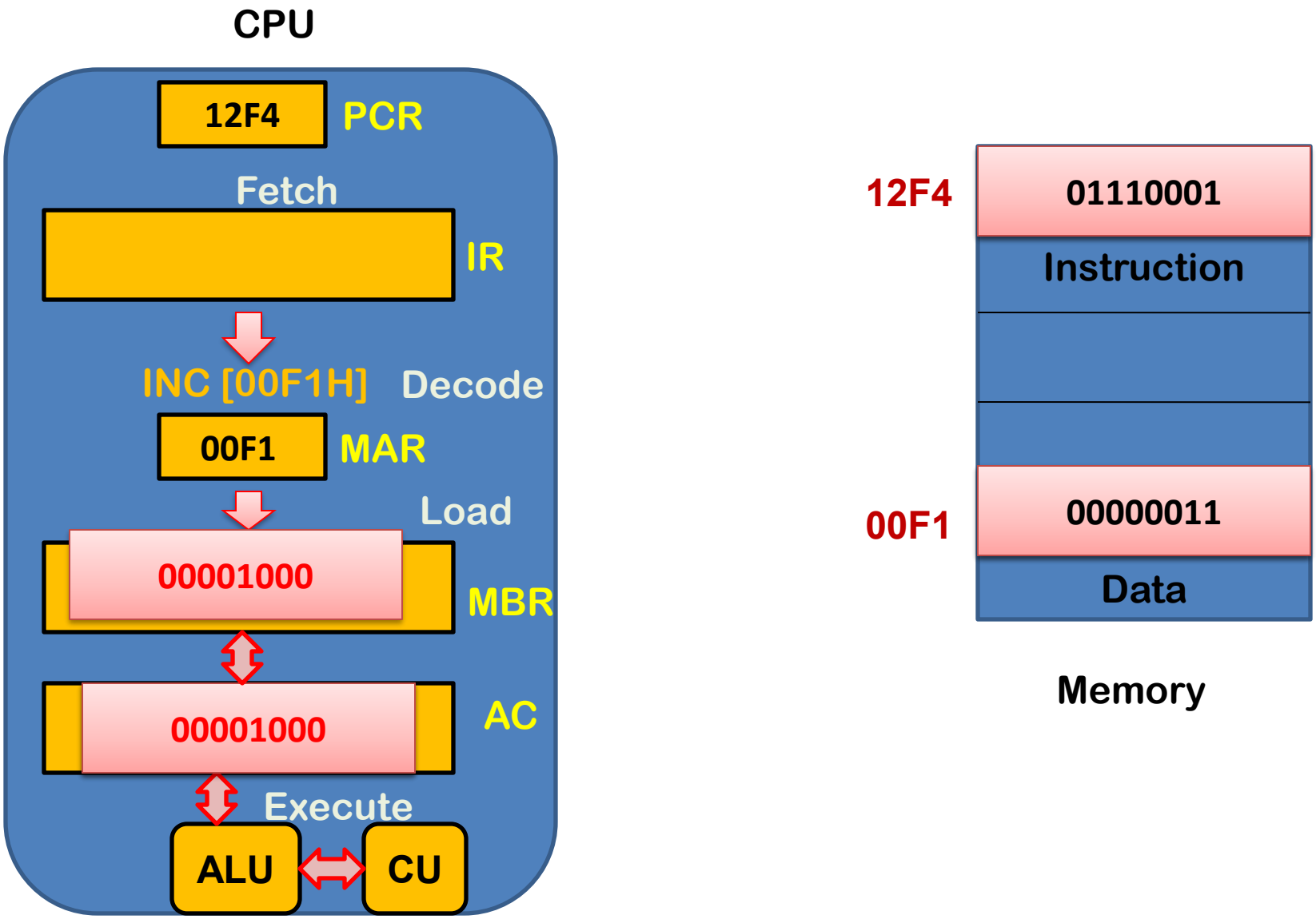
You need to know some basic concepts!



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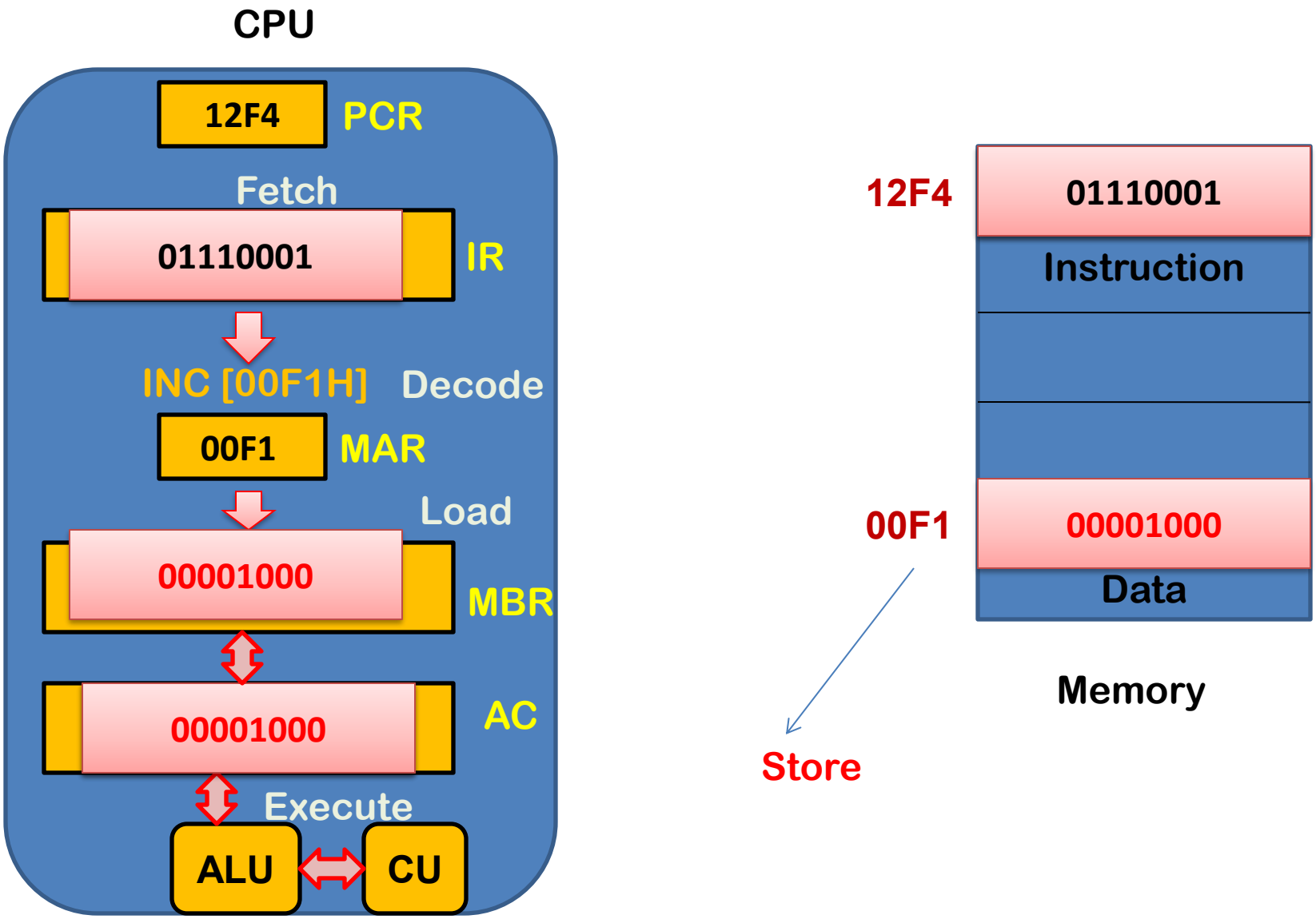

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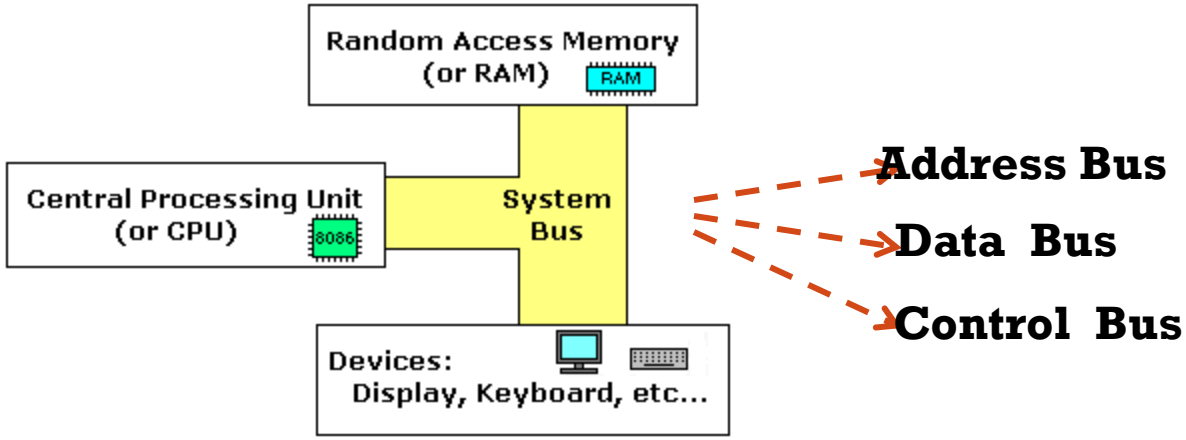

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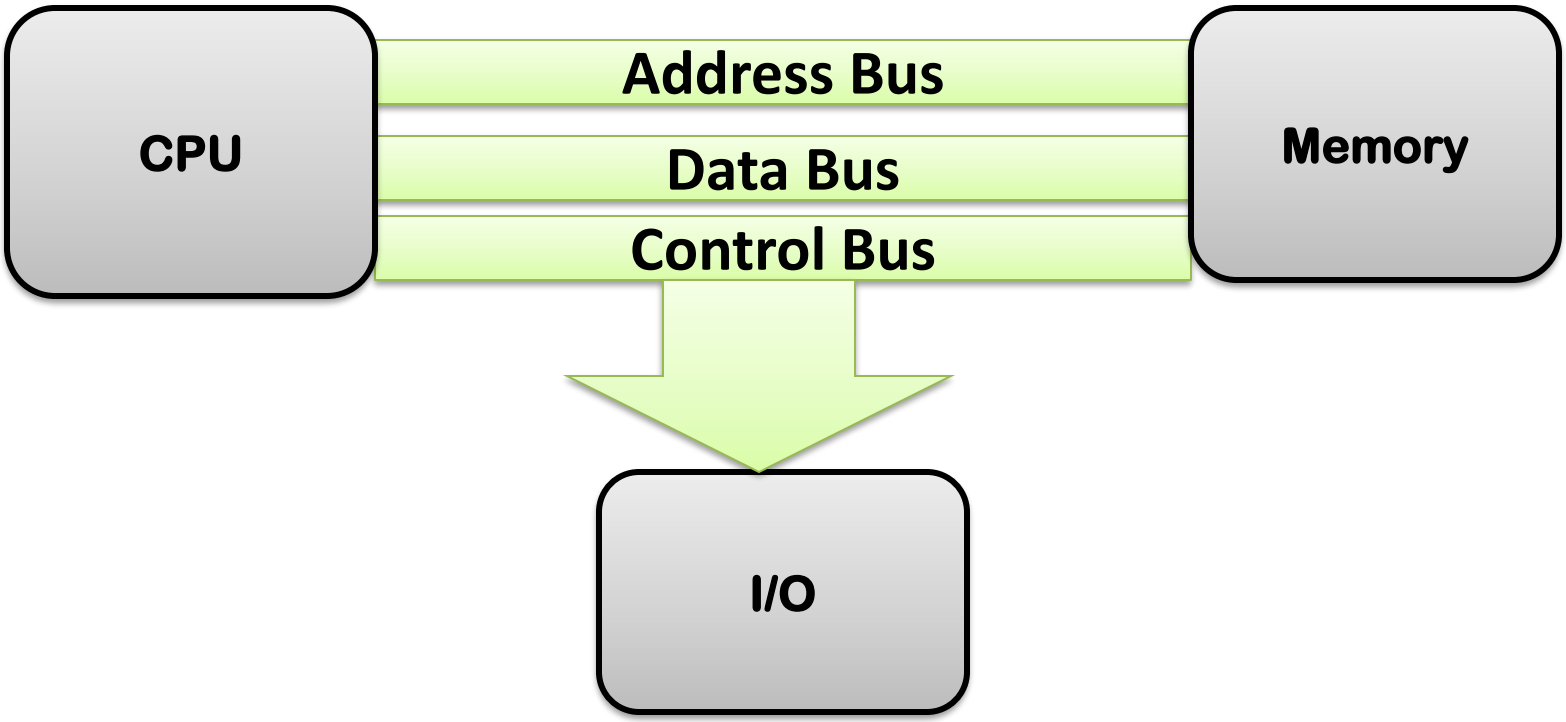

Note: n-bit microcontroller , n-bit Microprocessor

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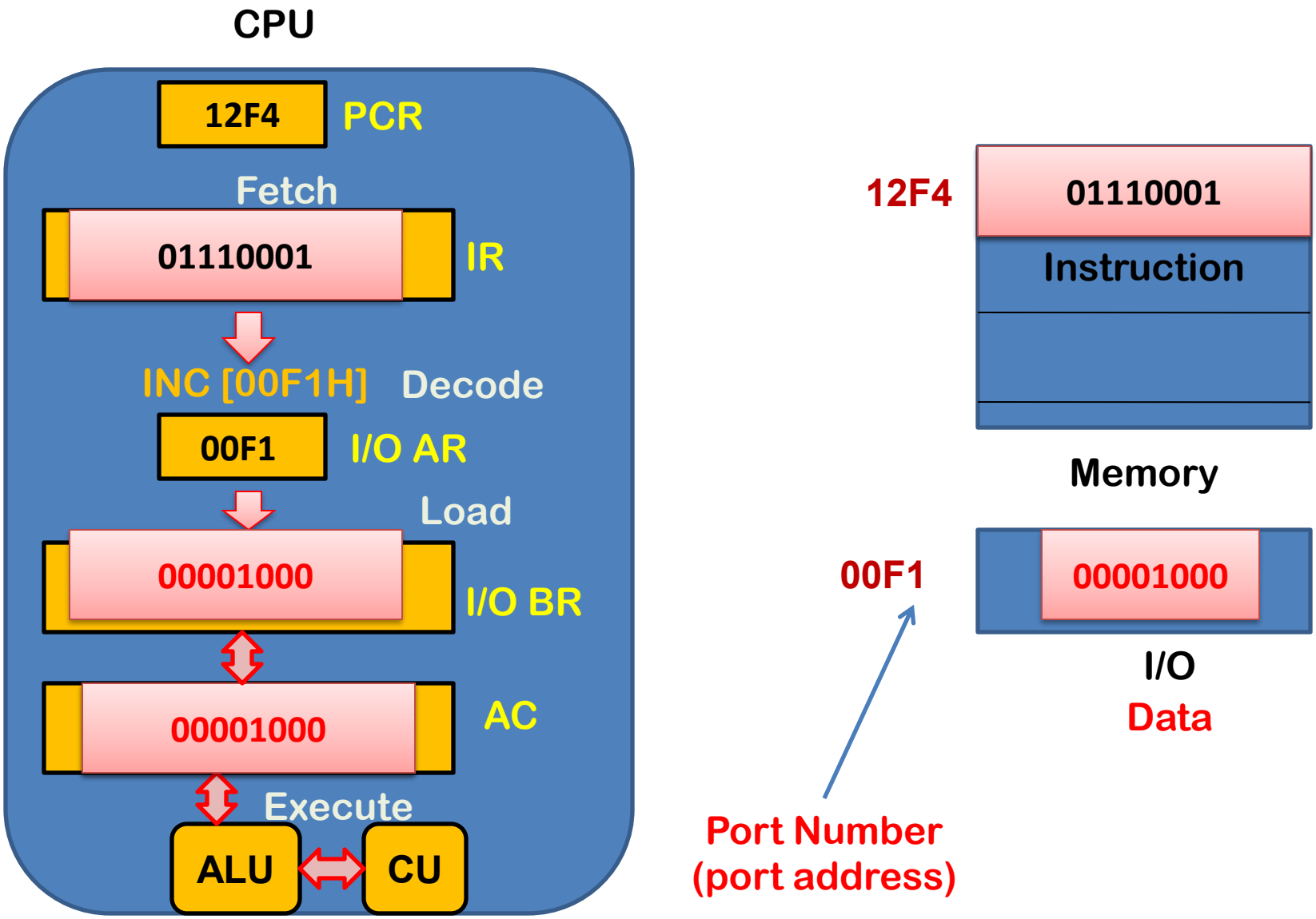
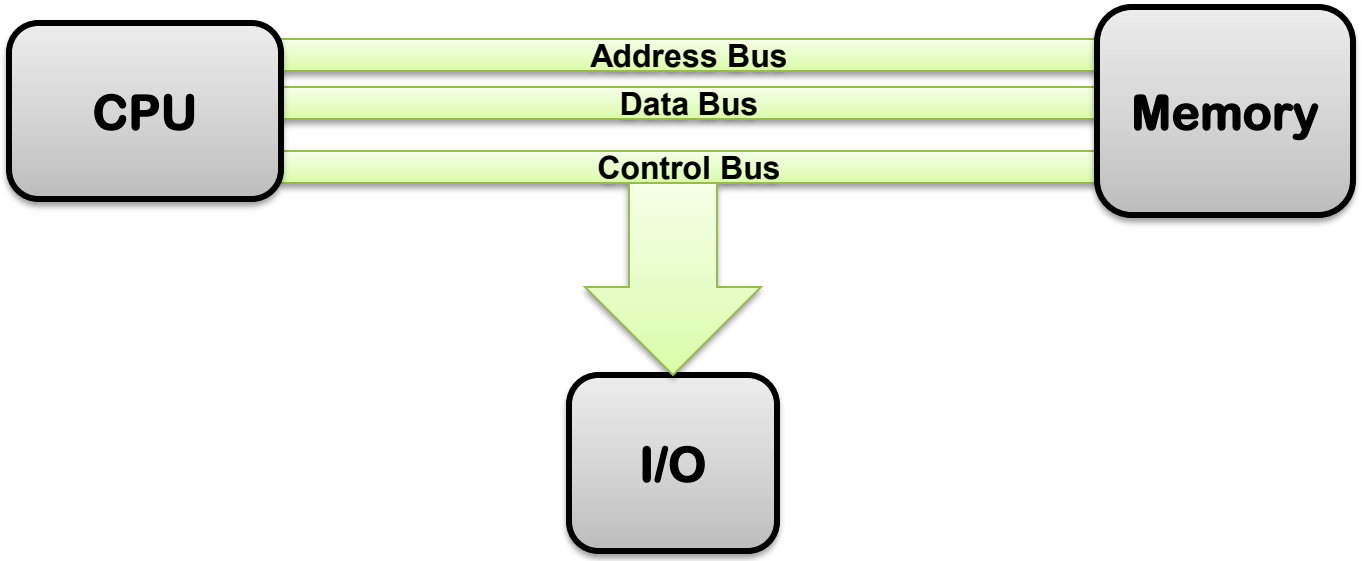


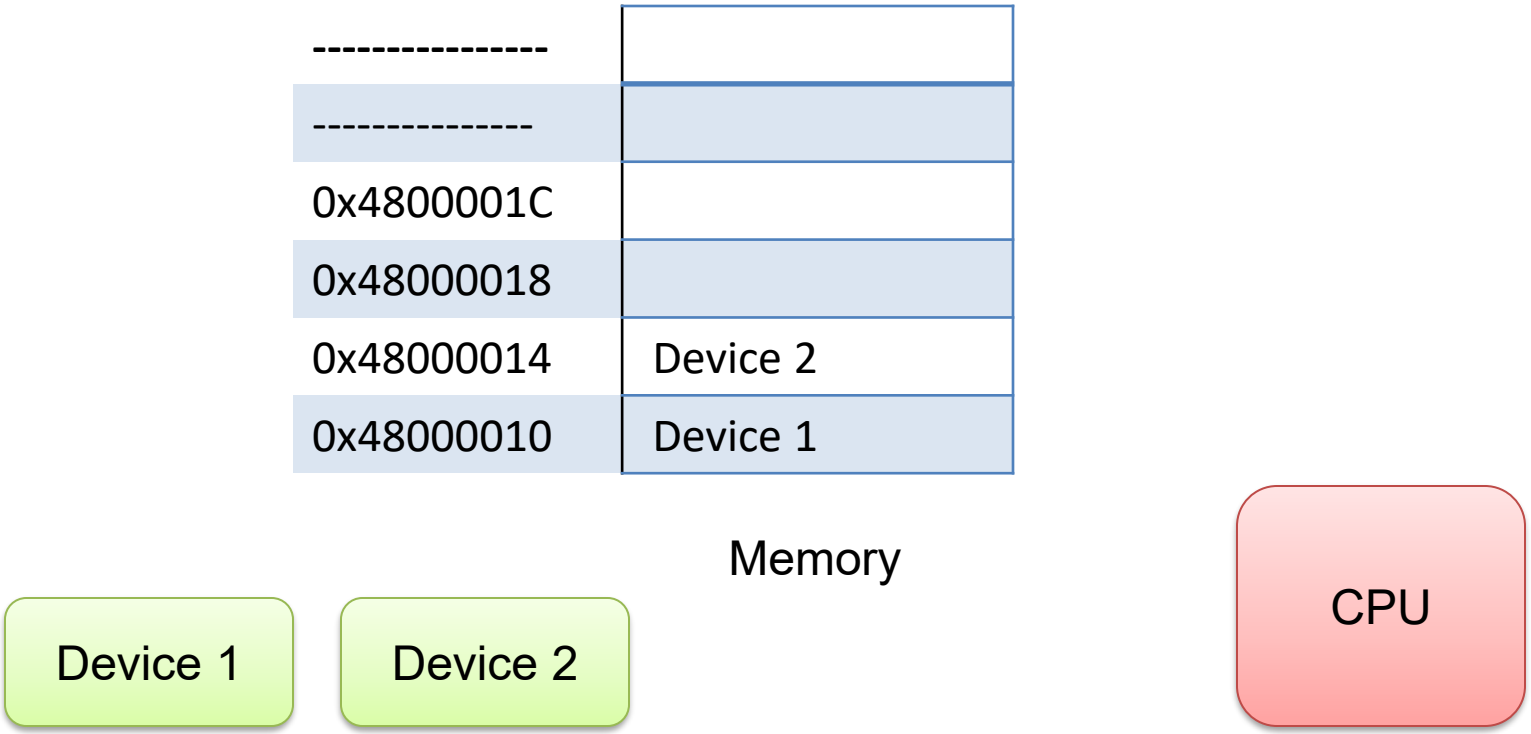
Programmed I/O

- Use a separate address space for I/O registers.
- There is an additional control signal “ Memory/IO ” for distinguishing between memory and I/O accesses.
- A separate IN and OUT instructions are needed for accessing the I/O registers (special instructions for I/O handling).

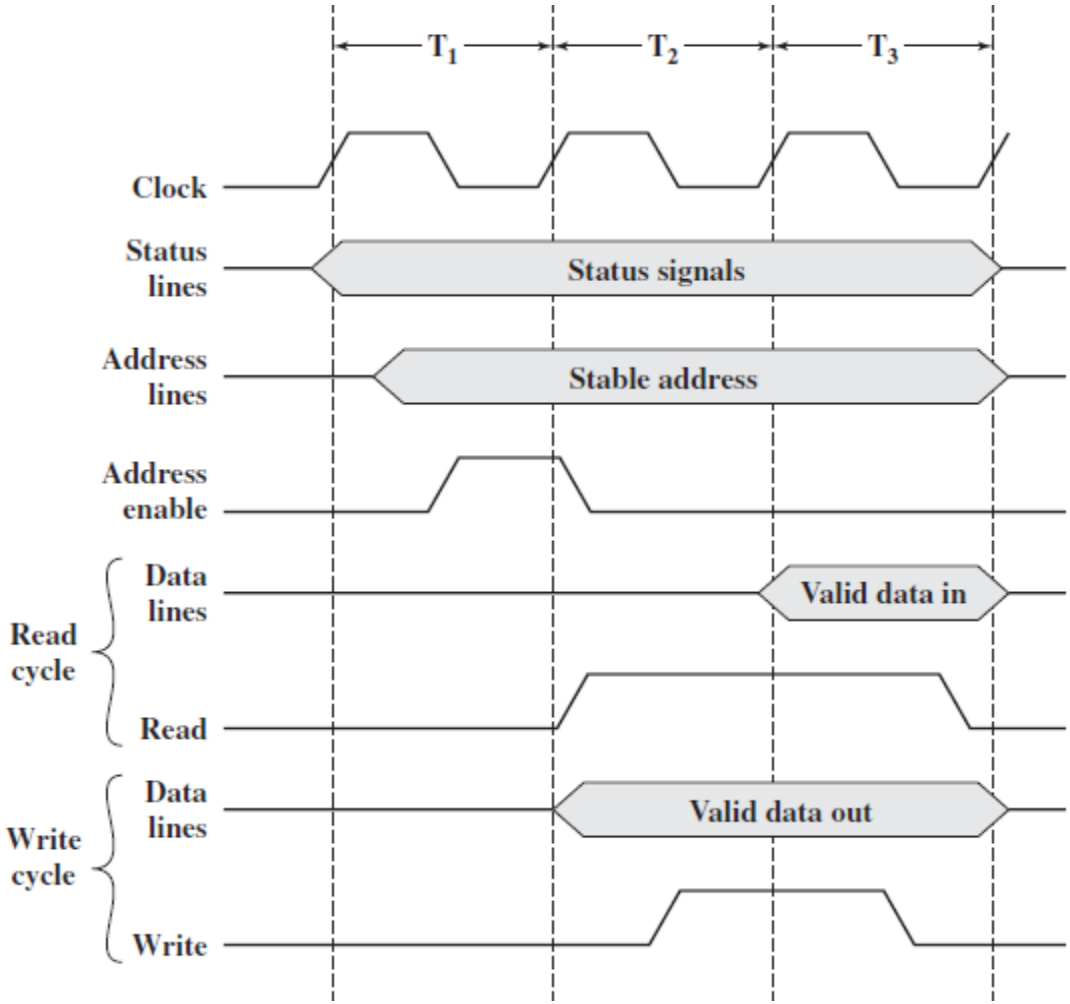


Memory-mapped I/O

- Each device register is assigned to a memory address.
- Instructions that access the memory and I/O devices are the same! (i.e. use native CPU load/store instructions).



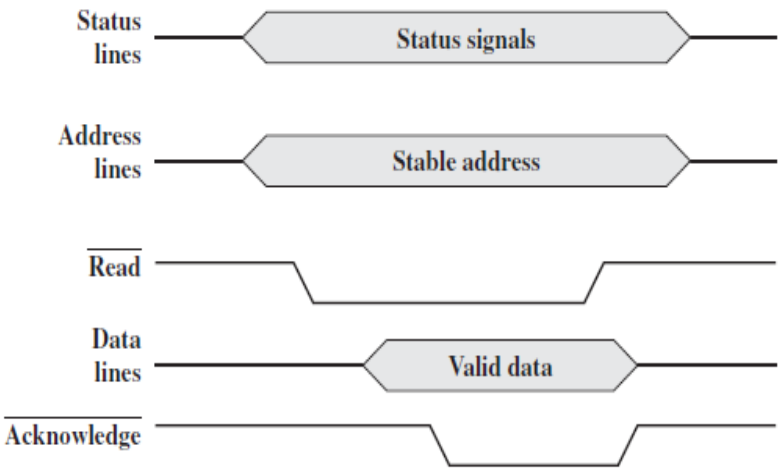
Synchronous Bus



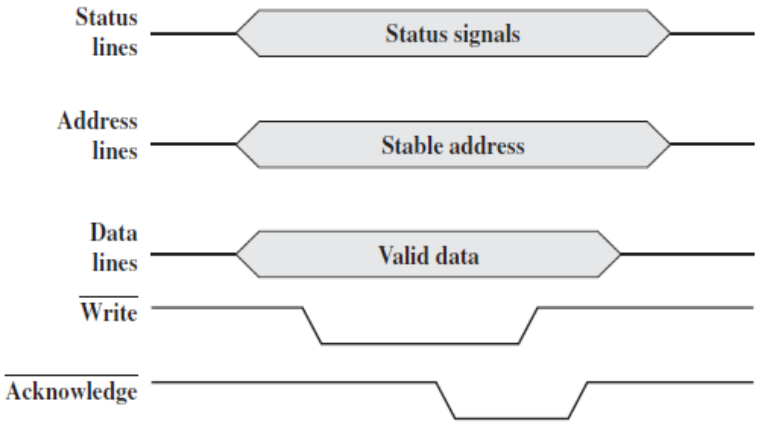
Synchronous Transmission/ Receiver System

- Transmitter and receivers are synchronized of clock.
- Data bits are transmitted with synchronization of clock.
- In a synchronized data transfer, we send bit one after another without gaps or start/stop bits.
- The responsibility of receiver to group the bits.
- Used in high – speed transmission.
- Assume the devices speed is the same.

Asynchronous Bus



(a) System bus read cycle



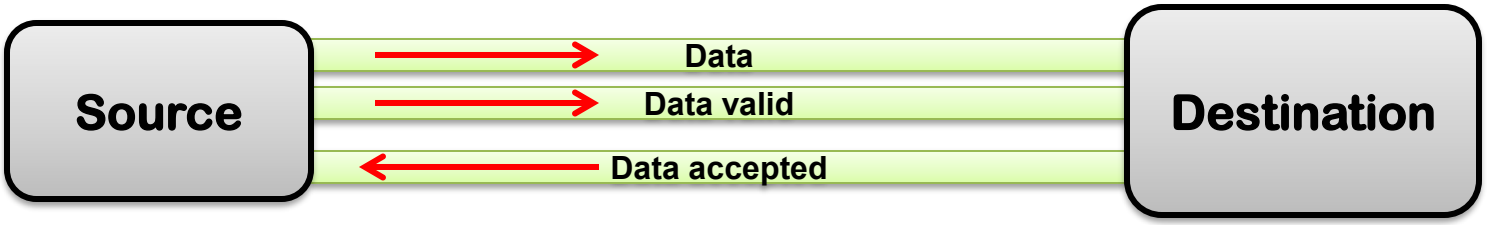
(b) System bus write cycle

Asynchronous Transmission/ Receiver System

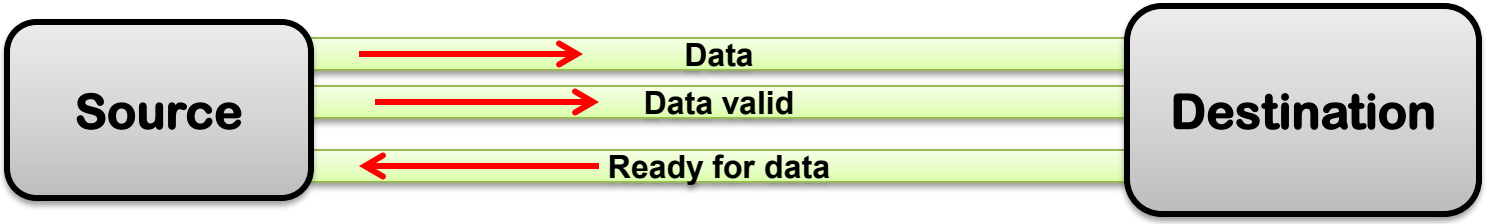
- Transmitters and receivers are not synchronized by clock.
- Bit's of data are transmitted at constant rate (regular interval).
- Transmitter can initiate transmission at any instance of time.
- Only 1 byte is sent at a time and there is ideal time between two consecutive bytes.
- Transmitter and receiver operate at different rates.
- Used in low – speed transmission.
- Handshaking data transfer (Acknowledgment)

Asynchronous Transmission/ Receiver System

- Handshaking data transfer (Acknowledgment)



(source initiated handshaking)



(Destination initiated handshaking)

Q

A hypothetical 12-bit microprocessor uses 12-bit addresses to access memory. Each address is transmitted twice on a 6-bit address bus.

A. What is the maximum memory size (in bytes) it can support?

Answer: 2^12 = 4096 bytes

B. What is the size of the address bus?

Answer: 6 bits

C. If each address were transmitted only once on the address bus, what would be the maximum supported memory size?

Answer: 2^6 = 64 bytes

Q

A. With memory-mapped I/O, I/O ports can be operated through all instructions that have a memory operand (T/F)

B. The ---------- bus is unidirectional bus controlled by CPU.

C. The ---------- bus is bidirectional bus that allows instructions and data to transfer from memory.

D. The --------- bus consists of heterogeneous collection of independent status, clock, and power lines

E. An Apple II computer uses 16-bit addresses to access the memory. Each address is transmitted twice on the address bus:

1. The size of the address bus is ----------
2. The maximum addressable memory is ---------