Cmod-A7-35T XADC Usage

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1 Introduction

This short PDF is made for electronic students using the XADC in the cmod-a7-35T. Reasoning for making this PDF is due to the hard time we had understanding the documentation from AMD's own userpage with documentation together with the short and simple documentation from Digilent itself. We'll throughout this document refer to different documentation pages. To make this easy for you, we'll put the documentation we used to understand this right here:

- https://digilent.com/reference/programmable-logic/cmod-a7/reference-manual
- 7 Series FPGAs and Zynq-7000 SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide (UG480)
- Vivado Design Suite 7 Series FPGA and Zynq 7000 SoC Libraries Guide (UG953)
- https://www.micro-nova.com/reading-and-reconfigure-the-xadc?

Be aware, that the program we used in this project is Vivado, and we write in VHDL language.

2 Own usage in project

For our project, we had to use the XADC to sample a signal with a frequency of 500 KHz. In our use, we had the entire Cmod board (see figure 1), and wanted to use only **one ADC channel**. Note that this board has 2 - and only 2 ADC channels routed to the pins from the Artix 7.

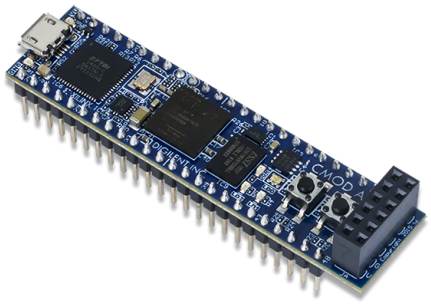

Figure 1: Cmod-A7-35T used in the project

3 What to know about the XADC on Cmod-A7-35T

The XADC on this FPGA has a lot to discover and is generally really nicely documented. Using the entire board (cmod board) along with the XADC is on the other hand a little tricky.

3.0.1 ADC connections to board

As described from the Cmod-A7, reference manual:
`https://digilent.com/reference/programmable-logic/cmod-a7/reference-manual`
Pins 15 and 16 of the DIP connector are used as analog inputs to the XADC module of the FPGA. The FPGA expects that the inputs range from 0-1 V, so we use an external circuit to scale down the input voltage from 3.3V. This circuit is shown in Figure 2. This circuit allows the XADC module to accurately measure any voltage between 0V and 3.3V (relative to GND on pin 25) that is applied to either of these pins."
This means, that it's possible to connect an external signal with a maximum amplitude of 3.3V.

Be aware when using this board, that it's only pins 15 and 16 on the connectorboard that is connected to the adc. The connection used in Vivado project and in the real XADC is therefore:

- Pin 15 → VAUX[4]
- Pin 16 → VAUX[12]

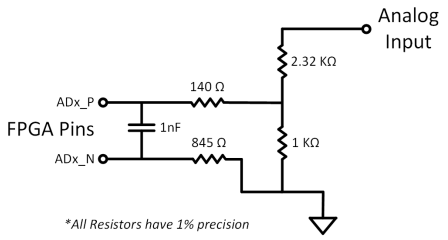

Figure 2: Analog Inputs

4 Vivado..

Described here is the things to do, to use the XADC in vivado

4.1 Setting up the XADC

Setting up the XADC in Vivado is generally quite simple. The setup we went with, comes straight from this guide (not using the Mercury2):
`https://www.micro-nova.com/reading-and-reconfigure-the-xadc?srsltid=AfmBOooFBhoj272lVoowWZl_rafvBFvq4O3z2NGUVDaxK_CPq15I2A34`

Quick step-guide:

1. Make Vivado projekt
2. Setup a block-design
3. Insert the XADC IP-block
4. Setup the XADC IP-block (described below)
5. Create VHDL Wrapper from block-design
6. Simulate Setup in testbench

4.1.1 Setting up the XADC IP-block

For setup on figure 3
interface option is chosen as **DRP**
timing mode is **Continuous Mode**
clock frequency is 100 MHz, to be able to sample with the frequency of 500 KHz
Startup Channel Selection is set to **Single channel**, since the use of this project only i one channel. If you want **more than one channel**, just select the **channel sequencer**.

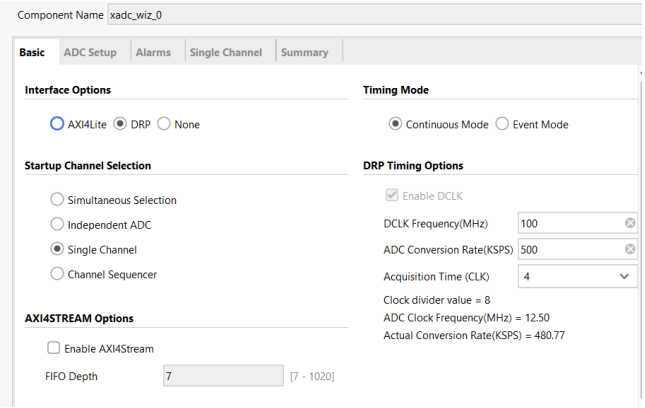

Figure 3: XADC IP-block Setup 1

The setup in figure 4 is in our project not relevant.

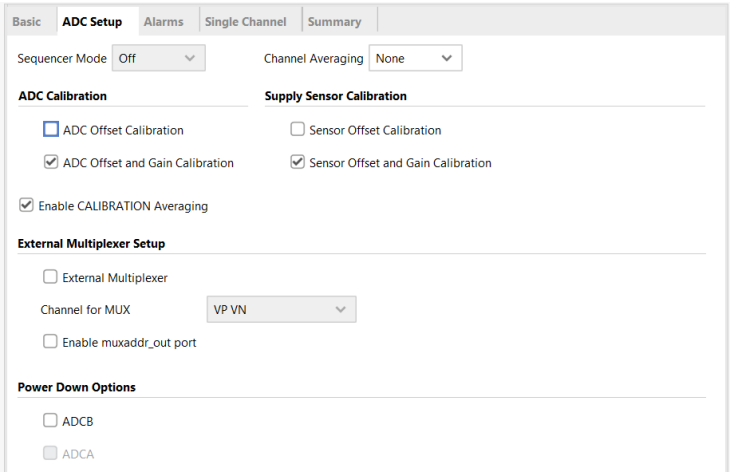

Figure 4: XADC IP-block Setup 2

The setup in figure 5 is in our project not relevant. The setup in figure 6

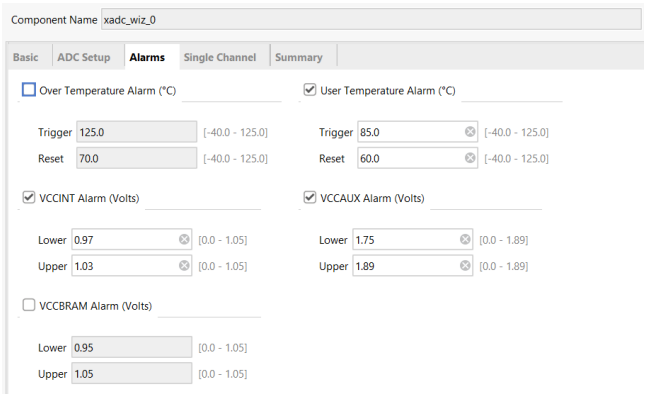

Figure 5: XADC IP-block Setup 3

is **quite important** Here is the place where we select the channel to measure on. In our project we used pin 15 (VAUX[4]). The only extern analog inputs available when using the Cmod-A7 board, are still VAUX[4] and VAUX[12]!!

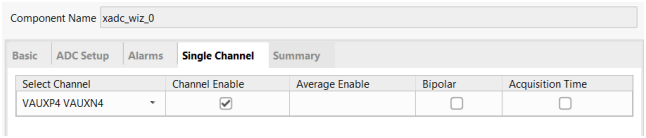

Figure 6: XADC IP-block Setup 4

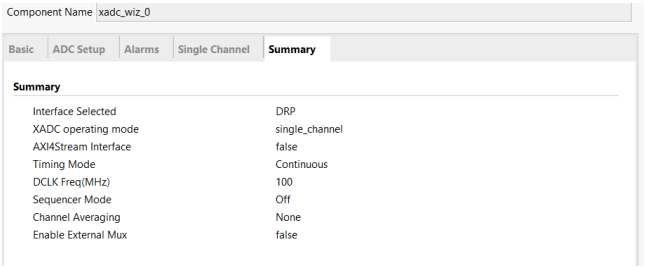

Figure 7: XADC IP-block Setup 5

4.2 Details in XADC IP-Block

4.2.1 Connections in the block-design

`https://docs.amd.com/viewer/attachment/qOeib0vlzXa1isUAfuFzOQ/wX4fvEpFE1dqdihEZyV6vQ`
When the XADC takes a measurement, the values converted are stored in in-

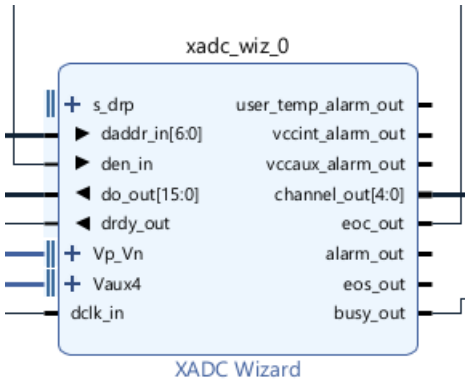

Figure 8: Vivado xadc ip block

tern registers. To read any of these values from the XADC you have to tell the XADC which register you want to read.

I/O	Used/not Used	Why...
Vp_Vn	Not used	These standard analog inputs is not connected to the Cmod-A7 board.
Vaux4	Used	Used here, to measure an extern analog signal on pin 15 on the Cmod-A7
dclk_in	Used	connect a 100 MHz clock to this input.
Alarms	Not connected	We haven't had the need to measure internal temperature or anything. therefor not used.
do_out	Used	This is the converted digital output after conversion of analog input.
den_in	Used	Used to start a new measurement as soon as the last mes has finnished. This is **connected to eoc_out**
eoc_out	Used	end of conversion is connected directly to den_in, to start a new measurement, when conversion is finnished
daddr_in	Used	this is used to tell the XADC which internal register we want to read from. In our case this is connected to a constant (20), since we use VAUX4. (See also figure 9).

Table 1: Caption

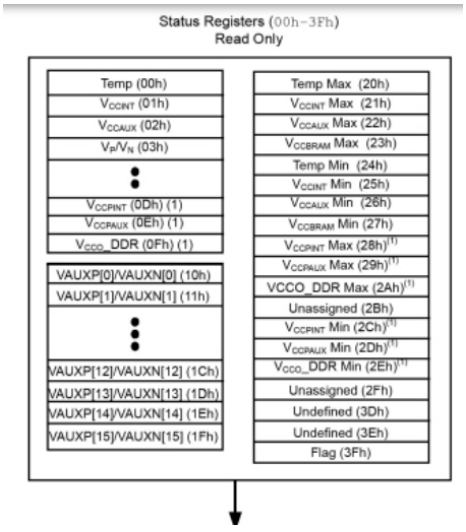

Figure 9: ADC Registers. from 7 Series FPGAs and Zynq-7000 SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide (UG480)