

# ESIstream

The Efficient Serial Interface

1

## ESISTREAM 62B64B

Get started with VCK190 loopback package

*VERSAL AI CORE XCV1902-2MSEVSVA2197*

# Summary

- 1 | Hardware setup
- 2 | From Vivado project creation to link synchronization
- 3 | Project overview
- 4 | From Vivado project creation to link synchronization
- 5 | Acquire RX data (62-bit)  
Using Vivado Integrated Logic Analyzer (ILA)
- 6 | Design example top file testbench simulation
- 7 | Application Note:  
Create an ESistream Gigabit Transceivers Block Design (.bd) from scratch on Versal.
- 8 | UART interface protocol

# Hardware Setup

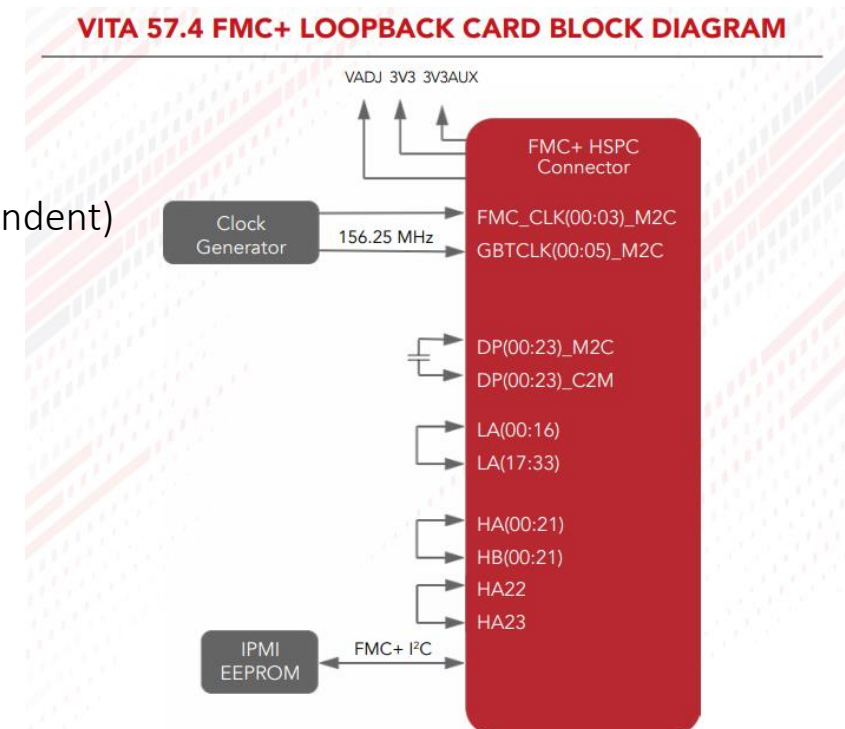
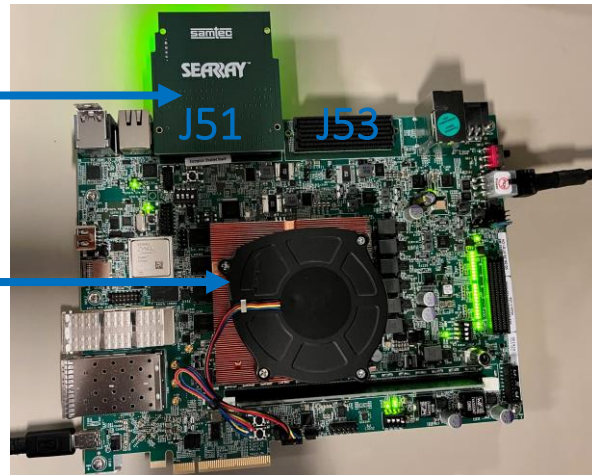
# Hardware setup

## Ordering information

- ❑ VCK190 Versal AI Core Evaluation kit [product web page](#).
  - ❑ Avnet: [EK-VCK190-G by AMD Xilinx Evaluation & Development Kits | Avnet](#)
- ❑ SAMTEC VITA 57.4 FMC+ HSPC Loopack Card [product web page](#)
  - ❑ Avnet [REF-197618-01 by Samtec Hardware Development Tools | Avnet](#)
  - ❑ Mouser: [REF-197618-01 Samtec | Mouser Europe](#)
  - ❑ FMC I/O voltage: VADJ=1.2 V, 1.5 V, 1.8 V, 2.5 V or 3.3 V (FPGA carrier card dependent)

Loopback board

VCK190 Evaluation kit



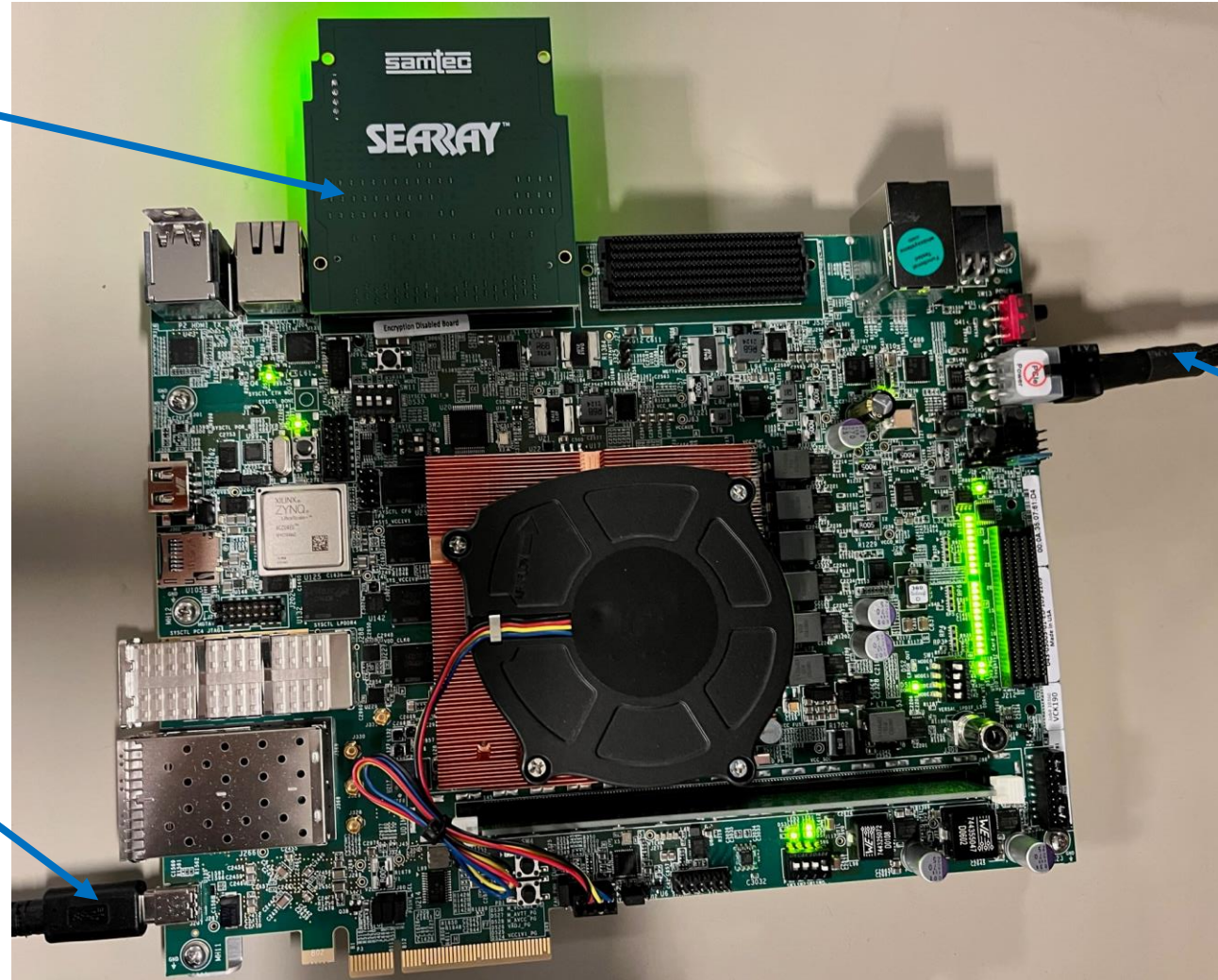
# Hardware setup

Connect cables and loopback board on J51

Connect XM107 loopback board

Connect power cable

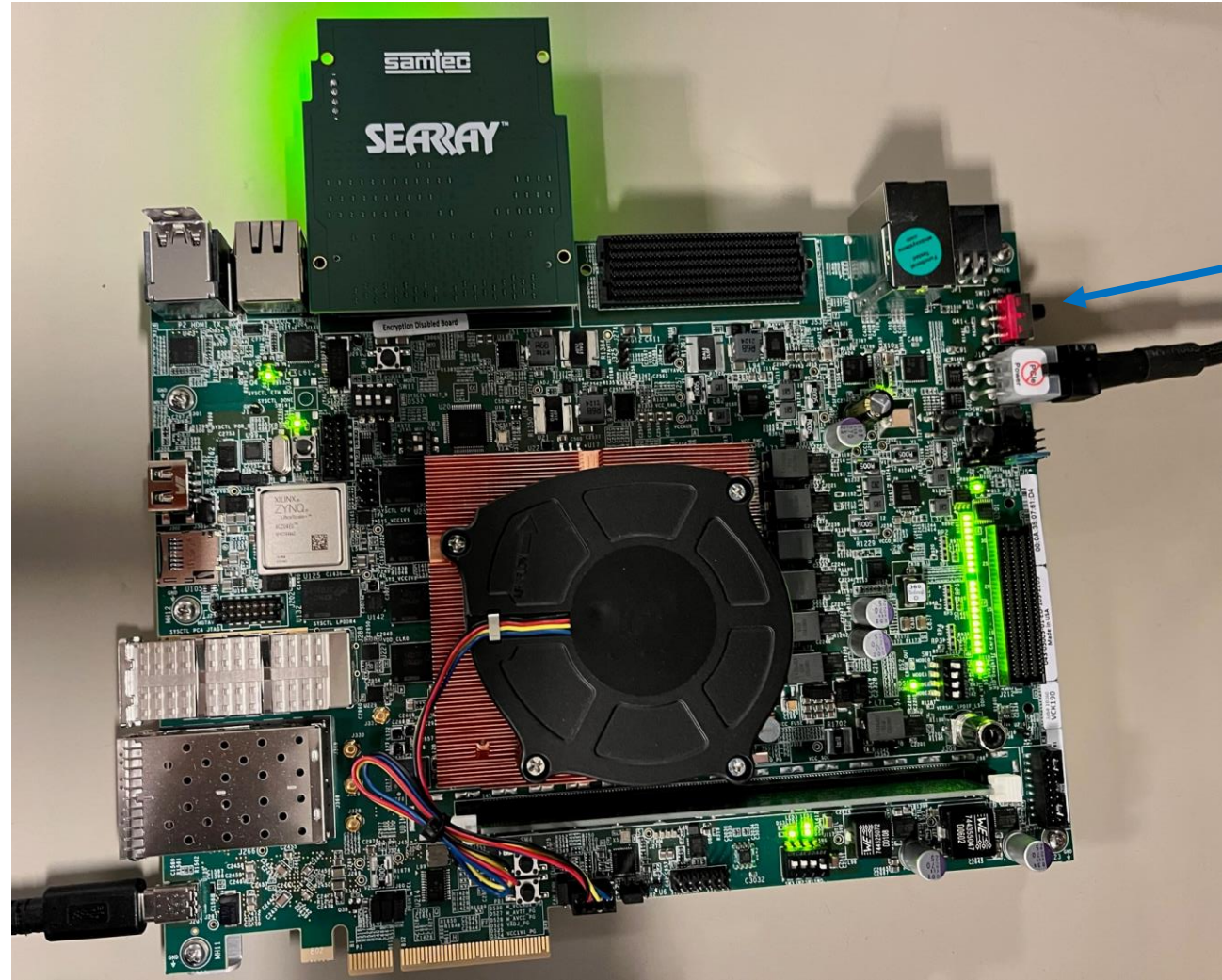
Connect USB C JTAG + UART cable between PC and VCK190





# Hardware setup

## Power-ON VCK190 Evaluation Kit

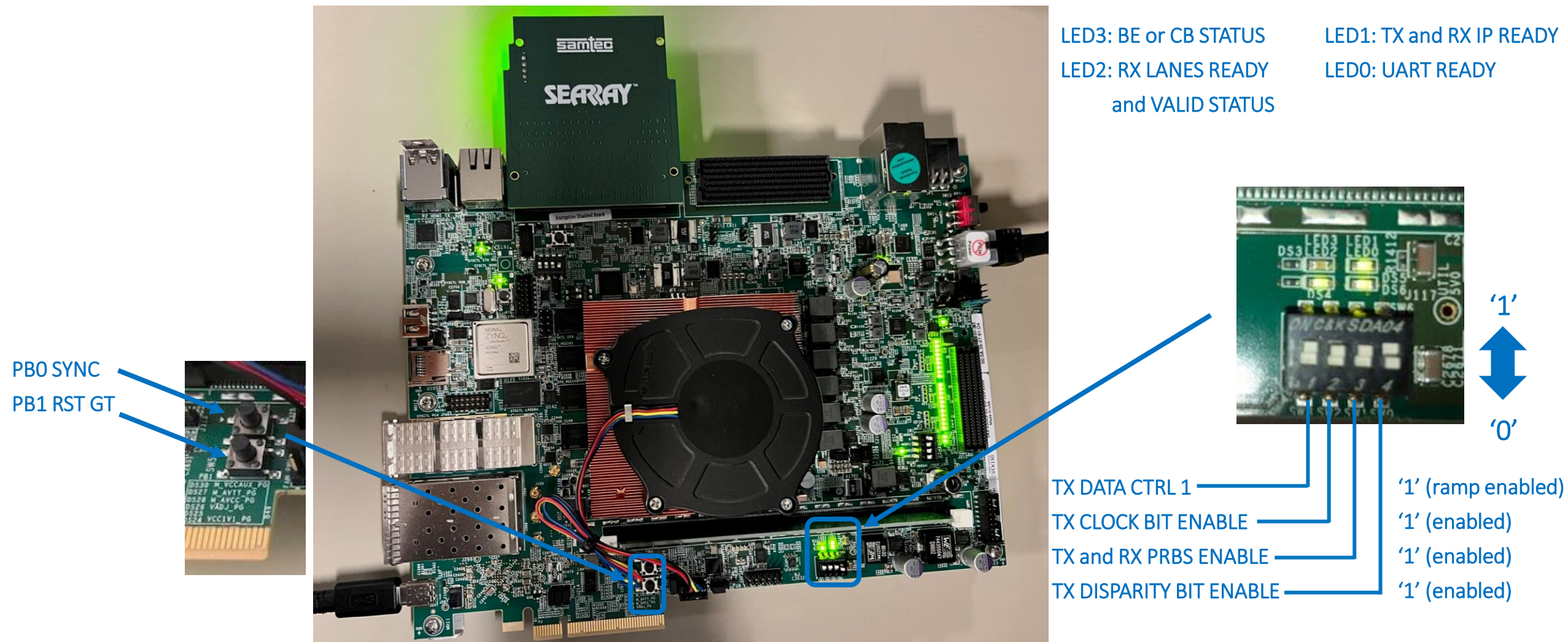


ON  
↕  
OFF

Switch ON SW13

# User interface

Push-Buttons (x2), Led (x4), Switches (x4)

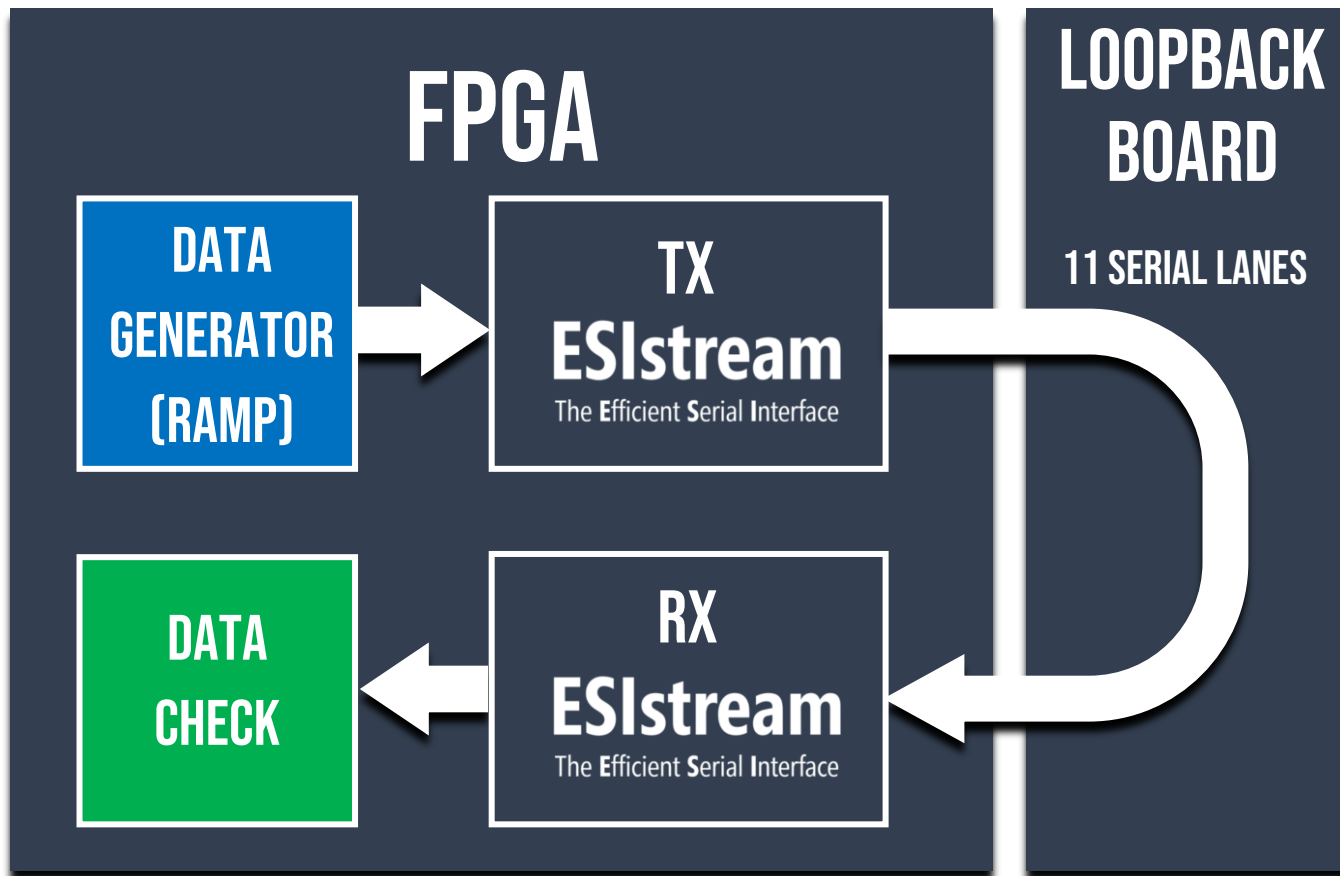


# Project overview



# Project overview

9



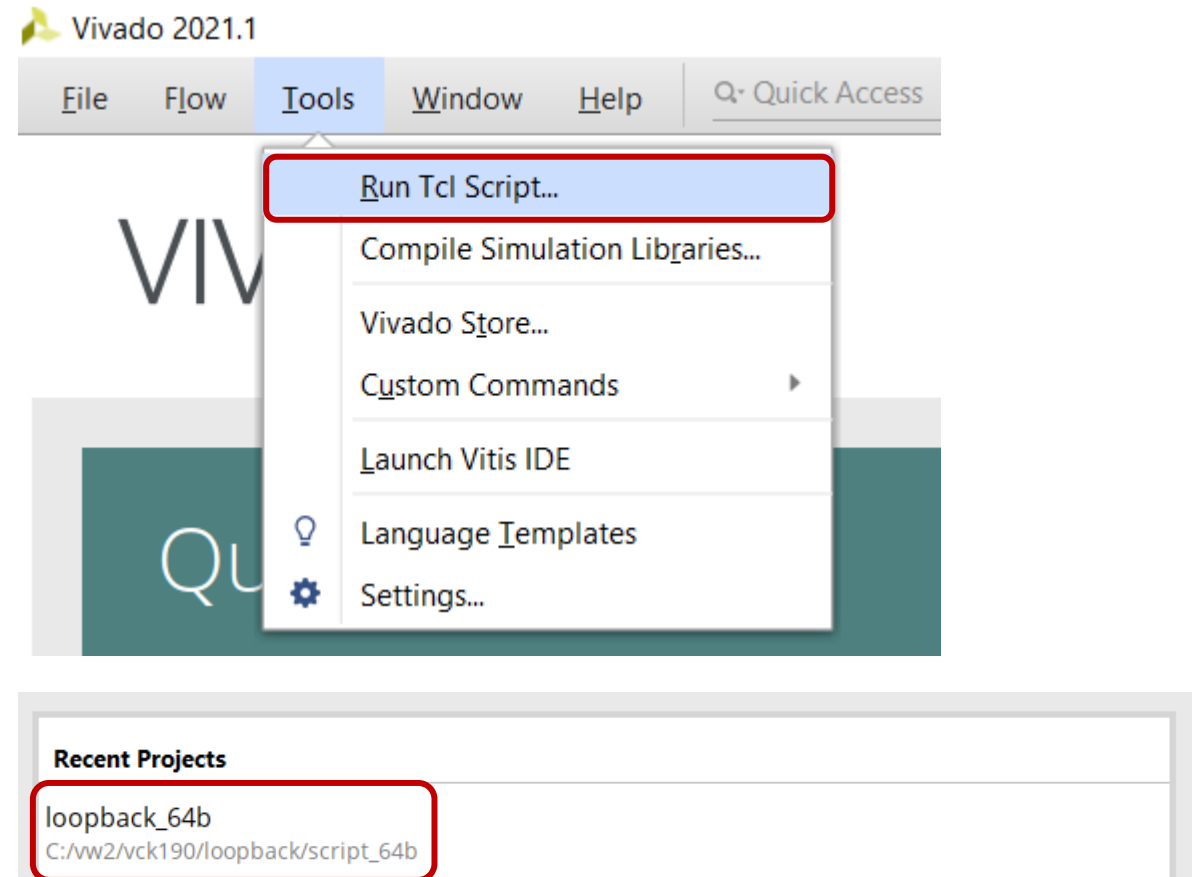
```
github > Package_ESistream62b64b_Xilinx_xcvc1902-vsua2197-2mp-e-s
Nom
├── loopback
├── src_common
└── src_esistream
```

```
github > Package_ESistream62b64b_Xilinx_xcvc1902-vsua2197-2mp-e-s > loopback
Nom
├── src_bd
├── src_ip
├── src_tb
├── esistream_62b64b_top.vhd
├── esistream62b64b_64.xdc
├── make_external_lcp11lock.tcl
└── script_64b.tcl
```

# From Vivado project creation to link synchronization

# Create Vivado project

- ❑ Open Vivado 2021.1
- ❑ Click on Tools > Run Tcl Script...
- ❑ Launch *script\_64b.tcl* available in *loopback/* package directory.
- ❑ Once project creation has completed...
- ❑ Click on *Recent projects* view to open it.



# Generate Device image

12

loopback\_64b - [C:/vw2/vck190/loopback/script\_64b/loopback\_64b.xpr] - Vivado 2021.1

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access

write\_device\_image Complete ✓

Default Layout

Flow Navigator

- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Device Image**
  - Open Hardware Manager

PROJECT MANAGER - loopback\_64b

Sources x Properties ? \_ □ □

Design Sources (1)

- esistream\_62b64b\_top (rtl) (esistream\_62b64b\_top.vhd) (10)

Constraints (1)

Simulation Sources (2)

Utility Sources

Project Summary

Overview | Dashboard

Status: ✓ Complete

Messages: 397 warnings

Active run: synth\_1

Part: xcvc1902-vsva2197-2MP-e-S

Strategy: Vivado Synthesis Defaults

Report Strategy: Vivado Synthesis Default Reports

Incremental synthesis: None

Status: ✓ Complete

Messages: 111 warnings

Active run: impl\_1

Part: xcvc1902-vsva2197-2MP-e-S

Strategy: Vivado Implementation Defaults

Report Strategy: Vivado Implementation Default Reports

Incremental implementation: None

DRC Violations

Summary: 40 warnings

Implemented DRC Report

Timing

Setup | Hold | Pulse Width

Worst Negative Slack (WNS): 0.171 ns

Total Negative Slack (TNS): 0 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 94564

Implemented Timing Report

Hierarchy IP Sources Libraries Compile Order

Tcl Console Messages Log Reports Design Runs x ? \_ □ □

Name	Constraints	Status	Progress	Elapsed	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	S
synth_1 (active)	constrs_1	synth_design Complete!	100%	00:11:03								27243	16194	0.0	0	0	
impl_1	constrs_1	write_device_image Complete!	100%	00:41:22	0.171	0.000	0.015	0.000	0.000	19.963	0	31216	25978	19.5	0	0	
Out-of-Context Module Runs																	
gty_brx_11lanes_64b		Submodule Runs Complete	100%	00:14:48													
axi_uartlite_0_synth_1	axi_uartlite_0	synth_design Complete!	100%	00:05:43								97	110	0.0	0	0	
clk_wizard_0_synth_1	clk_wizard_0	synth_design Complete!	100%	00:05:39								0	0	0.0	0	0	



# Load Device image

## Open hardware Manager

The screenshot shows the Vivado 2021.1 IDE interface. The Flow Navigator on the left lists various project tasks. The 'Open Hardware Manager' option under the 'PROGRAM AND DEBUG' section is highlighted with a red box and a red arrow. The main workspace displays the 'PROJECT MANAGER - loopback\_64b' window, which includes a 'Sources' pane, a 'Project Summary' pane, and a 'Design Runs' table.

**Flow Navigator:**

- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
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  - Open Elaborated Design
- SYNTHESIS
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- PROGRAM AND DEBUG
  - Generate Device Image
  - Open Hardware Manager**

**PROJECT MANAGER - loopback\_64b**

**Sources:** Design Sources (1)
 

- esistream\_62b64b\_top(rtl) (esistream\_62b64b\_top.vhd) (10)

 Constraints (1)
 

- Simulation Sources (2)

 Utility Sources

**Project Summary:** Overview | Dashboard

Status: **Complete**  
 Messages: 397 warnings  
 Active run: synth\_1  
 Part: xcvc1902-vsua2197-2MP-e-S  
 Strategy: Vivado Synthesis Defaults  
 Report Strategy: Vivado Synthesis Default Reports  
 Incremental synthesis: None

Status: **Complete**  
 Messages: 111 warnings  
 Active run: impl\_1  
 Part: xcvc1902-vsua2197-2MP-e-S  
 Strategy: Vivado Implementation Defaults  
 Report Strategy: Vivado Implementation Default Reports  
 Incremental implementation: None

**DRC Violations:** Summary: 40 warnings  
[Implemented DRC Report](#)

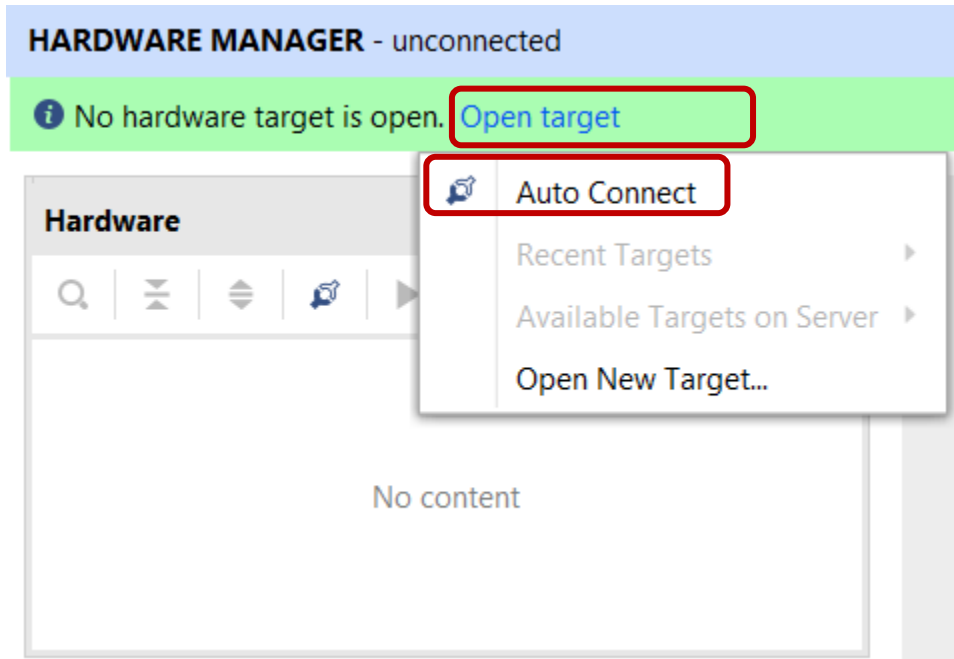
**Timing:** Worst Negative Slack (WNS): 0.171 ns  
 Total Negative Slack (TNS): 0 ns  
 Number of Failing Endpoints: 0  
 Total Number of Endpoints: 94564  
[Implemented Timing Report](#)

**Design Runs:**

Name	Constraints	Status	Progress	Elapsed	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	S
synth_1 (active)	constrs_1	synth_design Complete!	100%	00:11:03													
impl_1	constrs_1	write_device_image Complete!	100%	00:41:22	0.171	0.000	0.015	0.000	0.000	19.963	0	31216	25978	19.5	0	0	
Out-of-Context Module Runs																	
gty_brx_11lanes_64b		Submodule Runs Complete	100%	00:14:48													
axi_uartlite_0_synth_1	axi_uartlite_0	synth_design Complete!	100%	00:05:43								97	110	0.0	0	0	
clk_wizard_0_synth_1	clk_wizard_0	synth_design Complete!	100%	00:05:39								0	0	0.0	0	0	

# Load Device image

Click on Open target and Auto Connect



# Load Device image

Click on Program device and Program

**HARDWARE MANAGER** - localhost/xilinx\_tcf/Xilinx/282203141781A

There are no debug cores. [Program device](#) [Refresh device](#)

### Hardware

Name	Status
xilinx_tcf/Xilinx/28220314	Open
arm_dap_0 (0)	N/A
xcvc1902_1 (1)	Not programmed
SysMon (System Mon)	

### Hardware Device Properties

xcvc1902\_1

Name: xcvc1902\_1

Part: xcvc1902

ID code: 14CA8003

**General** Properties

### Program Device

Select a pdi programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the pdi programming file.

PDI file:  ...

Debug probes file:  ...

☒ Enable end of startup check

**Program** Cancel

Tcl Console x Messages Serial I/O Links Serial I/O Scans

### Program Device

Programming the device...

47%

**Background** Cancel

# Start link synchronization

Maximize ILA window

**HARDWARE MANAGER** - localhost/xilinx\_tcf/Xilinx/282203141781A

There are no serial I/O links. [Auto-detect links](#) [Create links](#)

**Hardware**

Name	Status
localhost (1)	Connected
xilinx_tcf/Xilinx/28220314	Open
arm_dap_0 (0)	N/A
xvc1902 1 (7)	Programmed

**Properties**

Select an object to see properties

**hw\_ila\_1**

Waveform - hw\_ila\_1

ILA Status: Idle

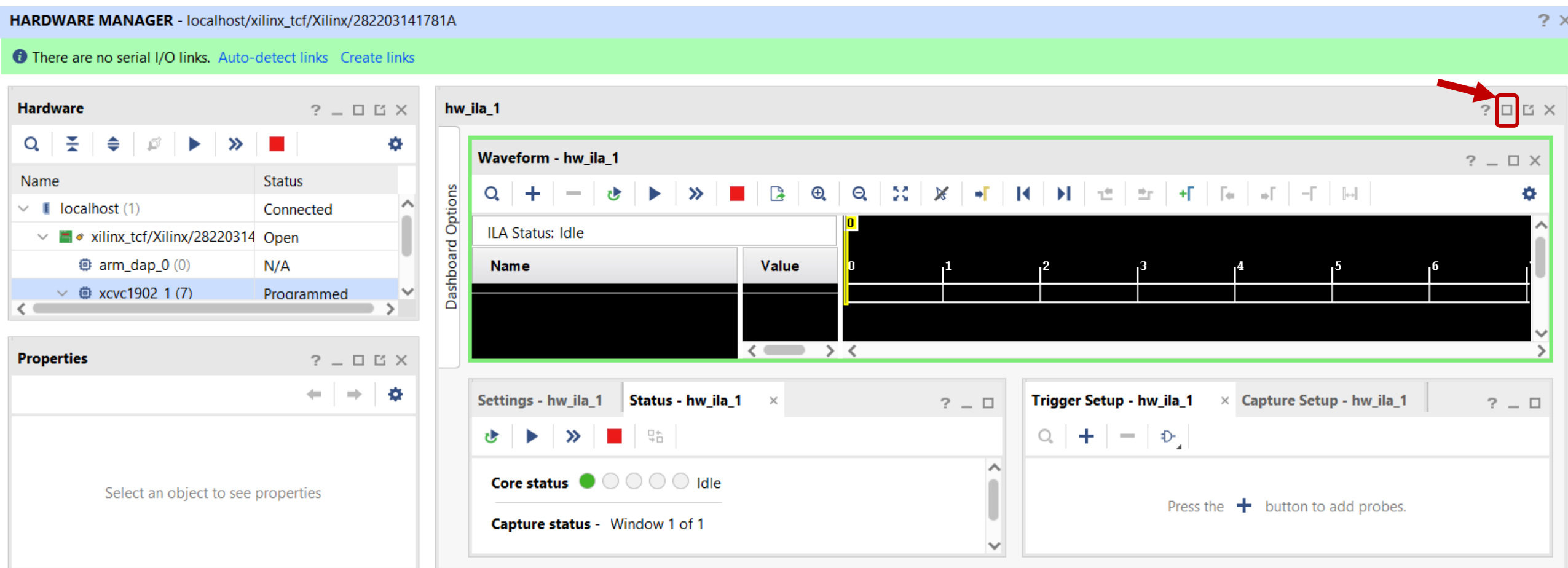
Name	Value

Settings - hw\_ila\_1    Status - hw\_ila\_1    Trigger Setup - hw\_ila\_1    Capture Setup - hw\_ila\_1

Core status: ● ○ ○ ○ ○ Idle

Capture status - Window 1 of 1

Press the + button to add probes.





# Start link synchronization

- ❑ Check UART is ready and ESistream TX and RX transceivers are ready: LED0 ON and LED 1 ON
- ❑ Push SYNC button (PB0)
  - ❑ The loopback communication between ESistream TX and RX through the loopback board has started.
- ❑ Check RX LANES are ready, LED2 ON.
- ❑ Check there is no communication error, LED3 OFF.
  - ❑ If one bit error is detected on one HSSL then LED3 is turned ON.



# Acquire RX data (62-bit)

Using Vivado Integrated Logic Analyzer (ILA)

# Acquire data in Vivado using JTAG and ILA.

In hardware manager, click on play button.

**HARDWARE MANAGER** - localhost/xilinx\_tcf/Xilinx/282203141781A

There are no serial I/O links. [Auto-detect links](#) [Create links](#)

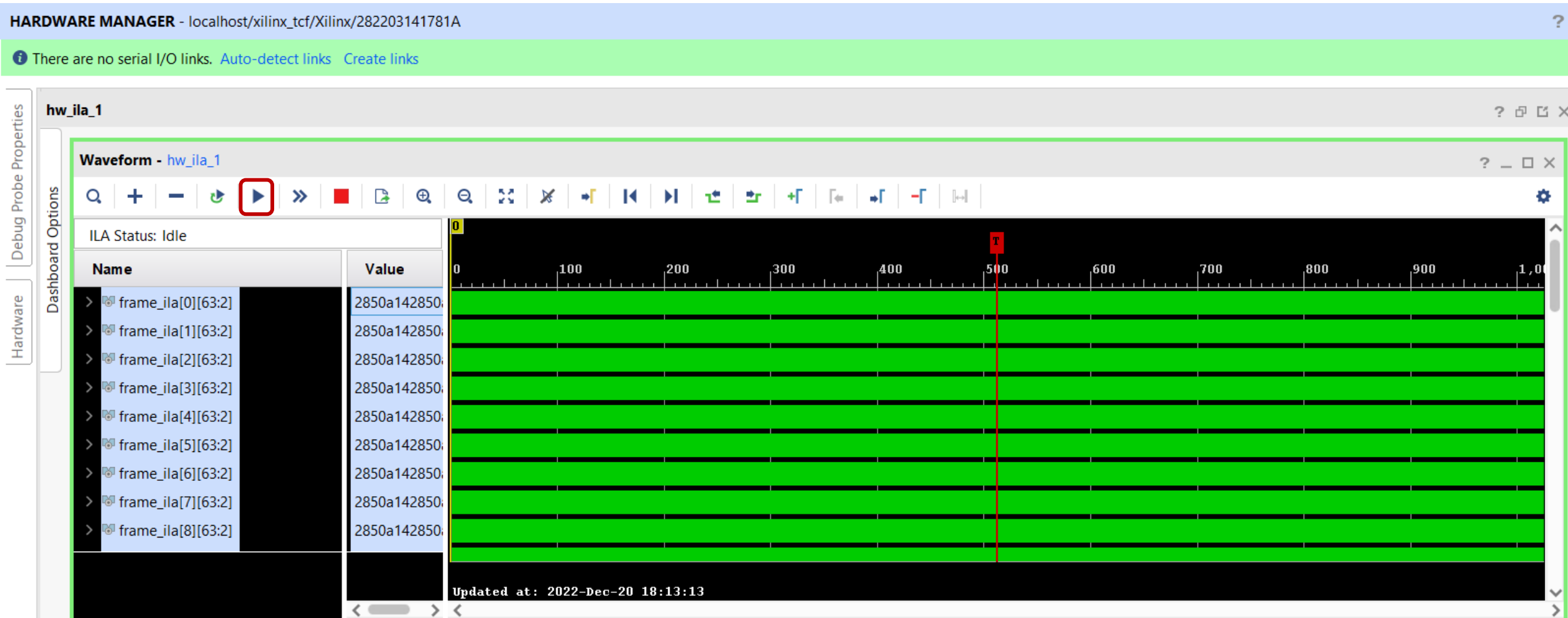
**hw\_ila\_1**

Waveform - hw\_ila\_1

ILA Status: Idle

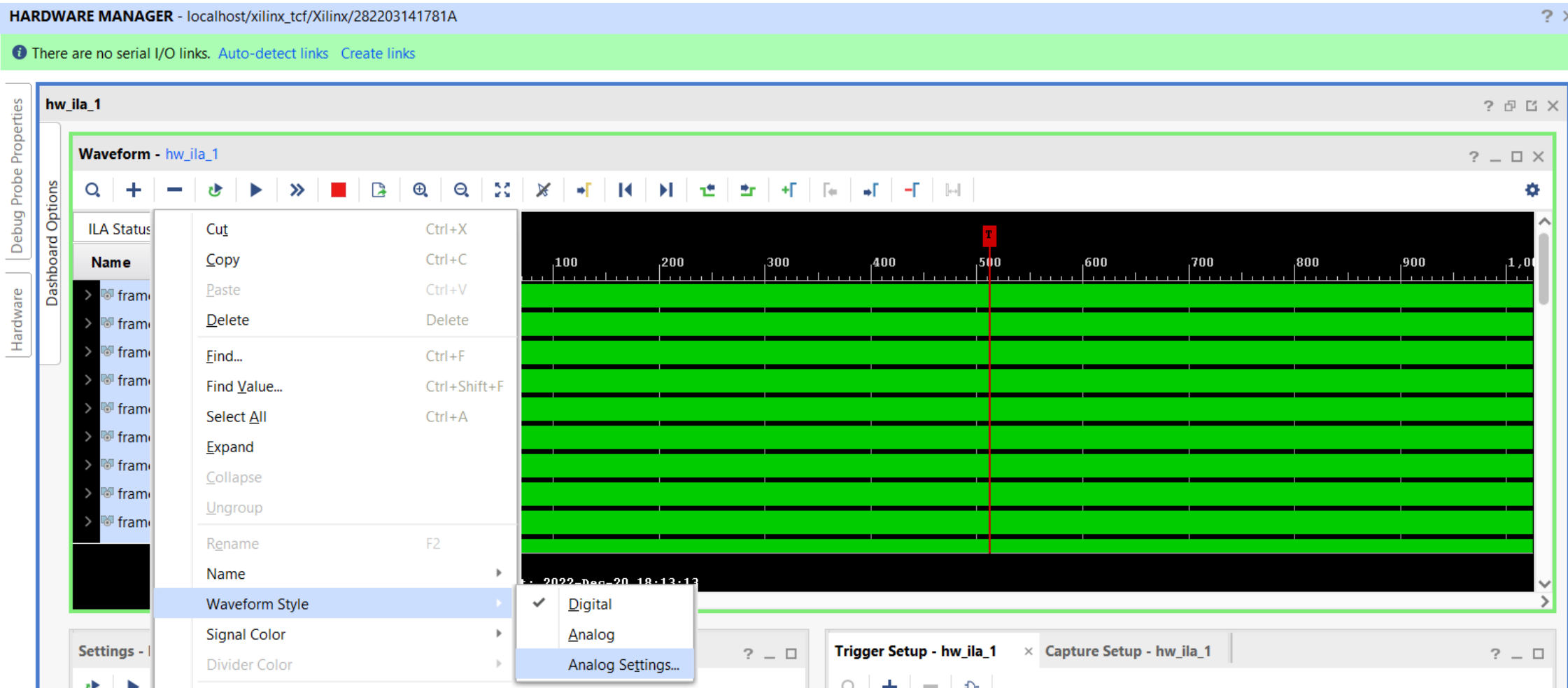
Name	Value
> frame_ila[0][63:2]	2850a142850
> frame_ila[1][63:2]	2850a142850
> frame_ila[2][63:2]	2850a142850
> frame_ila[3][63:2]	2850a142850
> frame_ila[4][63:2]	2850a142850
> frame_ila[5][63:2]	2850a142850
> frame_ila[6][63:2]	2850a142850
> frame_ila[7][63:2]	2850a142850
> frame_ila[8][63:2]	2850a142850

Updated at: 2022-Dec-20 18:13:13



# ILA Analog view

Select all lanes + right-click, then click on Waveform > Analog Settings...





# ILA Analog view

Select Hold and click on OK.

HARDWARE MANAGER - localhost/xilinx\_tcf/Xilinx/282203141781A

There are no serial I/O links. [Auto-detect links](#) [Create links](#)

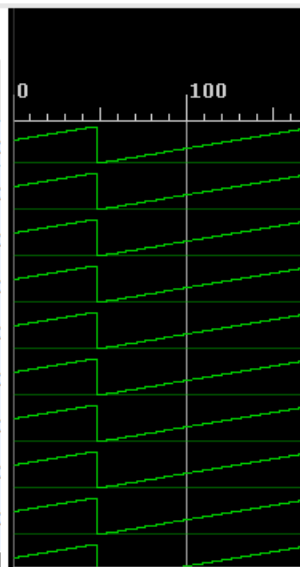
hw\_ila\_1

Waveform - hw\_ila\_1



ILA Status: Idle

Name	Value
> frame_ila[0][63:2]	2ddbb76eddt
> frame_ila[1][63:2]	2ddbb76eddt
> frame_ila[2][63:2]	2ddbb76eddt
> frame_ila[3][63:2]	2ddbb76eddt
> frame_ila[4][63:2]	2ddbb76eddt
> frame_ila[5][63:2]	2ddbb76eddt
> frame_ila[6][63:2]	2ddbb76eddt
> frame_ila[7][63:2]	2ddbb76eddt
> frame_ila[8][63:2]	2ddbb76eddt



Updated at: 2022-Dec-20 18:13:13

Analog Settings

Please specify the display settings for viewing the selected objects as analog waveforms.

Row height: 29 pixels

**Y Range**

☒ Auto  
☐ Fixed

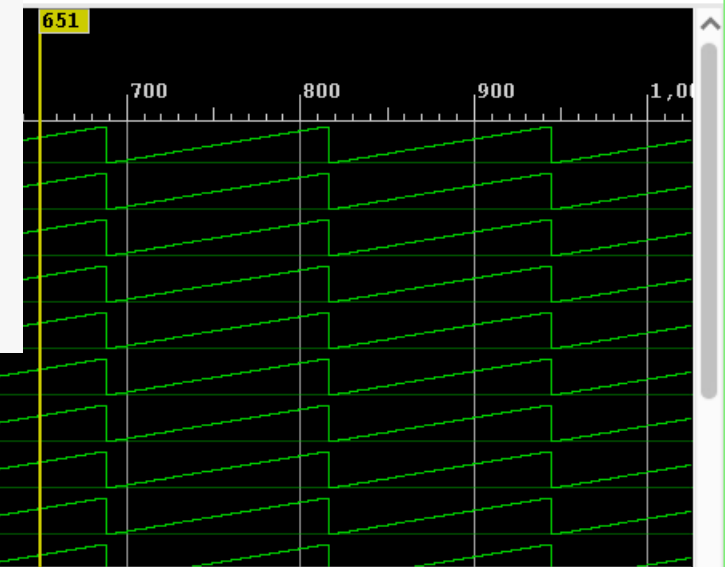
Min: 0 Max: 0

Interpolation style: ☐ Linear ☒ Hold

Off scale: ☒ Hide ☐ Clip ☐ Overlap

☒ Horizontal line Y Value: 0

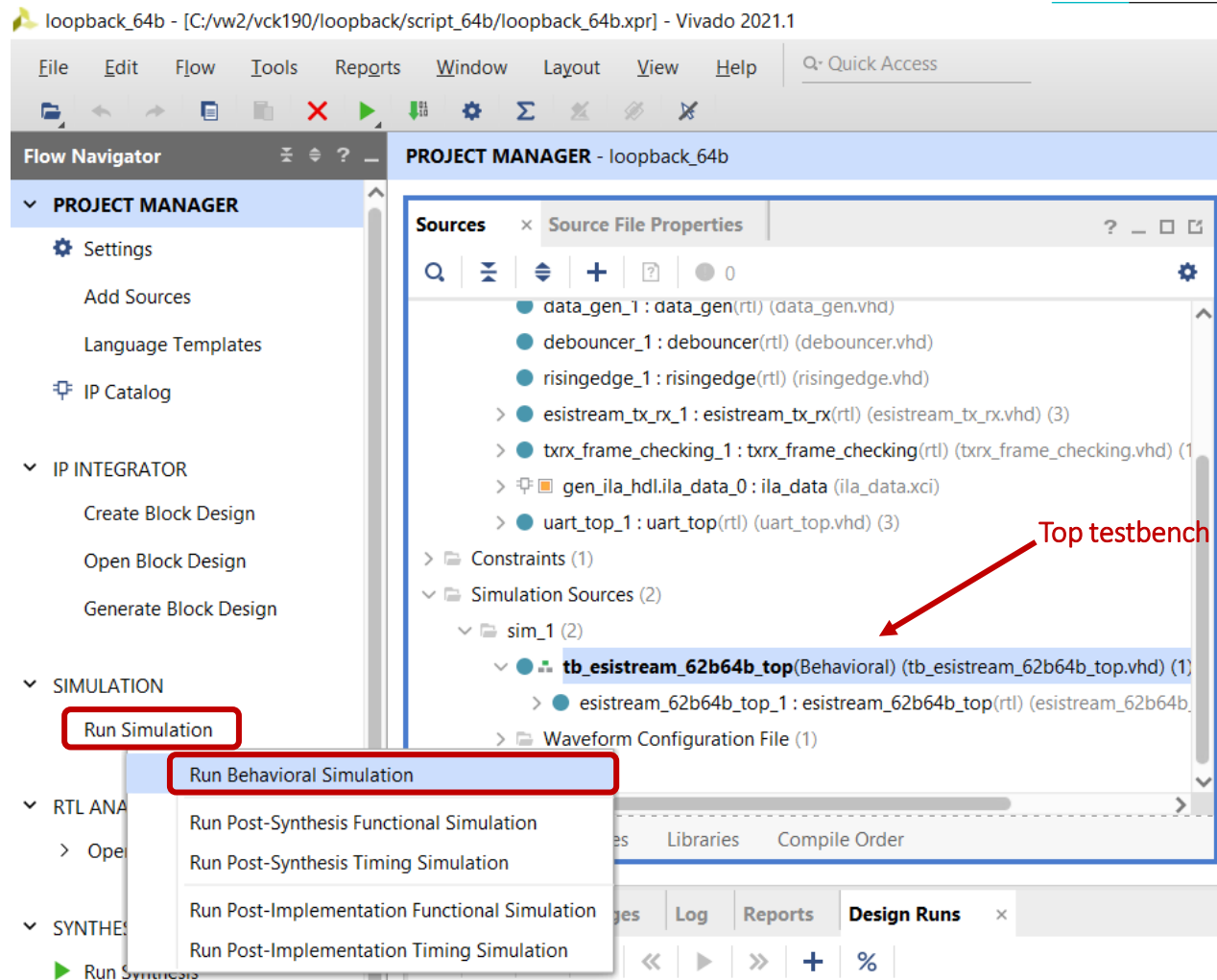
OK Cancel Apply



Design example top file  
testbench simulation

# Launch Vivado Simulator

Click on *Run simulation* and *Run Behavioral Simulation* to simulate the whole design.



# Run the simulation for 70 $\mu$ s

Click on Play button.

loopback\_64b - [C:/vw2/vck190/loopback/script\_64b/loopback\_64b.xpr] - Vivado 2021.1

File Edit Flow Tools Reports Window Layout View Run Help Q- Quick Access write\_device\_image Complete ✓

70  $\mu$ s

Flow Navigator

**PROJECT MANAGER**

- Settings
- Add Sources
- Language Templates
- IP Catalog

**IP INTEGRATOR**

- Create Block Design
- Open Block Design
- Generate Block Design

**SIMULATION**

- Run Simulation

**RTL ANALYSIS**

- Open Elaborated Design

**SYNTHESIS**

- Run Synthesis
- Open Synthesized Design

**IMPLEMENTATION**

- Run Implementation
- Open Implemented Design

**PROGRAM AND DEBUG**

**SIMULATION - Behavioral Simulation - Functional - sim\_1 - tb\_esistream\_62b64b\_top**

tb\_esistream\_62b64b\_top\_behav.wcfg\*

0.000000000 us 10.000000000 us 20.000000000 us 30.000000000 us 40.000000000 us 50.000000000 us 60.000000000 us

69.184316615 us

Name	Value
tb	
txrx_frame_checking	
esistream_tx_rx-port	
sync	0
ip_ready	1
db_en	1
cb_en	1
prbs_en	1
lanes_ready	1
be_status	0
cb_status	0
valid_status	1
data_out_62b[10:0][61:0]	13264c993264
[10][61:0]	13264c993264
[9][61:0]	13264c993264

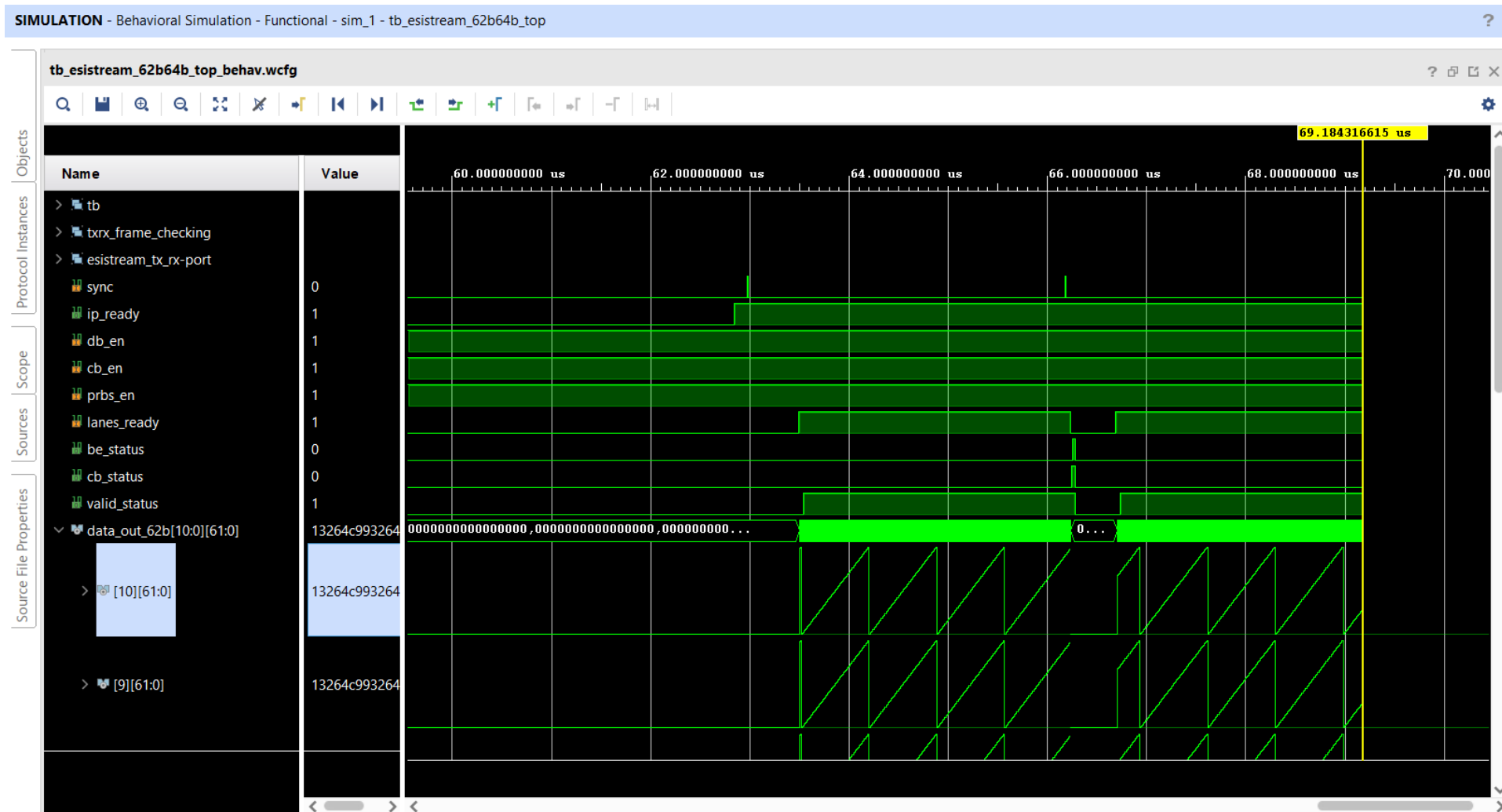
Tcl Console Messages Log

Sim Time: 69184316615 fs



# Run the simulation for 70 $\mu$ s (zoom)

25

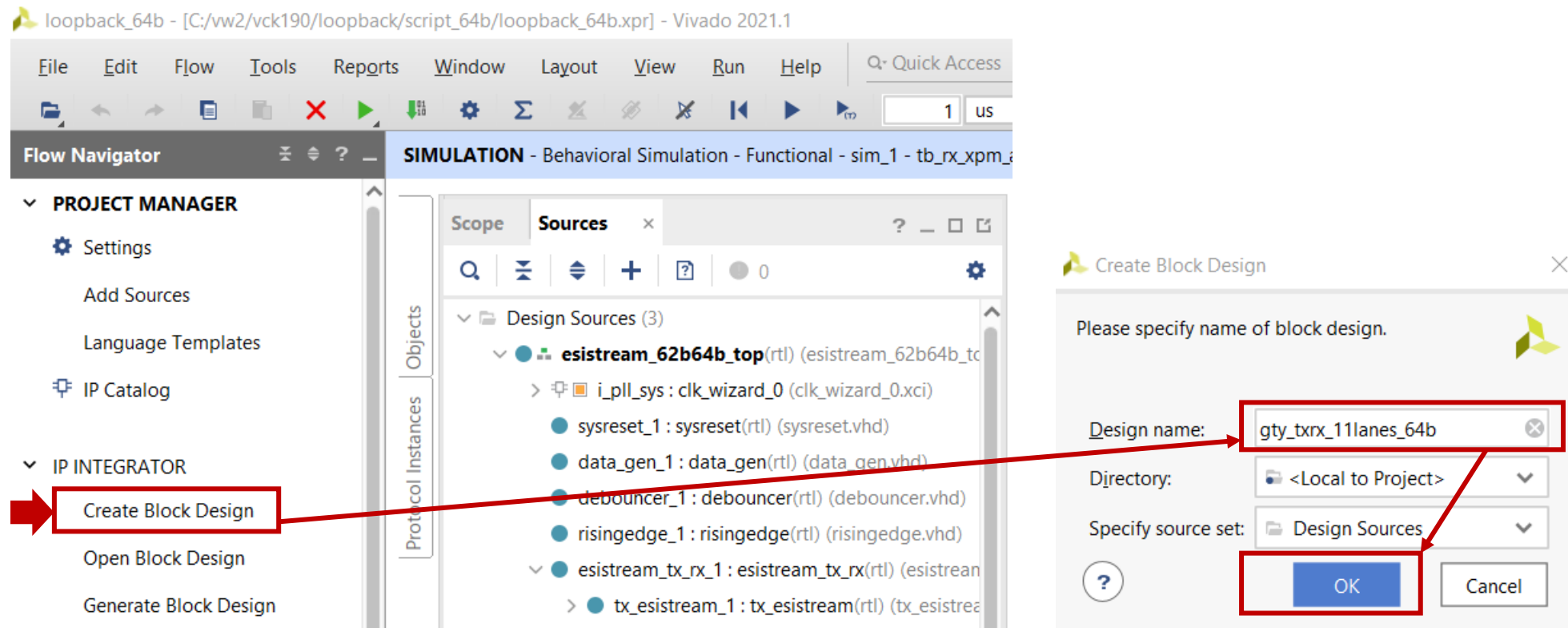


# Application Note:

Create an ESistream Gigabit Transceivers Block Design (.bd) from scratch on Versal.

# Application Note

Create ESistream Gigabit transceivers block design (.bd) from scratch.



# Application Note

Create ESStream Gigabit transceivers block design (.bd) from scratch.

The screenshot displays the Vivado 2021.1 IDE interface for a project named 'loopback\_64b'. The 'BLOCK DESIGN' tab is active, showing a design named 'gty\_txx\_11lanes\_64b'. The 'Sources' pane on the left lists the design file. The 'Diagram' pane on the right is empty, with a message: 'Design is empty. Press the + button to add IP.' A search bar in the top right of the diagram pane contains the text 'gt\_bridge\_ip', and a dropdown menu shows 'Versal ACAPs Transceivers Bridge IP' as the only match. Red arrows point to the search bar and the IP name in the dropdown, with labels 'Search for gt\_bridge\_ip' and 'Double click on Transceivers Bridge IP' respectively. Another red arrow points to the '+' button in the diagram pane. The 'Tcl Console' at the bottom shows a series of commands for updating the compile order, closing the block design, writing the design to a file, and deleting the original design file.

loopback\_64b - [C:/vw2/vck190/loopback/script\_64b/loopback\_64b.xpr] - Vivado 2021.1

File Edit Flow Tools Reports Window Layout View Help Q Quick Access

Flow Navigator

**PROJECT MANAGER**

- Settings
- Add Sources
- Language Templates
- IP Catalog

**IP INTEGRATOR**

- Create Block Design
- Open Block Design
- Generate Block Design

**SIMULATION**

- Run Simulation

**RTL ANALYSIS**

- Open Elaborated Design

**SYNTHESIS**

- Run Synthesis
- Open Synthesized Design

**BLOCK DESIGN - gty\_txx\_11lanes\_64b**

Sources Design Signals Board

gty\_txx\_11lanes\_64b

Properties

Select an object to see properties

Diagram

Search: gt\_bridge\_ip (1 match)

Versal ACAPs Transceivers Bridge IP

Design is empty. Press the + button to add IP.

Double click on Transceivers Bridge IP

Search for gt\_bridge\_ip

ENTER to select, ESC to cancel, Ctrl+Q for IP details

Tcl Console

```
update_compile_order -fileset sources_1
close_bd_design [get_bd_designs gty_txx_11lanes_64b]
Wrote : <C:/vw2/vck190/loopback/script_64b/loopback_64b.srcs/sources_1/bd/gty_txx_11lanes_64b/ui/bd_ad2b302a.ui>
export_ip_user_files -of_objects [get_files C:/vw2/vck190/loopback/script_64b/loopback_64b.srcs/sources_1/bd/gty_txx_11lanes_64b/gty_txx_11lanes_64b.bd] -no_script -re
remove_files C:/vw2/vck190/loopback/script_64b/loopback_64b.srcs/sources_1/bd/gty_txx_11lanes_64b/gty_txx_11lanes_64b.bd
file delete -force C:/vw2/vck190/loopback/script_64b/loopback_64b.srcs/sources_1/bd/gty_txx_11lanes_64b
```

# Application Note

Create ESIstream Gigabit transceivers block design (.bd) from scratch.

The screenshot displays the Vivado 2021.1 IDE interface for a project named 'loopback\_64b'. The main workspace is titled 'BLOCK DESIGN - gty\_txxr\_11lanes\_64b \*'. The interface is divided into several panes:

- Flow Navigator (Left):** Contains the 'PROJECT MANAGER' and 'IP INTEGRATOR' sections. The 'IP INTEGRATOR' section is active, showing options like 'Create Block Design', 'Open Block Design', and 'Generate Block Design'.
- Sources (Top Left):** Lists the project sources, including 'gty\_txxr\_11lanes\_64b' and 'gt\_bridge\_ip\_0 (Versal ACAPs Transceivers Bridge IP:1.1)'.
- Properties (Bottom Left):** A pane for viewing the properties of the selected object.
- Diagram (Center):** Shows the block design diagram. A red arrow points to the 'gt\_bridge\_ip\_0' block, with the text 'Double click on Transceivers Bridge IP' overlaid. The block's pin list is visible on the right side of the diagram.
- Tcl Console (Bottom):** Displays the command history and output for the 'create\_bd\_design' command.

The Tcl Console shows the following commands and output:

```
export_ip_user_files -of_objects [get_files C:/vw2/vck190/loopback/script_64b/loopback_64b.srcs/sources_1/bd/gty_txxr_11lanes_64b/gty_txxr_11lanes_64b.bd] -no_script -re
remove_files C:/vw2/vck190/loopback/script_64b/loopback_64b.srcs/sources_1/bd/gty_txxr_11lanes_64b/gty_txxr_11lanes_64b.bd
file delete -force C:/vw2/vck190/loopback/script_64b/loopback_64b.srcs/sources_1/bd/gty_txxr_11lanes_64b
file delete -force c:/vw2/vck190/loopback/script_64b/loopback_64b.gen/sources_1/bd/gty_txxr_11lanes_64b
create_bd_design "gty_txxr_11lanes_64b"
Wrote : <C:\vw2\vck190\loopback\script_64b\loopback_64b.srcs\sources_1\bd\gty_txxr_11lanes_64b\gty_txxr_11lanes_64b.bd>
```

# Application Note

Create ESStream Gigabit transceivers block design (.bd) from scratch.

Re-customize IP

X

Re-customize IP

X

## Versal ACAPs Transceivers Bridge IP (1.1)



Documentation IP Location

☐ Show disabled ports

Component Name

☐ Pass Through Mode

☒ Master Reset Enable

Transceiver type

Preset

GT direction

Number of Lanes  [1 - 20]

TX Master CLK source

RX Master CLK source

Transceiver Configs

OK

Cancel

## Versal ACAPs Transceivers Bridge IP (1.1)



Documentation IP Location

☐ Show disabled ports

Component Name

☒ Pass Through Mode

☒ Master Reset Enable

Transceiver type

Preset

GT direction

Number of Lanes  [1 - 20]

TX Master CLK source

RX Master CLK source

Transceiver Configs

OK

Cancel

# Application Note

Create ESistream Gigabit transceivers block design (.bd) from scratch.

Transceiver Configs

**Configure**

Protocols Presets Switch to Defaults

**CONFIG0**

**System**

Transceiver configuration preset: Start from scratch Transceiver type: GTY

**Configurations**

**TX Configurations**

Line rate (Gb/s): 10.3125 [1.2 - 28.21]

PLL type: LCPLL

**Reference clock Frequency**

Requested Reference Clock (MHz): 156.25 [60 - 820]

Actual Reference Clock (MHz): 156.250000000000

☐ Enablement of fractional feedback divider

Requested Reference Clock Source: R0

R0-R5 are logical ports.  
Refer summary.log in IP Sources area,  
for information on refclk ports and its associated frequencies

☐ PCIE enable

Encoding: RAW

User data width: 32

Internal data width: 32

Buffer: Enable (1)

**RX Configurations**

Line rate (Gb/s): 10.3125 [1.2 - 28.21]

PLL type: LCPLL

**Reference clock Frequency**

Requested Reference Clock (MHz): 156.25 [60 - 820]

Actual Reference Clock (MHz): 156.250000000000

☐ Enablement of fractional feedback divider

Requested Reference Clock Source: R0

R0-R5 are logical ports.  
Refer summary.log in IP Sources area,  
for information on refclk ports and its associated frequencies

Decoding: RAW

User data width: 32

Internal data width: 32

Buffer: Enable (1)

Clock alignment logic: Fast Sync

OK Cancel



# Application Note

Create ESistream Gigabit transceivers block design (.bd) from scratch.

Transceiver Configs

**Configure**

Protocols Presets Switch to Defaults

**CONFIG0**

**Configurations**

**TX Configurations**

Line rate (Gb/s) 12.8 [1.2 - 28.21]

PLL type LCPLL

**Reference clock Frequency**

Requested Reference Clock (MHz) 200.0 [60 - 820]

Actual Reference Clock (MHz) 200.00000000000000

☐ Enablement of fractional feedback divider

Requested Reference Clock Source R0

R0-R5 are logical ports.  
Refer summary.log in IP Sources area,  
for information on refclk ports and its associated frequencies

☐ PCIe enable

Encoding RAW

User data width 64

Internal data width 64

Buffer Enable (1)

Clock alignment logic Fast Sync

TXOUTCLK source TXOUTCLKPMA

**RX Configurations**

Line rate (Gb/s) 12.8 [1.2 - 28.21]

PLL type LCPLL

**Reference clock Frequency**

Requested Reference Clock (MHz) 200.0 [60 - 820]

Actual Reference Clock (MHz) 200.00000000000000

☐ Enablement of fractional feedback divider

Requested Reference Clock Source R0

R0-R5 are logical ports.  
Refer summary.log in IP Sources area,  
for information on refclk ports and its associated frequencies

Decoding RAW

User data width 64

Internal data width 64

Buffer Enable (1)

Clock alignment logic Fast Sync

Receiver elastic buffer bypass mode Multi-lane mode

RXOUTCLK source RXOUTCLKPMA

OK Cancel

# Application Note

Create ESistream Gigabit transceivers block design (.bd) from scratch.

**BLOCK DESIGN - gty\_txx\_11lanes\_64b \***

**Sources** | **Design** | **Signals** | **Board**

gt\_y\_txx\_11lanes\_64b  
gt\_bridge\_ip\_0 (Versal ACAPs Transceivers Bridge IP:1.1)

**Block Properties**

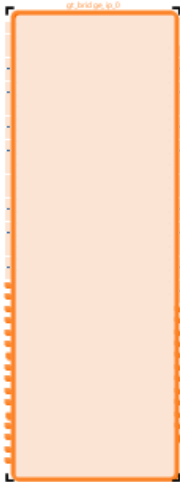
gt\_bridge\_ip\_0

Name: gt\_bridge\_ip\_0

**General** | Properties | IP

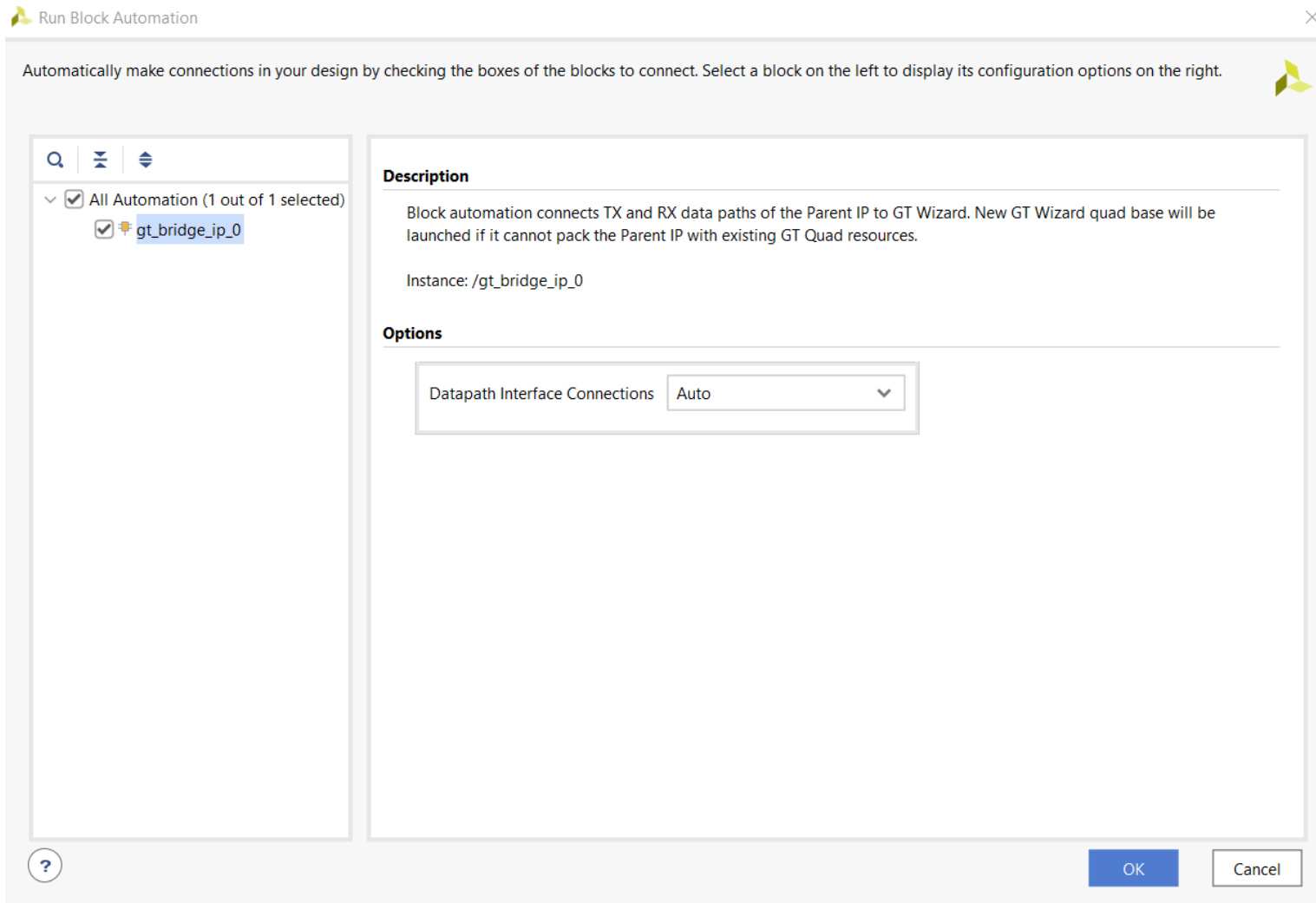
**Diagram**

Designer Assistance available. [Run Block Automation](#) [Run Connection Automation](#)



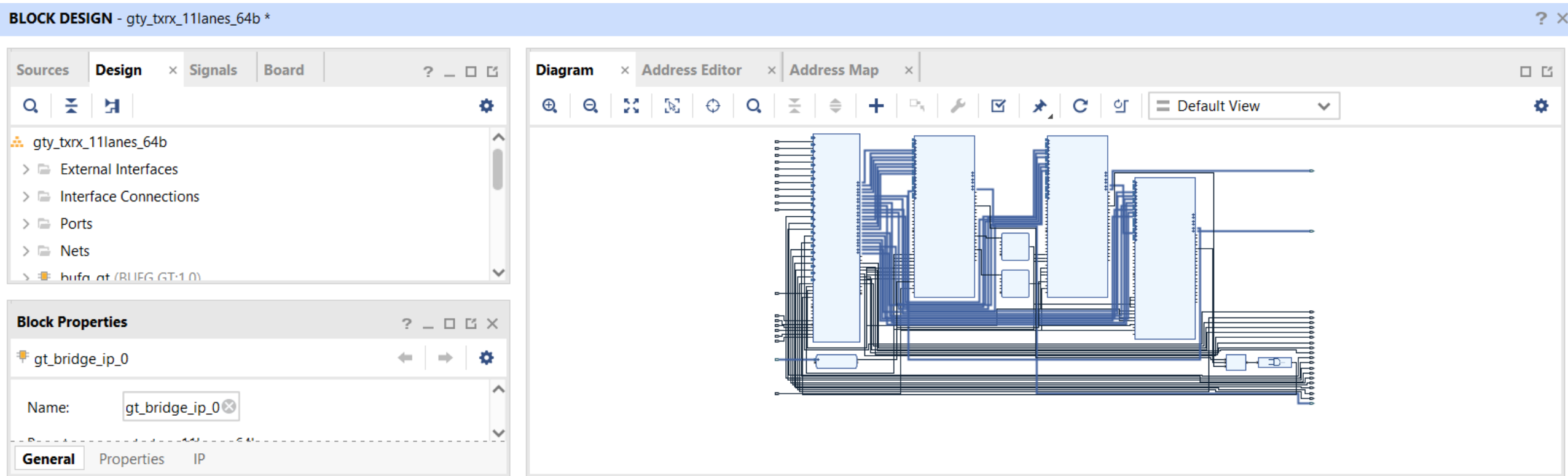
# Application Note

Create ESistream Gigabit transceivers block design (.bd) from scratch.



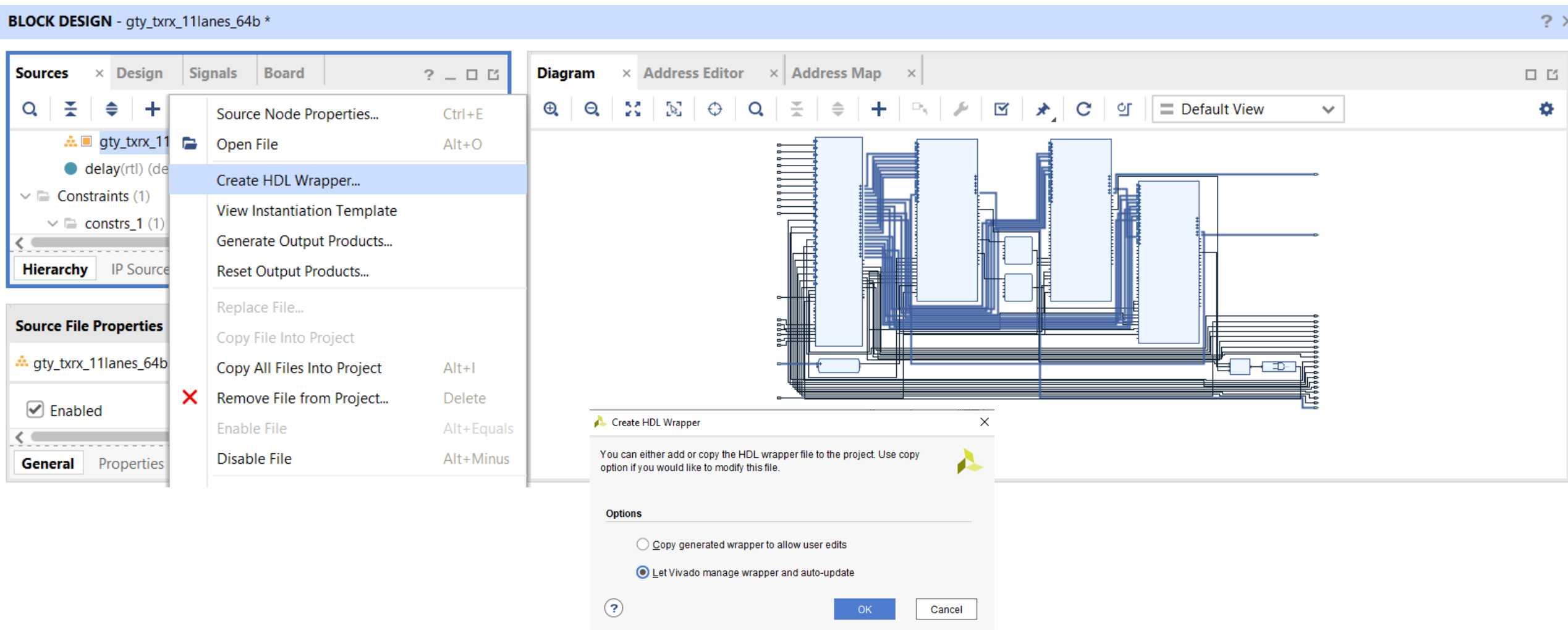
# Application Note

Create ESistream Gigabit transceivers block design (.bd) from scratch.



# Application Note

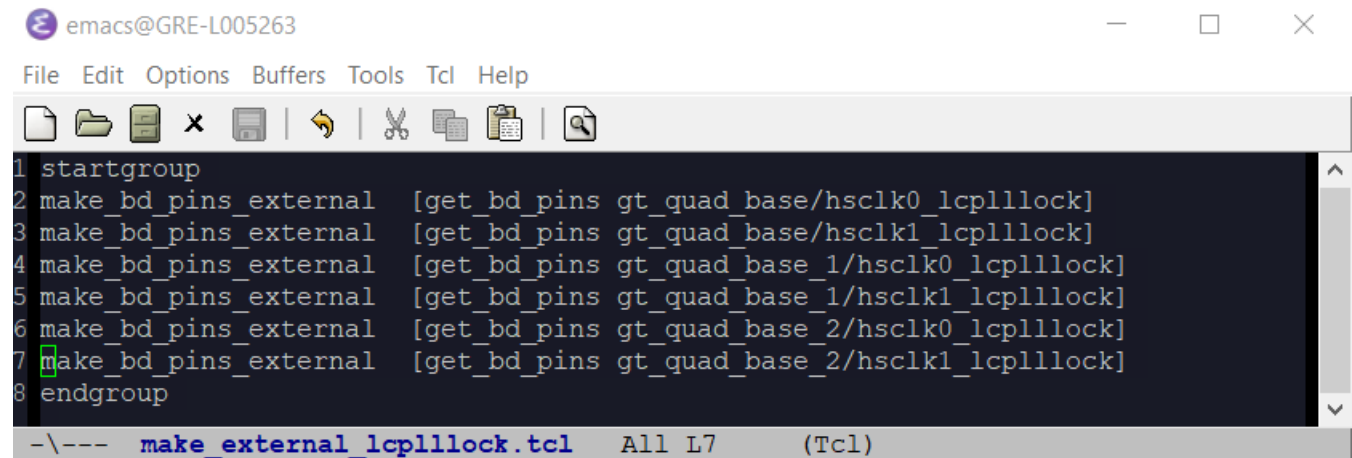
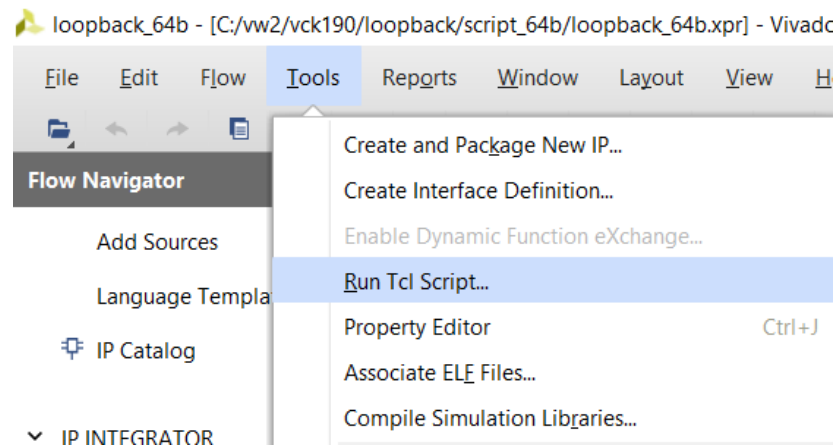
Create ESistream Gigabit transceivers block design (.bd) from scratch.



# Application Note

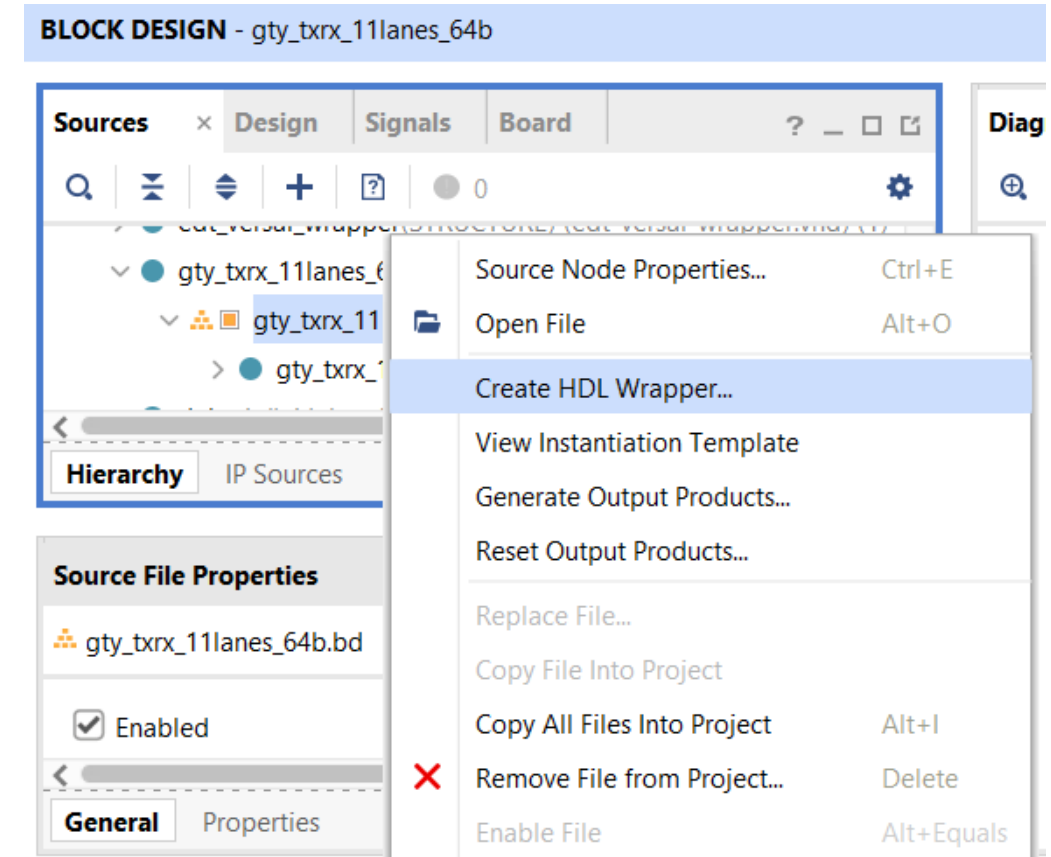
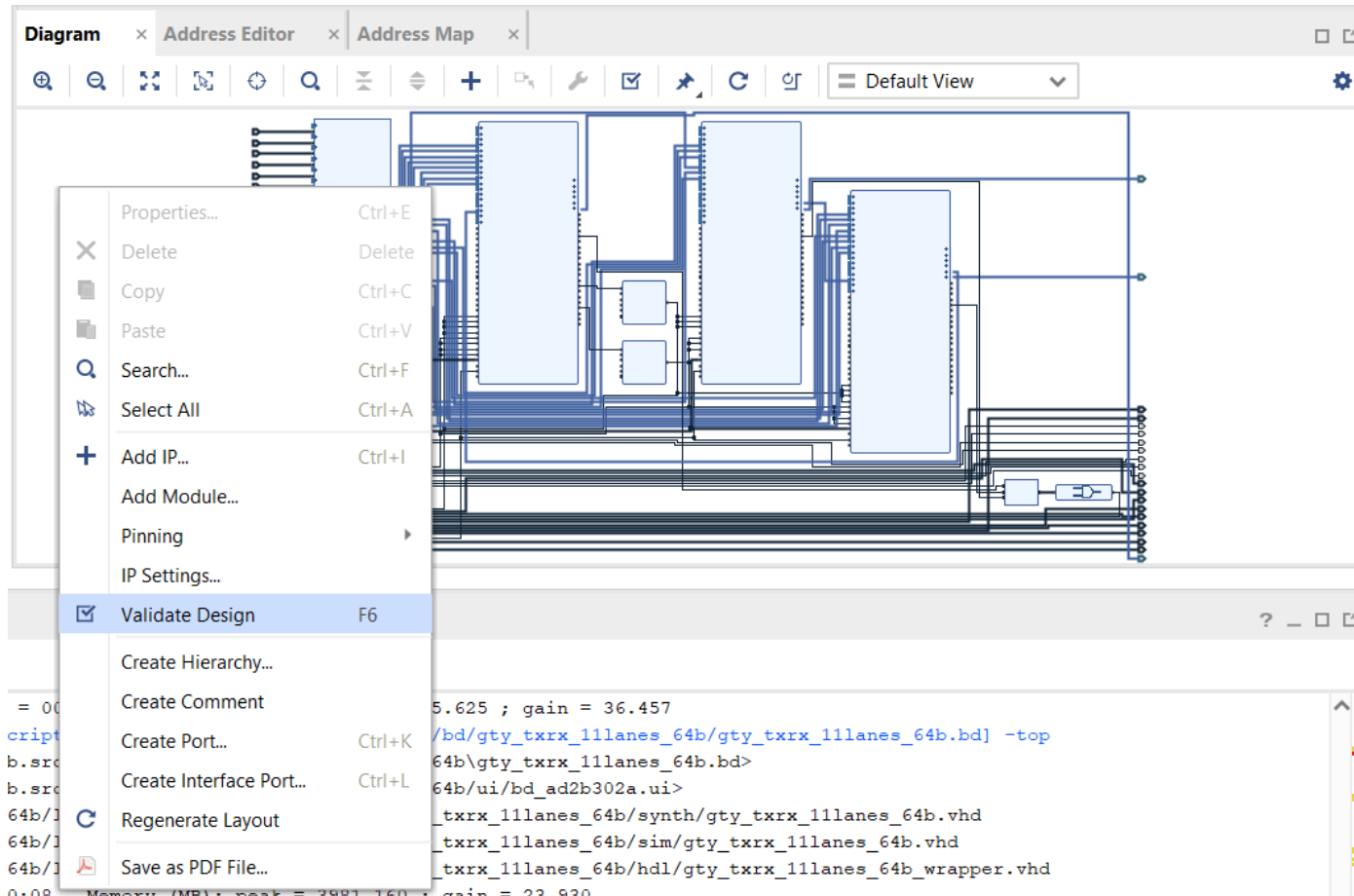
Create ESistream Gigabit transceivers block design (.bd) from scratch.

- ❑ Make external hsc1k0\_lcp1llock, hsc1k1\_lcp1llock signals from gt\_quad\_base, gt\_quad\_base\_1 and gt\_quad\_base\_2
- ❑ Tools > Run Tcl Script...
- ❑ Launch make\_external\_lcp1llock.tcl
- ❑ The Validate design and Create HDL wrapper...



# Application Note

Create ESIstream Gigabit transceivers block design (.bd) from scratch.





UART

# UART - FPGA interface protocol

## Write command

- The design embeds a UART slave which uses the following configuration:
  - Baud rate: 115200
  - Data Bits: 8
  - No parity

The UART frames layer protocol defined here allows to perform read and write operations on the registers listed in the register map.

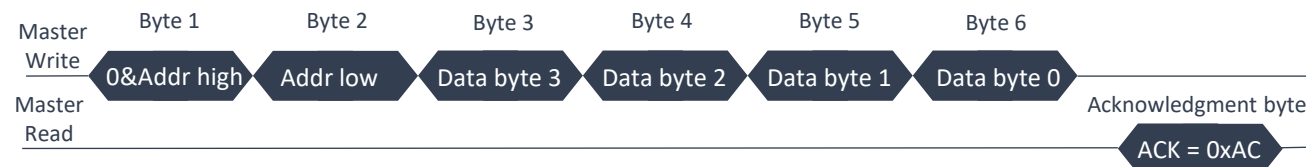
### Register Write operation:

The UART master must send the data in the order described on the figure below to be able to write a FPGA register.

Firstly, the master send the 15-bit register address and then the 32-bit data word.

- The **most significant bit of the first transmitted byte (bit 7) must be set to 0 for write operation.**
- The bits 6 down to 0 of the first transmitted byte contain the bit 14 down to 8 of the register address.
- The second byte contains the bit 7 down to 0 of the register address.
- The third byte contains the bit 31 down to 24 of the register data.
- The fourth byte contains the bit 23 down to 16 of the register data.
- The fifth byte contains the bit 15 down to 8 of the register data.
- The sixth byte contains the bit 7 down to 0 of the register data.

Finally, the master read the acknowledgment word to check that the communication has been done correctly. The acknowledgment word is a single byte of value 0xAC (172 is the decimal value).



# UART - FPGA interface protocol

## Read command

- The design embeds a UART slave which uses the following configuration:
  - Baud rate: 115200
  - Data Bits: 8
  - No parity

The UART frames layer protocol defined here allows to perform read and write operations on the registers listed in the register map.

### Register Read Operation

The UART master must send the data in the order described on the figure below to be able to read a FPGA register value. Firstly, the master send the 15-bit register address.

- The **most significant bit of the first transmitted byte (bit 7) must be set to 1 for read operation.**
- The bits 6 down to 0 of the first transmitted byte contain the bit 14 down to 8 of the register address.
- The second byte contains the bit 7 down to 0 of the register address.

Then, the master read the data and the acknowledgment word to check that the communication has been done correctly. The acknowledgment word is a single byte of value 0xAC (172 is the decimal value).

- The third byte contains the bit 31 down to 24 of the register data.
- The fourth byte contains the bit 23 down to 16 of the register data.
- The fifth byte contains the bit 15 down to 8 of the register data.
- The sixth byte contains the bit 7 down to 0 of the register data.

