ESRG
Embedded Systems
Research Group

CENTROALGORITMI

Project Status

PIEIC

Oscilloscope based in FPGA

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COMPETE

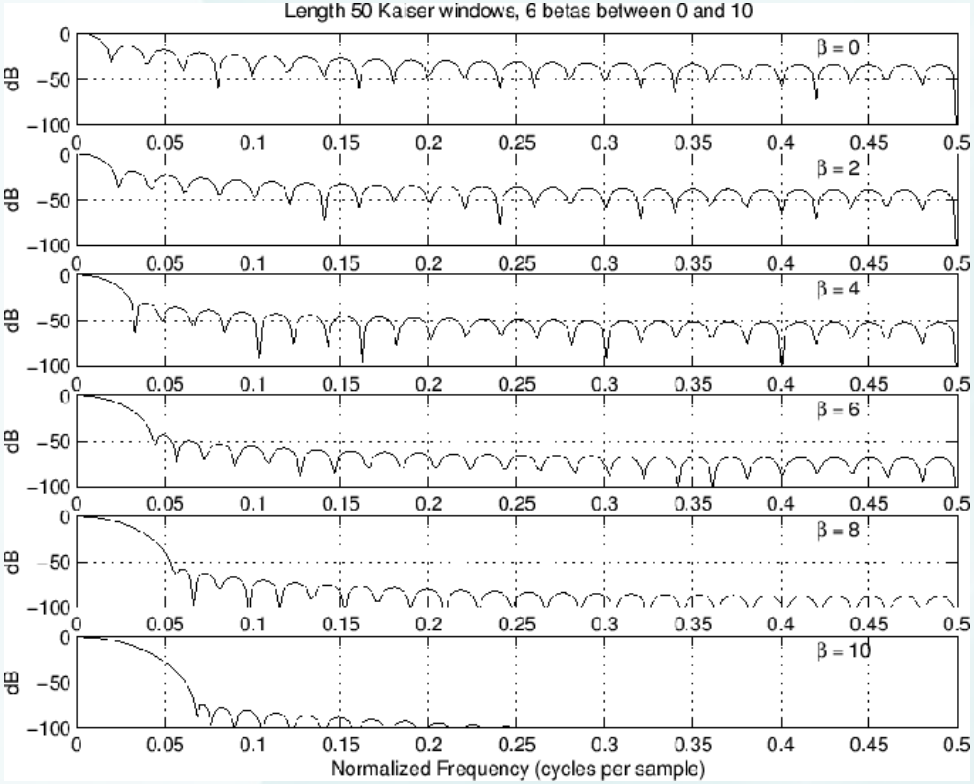
QREN Quadro de Referência Estratégico Nacional

União Europeia
Fundo Europeu de Desenvolvimento Regional

FCT Fundação para a Ciência e a Tecnologia
Ministério da Ciência, Tecnologia e Ensino Superior

Why Kaiser Window is best?

- Computes a length *n* window with parameter *beta*
- **One-parameter family** of window functions (*beta*)
  - **Trade-off** between main lobe width and secondary lobe attenuation
  - As ***beta* increases,** the relative sidelobe **attenuation decreases** and the **main lobe width increases**



Fixed-Point Arithmetics

Fixed-Point Arithmetic


```
1   #ifndef __FIXED_POINT_H__
2   #define __FIXED_POINT_H__
3
4   typedef uint16_t fixed_point_t;
5
6   #define FIXED_POINT_LEN     16
7   #define FRACTION_BITS       15
8
9   #endif // !__FIXED_POINT_H__
```

```
% get filter attributes
[coefs, M] = low_pass_filter(1000, [20 60], [0.1 0.1]);
% convert to fixed-point (15 fraction bit)
x_coefs = round(coefs * 2^15);
```

Fixed-Point Arithmetic


```c
/* Low Pass Filter
* Sampling freq: 1000 Hz
* Passband freq: 20 Hz
* Stopband freq: 60 Hz
* Ripples: 0.1
*/
// filter order
#define _M_ 28
// filter coefficients
const float coefs[_M_ + 1] =
{
    0.014604,0.022937,0.031619,0.040364,0.048874,
    0.056849,0.064003,0.070075,0.074839,0.078118,
    0.07979,0.07979,0.078118,0.074839,0.070075,
    0.064003,0.056849,0.048874,0.040364,0.031619,
    0.022937,0.014604
};

const fixed_point_t x_coefs[_M_ + 1] =
{
    479,752,1036,1323,1602,1863,2097,2296,
    2452,2560,2615,2615,2560,2452,2296,
    2097,1863,1602,1323,1036,752,479
};

int main(int argc, char *argv[])
{
    printf("\nfloating point coefs size: %d bytes\n", sizeof(coefs));
    printf("fixed point coefs size: %d bytes\n\n", sizeof(x_coefs));
    return 0;
}
```

```
PS C:\code> gcc -o main .\test.c
PS C:\code> ./main

floating point coefs size: 116 bytes
fixed point coefs size: 58 bytes
```

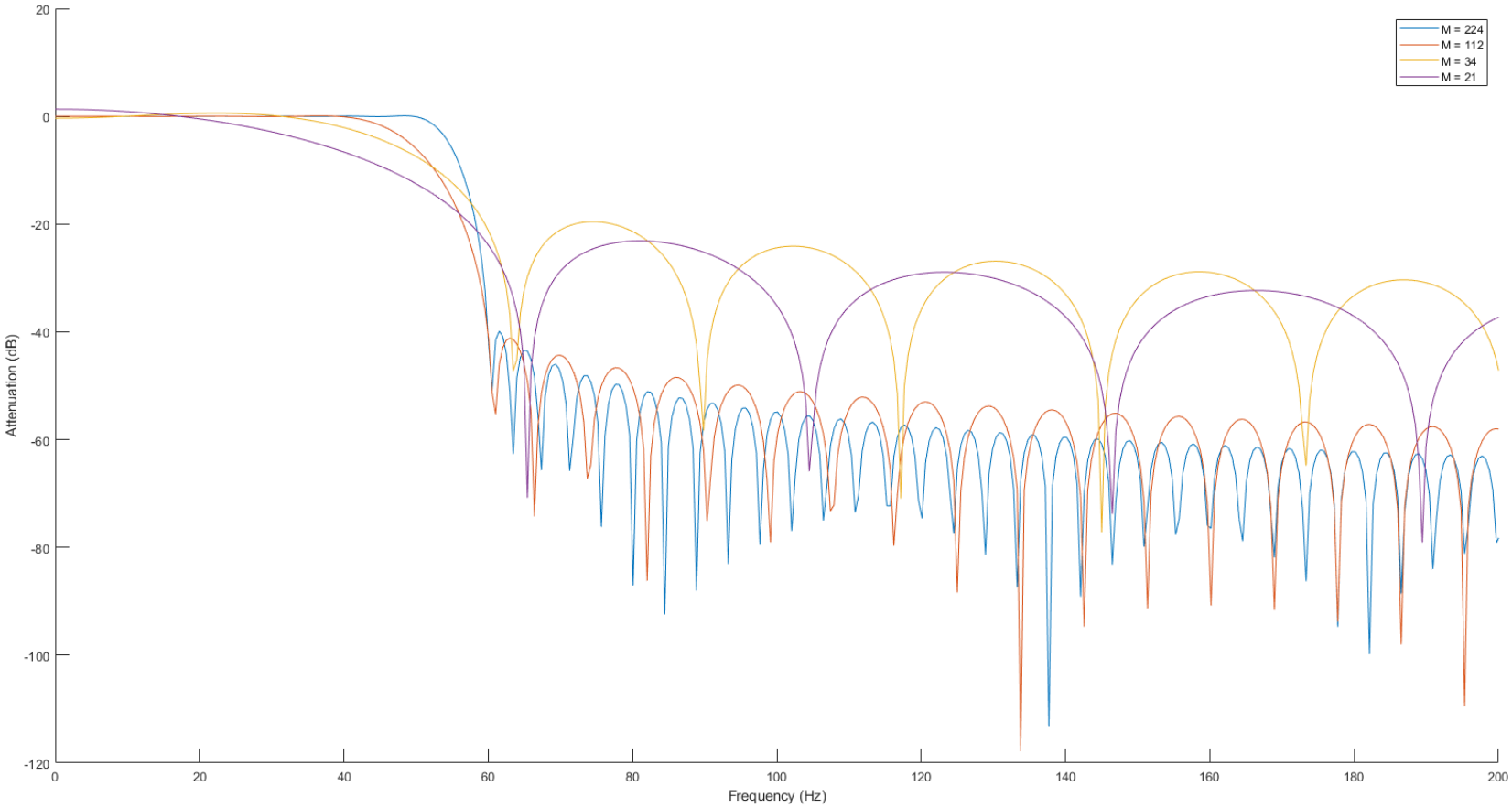
Fixed-Point Arithmetic


```c
void ADC_Callback(filter_t *filter)
{
  uint16_t y;
  uint16_t adcValue;

  // sample value
  adcValue = ADC_GetValue();

  // apply selected filter
  y = filter_calc(&filter, adcValue);
  // convert fixed-point to uint
  y *= pow(2, -FRACTION_BITS);

  // Send filtered signal to DAC
  output(y);
}
```

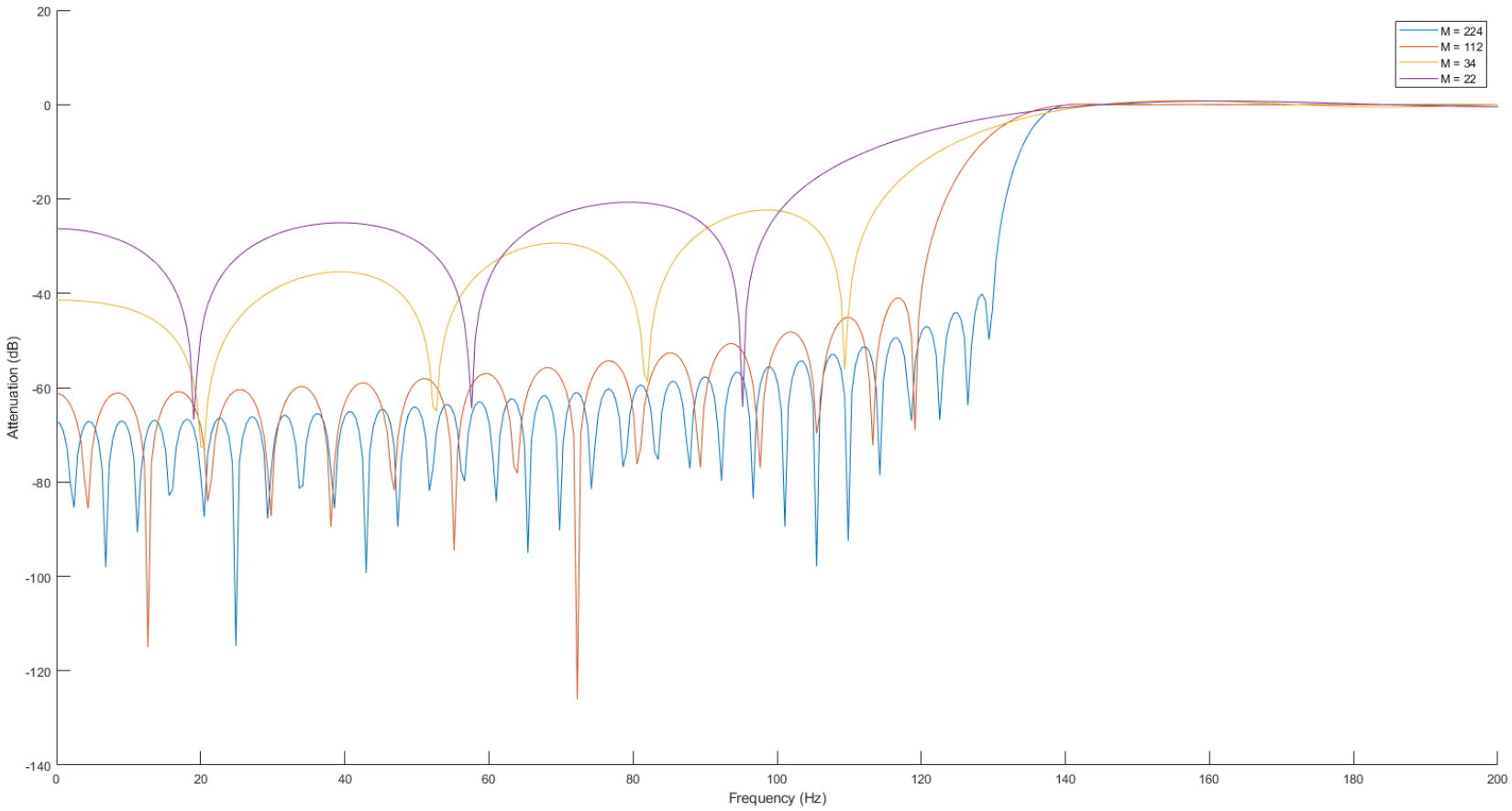
```c
int filter_calc(filter_t *ft, fixed_point_t x)
{
    int y = 0;
    int i = ft->M;

    while(i != 0)
    {
        // Update x_ant values
        ft->x_ant[i] = ft->x_ant[i-1];
        // Add to y only the x_ant values
        y += ft->x_coefs[i] * ft->x_ant[i];
        i--;
    }
    // Update last received X value
    ft->x_ant[0] = x;
    // Add it to y
    y += ft->x_coefs[i] * ft->x_ant[i];

    // add dc component
    y += ft->dc;

    // Return filtered (x) value
    return y;
}
```

Different Order Filters Comparison

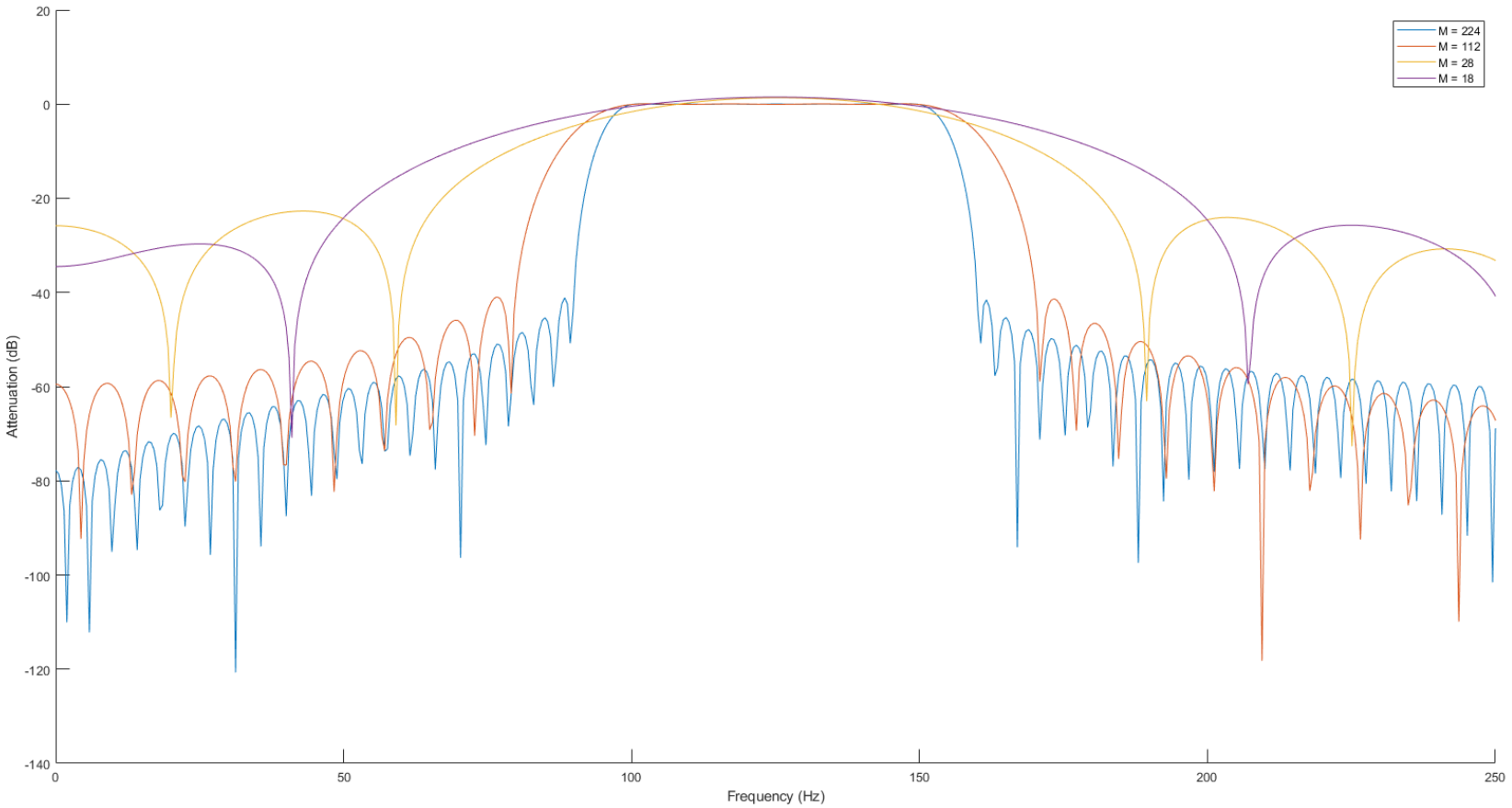
Low Pass Filter



High Pass Filter

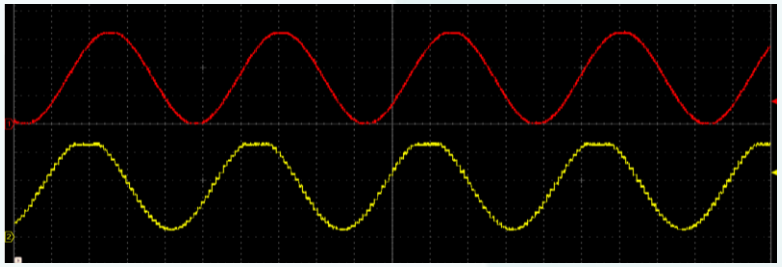


Band Pass Filter

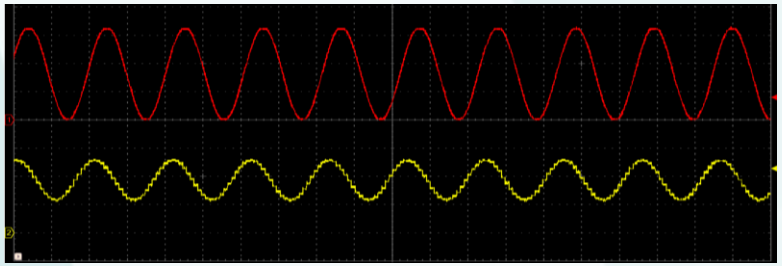


LPF response

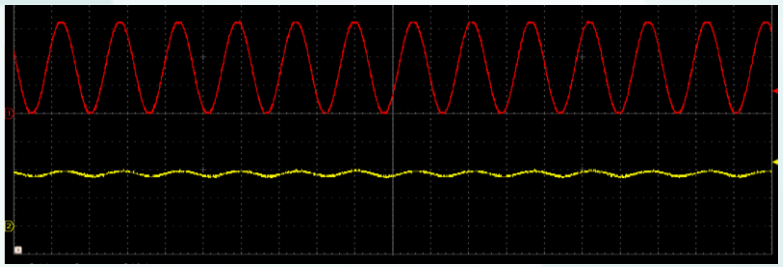
- M=90
  - 20 Hz



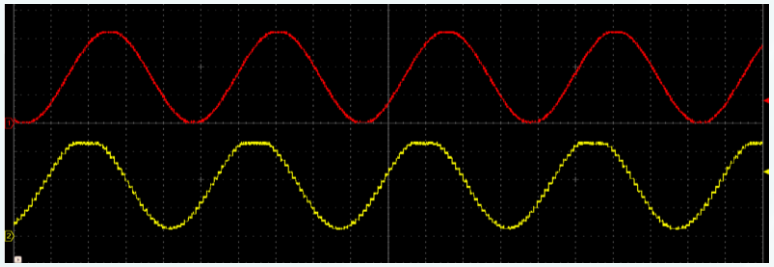
  - 50 Hz



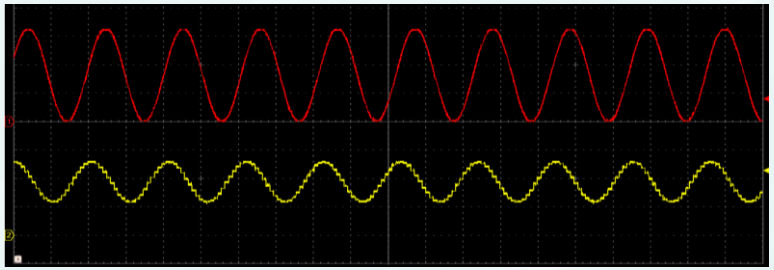
  - 100 Hz



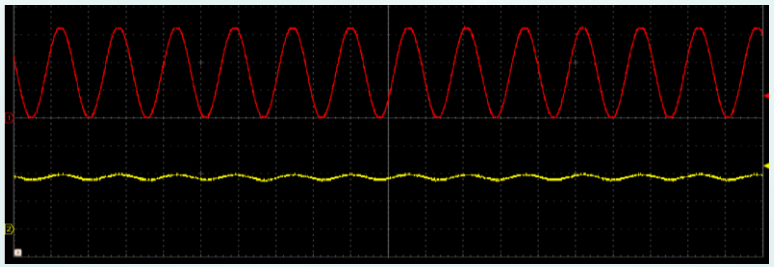
- M=28
  - 20 Hz



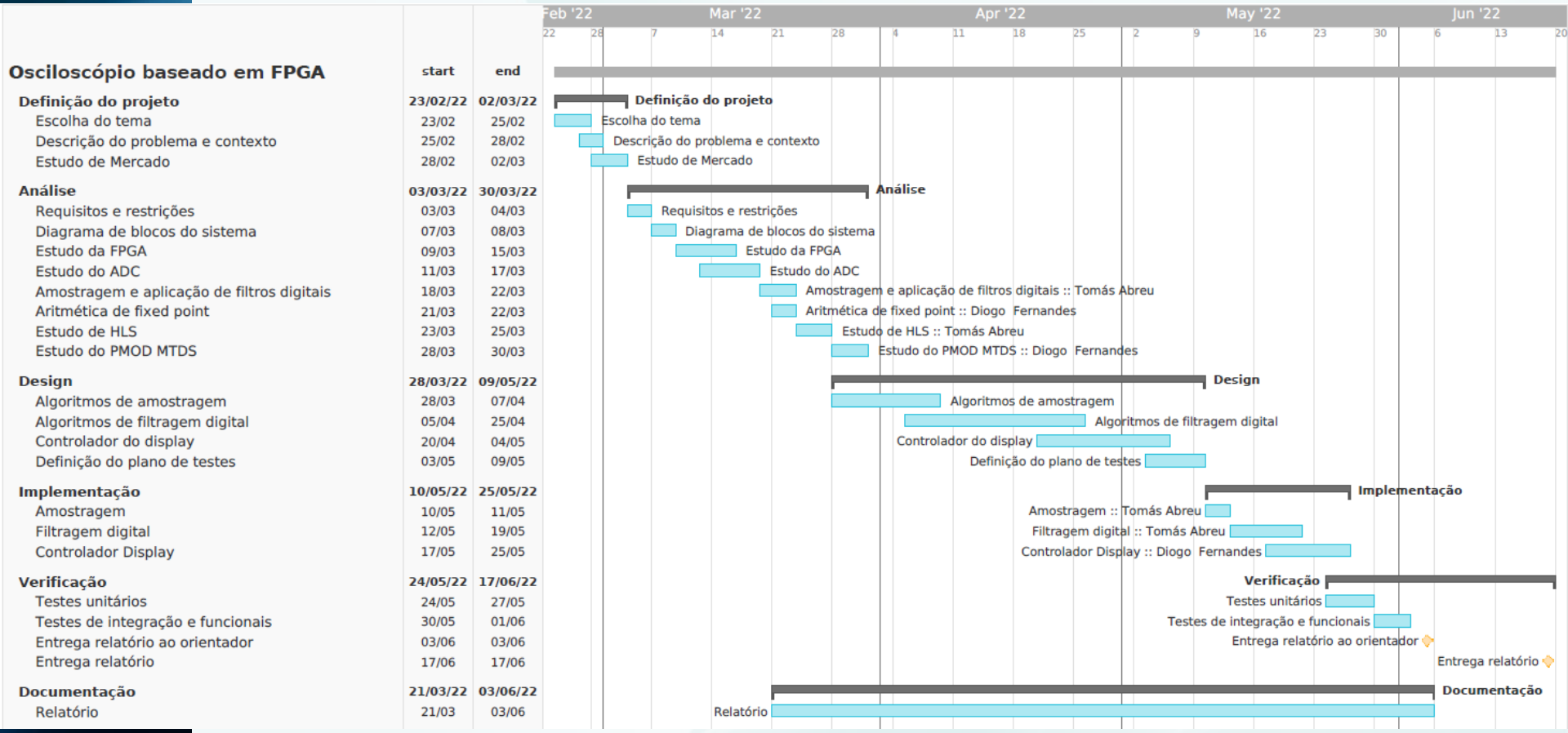
  - 50 Hz



  - 100 Hz



Gantt Diagram



Osciloscópio baseado em FPGA	start	end
Definição do projeto	**23/02/22**	**02/03/22**
Escolha do tema	23/02	25/02
Descrição do problema e contexto	25/02	28/02
Estudo de Mercado	28/02	02/03
Análise	**03/03/22**	**30/03/22**
Requisitos e restrições	03/03	04/03
Diagrama de blocos do sistema	07/03	08/03
Estudo da FPGA	09/03	15/03
Estudo do ADC	11/03	17/03
Amostragem e aplicação de filtros digitais	18/03	22/03
Aritmética de fixed point	21/03	22/03
Estudo de HLS	23/03	25/03
Estudo do PMOD MTDS	28/03	30/03
Design	**28/03/22**	**09/05/22**
Algoritmos de amostragem	28/03	07/04
Algoritmos de filtragem digital	05/04	25/04
Controlador do display	20/04	04/05
Definição do plano de testes	03/05	09/05
Implementação	**10/05/22**	**25/05/22**
Amostragem	10/05	11/05
Filtragem digital	12/05	19/05
Controlador Display	17/05	25/05
Verificação	**24/05/22**	**17/06/22**
Testes unitários	24/05	27/05
Testes de integração e funcionais	30/05	01/06
Entrega relatório ao orientador	03/06	03/06
Entrega relatório	17/06	17/06
Documentação	**21/03/22**	**03/06/22**
Relatório	21/03	03/06

Report Outline

- Introdução
  - Definição do problema
  - Estudo de mercado
- Estado da Arte
  - Amostragem
  - Filtros Digitais
  - Aritmética de fixed point
- Análise
  - Requisitos e restrições
  - Diagrama de blocos do sistema
- Especificação do Sistema
  - Placa de desenvolvimento Zybo Z7-10
  - ADC
  - …
  - Display PMOD MTDS
- Desenho do Sistema
  - Algoritmos de Amostragem
  - Algoritmos de Filtragem Digital
  - Controlador do Display
  - Definição do plano de testes
- Implementação do Sistema
- Resultados Experimentais

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Questions?