

# Vivado

## Initiation

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# Installation

- Download Vivado/Vitis installer:
  - <https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools.html>
  - Create an account and login to be able to download Vivado

## Version

2021.2

2021.1

2020.3

Vivado Archive

ISE Archive

CAE Vendor Libraries

Archive

## Vivado ML Edition - 2021.2 Full Product Installation

### Important Information

Vivado ML 2021.2 is now available for download:

- New device support for Artix® UltraScale+™: XCAU20P and XCAU25P
- Improved Intelligent Design Runs for push-button timing closure
- New example designs available in Vivado®
- Ease of use enhancements for HLS flows

We **strongly recommend** to use the web installers as it reduces download time and saves significant disk space.

Please see [Installer Information](#) for details.

### Note:

- Download verification is only supported with Google Chrome and Microsoft Edge web browsers.
- Beginning this release we will be offering only 2 Editions for Vivado ML. Please go to [product page](#) for more details.
- Vivado ML 2021.1 and later versions require upgrading your license server tools to the Flex 11.17.2.0 versions.

### Download Includes

Download Type

Last Updated

Answers

Documentation

Support Forums

Vivado ML Edition

Full Product Installation

Oct 27, 2021

[2021.x - Vivado Known Issues](#)

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[Installation and Licensing](#)

📄 Xilinx Unified Installer 2021.2: Windows Self Extracting Web Installer (EXE - 212.41 MB)

MD5 SUM Value : 76b60fc6a74338066f4e4dd0a855ec93

Download Verification ⓘ

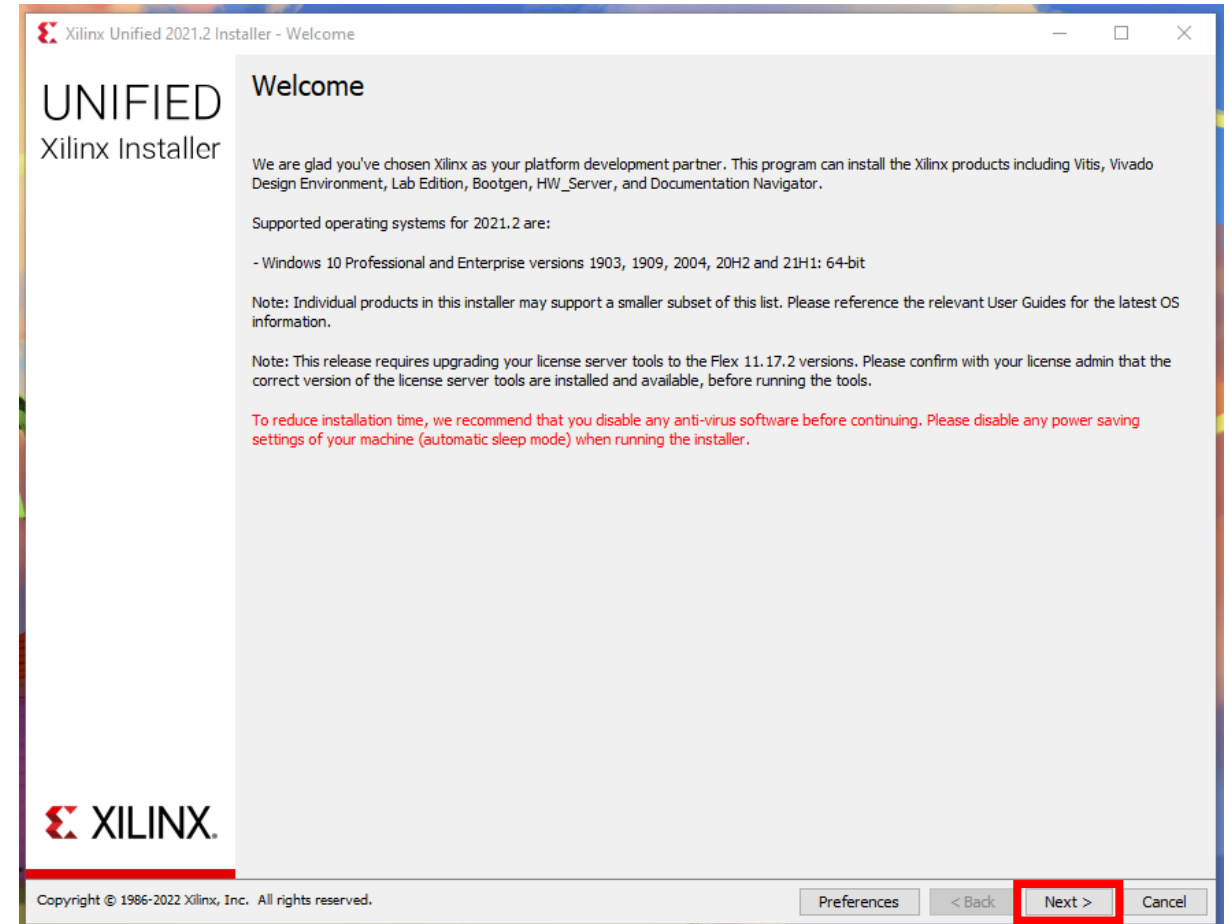
Digests

Signature

Public Key

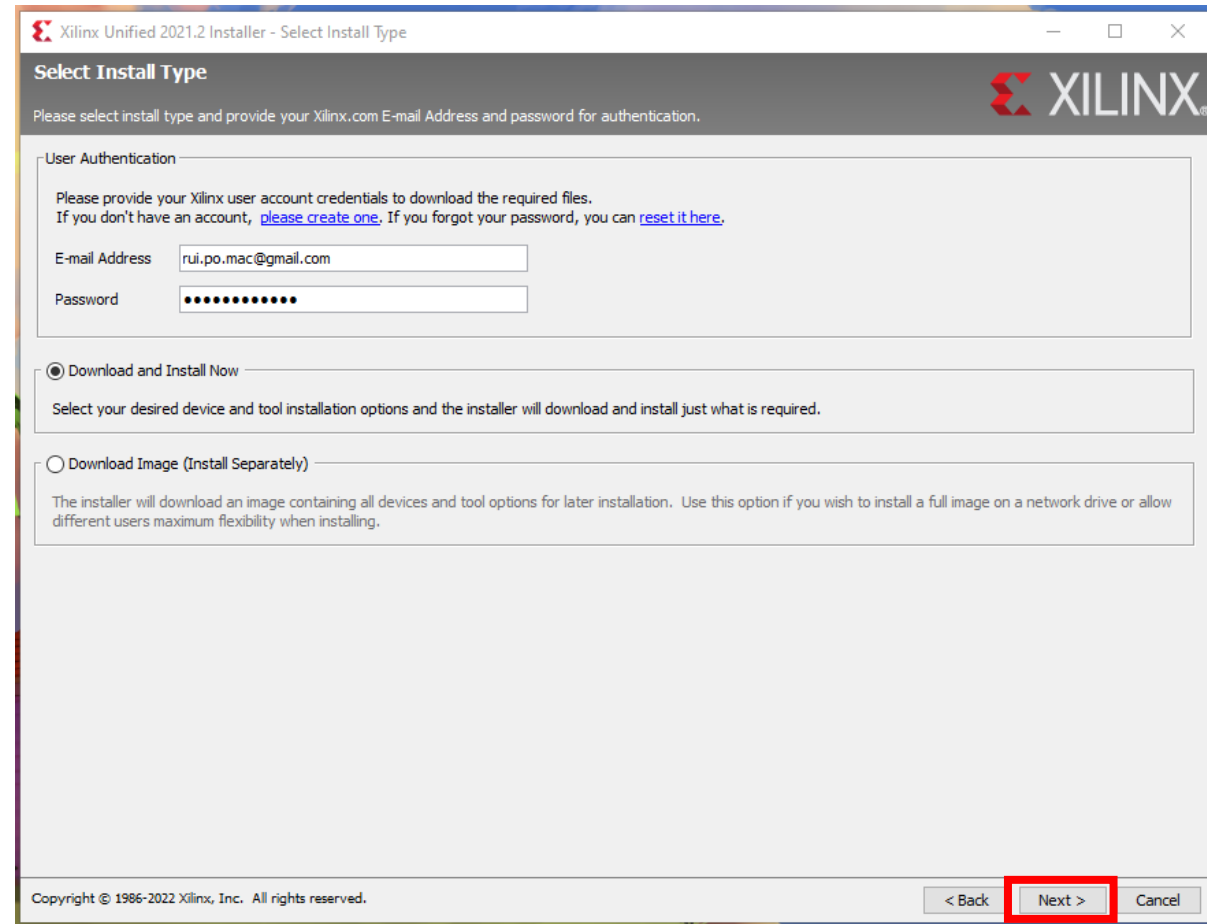
# Installation

- Execute the installer as administrator
- Next on the first window



# Installation

- Fill the user authentication form and select “Download and Install Now”
- Next



Xilinx Unified 2021.2 Installer - Select Install Type

**Select Install Type**

Please select install type and provide your Xilinx.com E-mail Address and password for authentication.

**User Authentication**

Please provide your Xilinx user account credentials to download the required files.  
If you don't have an account, [please create one](#). If you forgot your password, you can [reset it here](#).

E-mail Address:

Password:

☒ **Download and Install Now**

Select your desired device and tool installation options and the installer will download and install just what is required.

☐ **Download Image (Install Separately)**

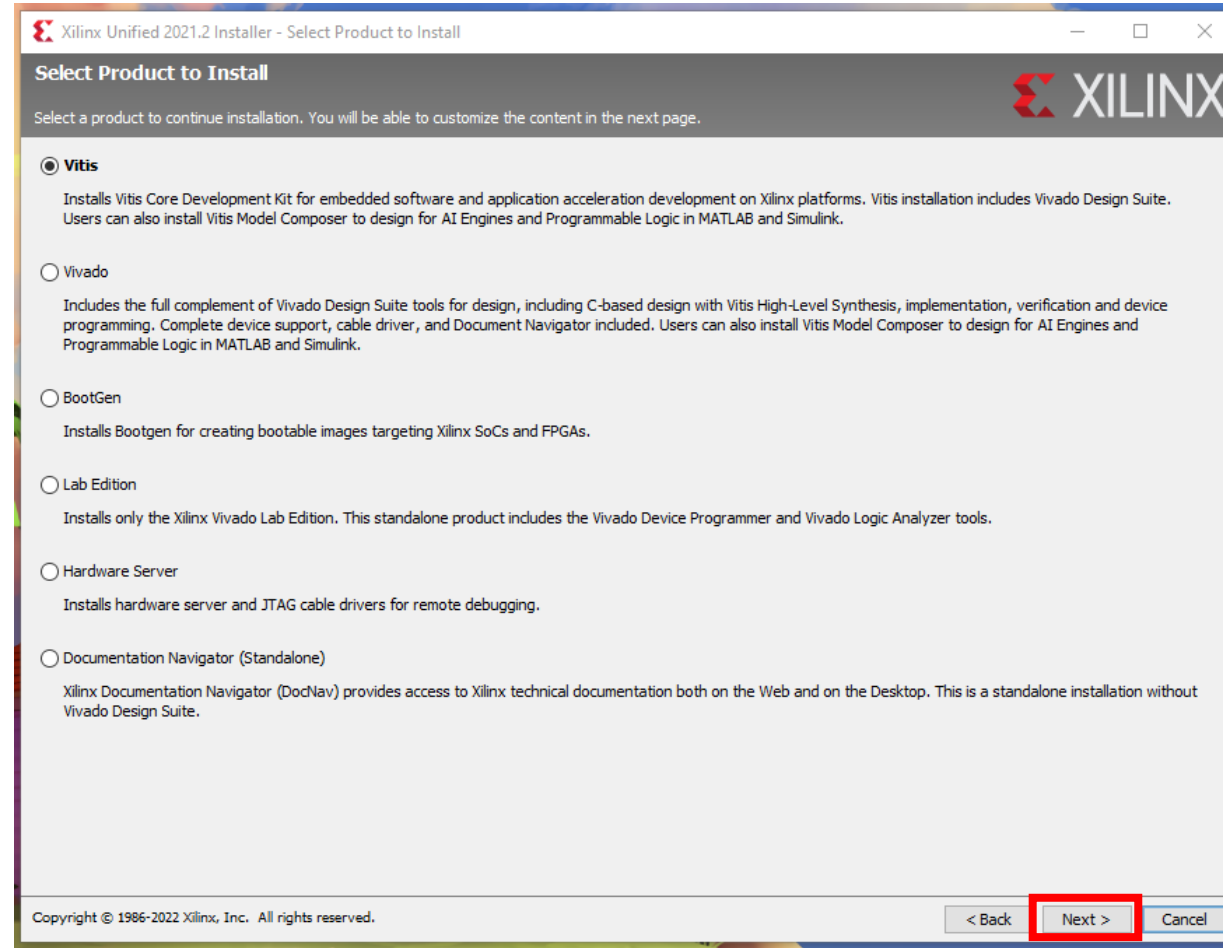
The installer will download an image containing all devices and tool options for later installation. Use this option if you wish to install a full image on a network drive or allow different users maximum flexibility when installing.

Copyright © 1986-2022 Xilinx, Inc. All rights reserved.

< Back **Next >** Cancel

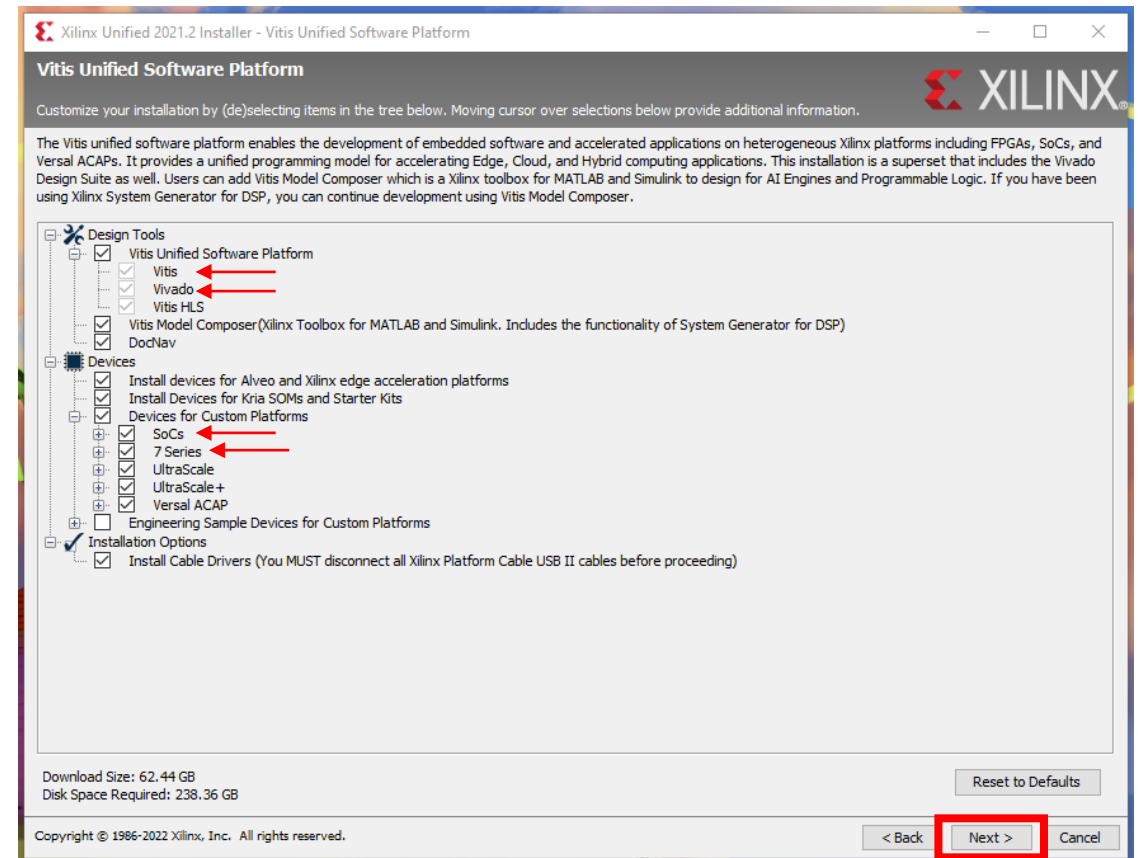
# Installation

- Select “Vitis” – This will install Vitis and Vivado
- Next



# Installation

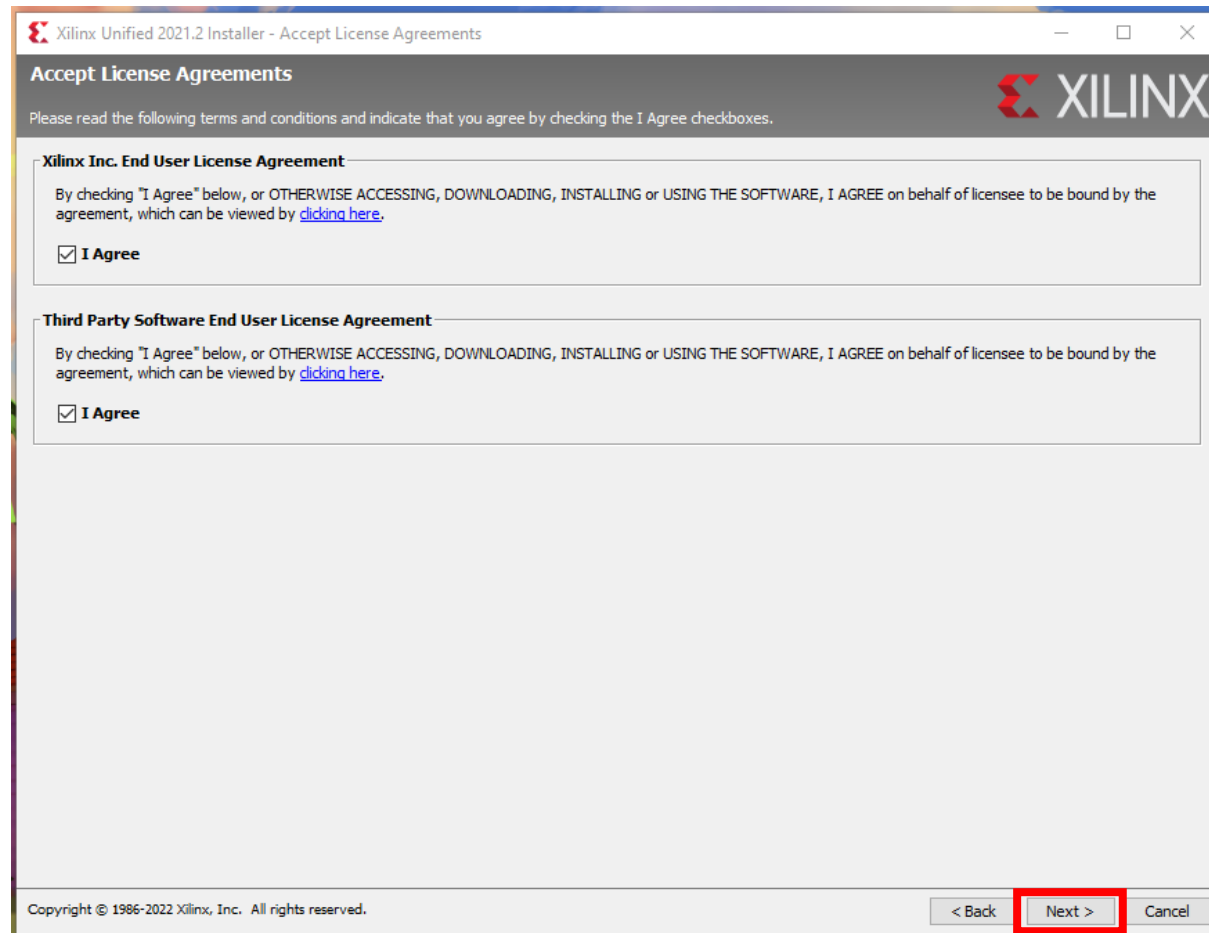
- Select the appropriated options then Next
- You do not have to install all Devices. If you want to save space, for this class you can just install the SOC's and 7 Series
- You can also decide not to install the Vitis HLS and the Vitis Model Composer





# Installation

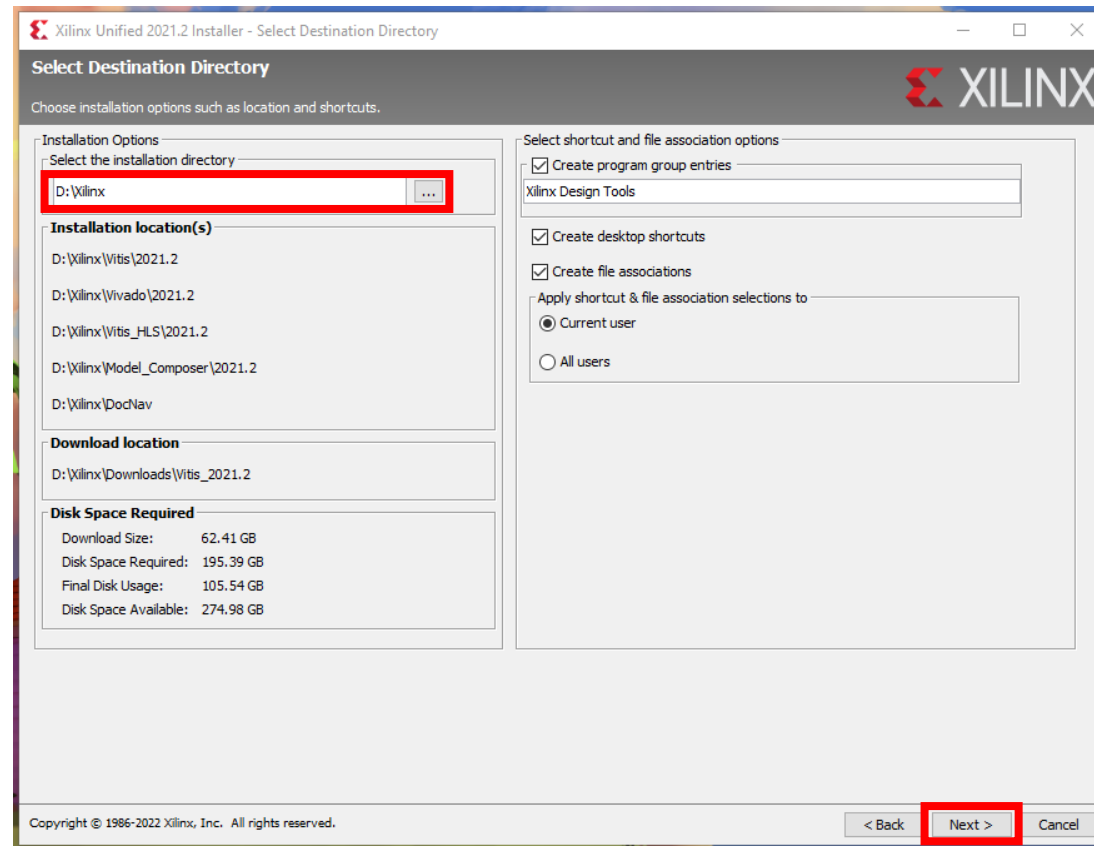
- Agree with the License Agreements and then Next





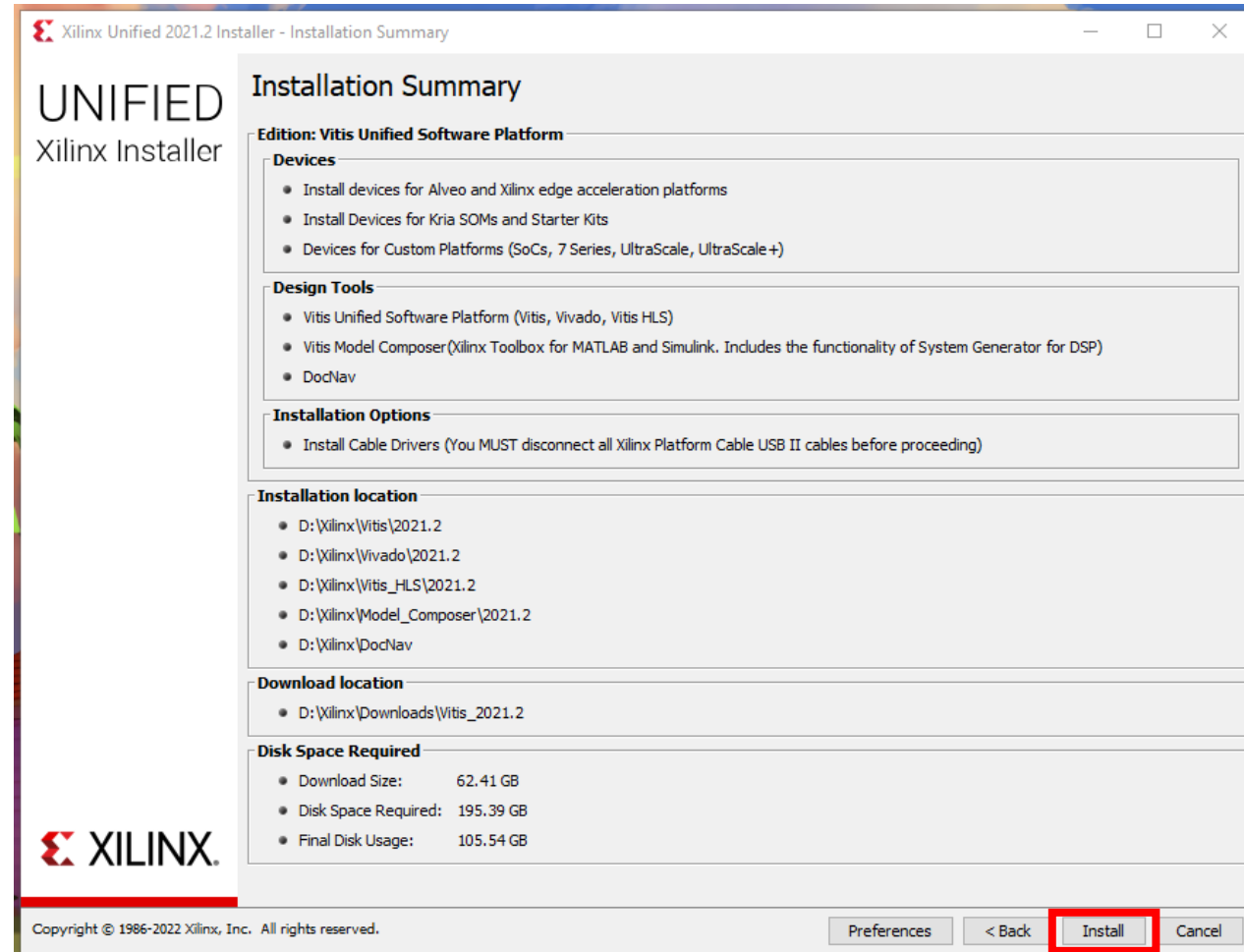
# Installation

- Select the directory to install – This should be as short as possible to avoid future path length problems
- Next



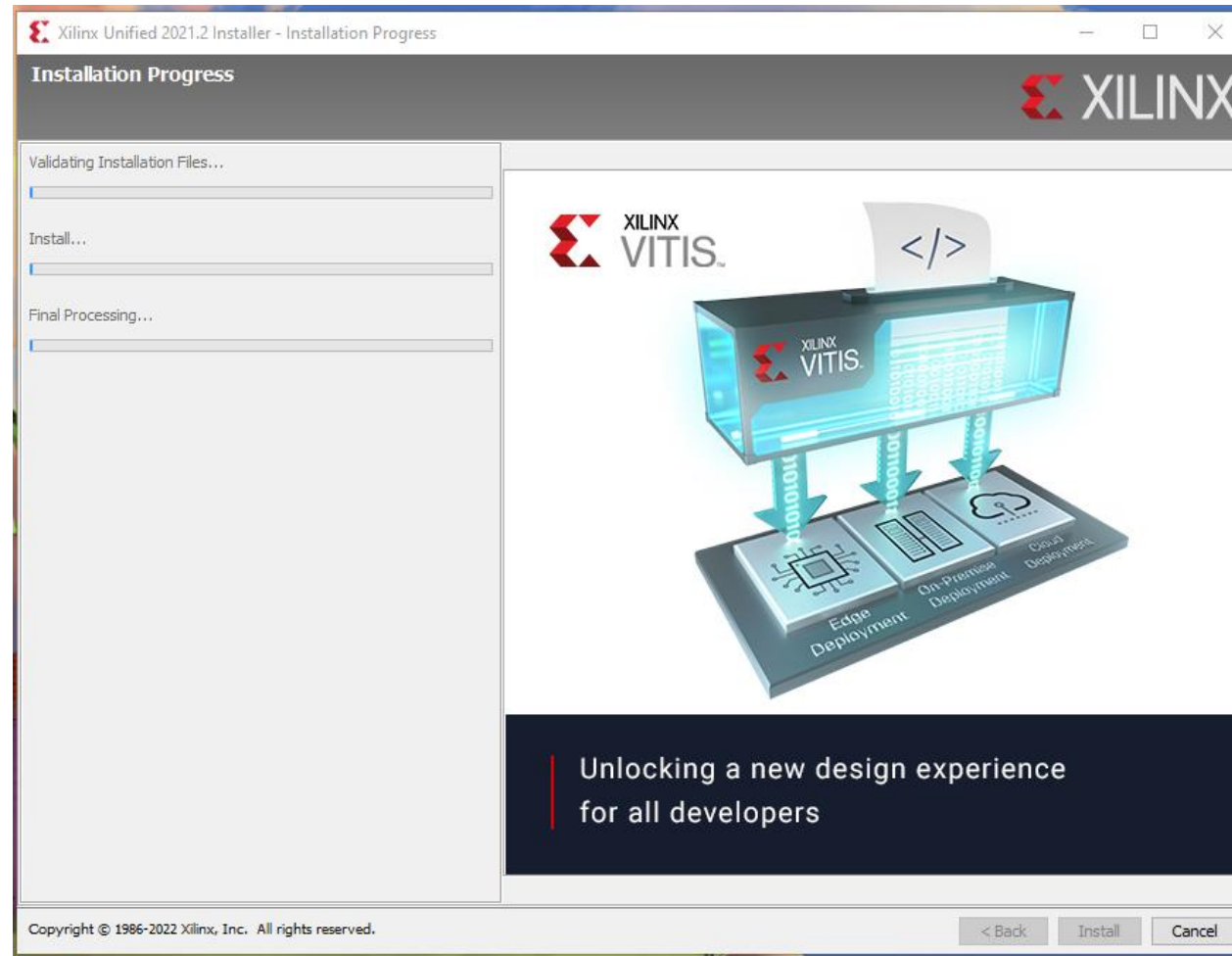
# Installation

- Confirm the installation information
- Install



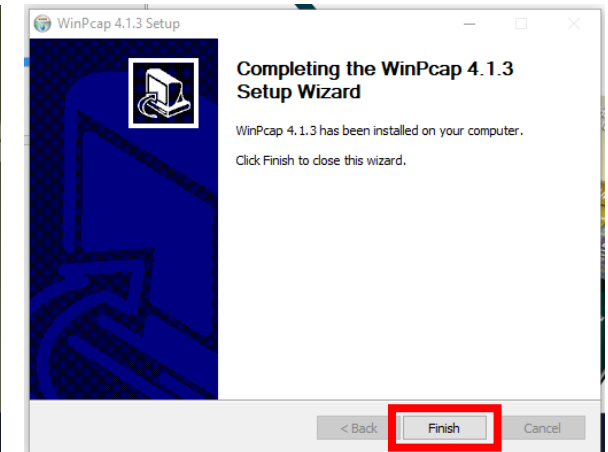
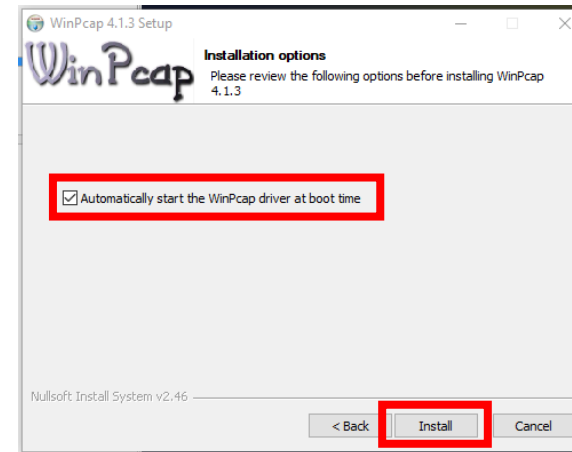
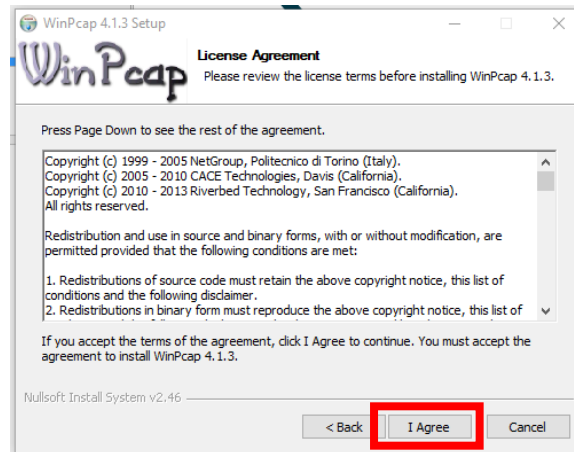
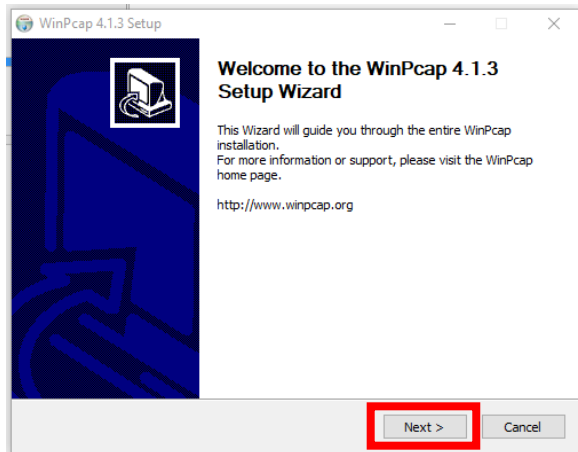
# Installation

- Go grab a coffee... This will take a while...



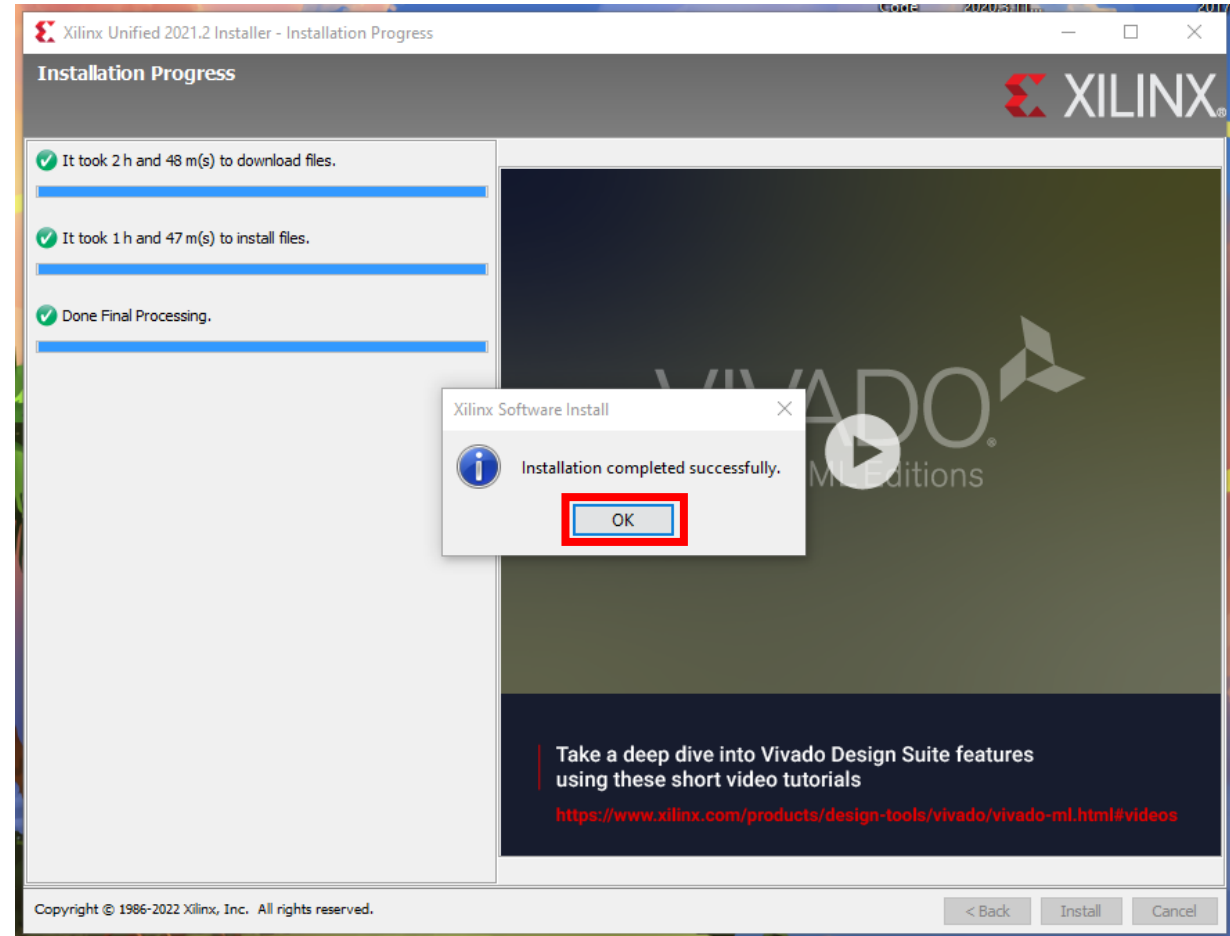
# Installation

- Almost there. Install the WinPcap



# Installation

- Congratulations, you are one step closer to become an FPGA Engineer

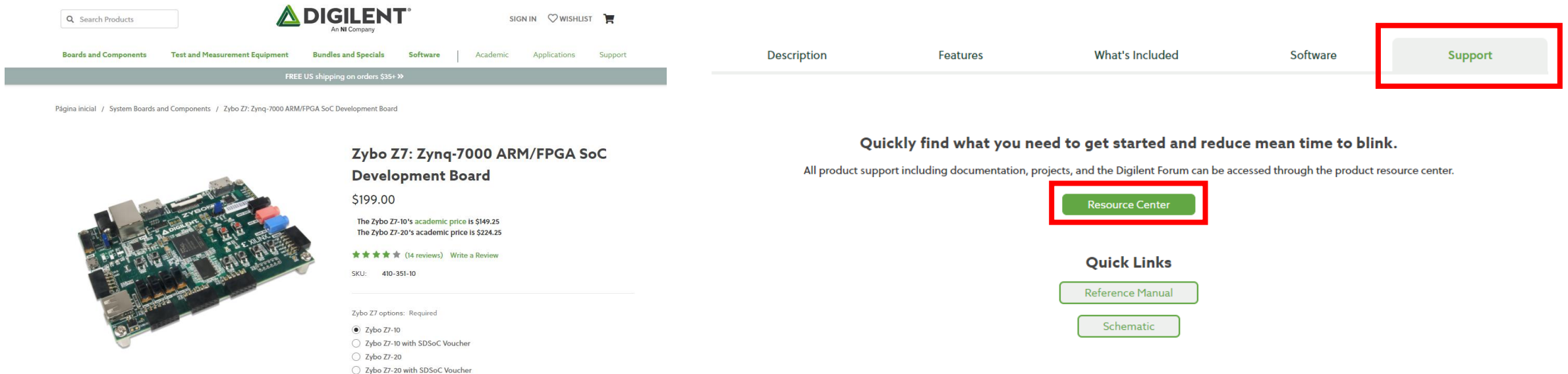


# Installing a new board

- Zybo board as example:
  - <https://digilent.com/shop/zybo-z7-zynq-7000-arm-fpga-soc-development-board/>
  - <https://digilent.com/reference/programmable-logic/zybo-z7/start?redirect=1>
  - [https://github.com/Digilent/vivado-boards?\\_ga=2.42031532.867636292.1643229174-1016055765.1642334752](https://github.com/Digilent/vivado-boards?_ga=2.42031532.867636292.1643229174-1016055765.1642334752)

# Installing a new board

- On the Digilent Zybo Z7 board page select:
  - Support->Resource Center



Search Products

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Boards and Components Test and Measurement Equipment Bundles and Specials Software Academic Applications Support

FREE US shipping on orders \$35+ >>

Página inicial / System Boards and Components / Zybo Z7: Zynq-7000 ARM/FPGA SoC Development Board

**Zybo Z7: Zynq-7000 ARM/FPGA SoC Development Board**

\$199.00

The Zybo Z7-10's academic price is \$149.25  
The Zybo Z7-20's academic price is \$224.25

★★★★★ (14 reviews) Write a Review

SKU: 410-351-10

Zybo Z7 options: Required

- ☒ Zybo Z7-10
- ☐ Zybo Z7-10 with SDSoc Voucher
- ☐ Zybo Z7-20
- ☐ Zybo Z7-20 with SDSoc Voucher

**Quickly find what you need to get started and reduce mean time to blink.**

All product support including documentation, projects, and the Digilent Forum can be accessed through the product resource center.

**Resource Center**

**Quick Links**

- Reference Manual
- Schematic



# Installing a new board

- On the Resource Center page, you can access the board documentation
- To get the Board files select the “Installing Vivado, Vitis, and Digilent Board Files” Tutorial link

## Documentation

- Master XDC Files
- Petalinux Support for Digilent Boards
- reVISION Platforms
- SDSoc Platforms
- Xilinx Zynq Datasheet
- Xilinx Zynq Technical Reference Manual
- Zybo Z7 Migration Guide
- Zybo Z7 Reference Manual
- Zybo Z7 Schematic

## Tutorials

- Installing Vivado, Vitis, and Digilent Board Files
  - Walks through installing Vivado and Vitis, the development environments used to create hardware and software applications targeting Digilent FPGA development boards.
- Getting Started with Vivado and Vitis for Baremetal Software Projects
  - Walks through using Vivado and Vitis to create a design in hardware and software that uses a processor to control buttons and LEDs.
- Getting Started with Vivado for Hardware-Only Designs
  - Walks through using Vivado to create a simple design that blinks a single LED.

▸ Legacy Xilinx Tools Tutorials

# Installing a new board

- On the tutorial page, search for the vivado-boards Github repository link and click it
- Save the zip file

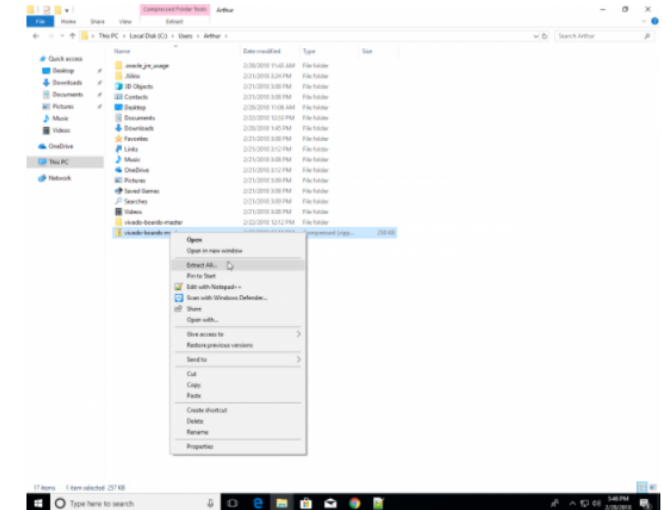
## Install Digilent's Board Files

Digilent provides *board files* for each FPGA development board. These files make it easy to select the correct part when creating a new project and allow for automated configuration of several complicated components (including the Zynq Processing System and Memory Interface Generator) used in many designs.

The board files will be copied into your version of Vivado's installation directory. At the end of this section, an alternate method of installation is presented, which users familiar with git may find more convenient.







Download the most recent [Master Branch ZIP Archive](#) of Digilent's [vivado-boards Github repository](#) and extract it.





Important! At the time of writing, if using a Spartan or Artix-based board for Microblaze designs, it is recommended to use an alternate version of the board files which better support the DDR memory present on some boards. This version of the board files can be downloaded via this link: [Microblaze-MIG.zip](#). Instructions for setting up DDR memory in a Microblaze design using these files can be found in [Getting Started with Vivado and Vitis for Baremetal Software Projects](#).






















# Installing a new board

- Extract the files and go to “new->board\_files”

 diligent-xdc-master.zip	26/01/2022 20:38	WinRAR ZIP archive	93 KB
 ds187-XC7Z010-XC7Z020-Data-Sheet.pdf	26/01/2022 20:39	Adobe Acrobat D...	2 569 KB
 uq585-Zynq-7000-TRM.pdf	26/01/2022 20:38	Adobe Acrobat D...	50 052 KB
 <b>vivado-boards-master.zip</b>	26/01/2022 20:40	WinRAR ZIP archive	373 KB
 zybo_z7_sch-public.pdf	26/01/2022 20:35	Adobe Acrobat D...	5 247 KB
 zybo-z7_rm.pdf	26/01/2022 20:35	Adobe Acrobat D...	1 549 KB

 <b>new</b>	14/09/2021 11:47	Pasta de ficheiros	
 old	14/09/2021 11:47	Pasta de ficheiros	
 utility	14/09/2021 11:47	Pasta de ficheiros	
 README.md	14/09/2021 11:47	Arquivo Fonte Ma...	2 KB

 <b>board_files</b>	14/09/2021 11:47	Pasta de ficheiros	
---	------------------	--------------------	--

 arty	14/09/2021 11:47	Pasta de ficheiros
 arty-a7-35	14/09/2021 11:47	Pasta de ficheiros
 arty-a7-100	14/09/2021 11:47	Pasta de ficheiros
 arty-s7-25	14/09/2021 11:47	Pasta de ficheiros
 arty-s7-50	14/09/2021 11:47	Pasta de ficheiros
 arty-z7-10	14/09/2021 11:47	Pasta de ficheiros
 arty-z7-20	14/09/2021 11:47	Pasta de ficheiros
 basys3	14/09/2021 11:47	Pasta de ficheiros
 cmod_a7-15t	14/09/2021 11:47	Pasta de ficheiros
 cmod_a7-35t	14/09/2021 11:47	Pasta de ficheiros
 cmod-s7-25	14/09/2021 11:47	Pasta de ficheiros
 cora-z7-07s	14/09/2021 11:47	Pasta de ficheiros
 cora-z7-10	14/09/2021 11:47	Pasta de ficheiros
 eclipse-z7	14/09/2021 11:47	Pasta de ficheiros
 genesys2	14/09/2021 11:47	Pasta de ficheiros
 genesys-zu-3eg	14/09/2021 11:47	Pasta de ficheiros
 genesys-zu-5ev	14/09/2021 11:47	Pasta de ficheiros
 nexys_video	14/09/2021 11:47	Pasta de ficheiros

# Installing a new board

- Select all the boards' folders and copy them
- Past them on "<installation root>/Xilinx/Vivado/<version>/data/boards/board\_files"
- If there is no board\_files directory just create one and past the boards there
- You are ready to go! Just open Vivado

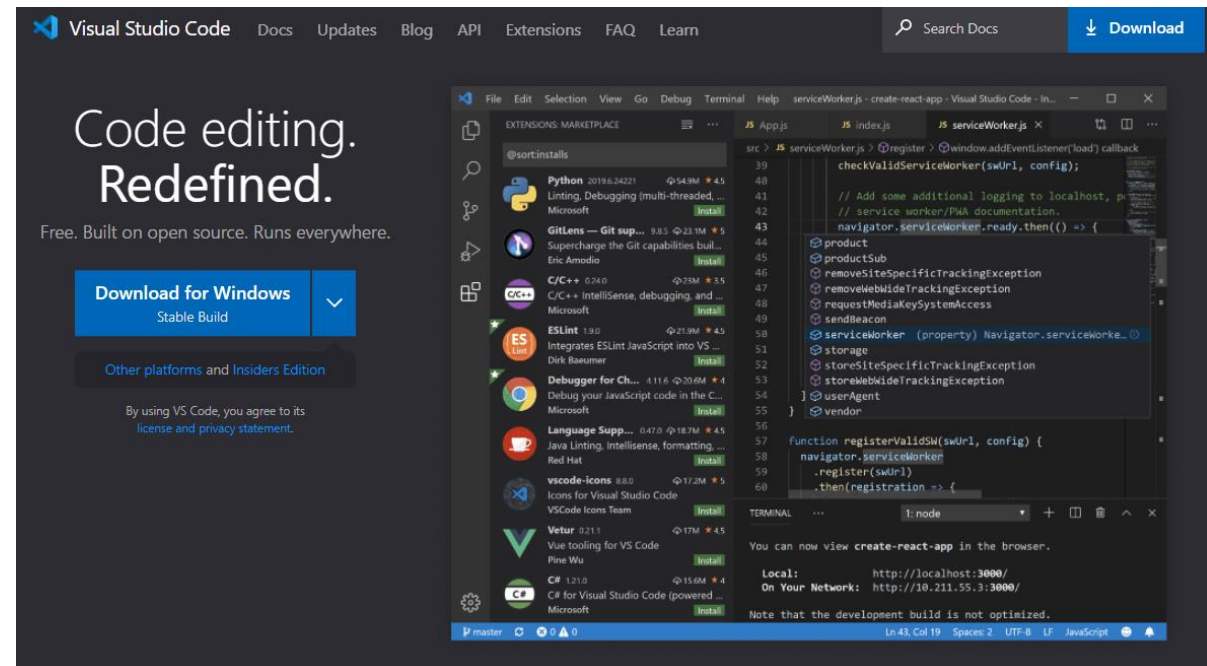
# Installing a new board

arty	14/09/2021 11:47	Pasta de ficheiros
arty-a7-35	14/09/2021 11:47	Pasta de ficheiros
arty-a7-100	14/09/2021 11:47	Pasta de ficheiros
arty-s7-25	14/09/2021 11:47	Pasta de ficheiros
arty-s7-50	14/09/2021 11:47	Pasta de ficheiros
arty-z7-10	14/09/2021 11:47	Pasta de ficheiros
arty-z7-20	14/09/2021 11:47	Pasta de ficheiros
basys3	14/09/2021 11:47	Pasta de ficheiros
cmmod_a7-15t	14/09/2021 11:47	Pasta de ficheiros
cmmod_a7-35t	14/09/2021 11:47	Pasta de ficheiros
cmmod-s7-25	14/09/2021 11:47	Pasta de ficheiros
cora-z7-07s	14/09/2021 11:47	Pasta de ficheiros
cora-z7-10	14/09/2021 11:47	Pasta de ficheiros
eclipse-z7	14/09/2021 11:47	Pasta de ficheiros
genesys2	14/09/2021 11:47	Pasta de ficheiros
genesys-zu-3eg	14/09/2021 11:47	Pasta de ficheiros
genesys-zu-5ev	14/09/2021 11:47	Pasta de ficheiros
nexys_video	14/09/2021 11:47	Pasta de ficheiros

C > Dados (D:) > Xilinx > Vivado > 2021.1 > data > boards > board_files			
Nome	Data de modificação	Tipo	Tamanho
arty	14/09/2021 11:47	Pasta de ficheiros	
arty-a7-35	26/01/2022 20:47	Pasta de ficheiros	
arty-a7-100	14/09/2021 11:47	Pasta de ficheiros	
arty-s7-25	14/09/2021 11:47	Pasta de ficheiros	
arty-s7-50	14/09/2021 11:47	Pasta de ficheiros	
arty-z7-10	14/09/2021 11:47	Pasta de ficheiros	
arty-z7-20	14/09/2021 11:47	Pasta de ficheiros	
basys3	14/09/2021 11:47	Pasta de ficheiros	
cmmod_a7-15t	14/09/2021 11:47	Pasta de ficheiros	
cmmod_a7-35t	14/09/2021 11:47	Pasta de ficheiros	
cmmod-s7-25	14/09/2021 11:47	Pasta de ficheiros	
cora-z7-07s	14/09/2021 11:47	Pasta de ficheiros	
cora-z7-10	14/09/2021 11:47	Pasta de ficheiros	
eclipse-z7	14/09/2021 11:47	Pasta de ficheiros	
genesys2	14/09/2021 11:47	Pasta de ficheiros	
genesys-zu-3eg	14/09/2021 11:47	Pasta de ficheiros	
genesys-zu-5ev	14/09/2021 11:47	Pasta de ficheiros	
nexys_video	14/09/2021 11:47	Pasta de ficheiros	

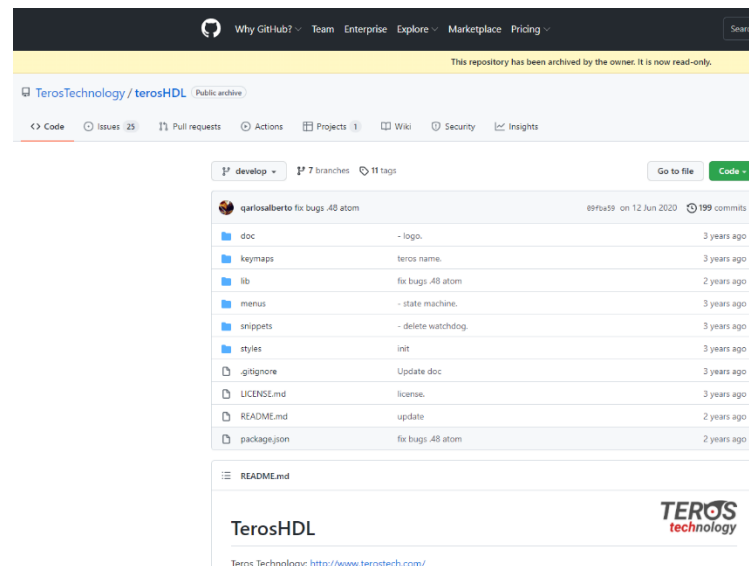
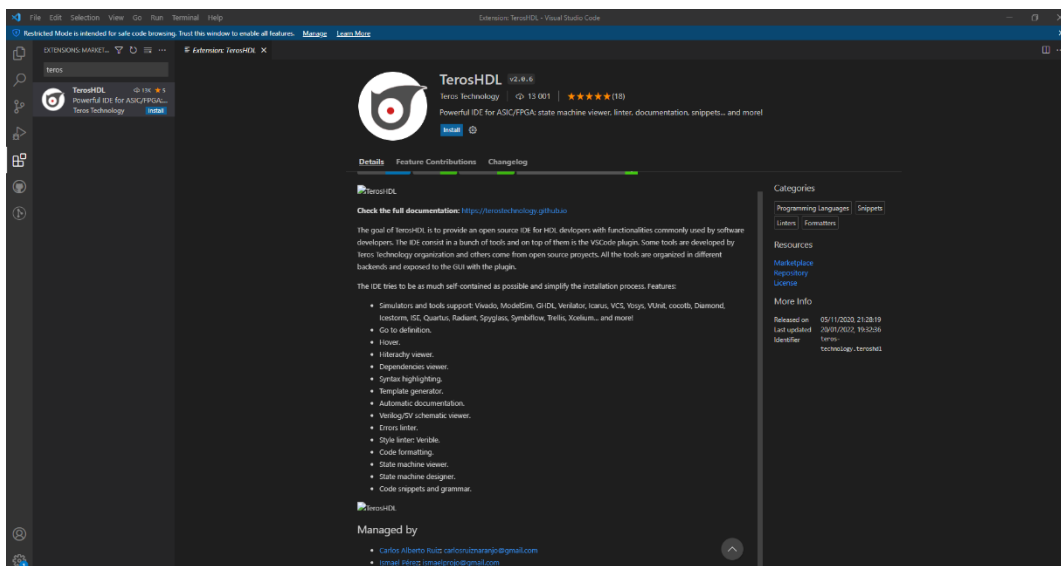
# HDL Coding

- Visual Studio Code: <https://code.visualstudio.com/>
  - Code editor
  - Has multiple add-ons that are useful for HDL development, such as TerosHDL



# HDL Coding

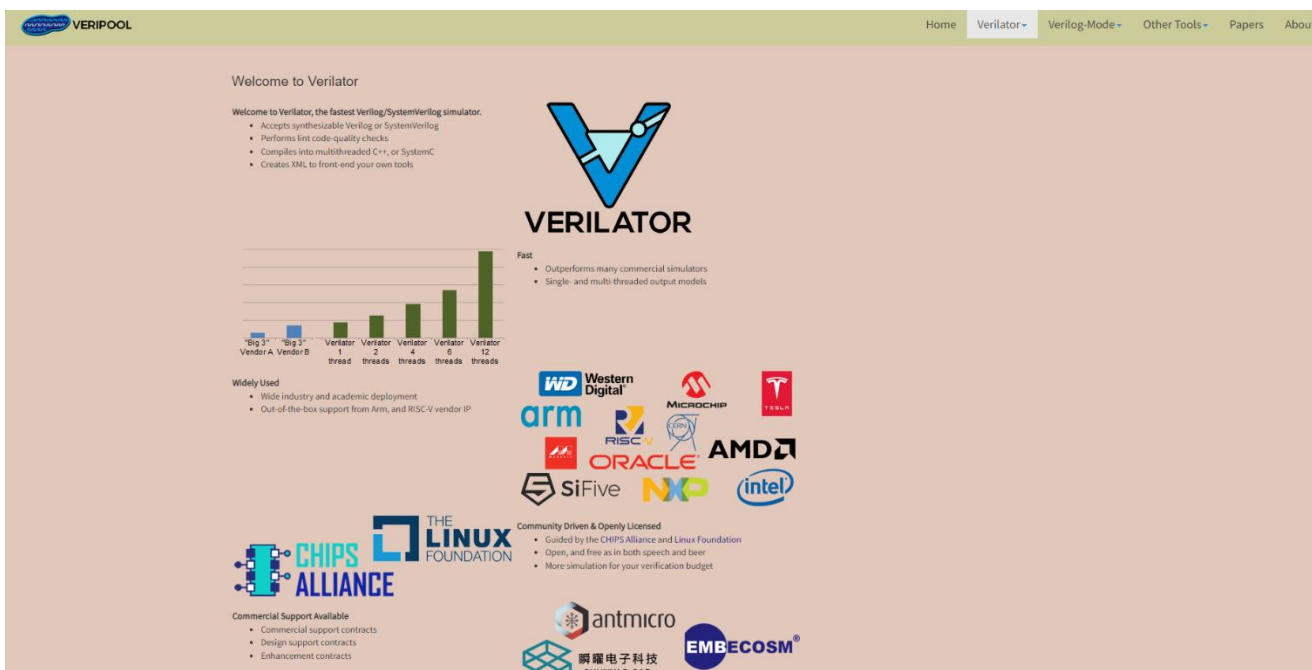
- TerosHDL: <https://github.com/TerosTechnology/terosHDL>
- HDL IDE
- Useful as a VS Code extension since it automatically generates designs documentation





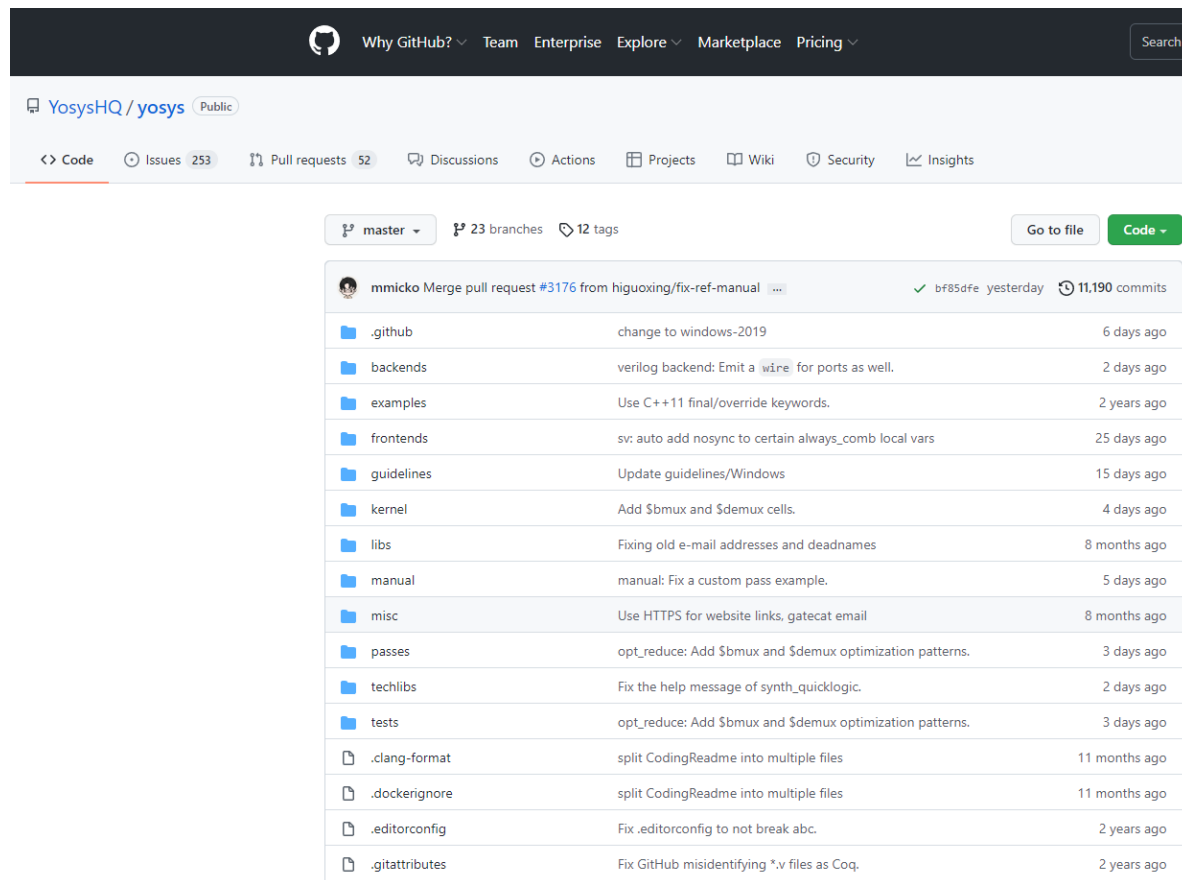
# HDL Coding

- Veriator: <https://www.veripool.org/verilator/>
- Verilog/SystemVerilog Simulator
- Has lint capabilities



# HDL Coding

- Yosys: <https://github.com/YosysHQ/yosys>
- Synthesis tool



The screenshot shows the GitHub repository page for YosysHQ/yosys. The repository is public and has 23 branches and 12 tags. The main branch is master. The repository has 11,190 commits. The repository is a synthesis tool for HDL coding.

File	Commit Message	Time Ago
.github	change to windows-2019	6 days ago
backends	verilog backend: Emit a wire for ports as well.	2 days ago
examples	Use C++11 final/override keywords.	2 years ago
frontends	sv: auto add nosync to certain always_comb local vars	25 days ago
guidelines	Update guidelines/Windows	15 days ago
kernel	Add \$bmux and \$demux cells.	4 days ago
libs	Fixing old e-mail addresses and deadnames	8 months ago
manual	manual: Fix a custom pass example.	5 days ago
misc	Use HTTPS for website links, gatecat email	8 months ago
passes	opt_reduce: Add \$bmux and \$demux optimization patterns.	3 days ago
techlibs	Fix the help message of synth_quicklogic.	2 days ago
tests	opt_reduce: Add \$bmux and \$demux optimization patterns.	3 days ago
.clang-format	split CodingReadme into multiple files	11 months ago
.dockerignore	split CodingReadme into multiple files	11 months ago
.editorconfig	Fix .editorconfig to not break abc.	2 years ago
.gitattributes	Fix GitHub misidentifying *.v files as Coq.	2 years ago

THANK YOU!

ANY QUESTIONS?

`rui.machado@dtx-colab.pt`