1. Description

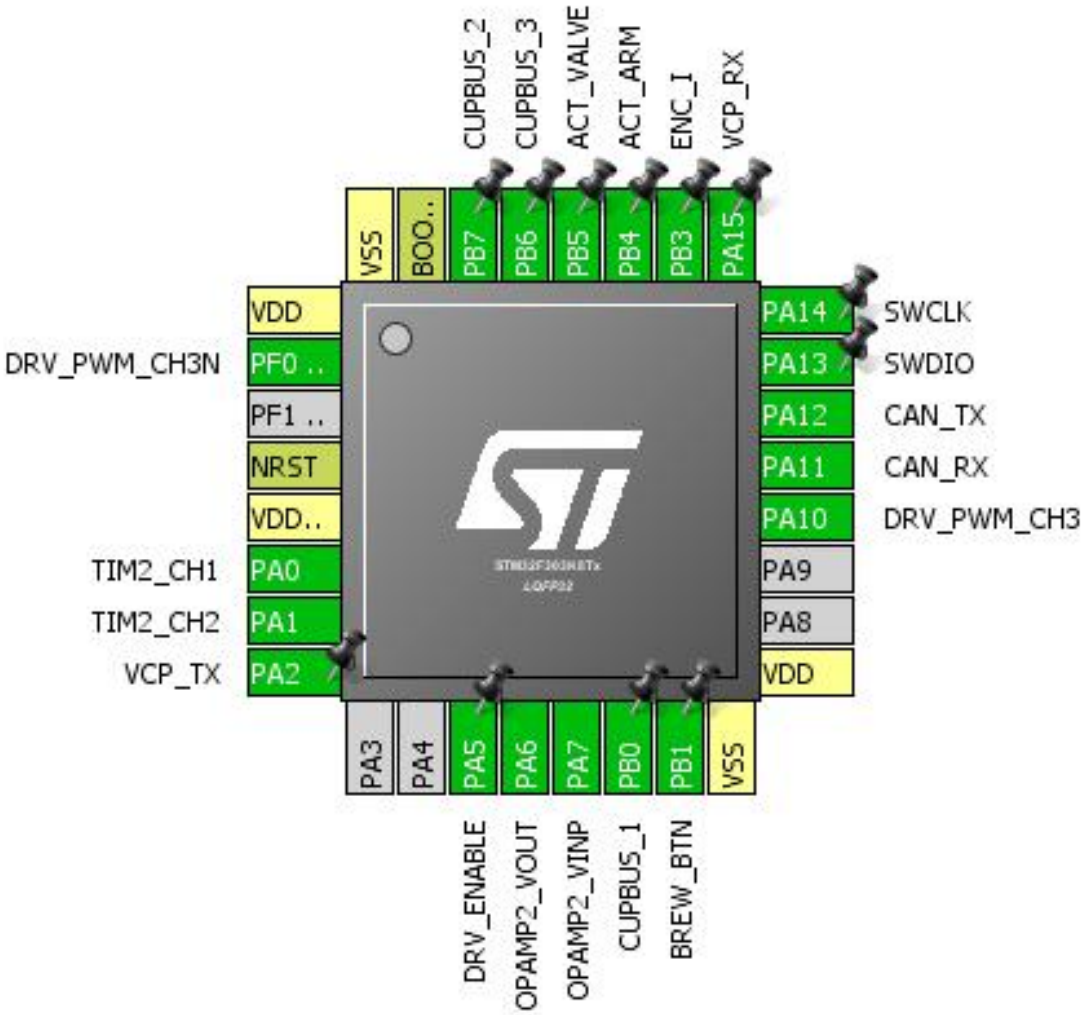
1.1. Project

Project Name	ETA_Kaffedisp_F303
Board Name	NUCLEO-F303K8
Generated with:	STM32CubeMX 4.27.0
Date	10/31/2018

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303K8Tx
MCU Package	LQFP32
MCU Pin number	32

2. Pinout Configuration

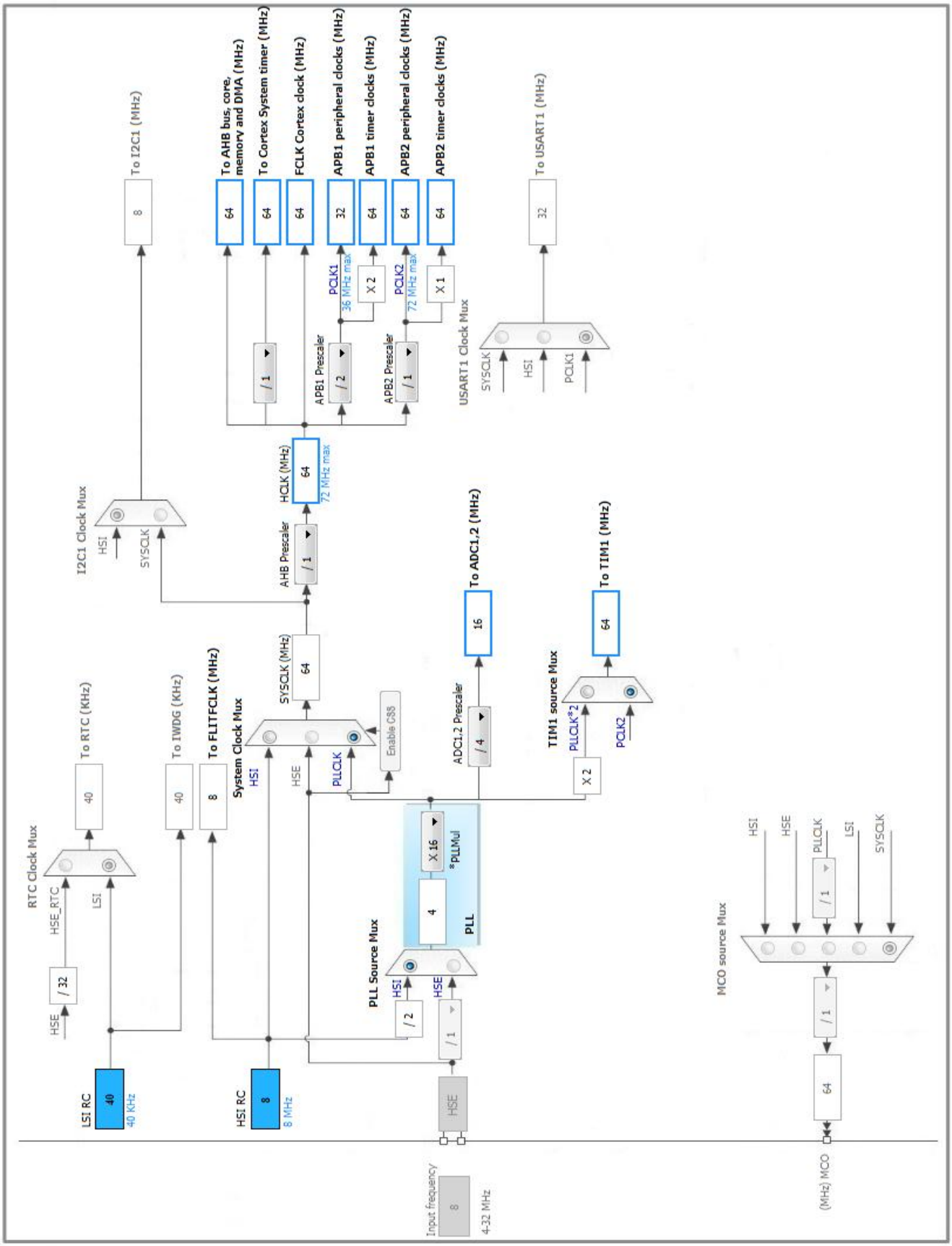


3. Pins Configuration

Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PF0 / OSC_IN	I/O	TIM1_CH3N	DRV_PWM_CH3N
4	NRST	Reset		
5	VDDA/VREF+	Power		
6	PA0	I/O	TIM2_CH1	
7	PA1	I/O	TIM2_CH2	
8	PA2	I/O	USART2_TX	VCP_TX
11	PA5 *	I/O	GPIO_Output	DRV_ENABLE
12	PA6	I/O	OPAMP2_VOUT	
13	PA7	I/O	OPAMP2_VINP	
14	PB0 *	I/O	GPIO_Input	CUPBUS_1
15	PB1 *	I/O	GPIO_Input	BREW_BTN
16	VSS	Power		
17	VDD	Power		
20	PA10	I/O	TIM1_CH3	DRV_PWM_CH3
21	PA11	I/O	CAN_RX	
22	PA12	I/O	CAN_TX	
23	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
24	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
25	PA15	I/O	USART2_RX	VCP_RX
26	PB3 *	I/O	GPIO_Input	ENC_I
27	PB4 *	I/O	GPIO_Output	ACT_ARM
28	PB5 *	I/O	GPIO_Output	ACT_VALVE
29	PB6 *	I/O	GPIO_Input	CUPBUS_3
30	PB7 *	I/O	GPIO_Input	CUPBUS_2
31	BOOT0	Boot		
32	VSS	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC2

IN3: OPAMP2 Output Single-Ended

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 3
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. CAN

mode: Mode

5.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	16
Time Quantum	**500.0 ***
Time Quanta in Bit Segment 1	1 Time
Time Quanta in Bit Segment 2	1 Time
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

5.3. OPAMP2

Mode: Follower

5.3.1. Parameter Settings:

Basic Parameters:

User Trimming	Disable

5.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.5. TIM1

Clock Source : Internal Clock

Channel3: PWM Generation CH3 CH3N

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	0

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 3 and 3N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

5.6. TIM2

Combined Channels: Encoder Mode

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0xffff ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**4 ***
____ Parameters for Channel 2 ____	
Polarity	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**4 ***

5.7. USART2

Mode: Asynchronous

5.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	38400
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
CAN	PA11	CAN_RX	Alternate Function Push Pull	No pull up pull down	**High ***	
	PA12	CAN_TX	Alternate Function Push Pull	No pull up pull down	**High ***	
OPAMP2	PA6	OPAMP2_VOUT	Analog mode	No pull up pull down	n/a	
	PA7	OPAMP2_VINP	Analog mode	No pull up pull down	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
TIM1	PF0 / OSC_IN	TIM1_CH3N	Alternate Function Push Pull	No pull up pull down	Low	DRV_PWM_CH3N
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull up pull down	Low	DRV_PWM_CH3
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull up pull down	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull up pull down	Low	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull up pull down	**High ***	VCP_TX
	PA15	USART2_RX	Alternate Function Push Pull	No pull up pull down	**High ***	VCP_RX
GPIO	PA5	GPIO_Output	Output Push Pull	No pull up pull down	Low	DRV_ENABLE
	PB0	GPIO_Input	Input mode	No pull up pull down	n/a	CUPBUS_1
	PB1	GPIO_Input	Input mode	No pull up pull down	n/a	BREW_BTN
	PB3	GPIO_Input	Input mode	No pull up pull down	n/a	ENC_I
	PB4	GPIO_Output	Output Push Pull	No pull up pull down	Low	ACT_ARM
	PB5	GPIO_Output	Output Push Pull	No pull up pull down	Low	ACT_VALVE
	PB6	GPIO_Input	Input mode	No pull up pull down	n/a	CUPBUS_3
	PB7	GPIO_Input	Input mode	No pull up pull down	n/a	CUPBUS_2

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
CAN TX interrupt	unused		
CAN RX0 interrupt	unused		
CAN RX1 interrupt	unused		
CAN SCE interrupt	unused		
TIM1 break and TIM15 interrupts	unused		
TIM1 update and TIM16 interrupts	unused		
TIM1 trigger and commutation and TIM17 interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
USART2 global interrupt / USART2 wake-up interrupt through EXT line 26	unused		
Floating point unit interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303K8Tx
Datasheet	025083_Rev5

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	ETA_Kaffedisp_F303
Project Folder	C:\Users\eta\Atollic\TrueSTUDIO\STM32_workspace_9.0\ETA_Kaffedisp_F303
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_F3 V1.9.1

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report