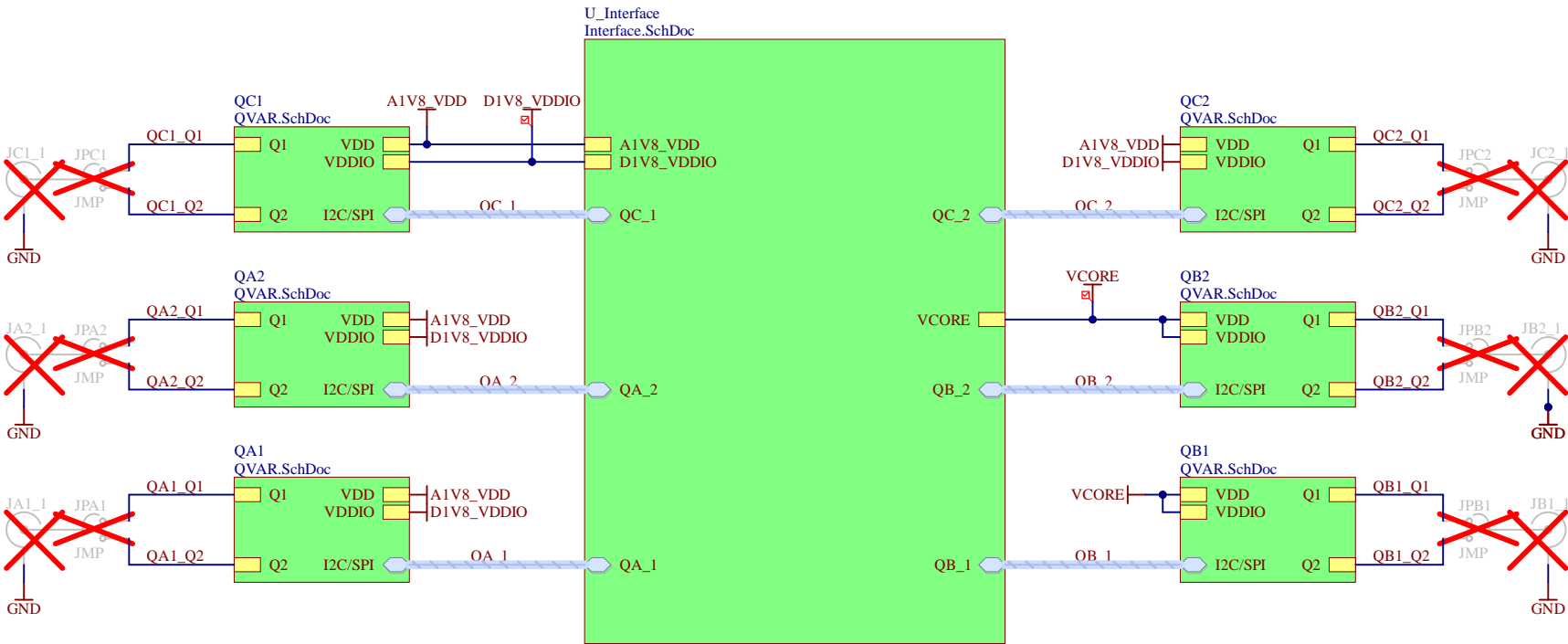
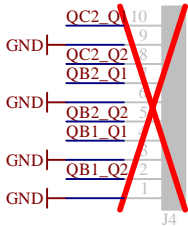
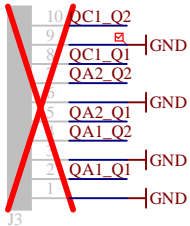


the 2 QVAR attached to I2CB have to be supplied by VCORE!



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File: main.SchDoc

Project:

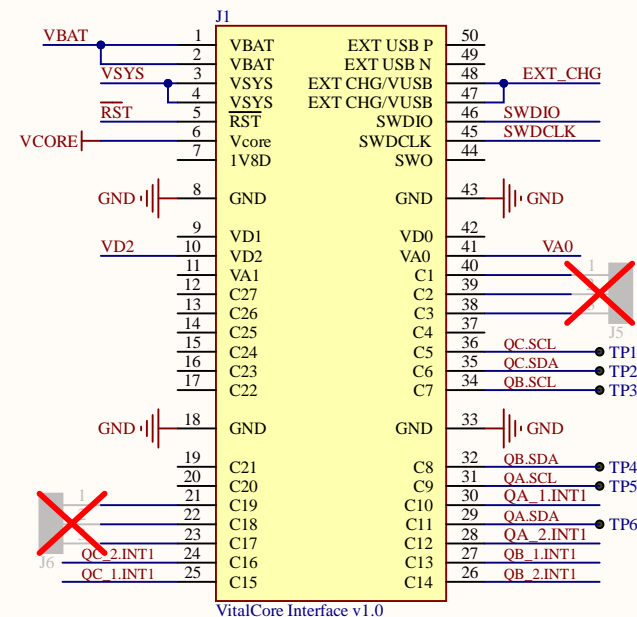
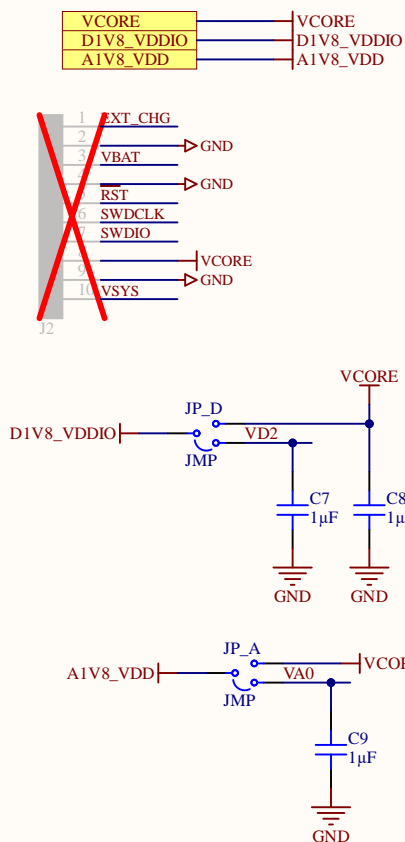
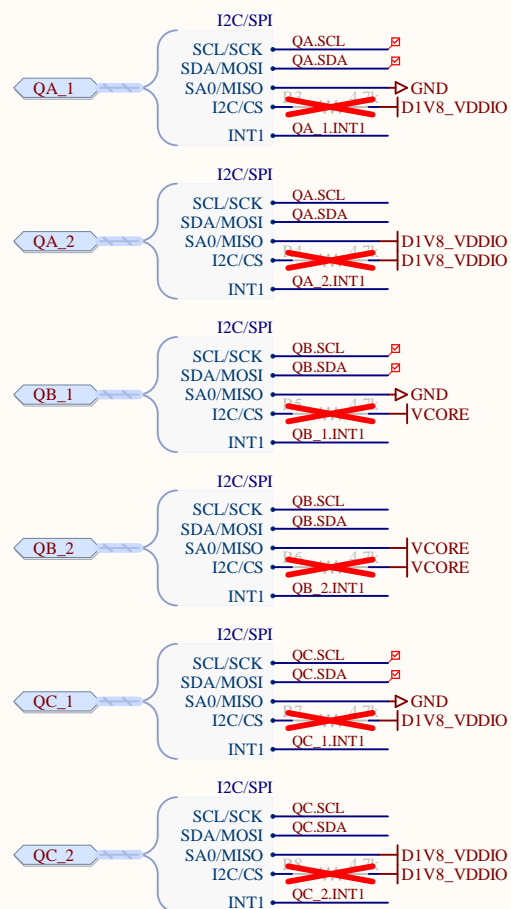
*

Drawn By: *

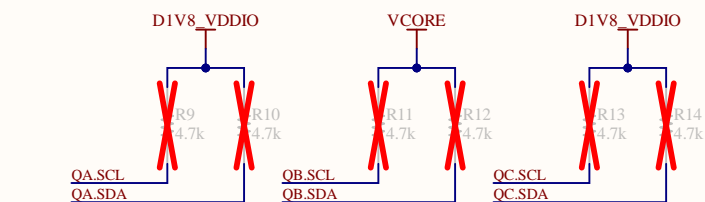
Checked By: *

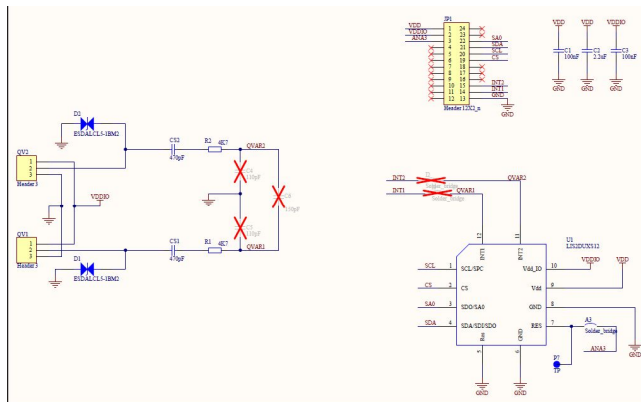
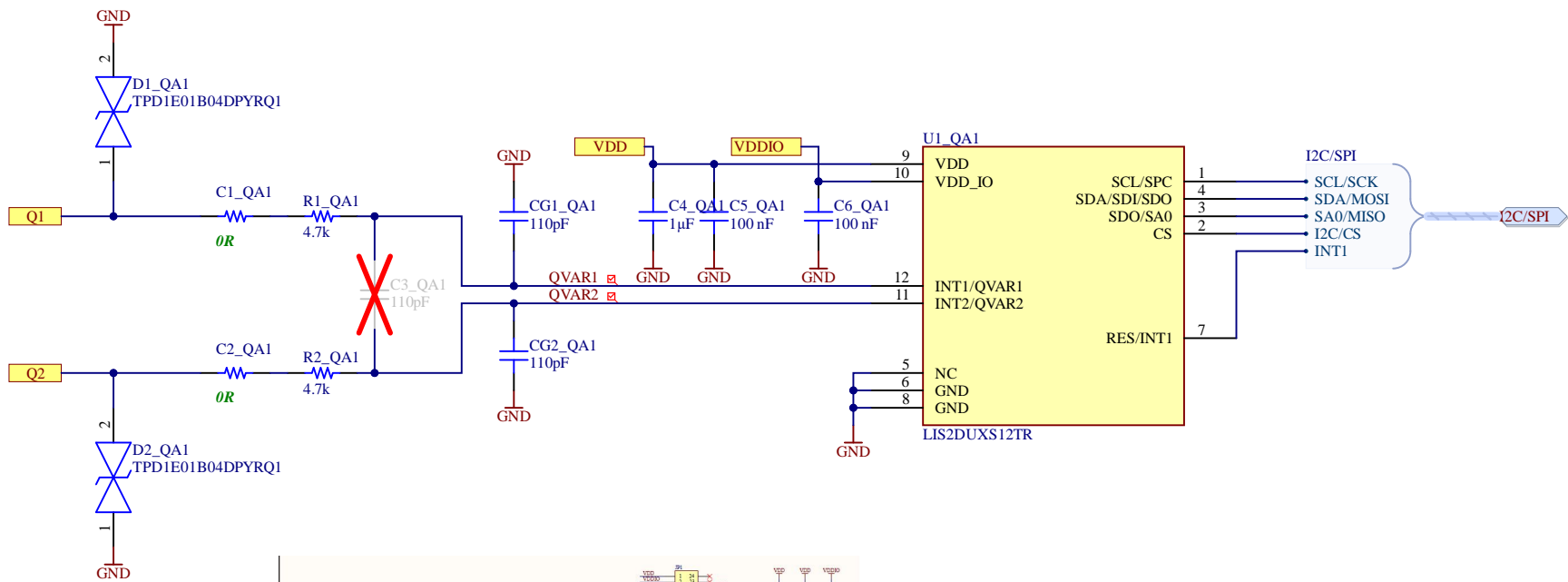
Sheet: 1 / 3

△ the 2 QVAR attached to I2CB have to be supplied by VCORE!

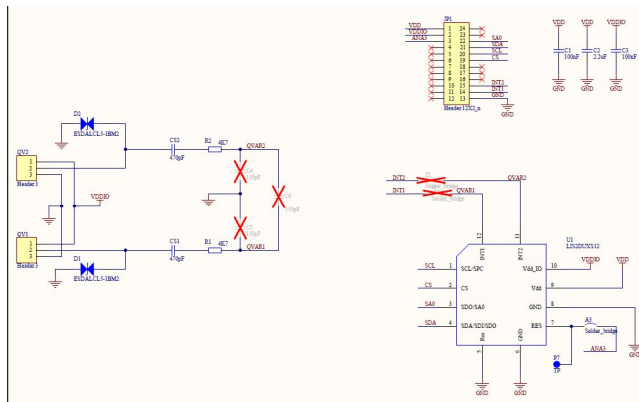
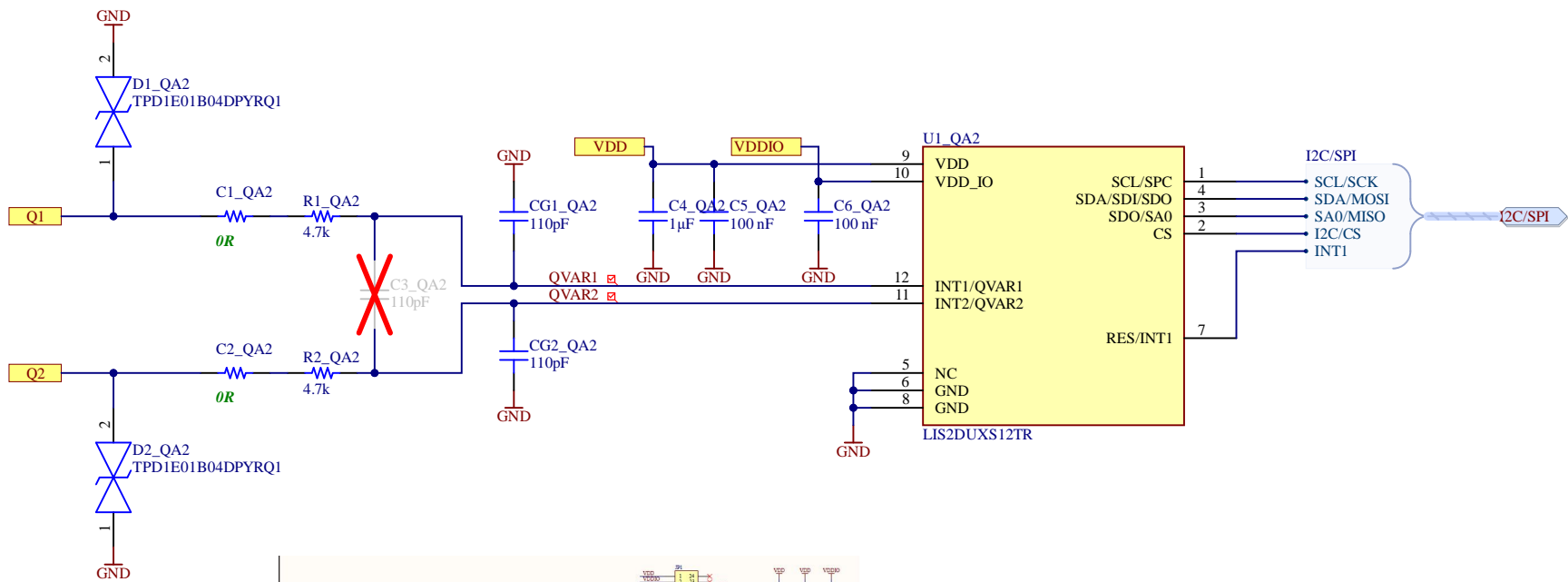


SWDIO and SWDCLK have to be connected externally in an ideal case. For emergency requirements a solderpad is supplied

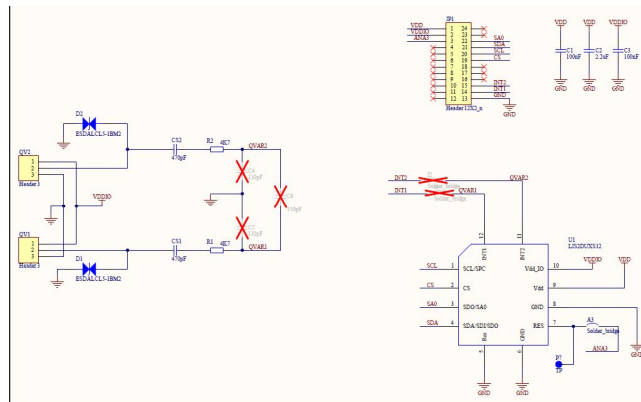
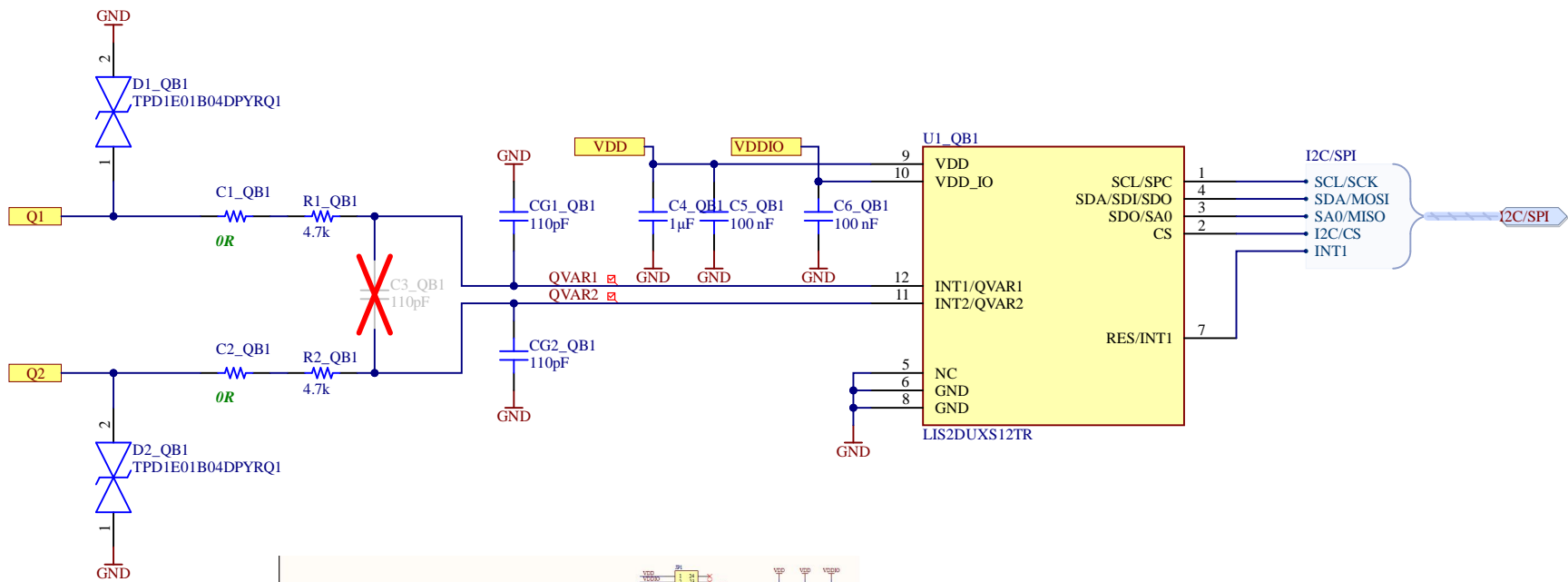




| | |
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| | * |
| | Drawn By: * |
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| Rev: 1.0 | |
| Variation: Fabrication | |
| File: QVAR.SchDoc | Sheet: 3 / 3 |



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| | Drawn By: * |
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| Variation: Fabrication | |
| File: QVAR.SchDoc | |



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Variation: Fabrication

File: QVAR.SchDoc

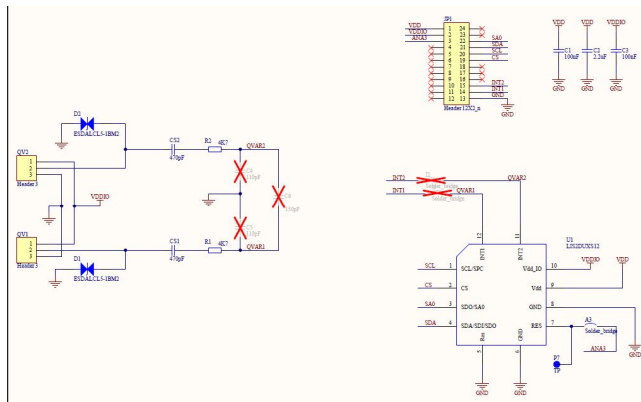
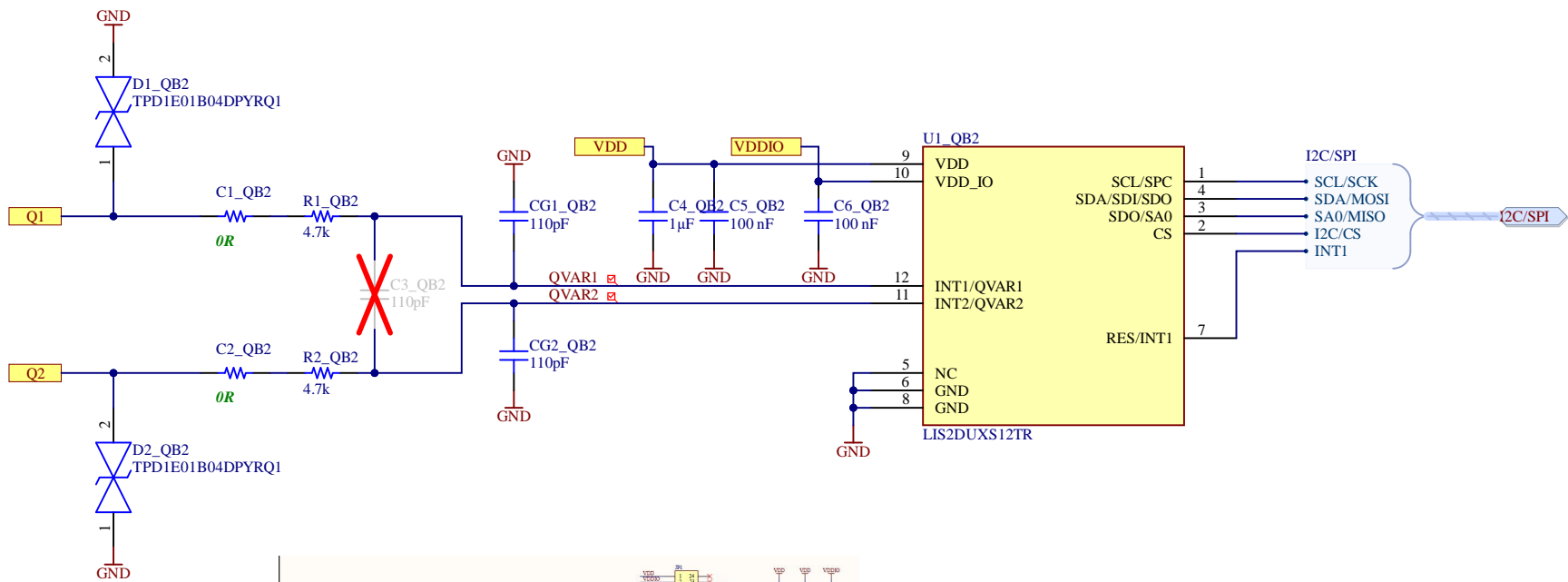
Project:

*

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Sheet: 3 / 3



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File: QVAR.SchDoc

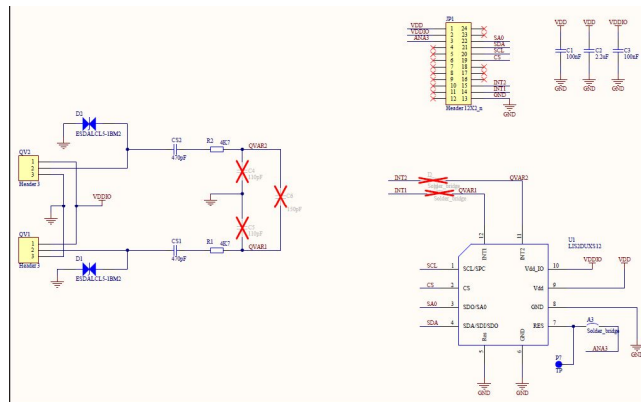
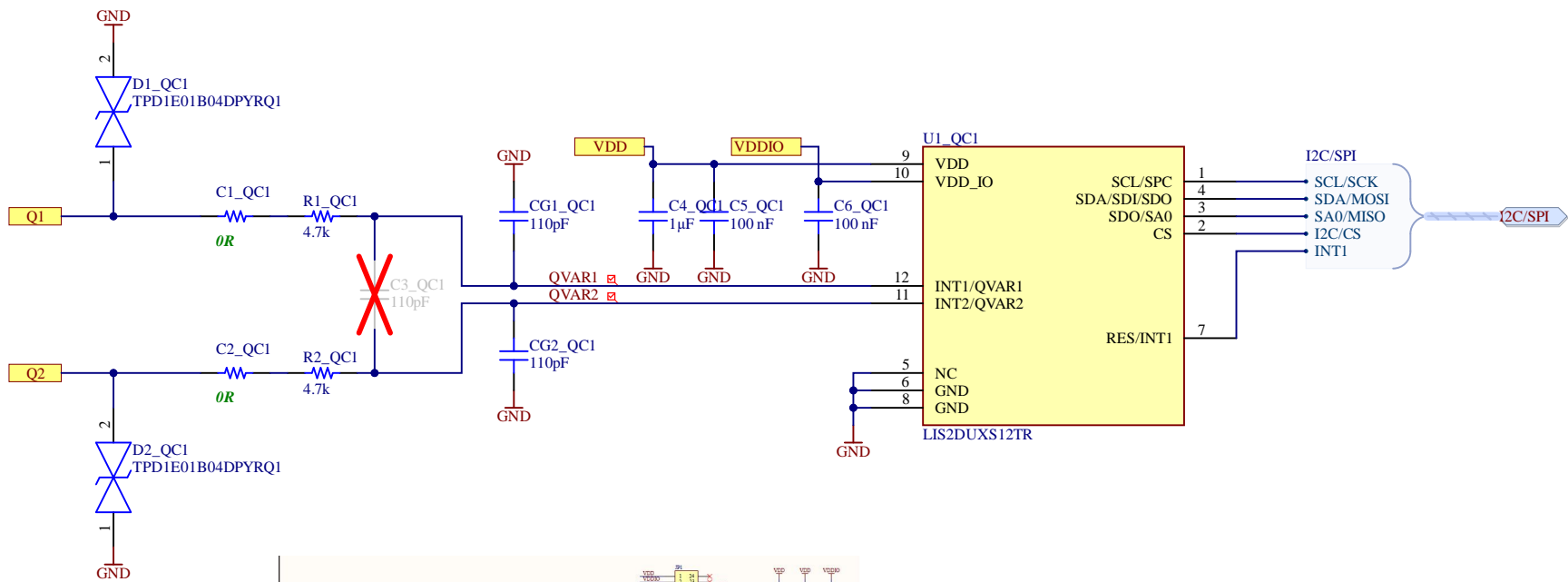
Project:

*

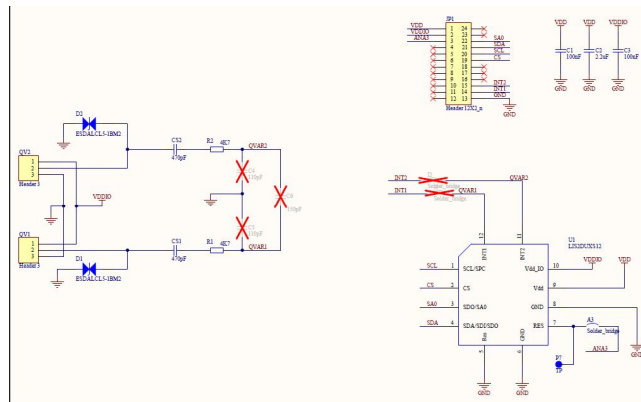
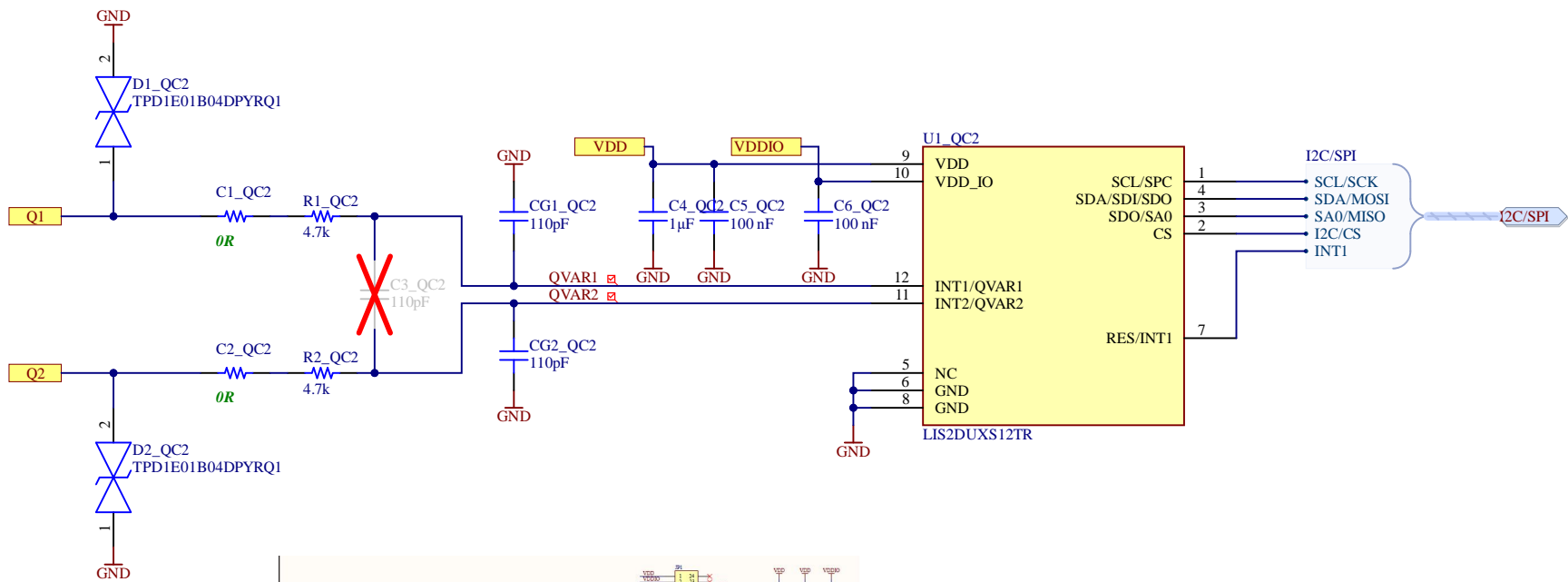
Drawn By: *

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Sheet: 3 / 3



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| Rev: 1.0 | |
| Variation: Fabrication | |
| File: QVAR.SchDoc | Sheet: 3 / 3 |



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| Variation: Fabrication | |
| File: QVAR.SchDoc | Sheet: 3 / 3 |

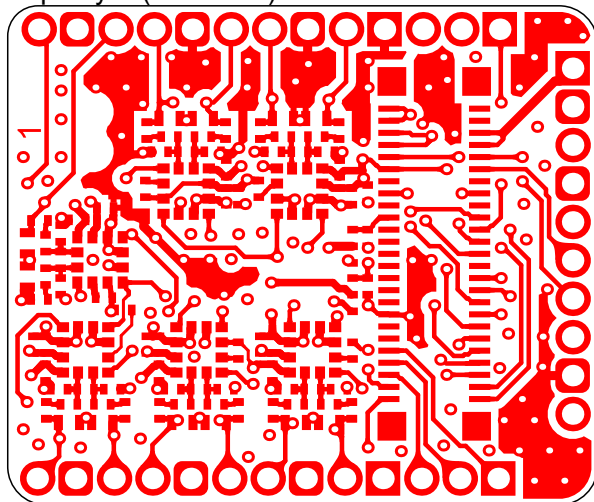
A

B

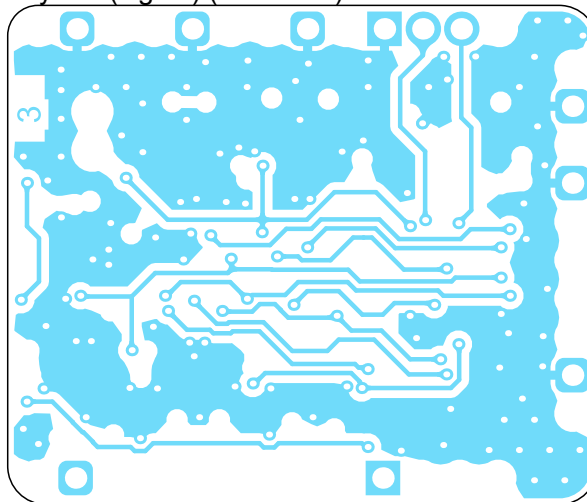
C

D

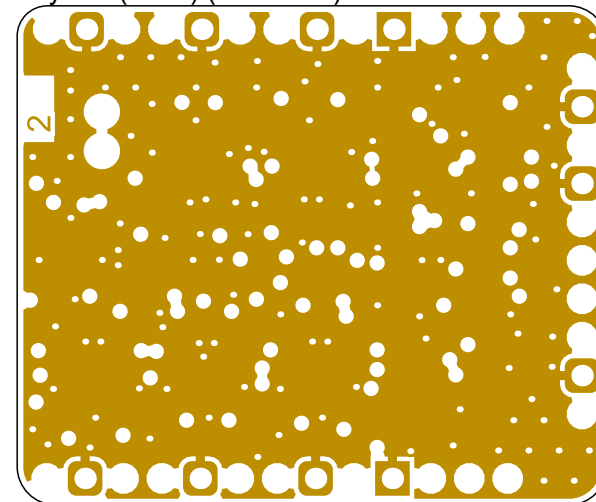
Top Layer (Scale 4:1)



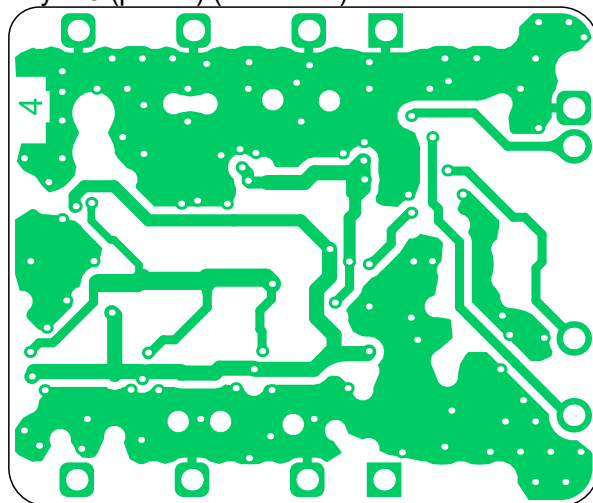
Layer 2 (signal) (Scale 4:1)



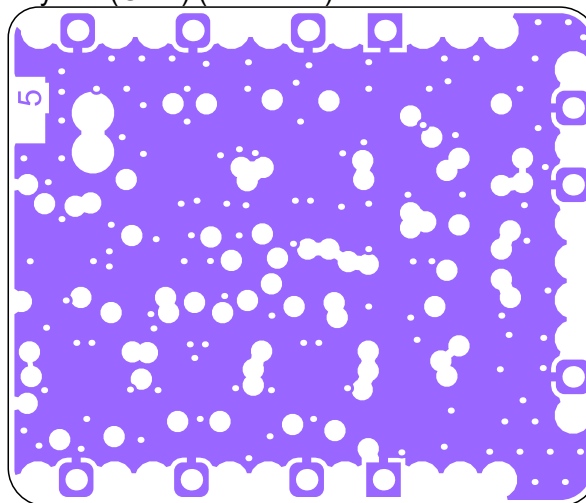
Layer 1 (GND) (Scale 4:1)



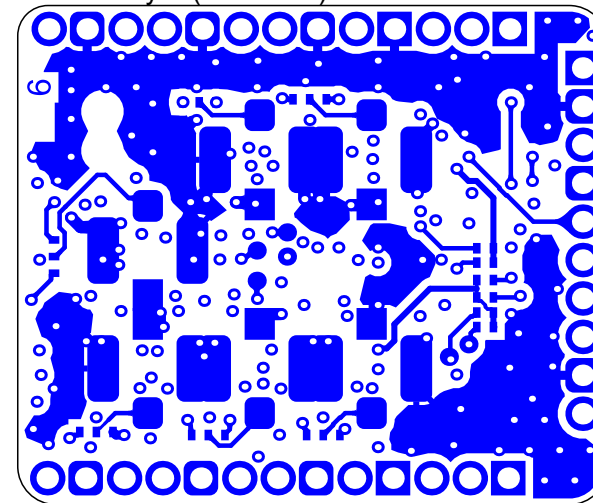
Layer 3 (power) (Scale 4:1)



Layer 4 (GND) (Scale 4:1)



Bottom Layer (Scale 4:1)

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Variant: Fabrication

File: DOC_ART.PCBDwf

Project:

Art

Drawn By:

Checked By:

Sheet: 1/1

A

B

C

D

1

1

2

2

3

3

4

4

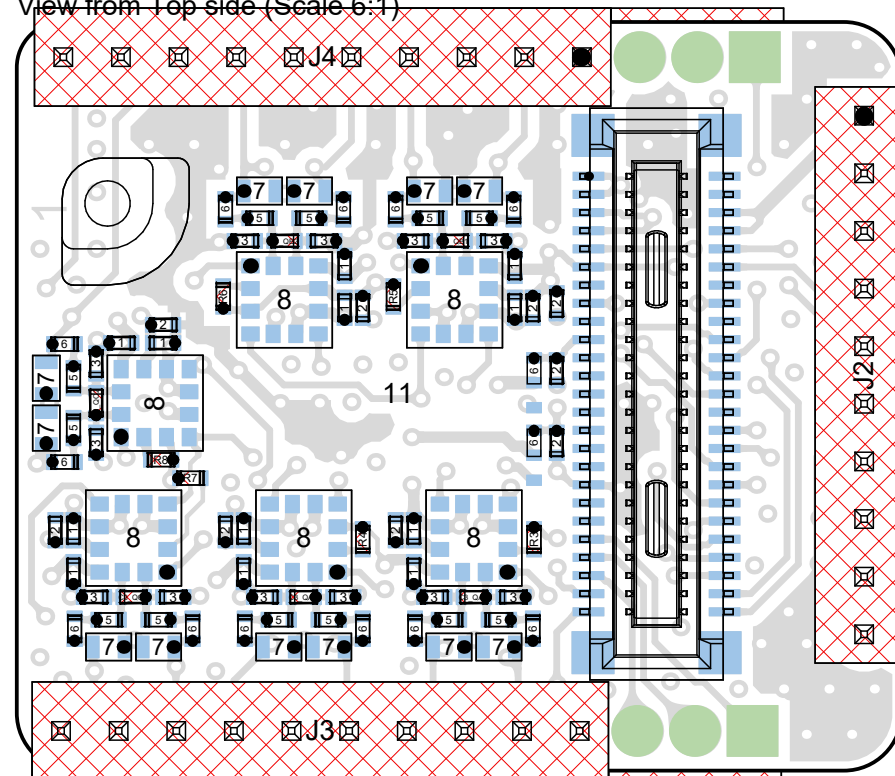
A

B

C

D

View from Top side (Scale 6:1)

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Revision: 1.0

Variant: Fabrication

File: DOC_ASSEMBLY.PCBDwf

Project:

Assembly

Drawn By:

Checked By:

Sheet: 1/2

A

B

C

D

1

1

2

2

3

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4

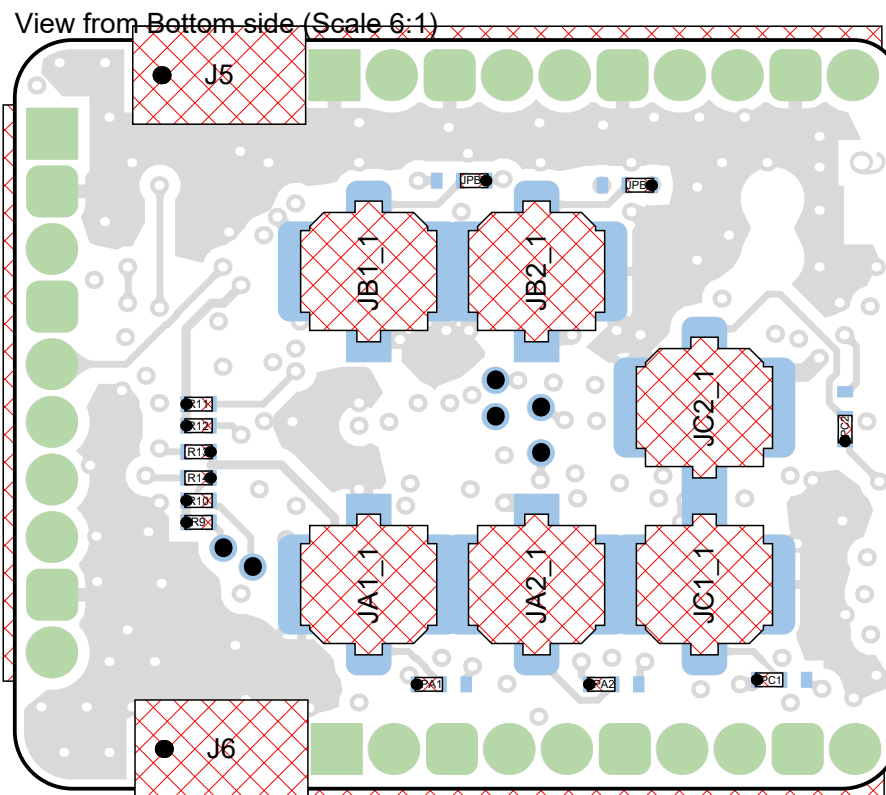
4

A

B

C

D

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Revision: 1.0

Variant: Fabrication

File: DOC_ASSEMBLY.PCBDwf

Project:

Assembly

Drawn By:

Checked By:

Sheet: 2/2

A

B

C

D

1

1

2

2

3

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4

4

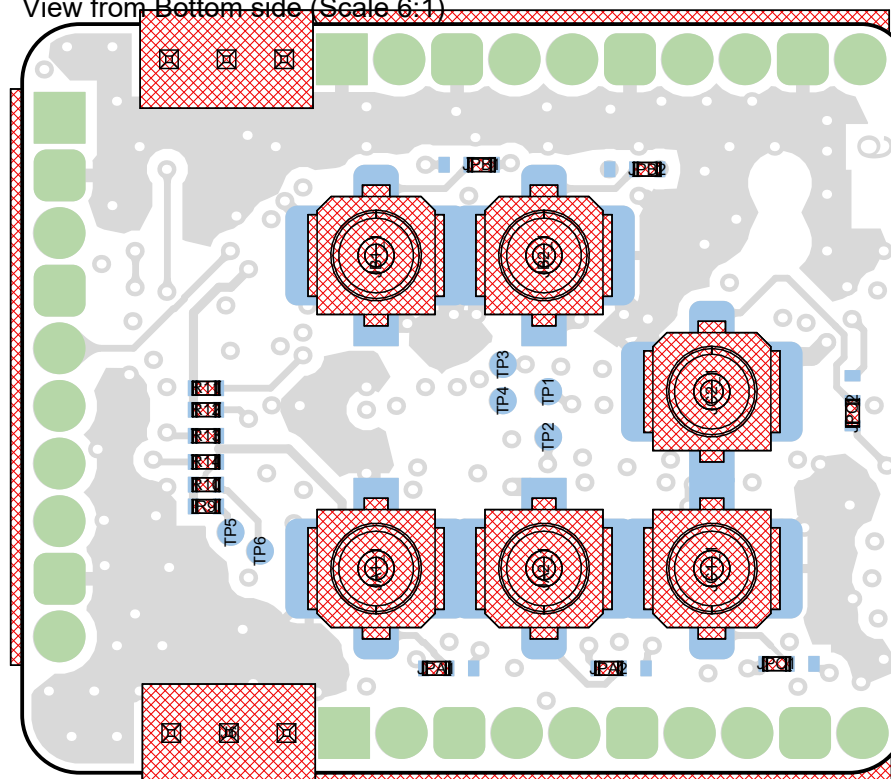
A

B

C

D

View from Bottom side (Scale 6:1)

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Revision: 1.0

Variant: Fabrication

File: DOC_CONN.PCBDwf

Project:

Connectors

Drawn By:

Checked By:

Sheet: 1/2

A

B

C

D

1

1

2

2

3

3

4

4

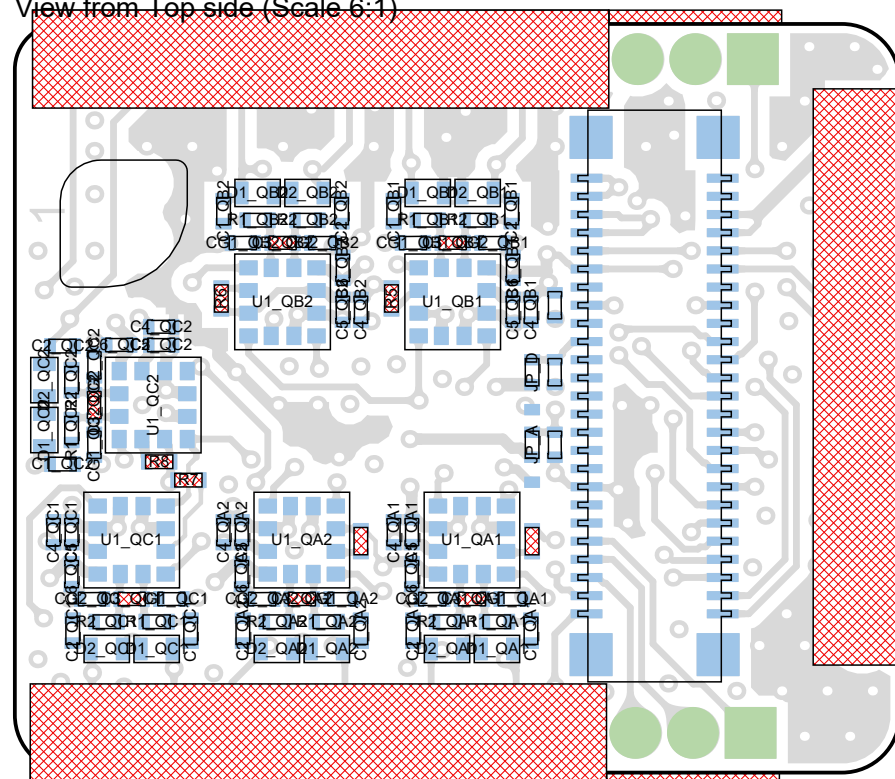
A

B

C

D

View from Top side (Scale 6:1)

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Variant: Fabrication

File: DOC_CONN.PCBDwf

Project:

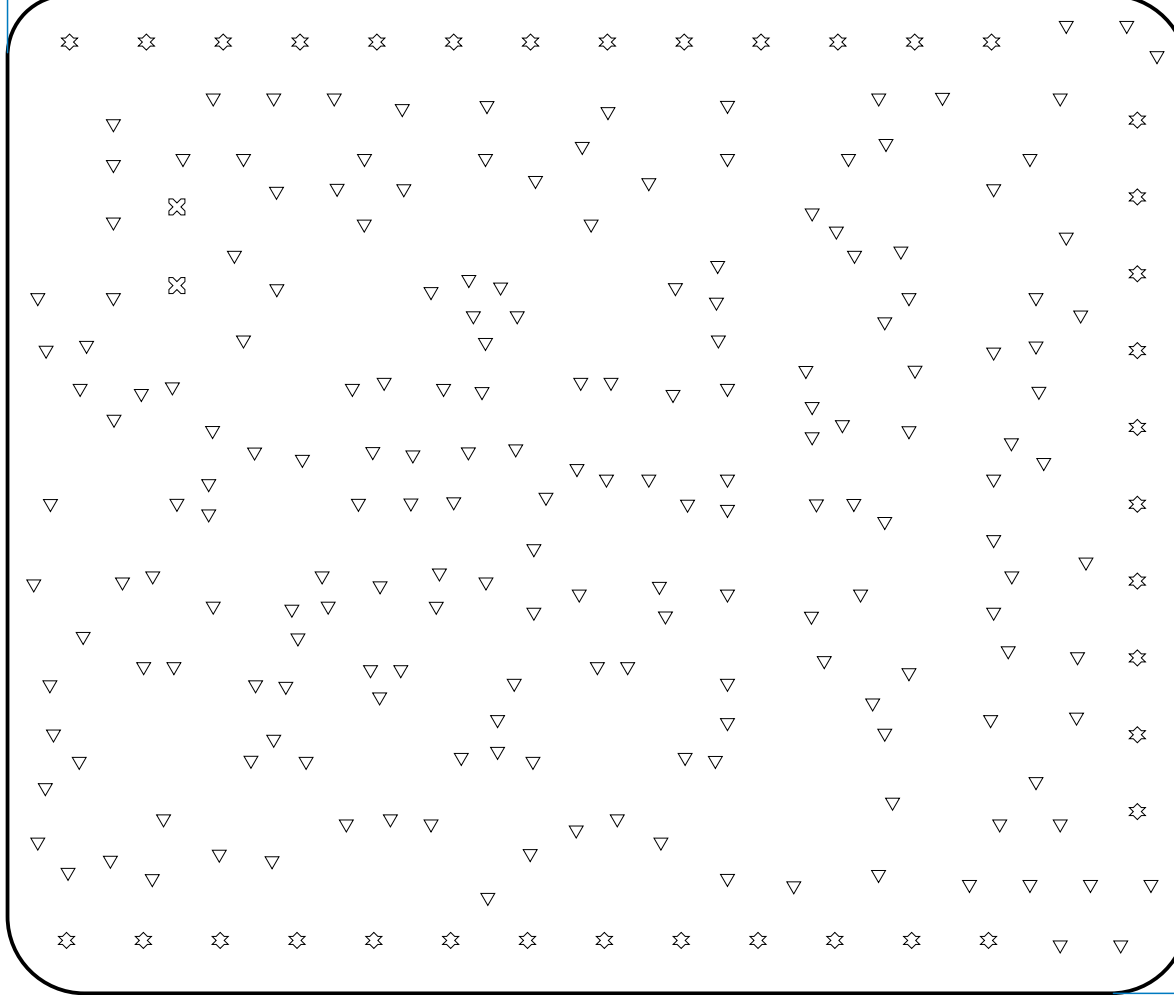
Connectors

Drawn By:

Checked By:

Sheet: 2/2

Drill Drawing View (Scale 8:1)



Drill Table

| Symbol | Count | Hole Size | Plated | Drill Layer Pair |
|-----------|-------|-----------|------------|--------------------------|
| ▽ | 193 | 0.20mm | Plated | Top Layer - Bottom Layer |
| ☆ | 36 | 0.71mm | Plated | Top Layer - Bottom Layer |
| ⊗ | 2 | 0.90mm | Non-Plated | Top Layer - Bottom Layer |
| 231 Total | | | | |

| | |
|--|----------------------------------|
| ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich | Project: Manufacturing |
| Laboratory: ETHZ D-ITET PBL Date: 13/11/2023 19:01 Revision: 1.0 Variant: Fabrication File: DOC_MANUFACTURE.PCBDwf | Drawn By: Checked By: |
| Sheet: 1/2 | |

A

B

C

D

Layer Stack Legend

| Layer | Type | Gerber | Thickness |
|---------------------------------|----------------|--------|-----------|
| Board Layer Stack Top Solder | Solder Mask | GTS | 0.025mm |
| Top Surface Finish | Surface Finish | | 0.004mm |
| Top Layer | Signal | GTL | 0.035mm |
| | Dielectric | | 0.099mm |
| Layer 1 (GND) | Signal | G1 | 0.015mm |
| | Dielectric | | 0.350mm |
| Layer 2 (signal) | Signal | G2 | 0.015mm |
| | Dielectric | | 0.109mm |
| Layer 3 (power) | Signal | G3 | 0.015mm |
| | Dielectric | | 0.350mm |
| Layer 4 (GND) | Signal | G4 | 0.015mm |
| | Dielectric | | 0.099mm |
| Bottom Layer | Signal | GBL | 0.035mm |
| Bottom Surface Finish | Surface Finish | | 0.004mm |
| Board Layer Stack Bottom Solder | Solder Mask | GBS | 0.025mm |

NOTES:

- Via in pad
- 0.8mm Board: Use JLCPCB standard stackup
- ENIG finish.

| | |
|--|----------------------------------|
| <div><div><div>ETH</div><div>Eidgenössische Technische Hochschule Zürich</div><div>Swiss Federal Institute of Technology Zurich</div></div><div>Laboratory: ETHZ D-ITET PBL</div><div>Date: 13/11/2023 19:01</div><div>Revision: 1.0</div><div>Variant: Fabrication</div><div>File: DOC_MANUFACTURE.PCBDwf</div></div> | Project: Manufacturing |
| | Drawn By: Checked By: |
| Sheet: 2/2 | |

A

B

C

D

A

B

C

D

Bill Of Materials

| Line # | Designator | Name | Quantity | Design Item Id | Manufacturer | Manufacturer Part Number |
|--------|---|--------------------------|----------|-----------------------------|--------------------|--------------------------|
| 1 | C5_QA1, C5_QA2, C5_QB1, C5_QB2, C5_QC1, C5_QC2, C6_QA1, C6_QA2, C6_QB1, C6_QB2, C6_QC1, C6_QC2 | 100 nF | 12 | CAP_0201_100n_10V | Murata | GRM033R6YA104ME14D |
| 2 | C4_QA1, C4_QA2, C4_QB1, C4_QB2, C4_QC1, C4_QC2, C7, C8, C9 | 1µF | 9 | CAP_0201_1u_10V | Murata | GRM033C81A105ME05D |
| 3 | CG1_QA1, CG1_QA2, CG1_QB1, CG1_QB2, CG1_QC1, CG1_QC2, CG2_QA1, CG2_QA2, CG2_QB1, CG2_QB2, CG2_QC1, CG2_QC2 | 110pF | 12 | CAP_0201_110p_50V | Murata | GRM0335C1H111JA01D |
| 5 | R1_QA1, R1_QA2, R1_QB1, R1_QB2, R1_QC1, R1_QC2, R2_QA1, R2_QA2, R2_QB1, R2_QB2, R2_QC1, R2_QC2 | 4.7k | 12 | R_0201_4.7K | Panasonic | ERJ-1GNF4701C |
| 6 | C1_QA1, C1_QA2, C1_QB1, C1_QB2, C1_QC1, C1_QC2, C2_QA1, C2_QA2, C2_QB1, C2_QB2, C2_QC1, C2_QC2 | 0R | 12 | R_0201_0R_short_cap | Panasonic | ERJ-1GN0R00C |
| 6 | JP_A, JP_D | JMP | 2 | JMP_0201_3w | Panasonic | ERJ-1GN0R00C |
| 7 | D1_QA1, D1_QA2, D1_QB1, D1_QB2, D1_QC1, D1_QC2, D2_QA1, D2_QA2, D2_QB1, D2_QB2, D2_QC1, D2_QC2 | TPD1E01B04DPYRQ1 | 12 | TPD1E01B04DPYRQ1 | Texas Instruments | TPD1E01B04DPYRQ1 |
| 8 | U1_QA1, U1_QA2, U1_QB1, U1_QB2, U1_QC1, U1_QC2 | LIS2DUXS12TR | 6 | LIS2DUXS12TR | STMicroelectronics | LIS2DUXS12TR |
| 11 | J1 | VitalCore Interface v1.0 | 1 | BACKPACK_INTERFACE_ V1.0 | Hirose | DF40C(2.0)-50DS-0.4V(51) |



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Revision: 1.0

Variant: Fabrication

File: DOC_BOM.PCBDwf

Project:

BOM

Drawn By:

Checked By:

Sheet: 1/1

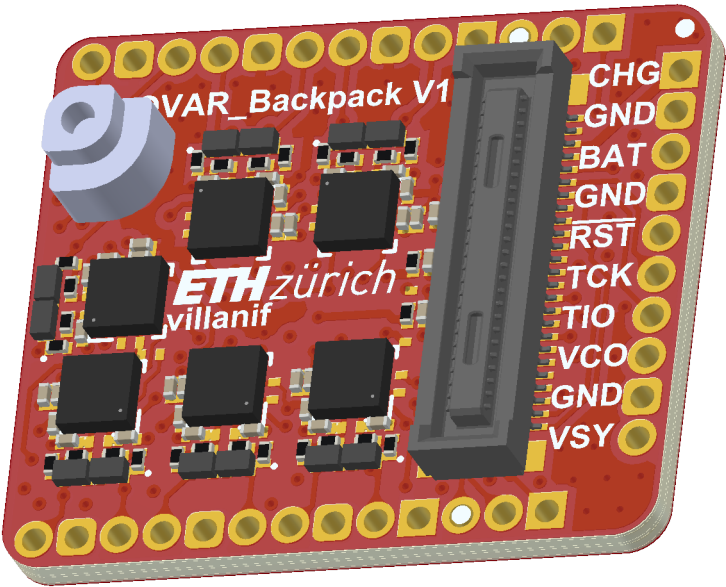
A

B

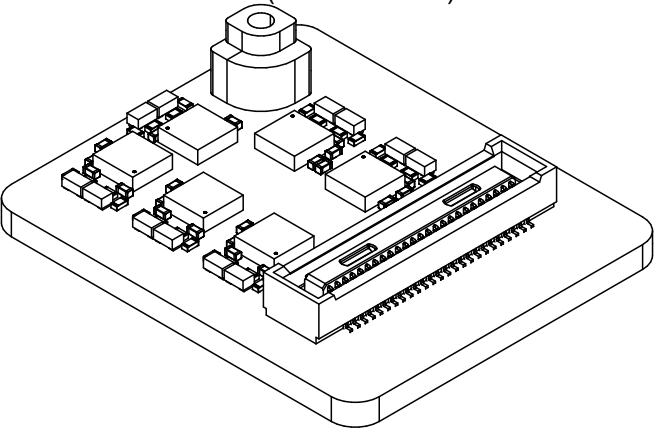
C

D

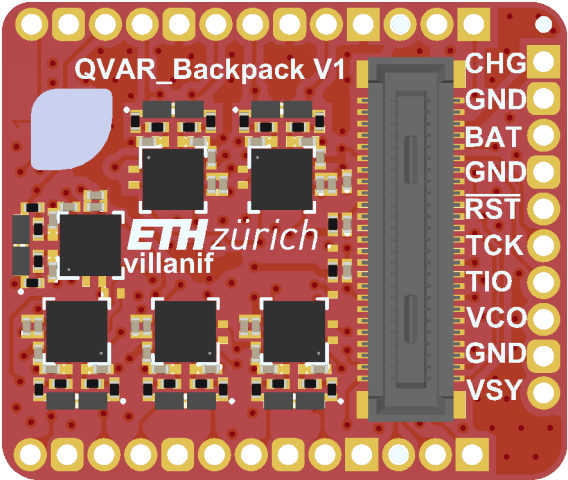
Realistic View



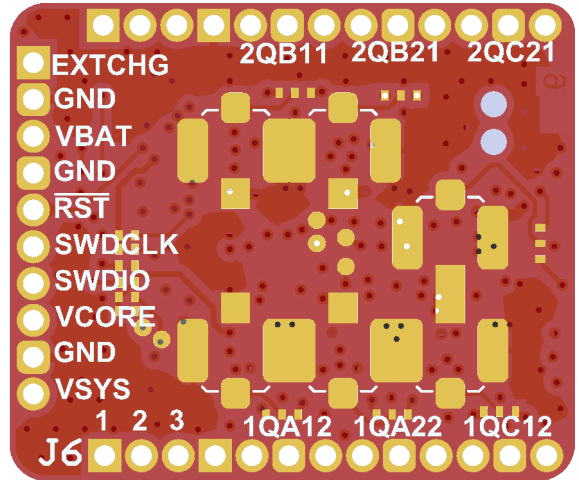
View from Front side (Scale 3.528:1)



Realistic View



Realistic View



ETH

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Date: 13/11/2023 19:02

Revision: 1.0

Variant: Fabrication

File: DOC_3D.PCBDwf

Project:
3D Render

Drawn By:
Checked By: