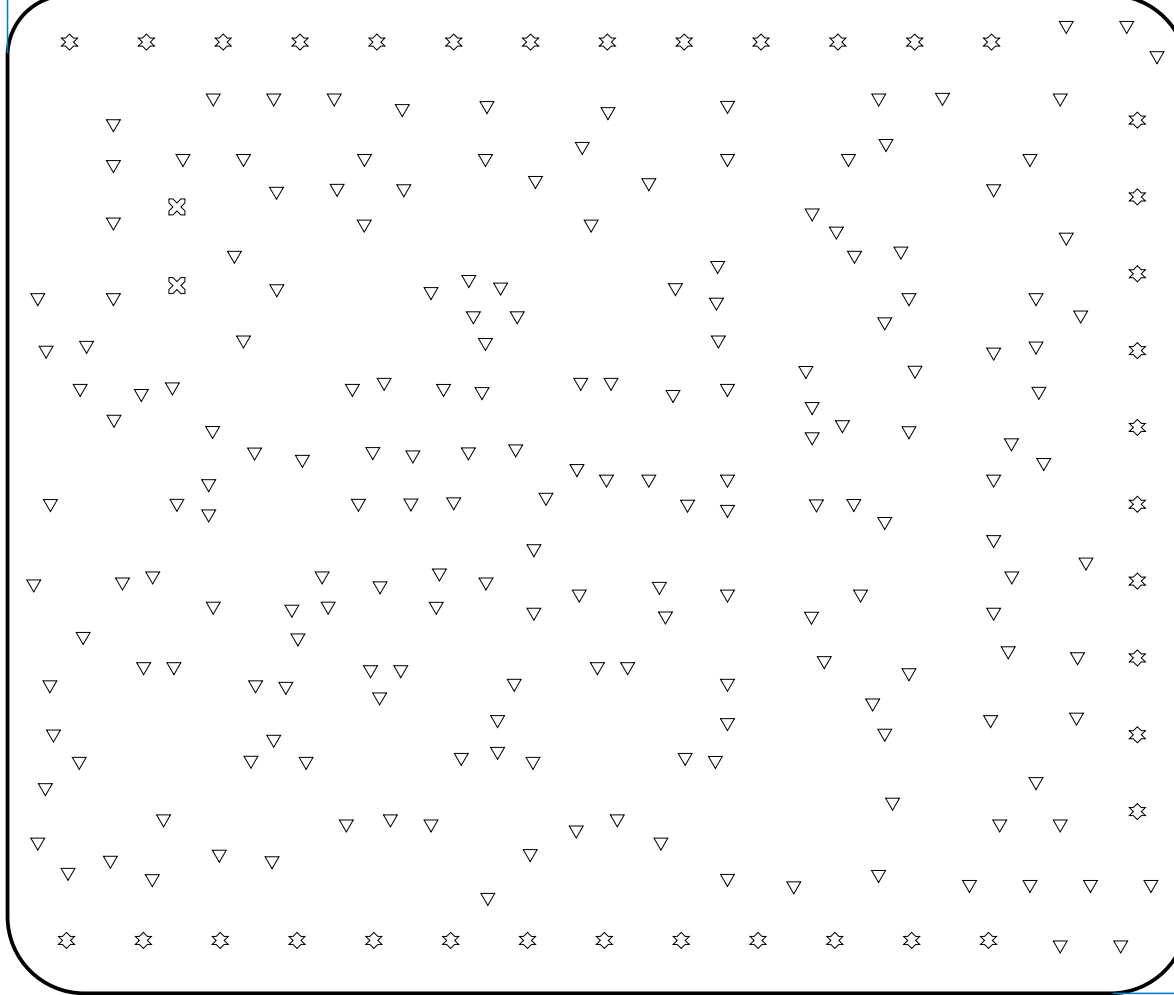


Drill Drawing View (Scale 8:1)



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair
▽	193	0.20mm	Plated	Top Layer - Bottom Layer
☆	36	0.71mm	Plated	Top Layer - Bottom Layer
⊗	2	0.90mm	Non-Plated	Top Layer - Bottom Layer
231 Total				

ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: Qvar 6 Channel Vitalcore Backpack
	Manufacturing
Laboratory: ETHZ D-ITET PBL	Drawn By: villanif
Date: 21/07/2025 14:05	Checked By: topolonelli, nschae, peterste
Revision: 1.0	
Variant: Fabrication	
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Layer Stack Legend

Layer	Type	Gerber	Thickness
Board Layer Stack Top Solder	Solder Mask	GTS	0.025mm
Top Surface Finish	Surface Finish		0.004mm
Top Layer	Signal	GTL	0.035mm
	<i>Dielectric</i>		<i>0.099mm</i>
Layer 1 (GND)	Signal	G1	0.015mm
	<i>Dielectric</i>		<i>0.350mm</i>
Layer 2 (signal)	Signal	G2	0.015mm
	<i>Dielectric</i>		<i>0.109mm</i>
Layer 3 (power)	Signal	G3	0.015mm
	<i>Dielectric</i>		<i>0.350mm</i>
Layer 4 (GND)	Signal	G4	0.015mm
	<i>Dielectric</i>		<i>0.099mm</i>
Bottom Layer	Signal	GBL	0.035mm
Bottom Surface Finish	Surface Finish		0.004mm
Board Layer Stack Bottom Solder	Solder Mask	GBS	0.025mm

NOTES:

- Via in pad
- 0.8mm Board: Use JLCPCB standard stackup
- ENIG finish.



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