

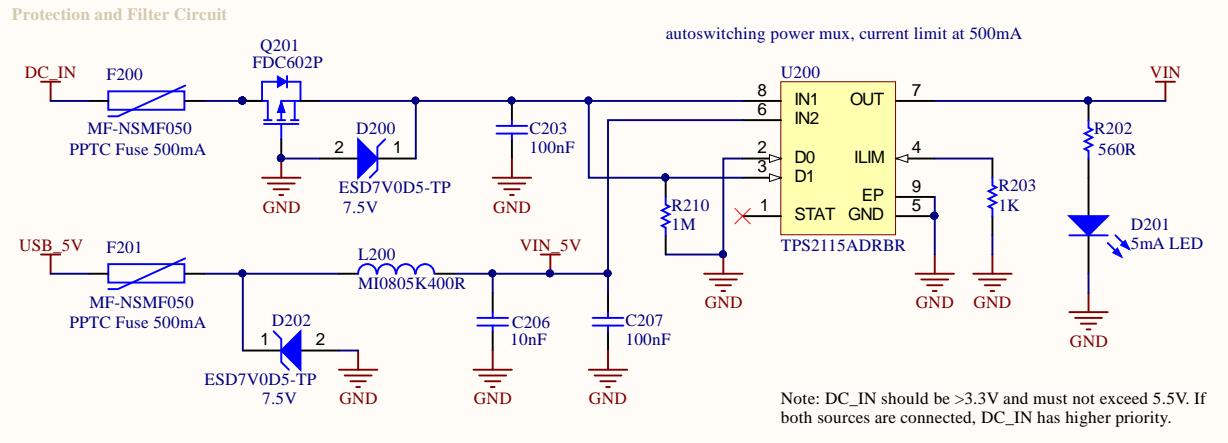
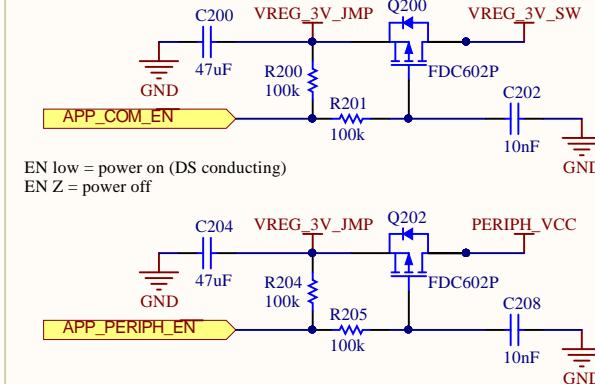
**ETHZurich**  
Logo ETH Zurich



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Swiss Federal Institute of Technology Zurich

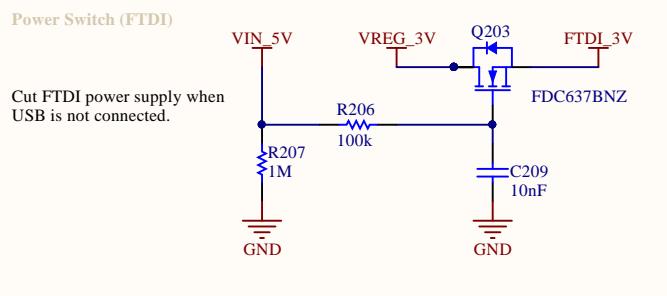
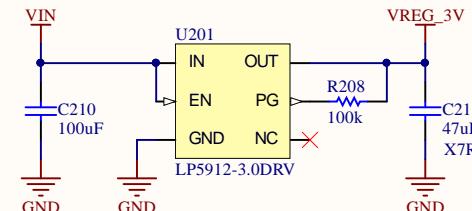
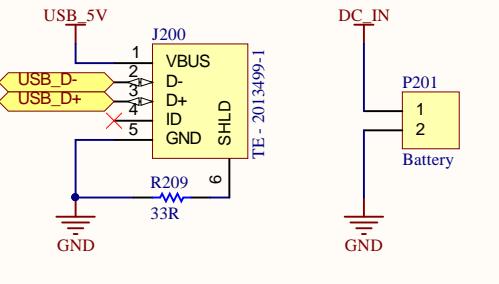
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Datum: 17/08/2017 10:35:34			Ersteller: Reto Da Forno	Seite 1 von 6
File: C:\Users\Public\Documents\Altium\Projects\DPP2_Dev_Board\Overview.SchDoc				

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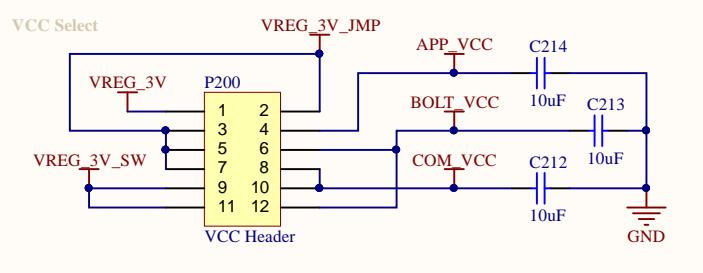
**Power Switch (COM & APP peripherals)**

B

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**Regulator (500mA LDO)****Input Connectors (Micro USB and DC\_IN)**

D



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Zeichnung Titel:

## DPP2 Dev Board - Power Supply

Zeichnungsnummer: *	Rev. 1.0	Format: A4 Q	Institut: Computer Engineering Group, TIK	Projekt: Power.SchDoc
Datum: 17/08/2017	10:35:34	Ersteller: Reto Da Forno	Seite 2 von 6	
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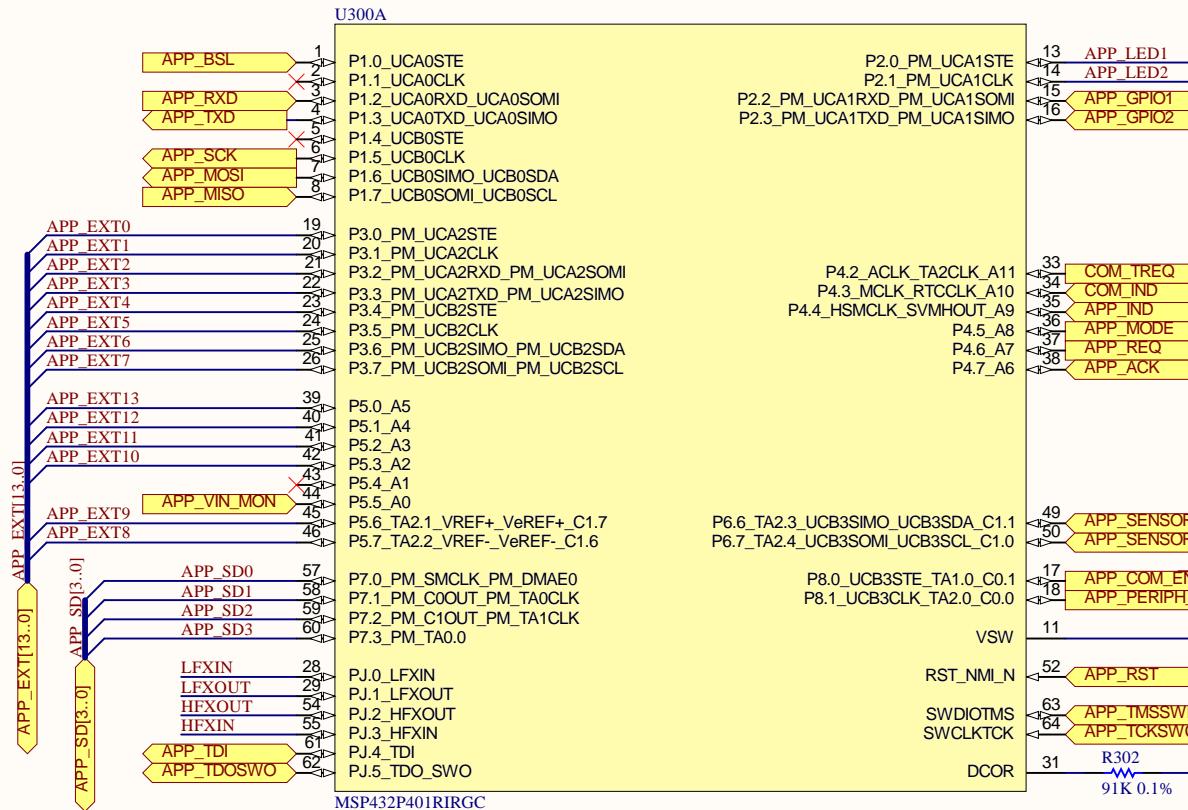
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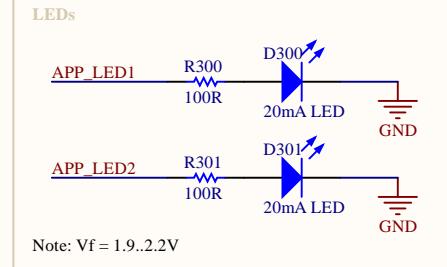
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Note: P2.0 - P2.3 are high drive pins (up to 20mA)



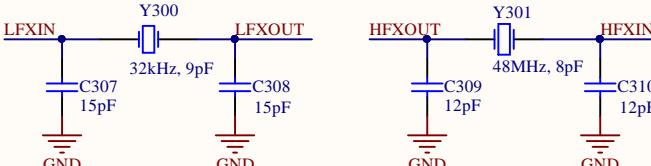
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External crystal oscillators (LF and HF)



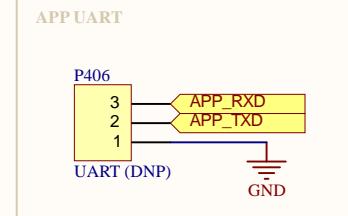
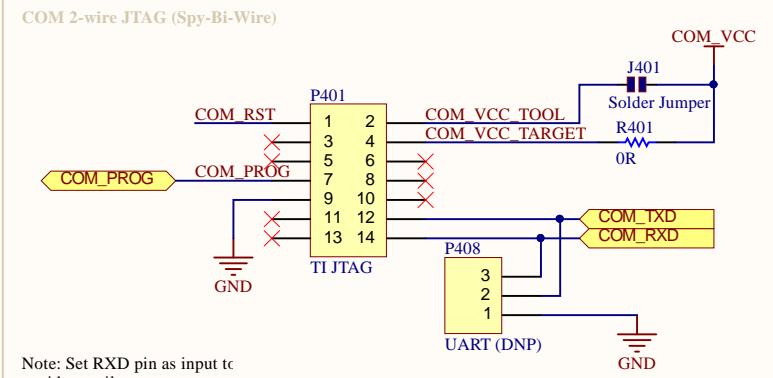
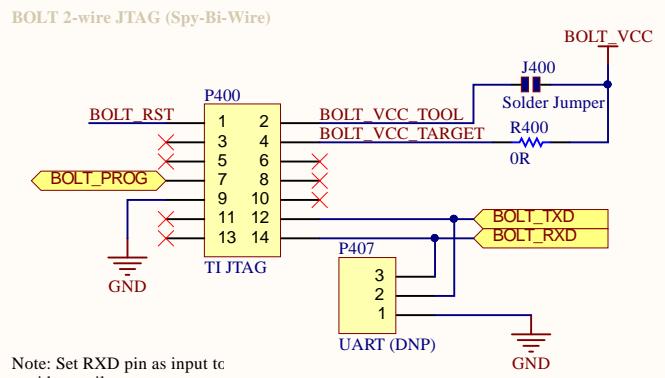
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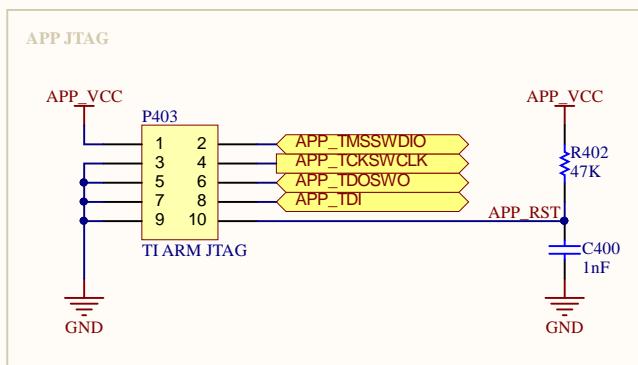
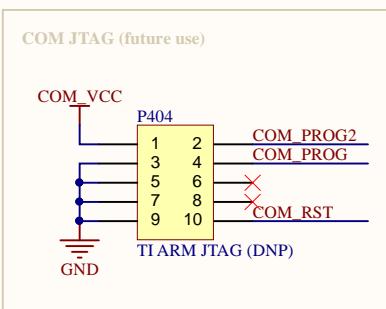
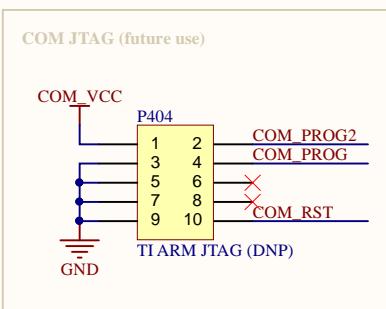
**DPP2 Dev Board - MSP432 Microcontroller**

Zeichnungsnummer: *	Rev. 1.0	Format: A4 Q	Institut: Computer Engineering Group, TIK	Projekt: Microcontroller.SchDoc
Datum: 17/08/2017	10:35:34	Ersteller: Reto Da Forno	Seite 3 von 6	
File: C:\Users\Public\Documents\Altium\Projects\DPP2_Dev_Board\Microcontroller.SchDoc				

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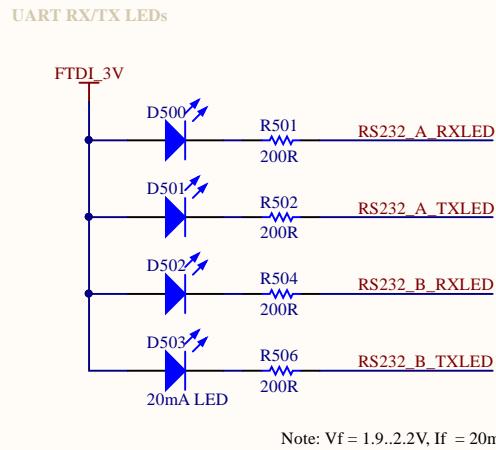
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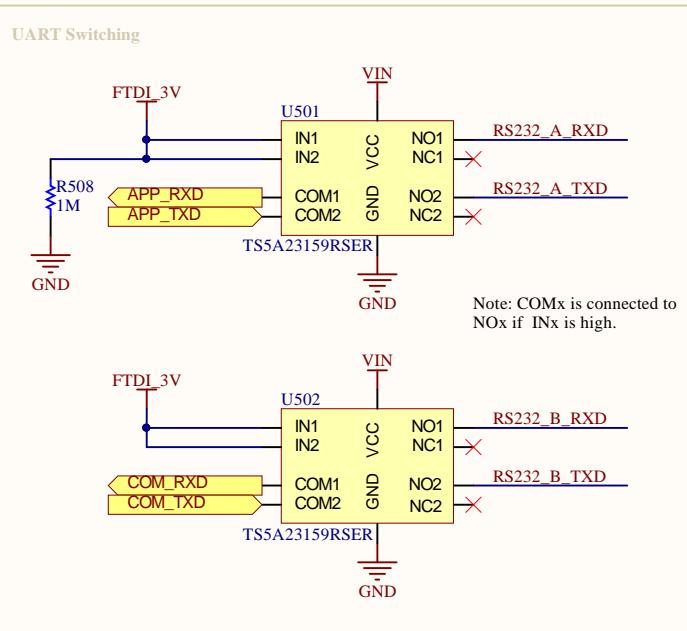
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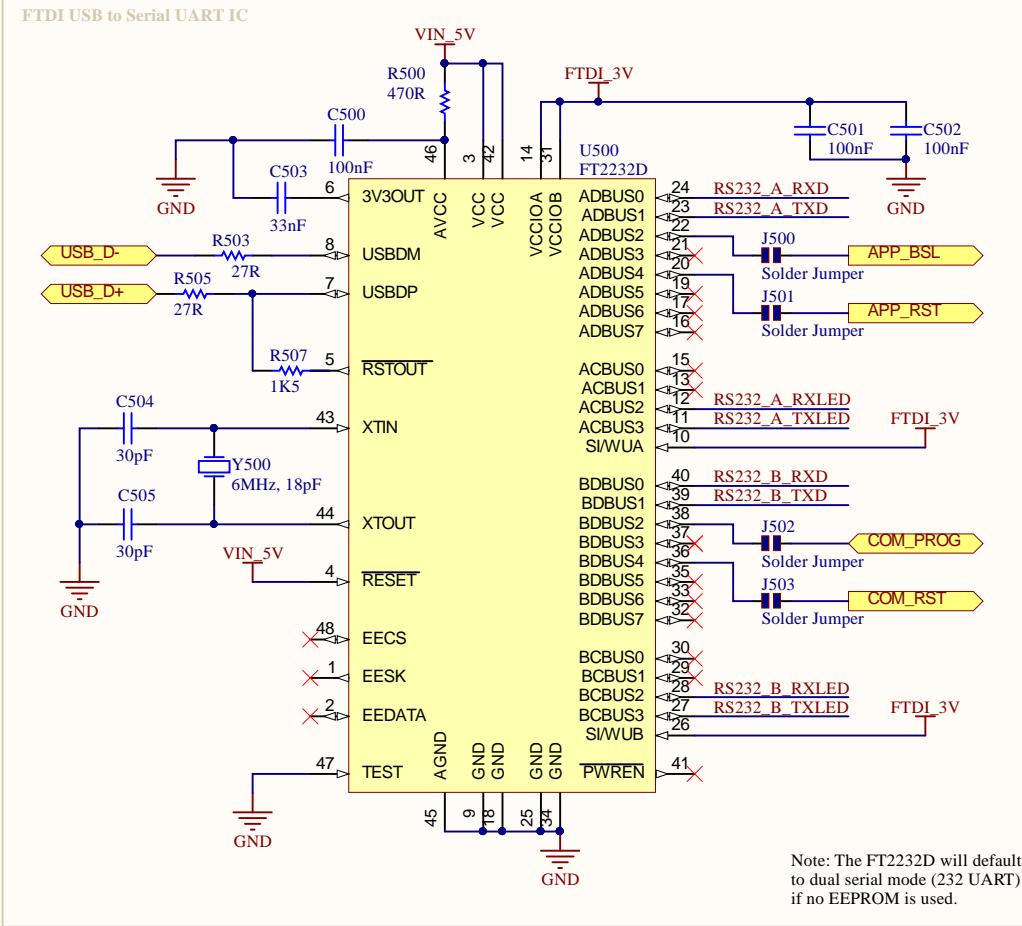
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Zeichnungsnummer: \* Rev: 1.0 Format: Institut: Computer Engineering Group, TIK Projekt: Serial.SchDoc

Datum: 17/08/2017 10:35:34 Ersteller: Reto Da Forno Seite 5 von 6

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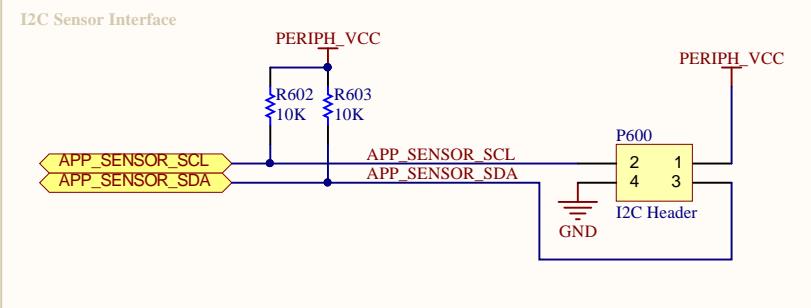
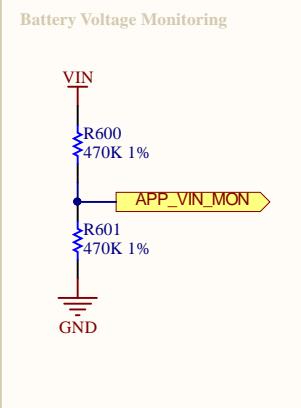
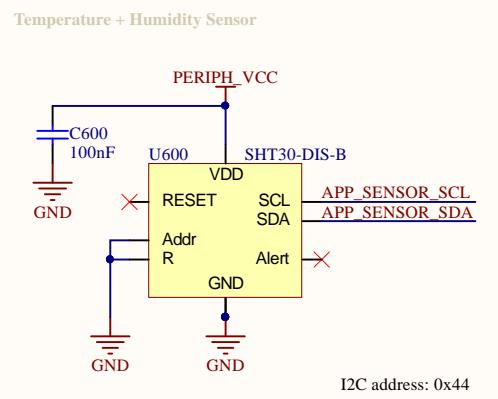
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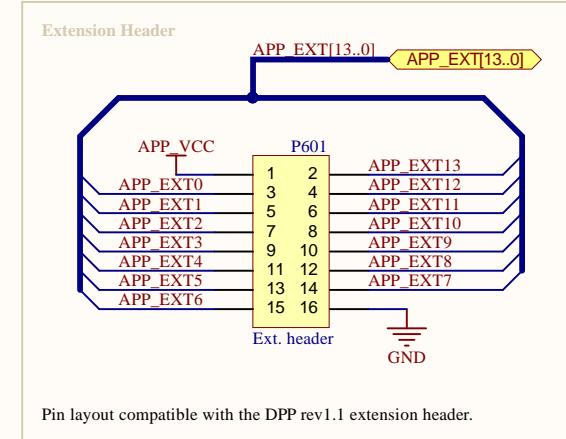
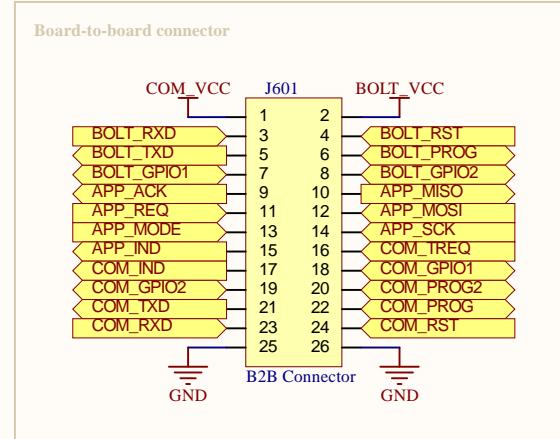
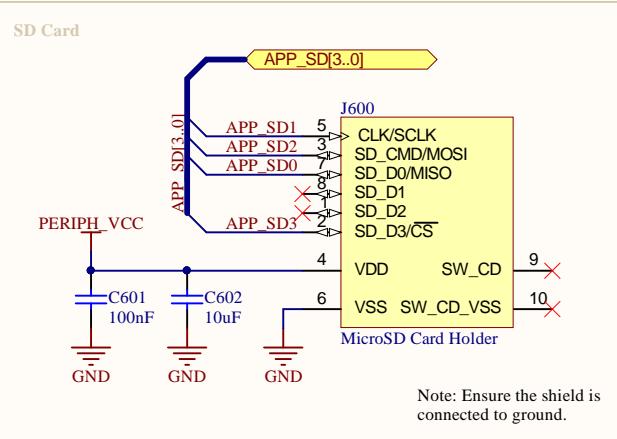
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Zeichnungs Titel:

**DPP2 Dev Board - Peripherals**

Eidgenössische Technische Hochschule Zürich  
Swiss Federal Institute of Technology Zurich

Zeichnungsnummer: \*

Rev. 1.0

Datum: 17/08/2017 10:35:35

Format: Institut: Computer Engineering Group, TIK

Projekt: Peripherals.SchDoc

A4 Q Ersteller: Reto Da Forno

Seite 6 von 6

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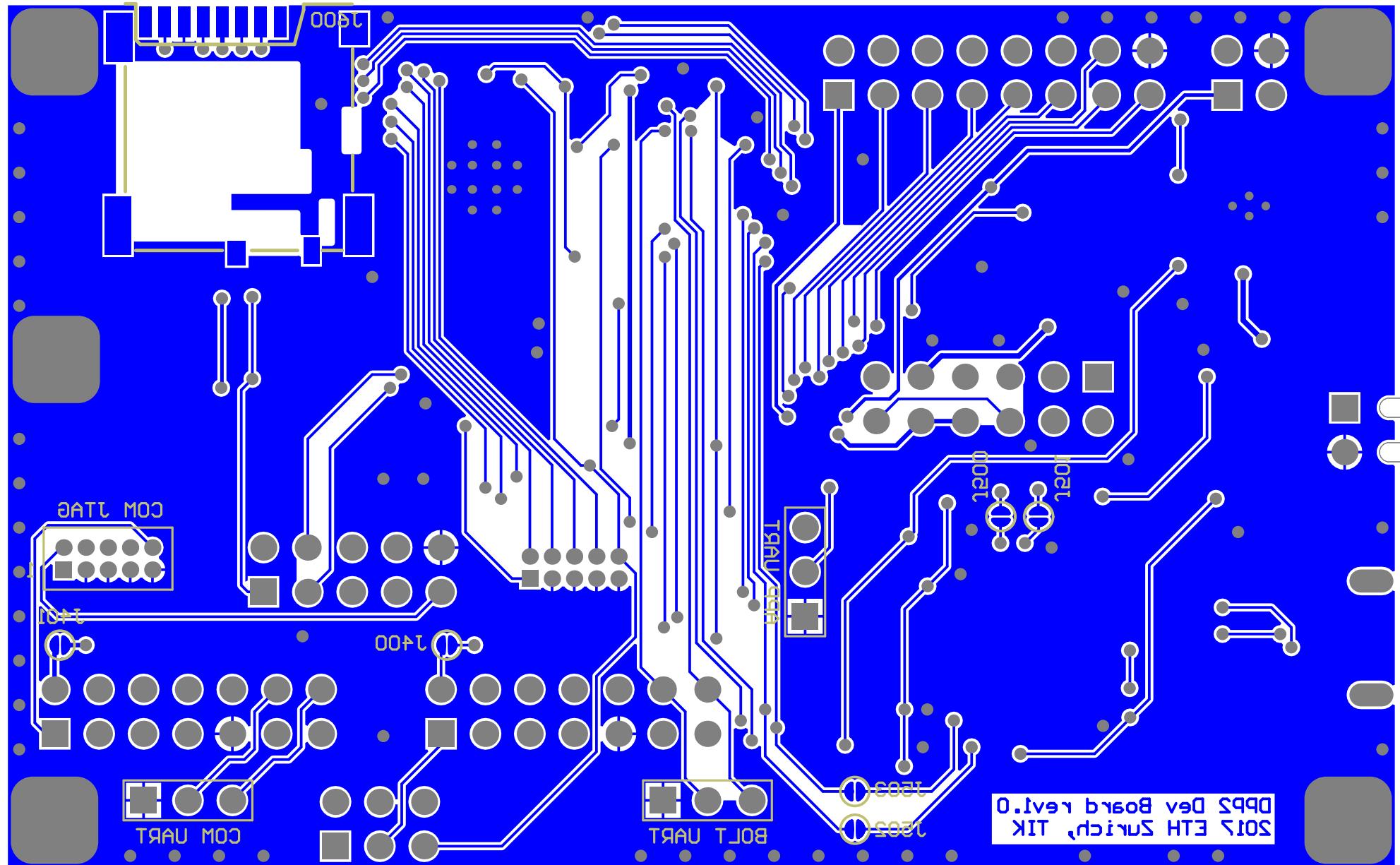
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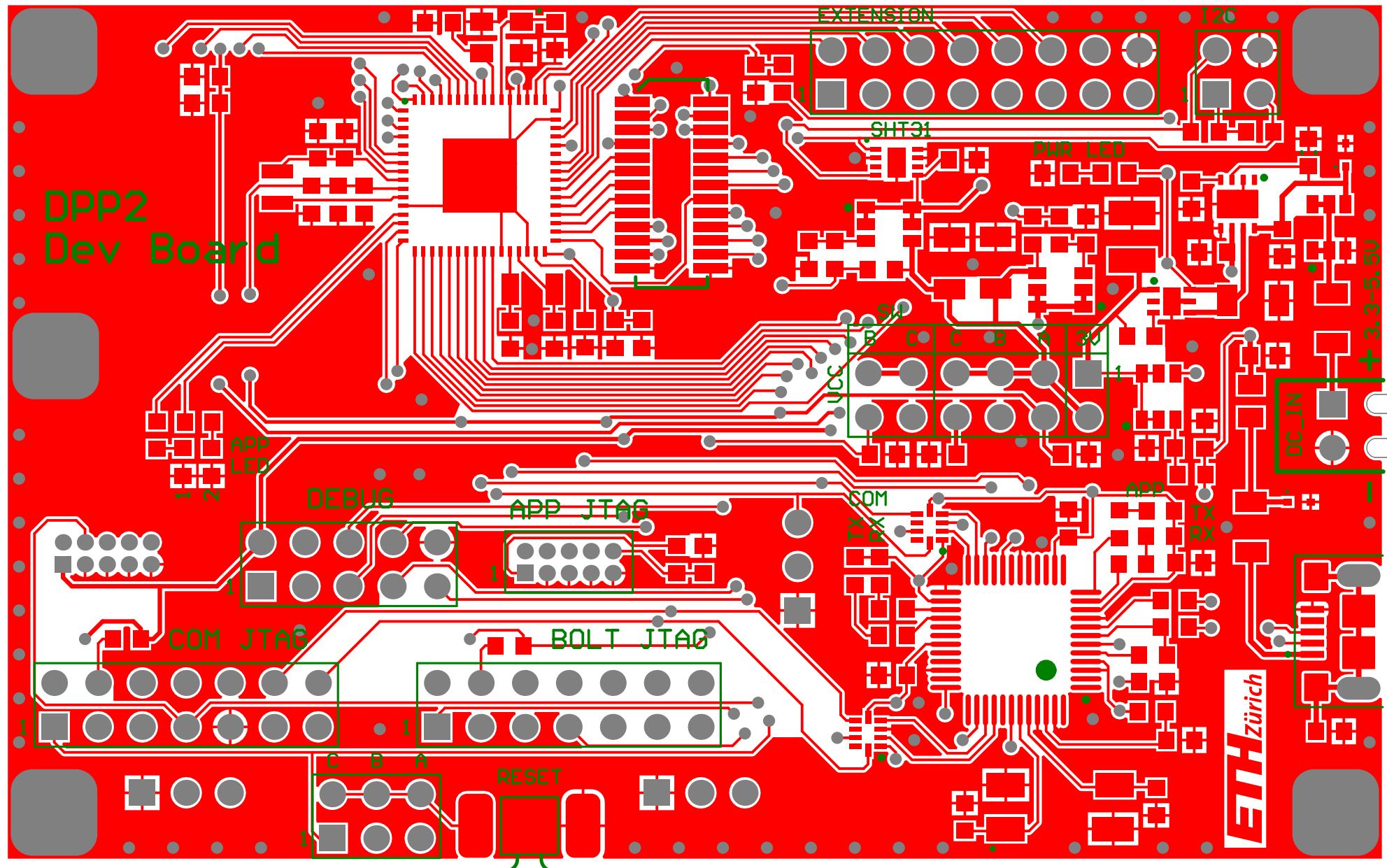
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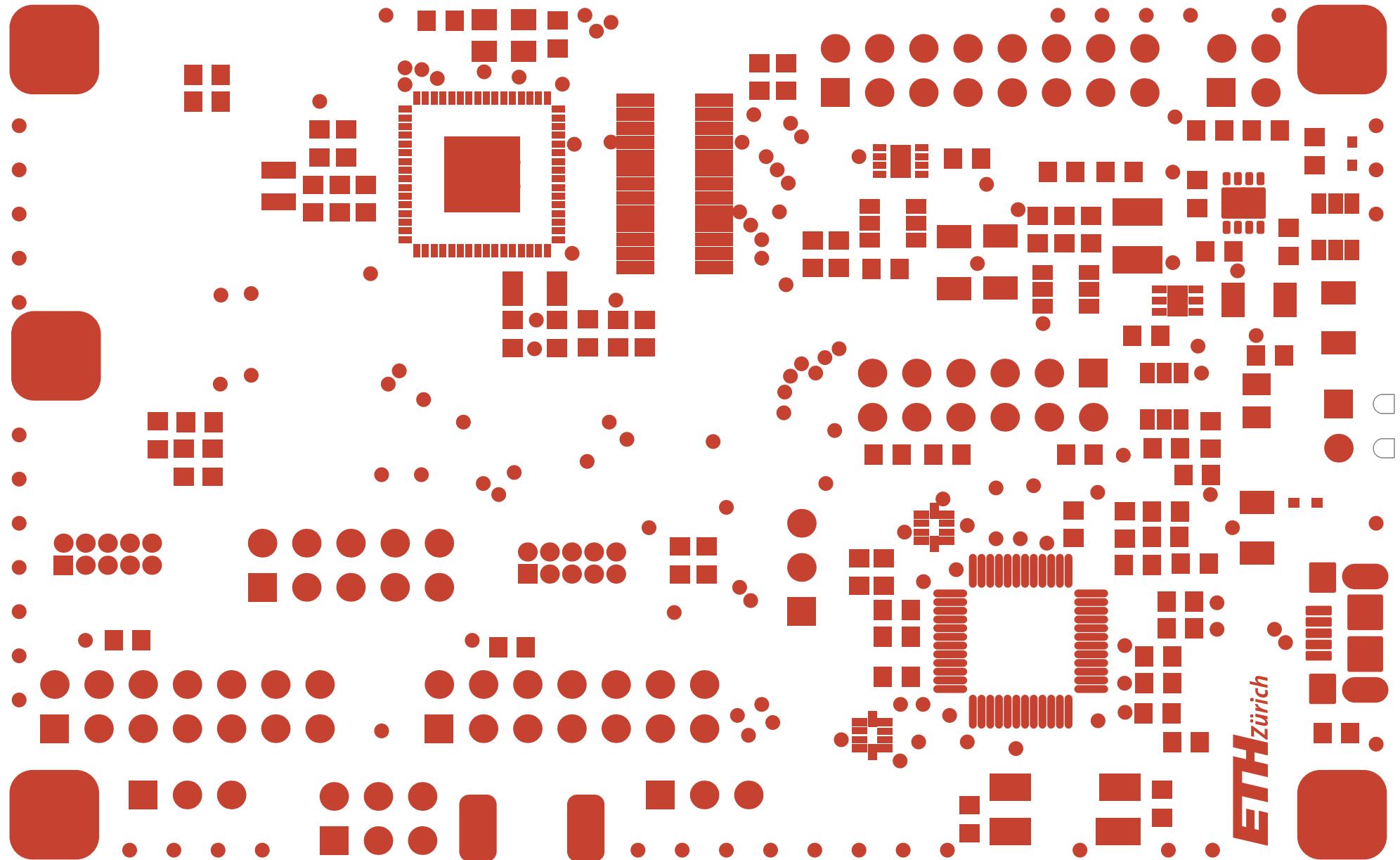
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*ETH* Zürich

