

A

A

B

B

C

C

D

D



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Swiss Federal Institute of Technology Zurich

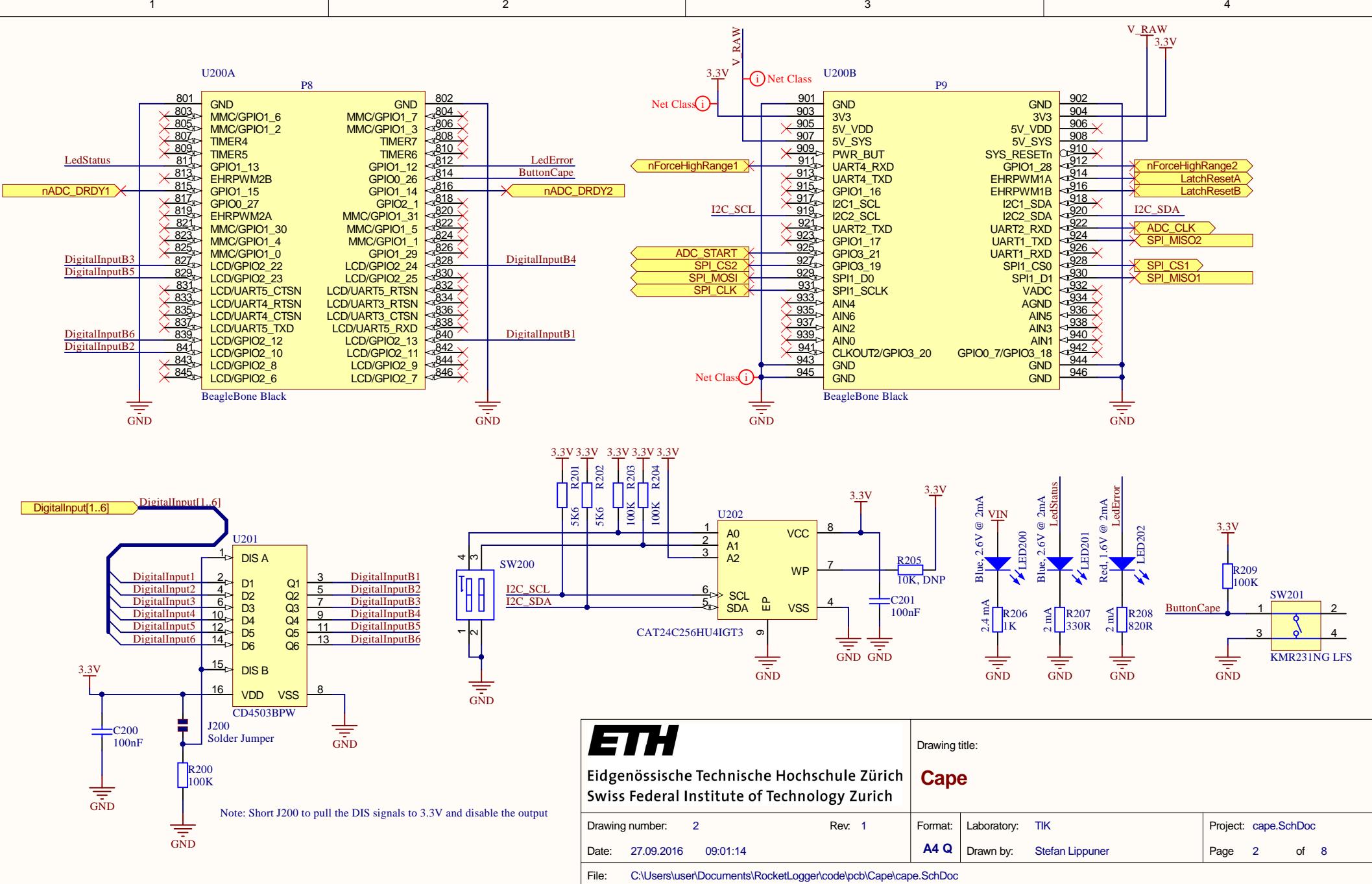
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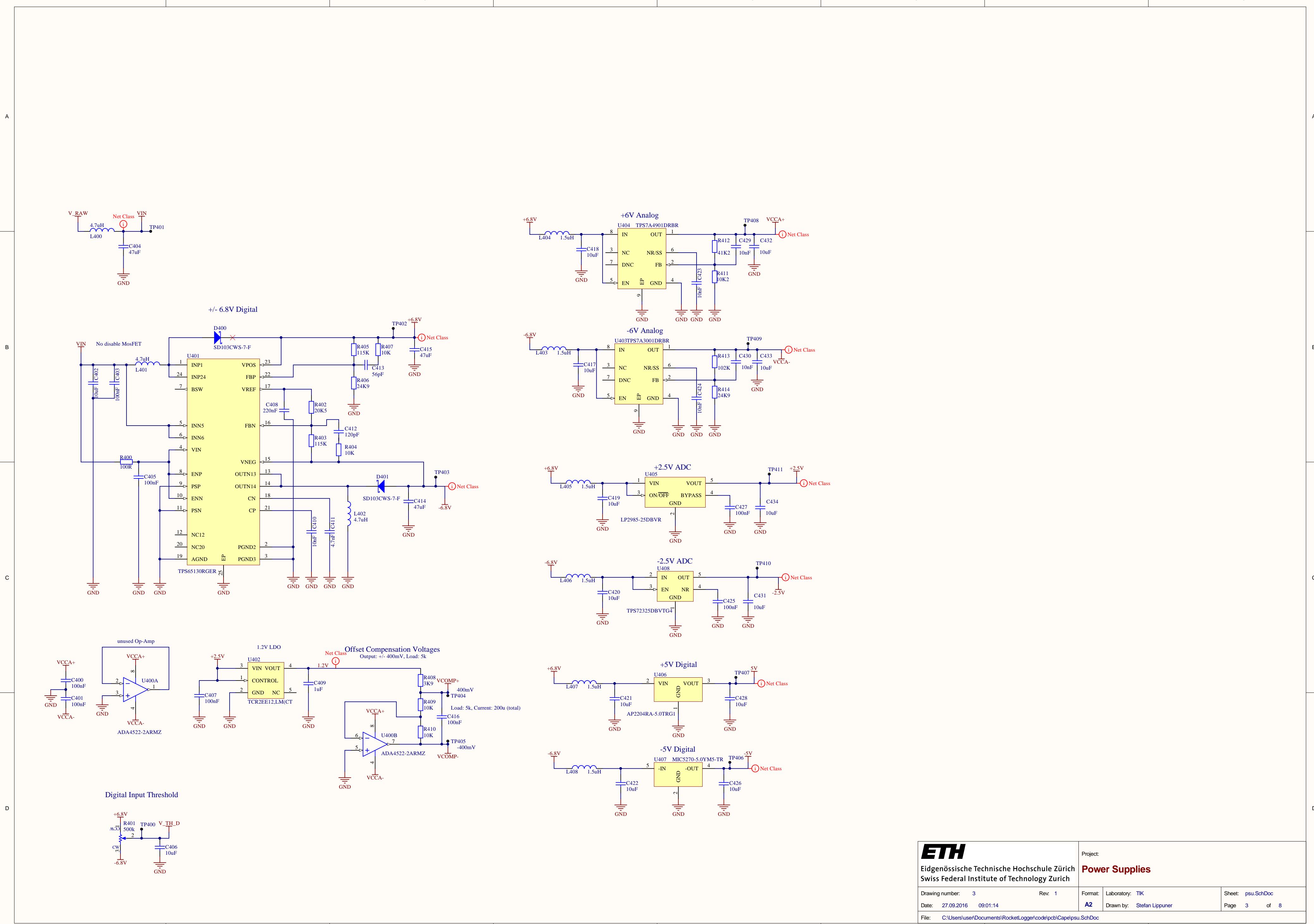
Top

Drawing number: 1 Rev: 1 Format: Laboratory: TIK Sheet: top.SchDoc

Date: 27.09.2016 09:01:14 A3 Drawn by: Stefan Lippuner

File: C:\Users\user\Documents\RocketLogger\code\pcb\Cape\top.SchDoc

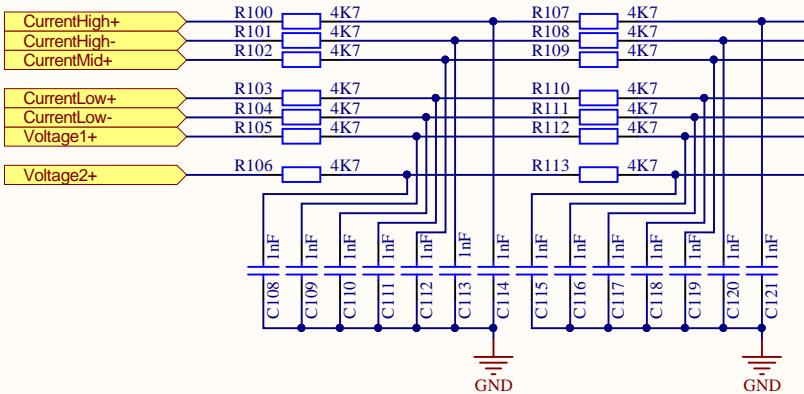




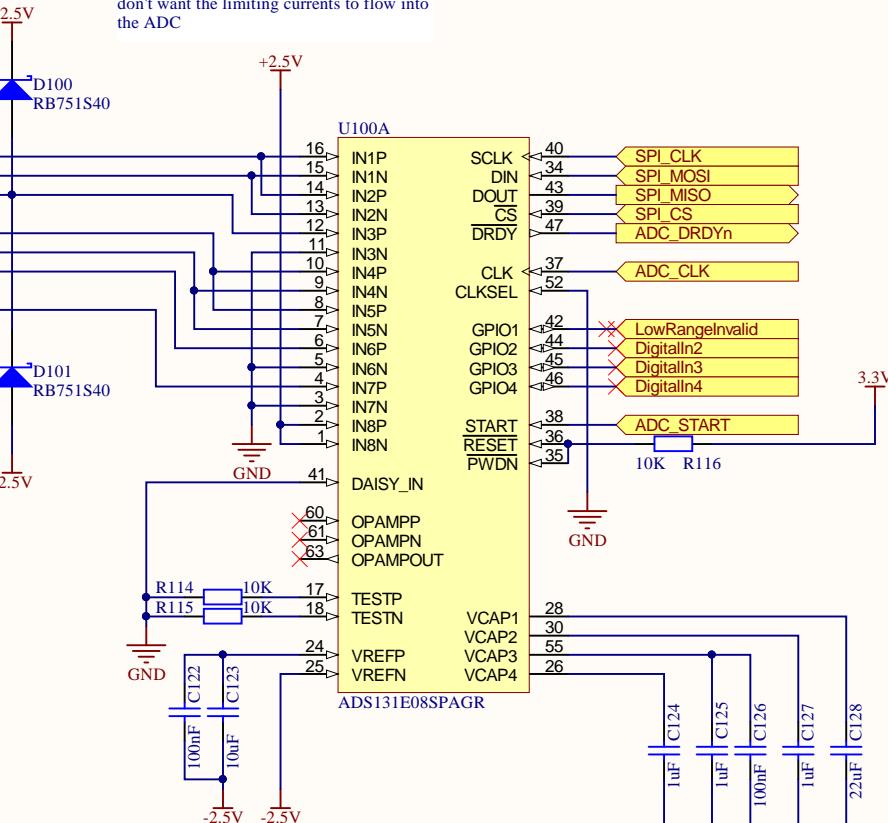
A

Resistors limit input current to 638uA

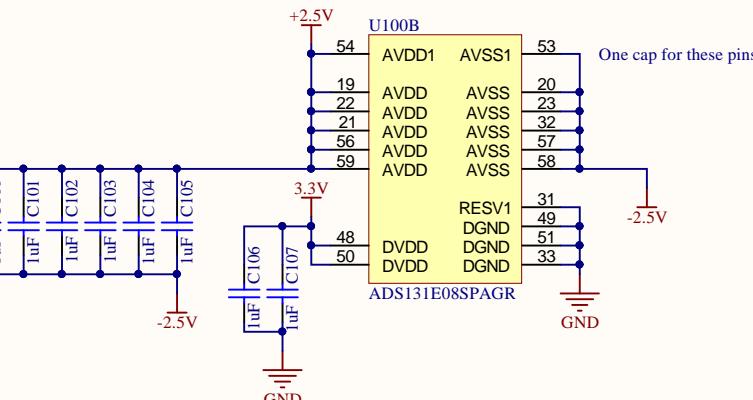
2nd order filter, -3dB @ 33.9kHz



The medium range voltages can exceed the ADC supply during normal operation, we don't want the limiting currents to flow into the ADC



B



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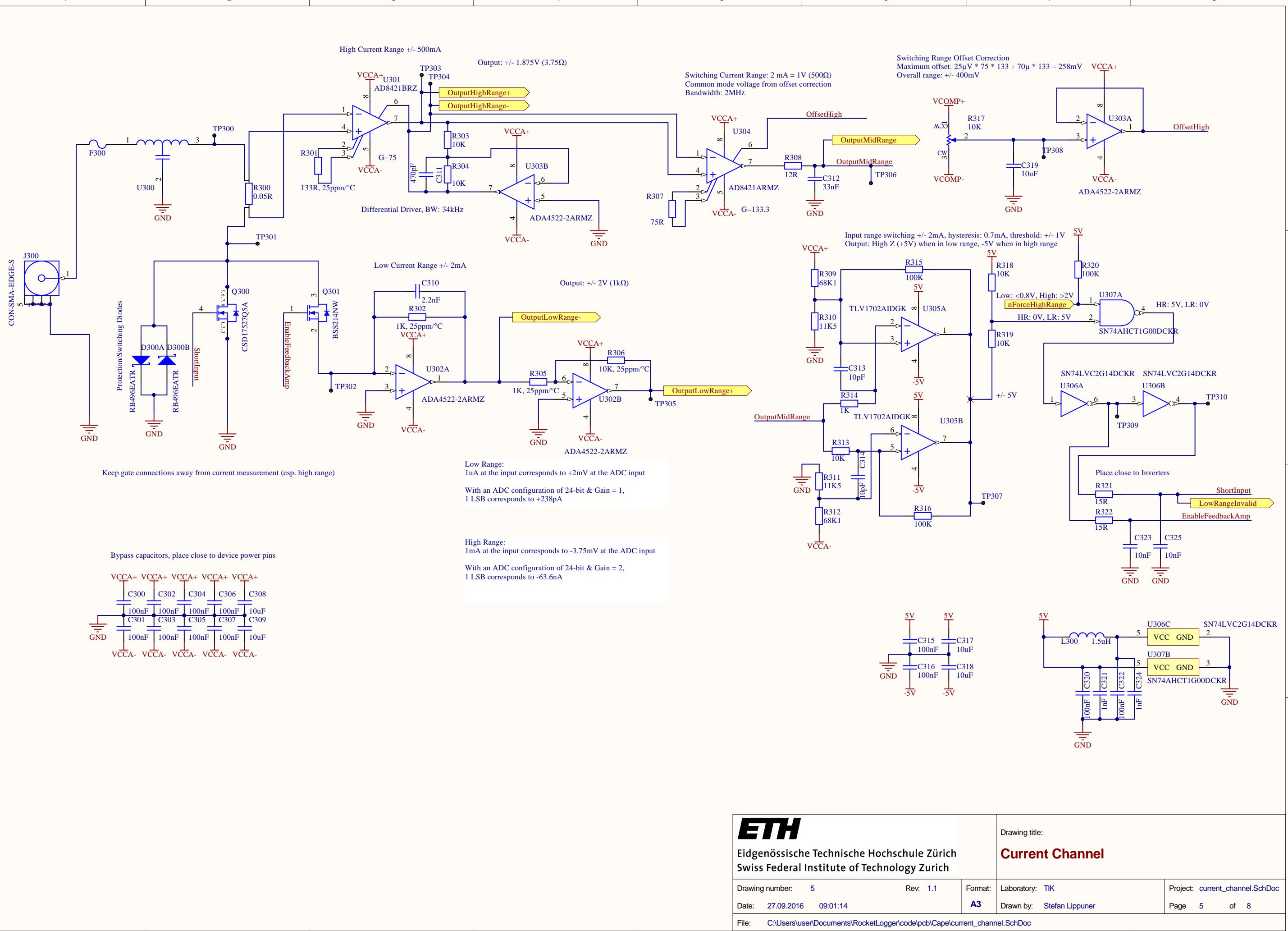
Drawing number: 4 Rev. 1 Format: Laboratory: TIK Project: adc.SchDoc

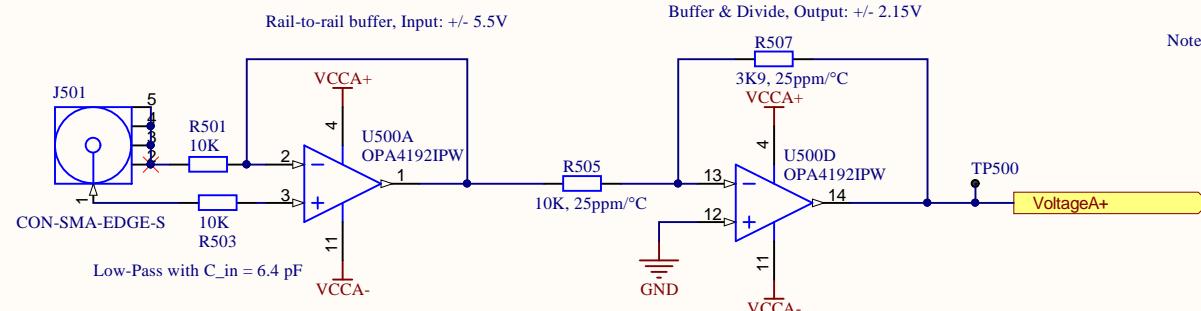
Date: 27.09.2016 09:01:14 Format: A4 Q Drawn by: Stefan Lippuner

File: C:\Users\user\Documents\RocketLogger\code\pcb\Cape\adc.SchDoc Page 4 of 8

Drawing title:

ADC

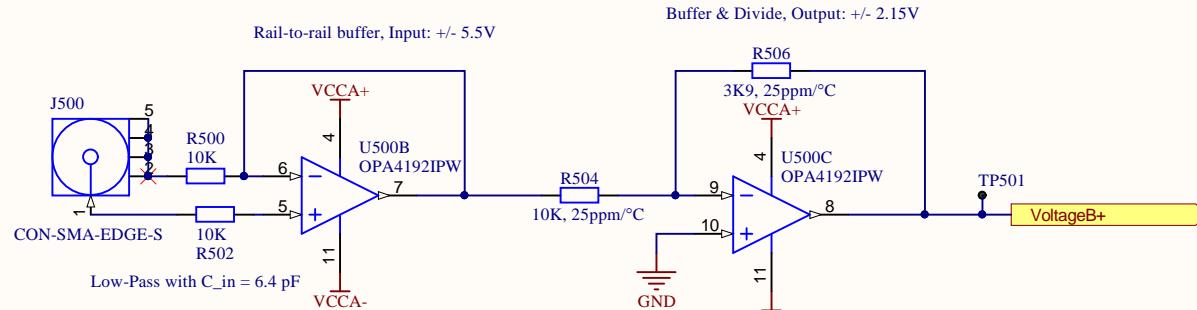




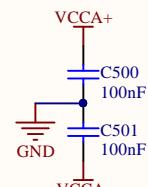
Note: Two channels share an Op Amp

1V at the input corresponds to -390mV at the ADC input

With an ADC configuration of 24-bit & Gain = 1,
1 LSB corresponds to -1.22 μ V



Note: For pseudo-differential inputs, the maximum amplitude
is +/- 2.2V



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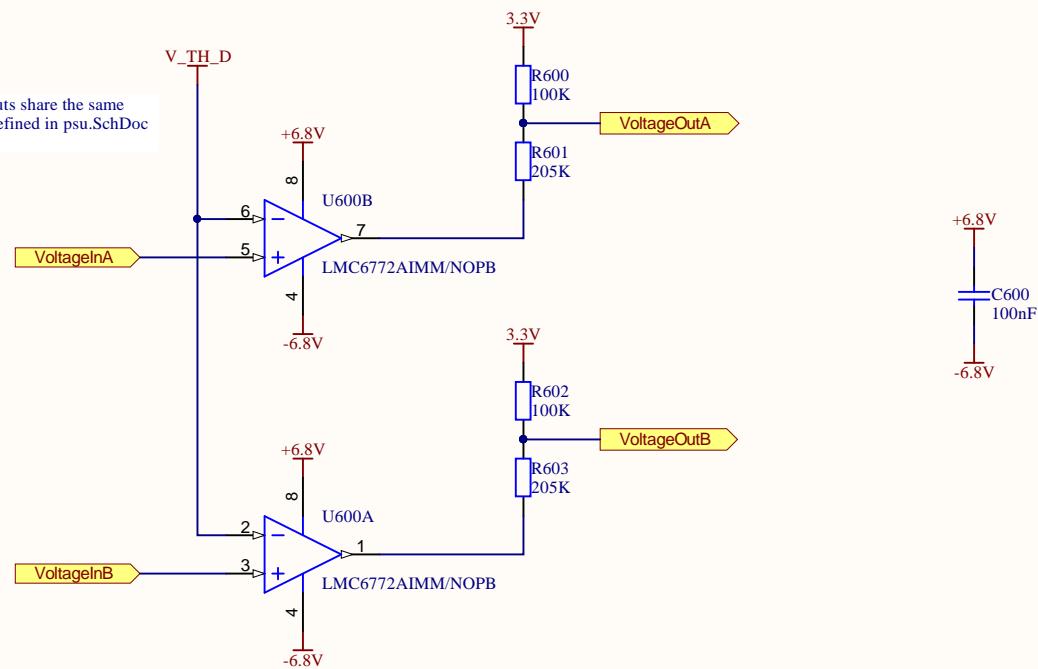
Drawing title:

Voltage Channel

Drawing number:	6	Rev.	1	Format:	Laboratory:	TIK	Project:	voltage_channel.SchDoc
Date:	27.09.2016	09:01:14		A4 Q	Drawn by:	Stefan Lippuner		
File:	C:\Users\user\Documents\RocketLogger\code\pcb\Cape\voltage_channel.SchDoc							

A

Note: All the digital inputs share the same (adjustable) threshold, defined in psu.SchDoc



B

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Drawing title:

Digital Voltage Channel

Drawing number: 7 Rev. 1

Date: 27.09.2016 09:01:14

File: C:\Users\user\Documents\RocketLogger\code\pcb\Cape\digital_voltage_channel.SchDoc

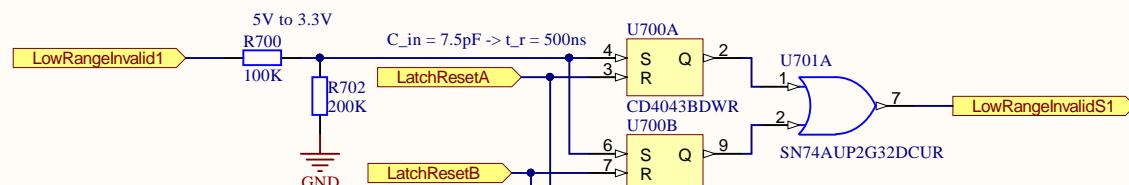
Format: Laboratory: TIK

A4 Q Drawn by: Stefan Lippuner

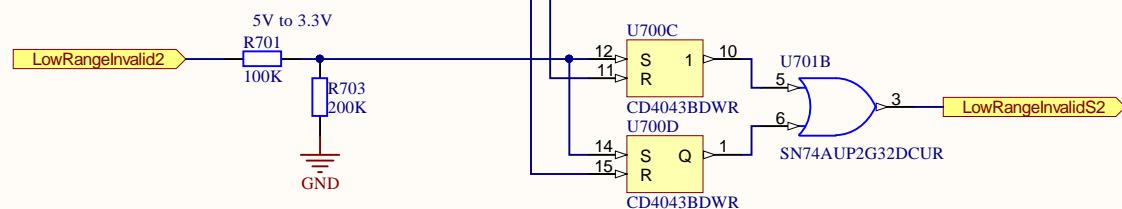
Project: digital_voltage_channel.SchDoc

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A

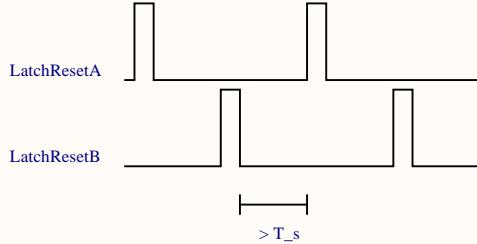
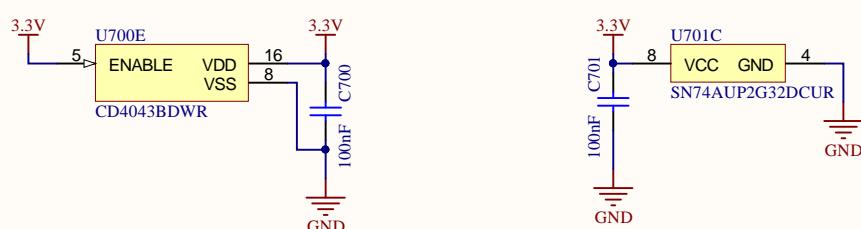


B



C

This circuit stretches the (potentially) short pulses on the LowRangeInvalid signals, such that the ADC can actually detect them. In order to guarantee that, the periods between the non-overlapping reset periods for the two latches must be longer than the sampling period.



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Drawing title:

Range Valid Signal Stretching

Drawing number: 8	Rev. 1	Format: A4 Q	Laboratory: TIK	Project: range_valid_stretching.SchDoc
Date: 27.09.2016 09:01:14		Drawn by: Stefan Lippuner		
File: C:\Users\user\Documents\RocketLogger\code\pcb\Cape\range_valid_stretching.SchDoc				Page 8 of 8

