

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project:
Top

Drawing number:	1	Rev:	1	Format:	Laboratory: TIK	Sheet:	top.SchDoc
Date:	03.11.2016	14:13:00		A3	Drawn by:	Stefan Lippuner	
File: C:\Users\user\Documents\Rocketlogger\hardware\pcb\Cape\top.SchDoc							Page 1 of 8

1

2

3

4

A

B

C

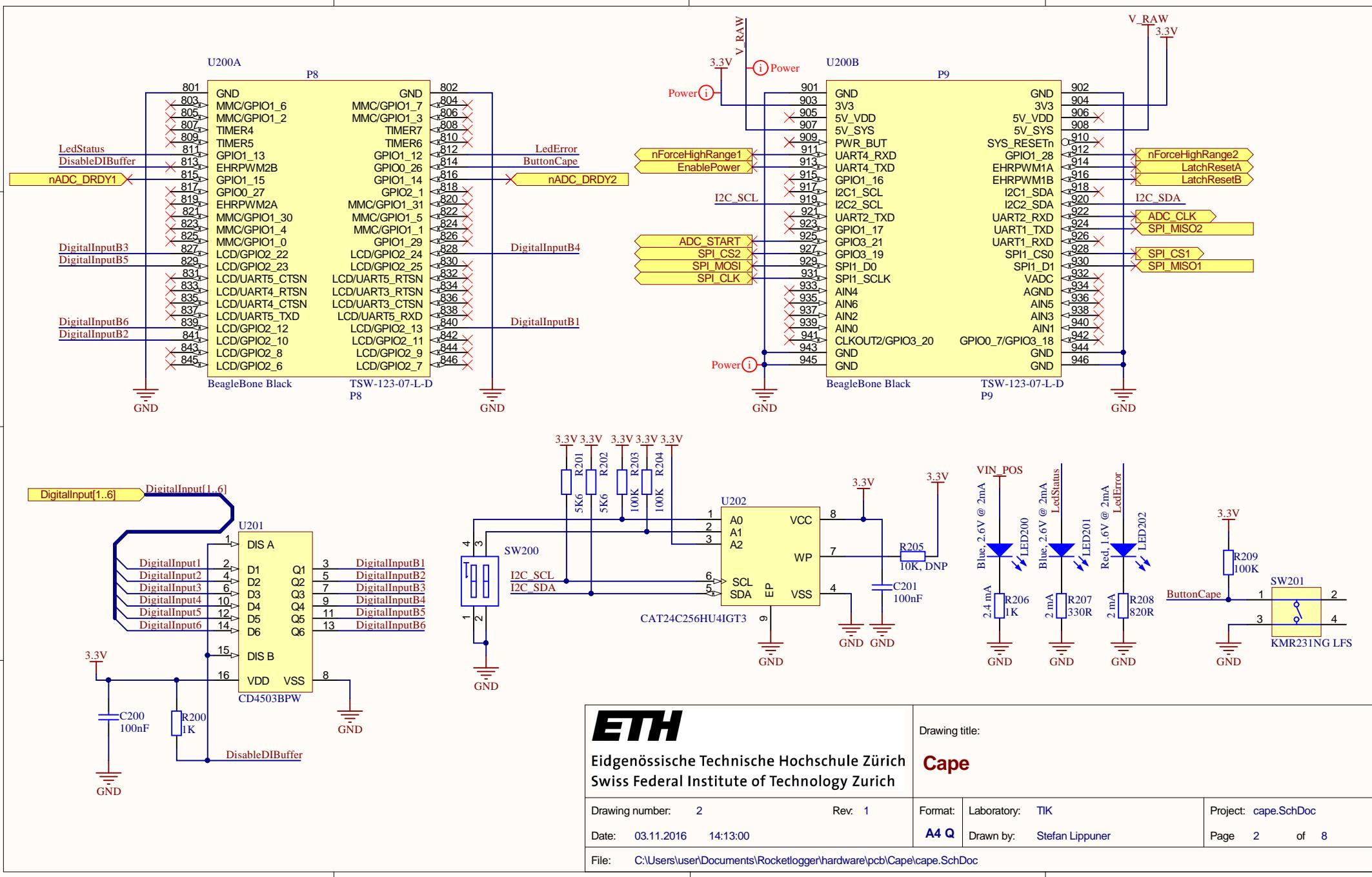
D

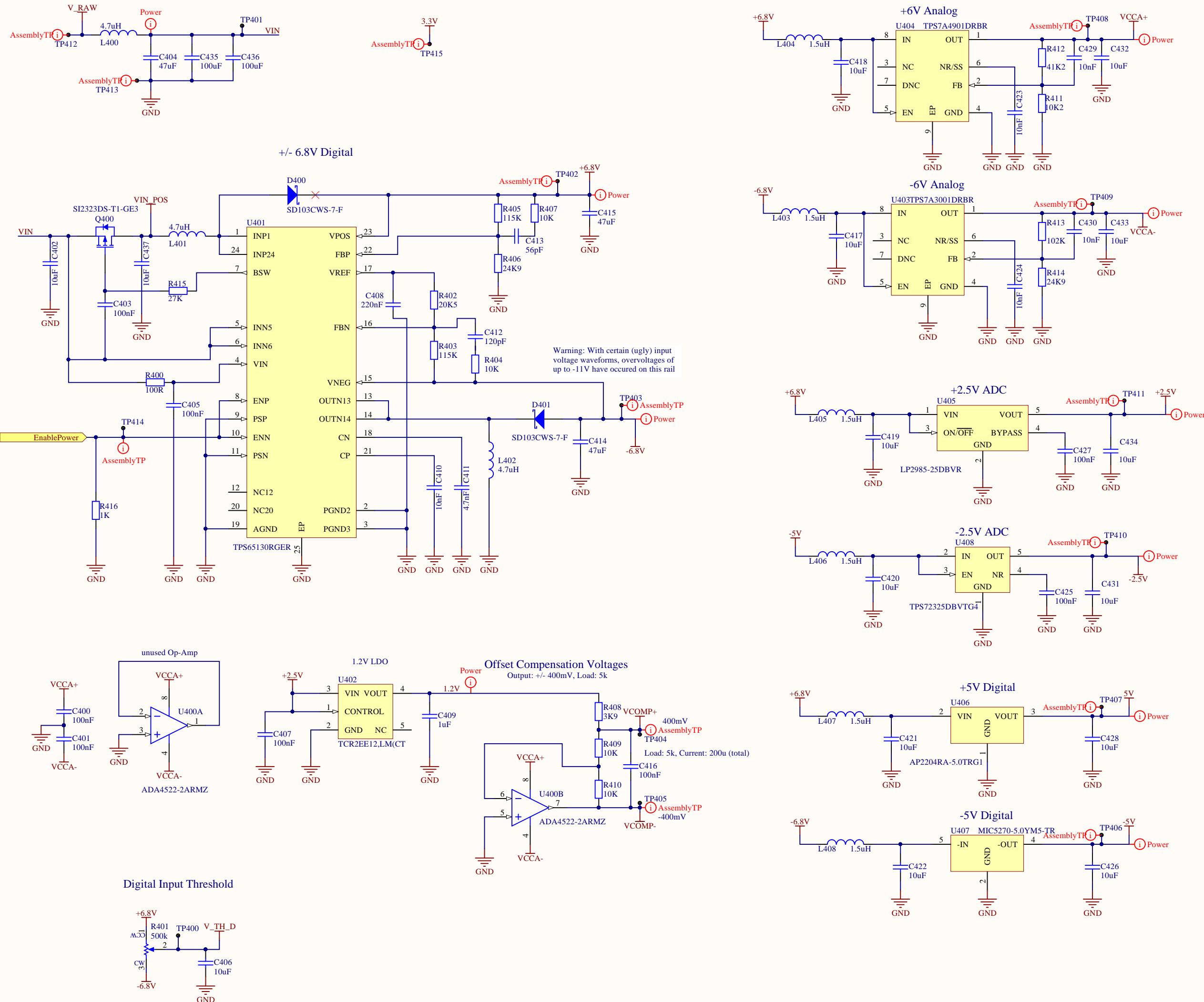
A

B

C

D

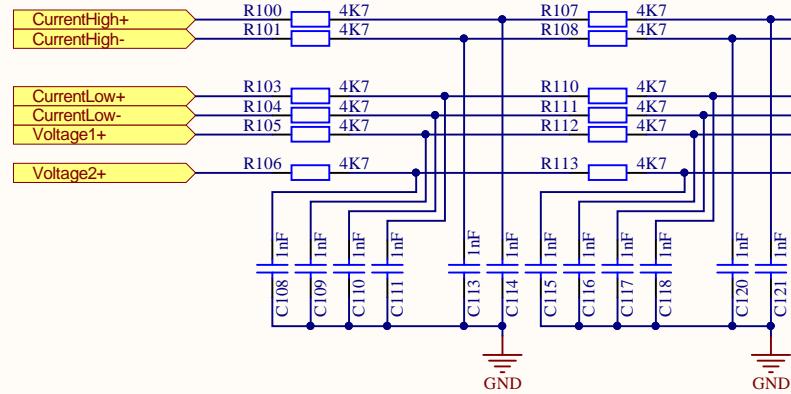




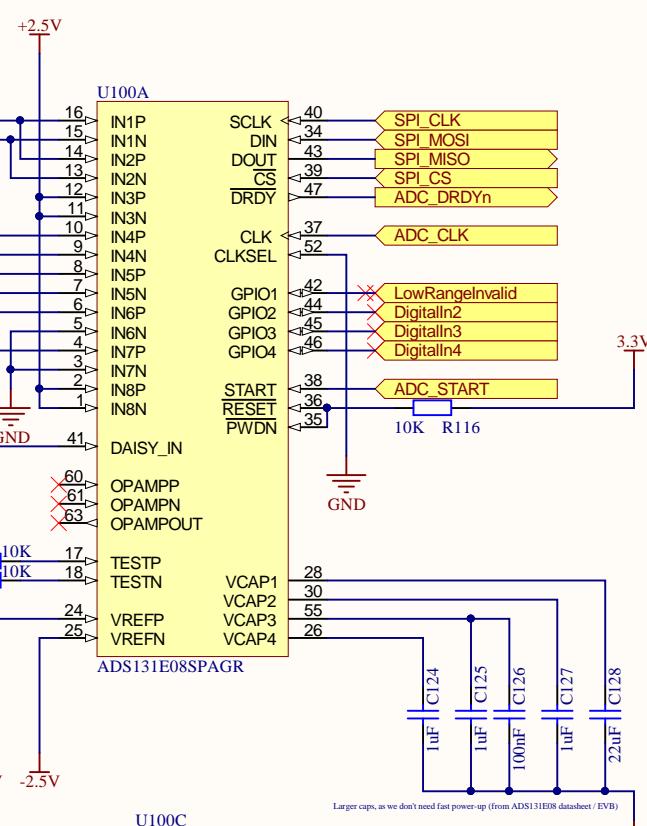
A

Resistors limit input current to 638uA

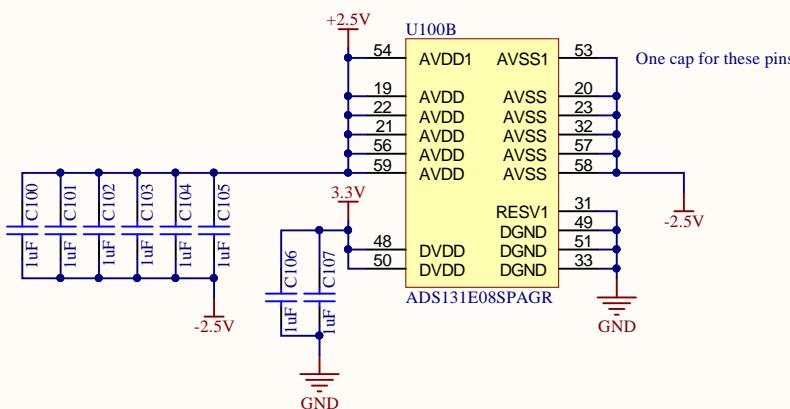
2nd order filter, -3dB @ 33.9kHz



B



C



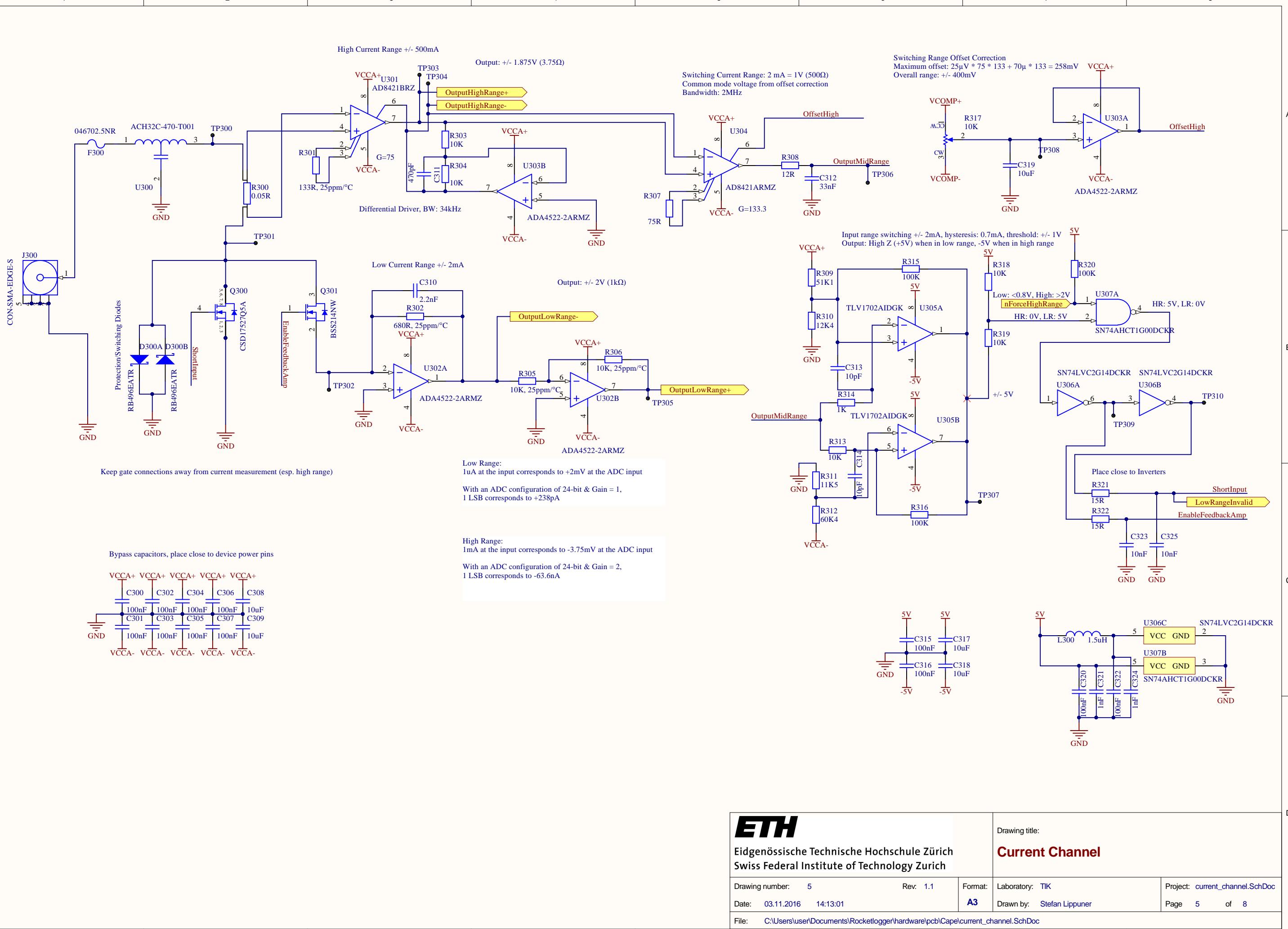
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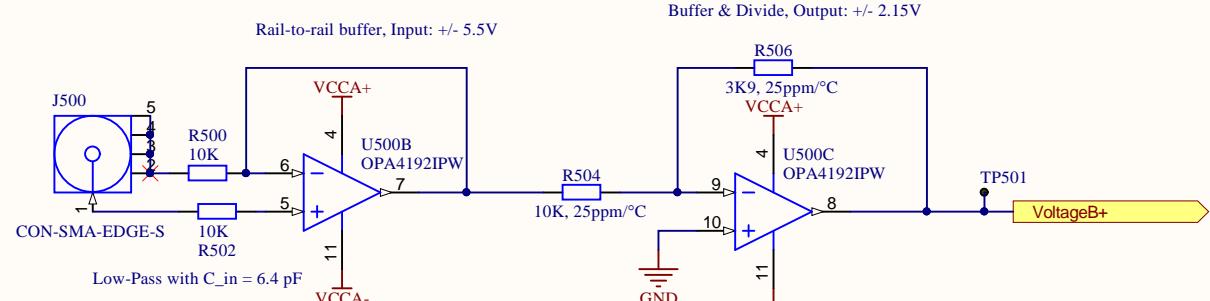
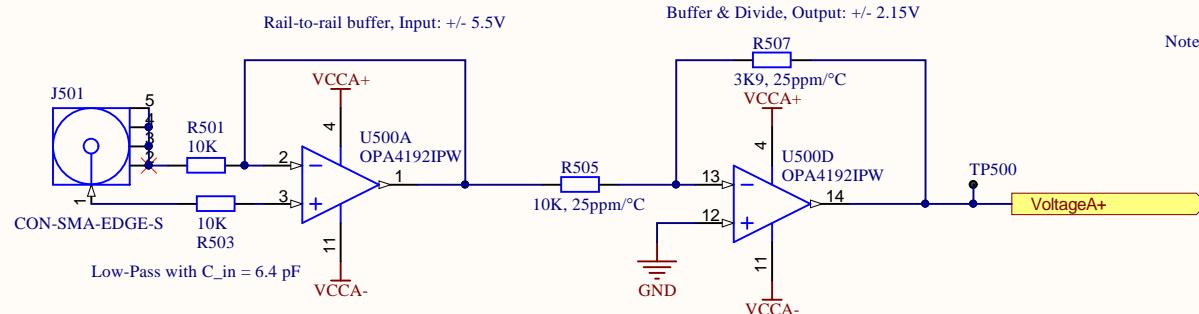
ETH
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Drawing title:

ADC

Drawing number: 4	Rev. 1	Format: A4 Q	Laboratory: TIK	Project: adc.SchDoc
Date: 03.11.2016 14:13:01		Drawn by: Stefan Lippuner		Page 4 of 8
File: C:\Users\user\Documents\Rocketlogger\hardware\pcb\Cape\adc.SchDoc				





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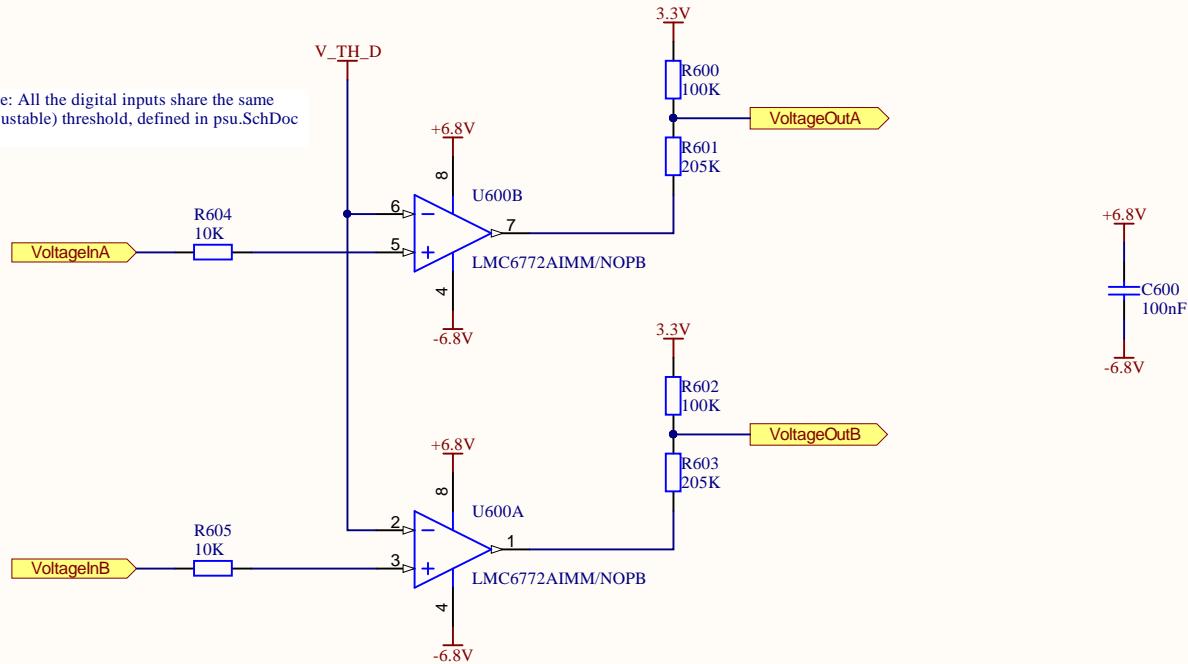
Drawing title:

Voltage Channel

Drawing number:	6	Rev.	1	Format:	Laboratory:	TIK	Project:	voltage_channel.SchDoc
Date:	03.11.2016	14:13:01		A4 Q	Drawn by:	Stefan Lippuner	Page	6 of 8
File:	C:\Users\user\Documents\Rocketlogger\hardware\pcb\Cape\voltage_channel.SchDoc							

A

Note: All the digital inputs share the same (adjustable) threshold, defined in psu.SchDoc



B

A

B

C

C

D

D



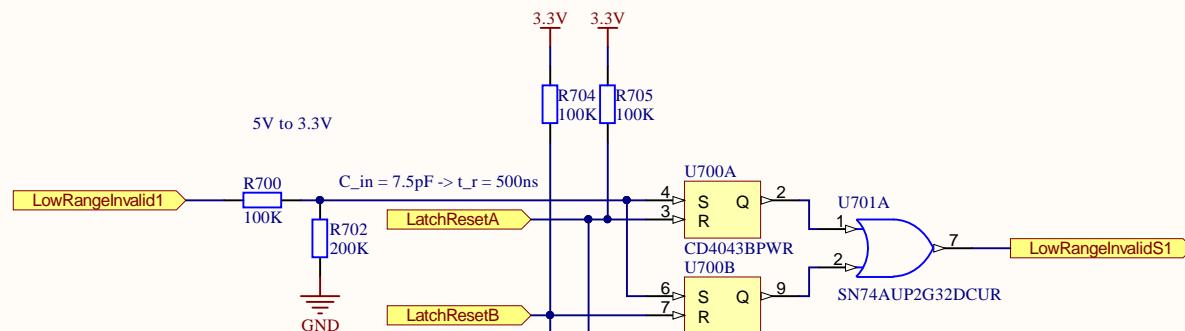
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Drawing title:

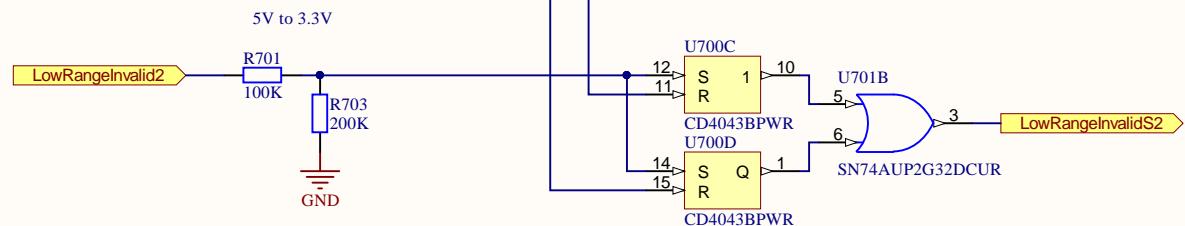
Digital Voltage Channel

Drawing number: 7	Rev. 1	Format: A4 Q	Laboratory: TIK	Project: digital_voltage_channel.SchDoc
Date: 03.11.2016 14:13:01		Drawn by: Stefan Lippuner		Page 7 of 8
File: C:\Users\user\Documents\Rocketlogger\hardware\pcb\Cape\digital_voltage_channel.SchDoc				

A

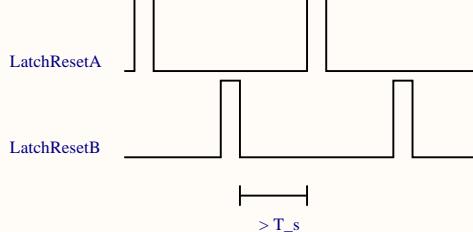
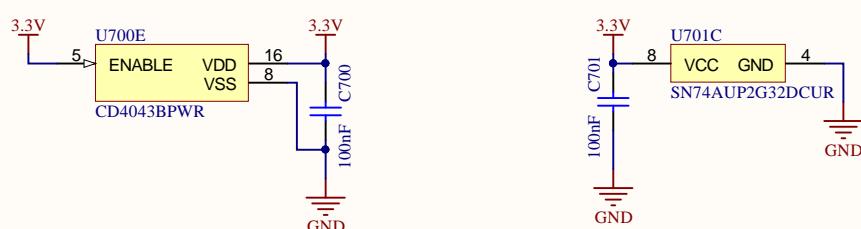


B



C

This circuit stretches the (potentially) short pulses on the LowRangelInvalid signals, such that the ADC can actually detect them. In order to guarantee that, the periods between the non-overlapping reset periods for the two latches must be longer than the sampling period.



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Drawing title:

Range Valid Signal Stretching

Drawing number: 8	Rev. 1	Format: A4 Q	Laboratory: TIK	Project: range_valid_stretching.SchDoc
Date: 03.11.2016 14:13:01		Drawn by: Stefan Lippuner		
File: C:\Users\user\Documents\Rocketlogger\hardware\pcb\Cape\range_valid_stretching.SchDoc				

