

1

2

3

4

A

B

C

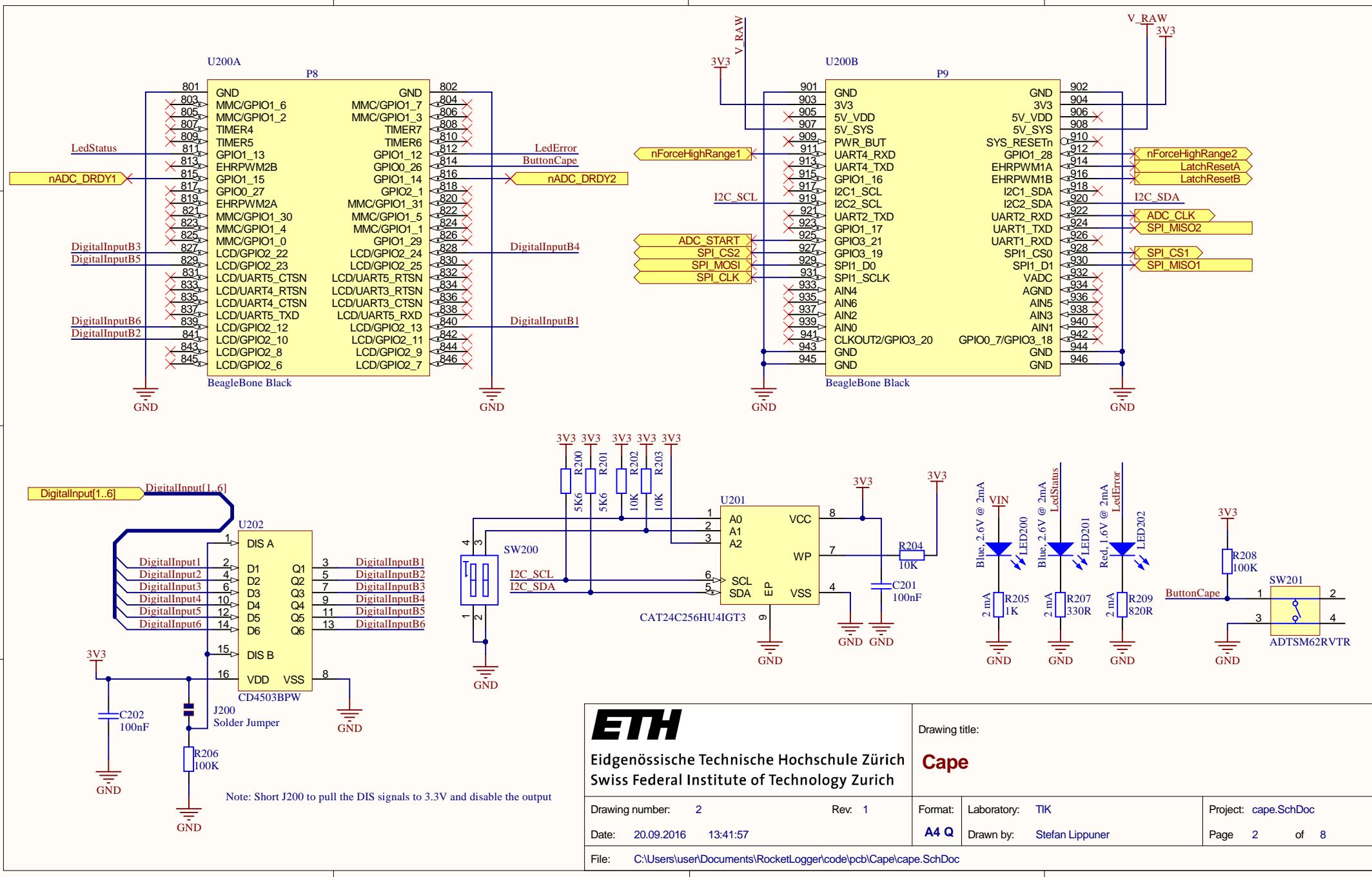
D

A

B

C

D



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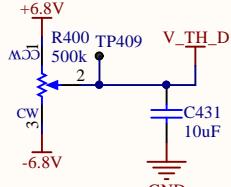
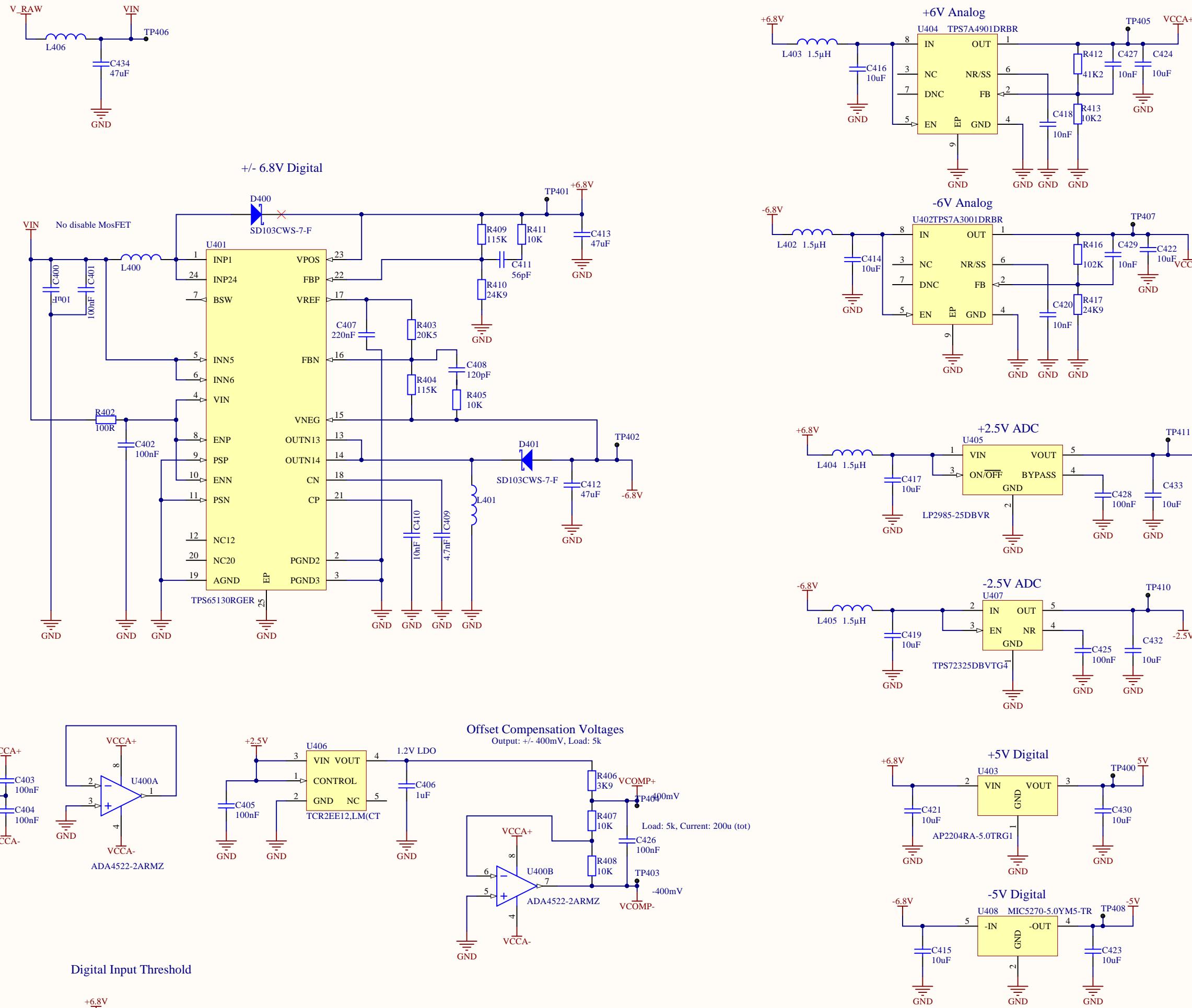
Drawing number: 2 Rev. 1 Format: A4 Q Laboratory: TIK Project: cape.SchDoc

Date: 20.09.2016 13:41:57 Drawn by: Stefan Lippuner Page 2 of 8

File: C:\Users\user\Documents\RocketLogger\code\pcb\Cape\cape.SchDoc

Drawing title:

Cape

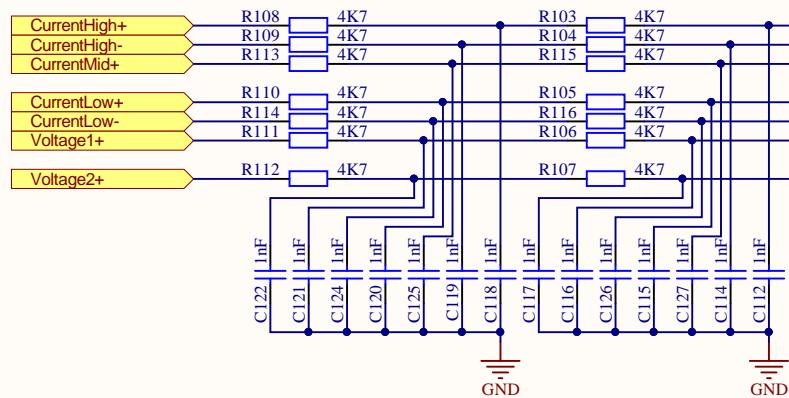


Drawing number: 3 Rev: 1 Format: Laboratory: TIK Sheet: psu.SchDoc  
Date: 20.09.2016 13:41:57 A2 Drawn by: Stefan Lippuner Page 3 of 8  
File: C:\Users\user\Documents\RocketLogger\code\pcb\Capelsu.SchDoc

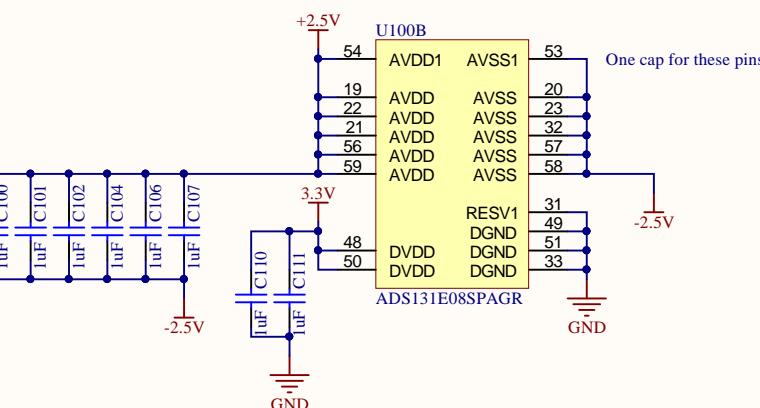
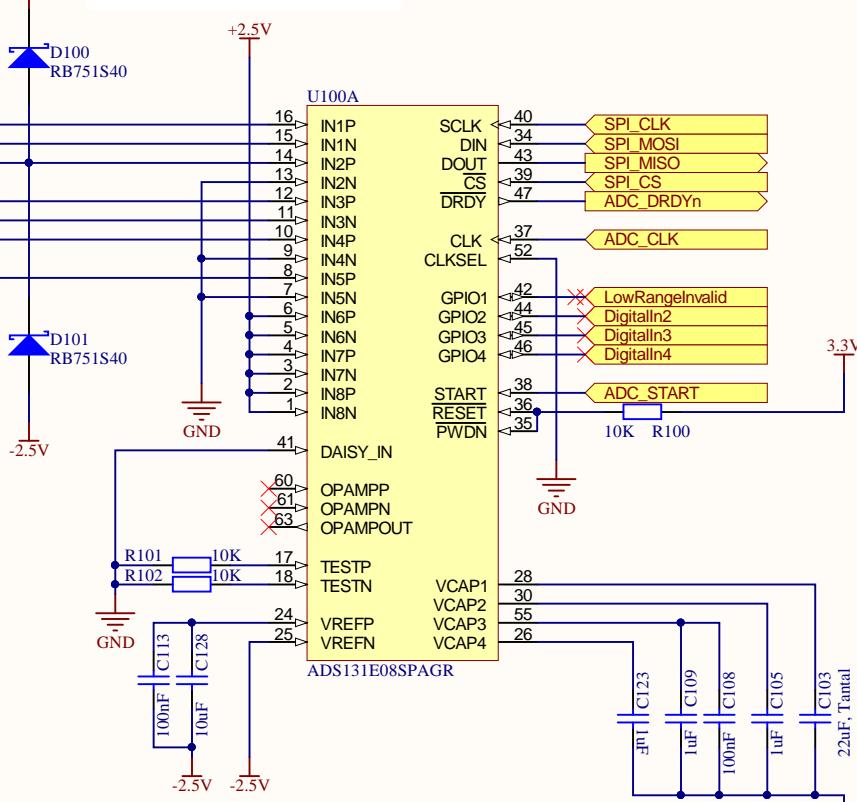
A

Resistors limit input current to 638uA

2nd order filter, -3dB @ 33.9kHz



The medium range voltages can exceed the ADC supply during normal operation, we don't want the limiting currents to flow into the ADC

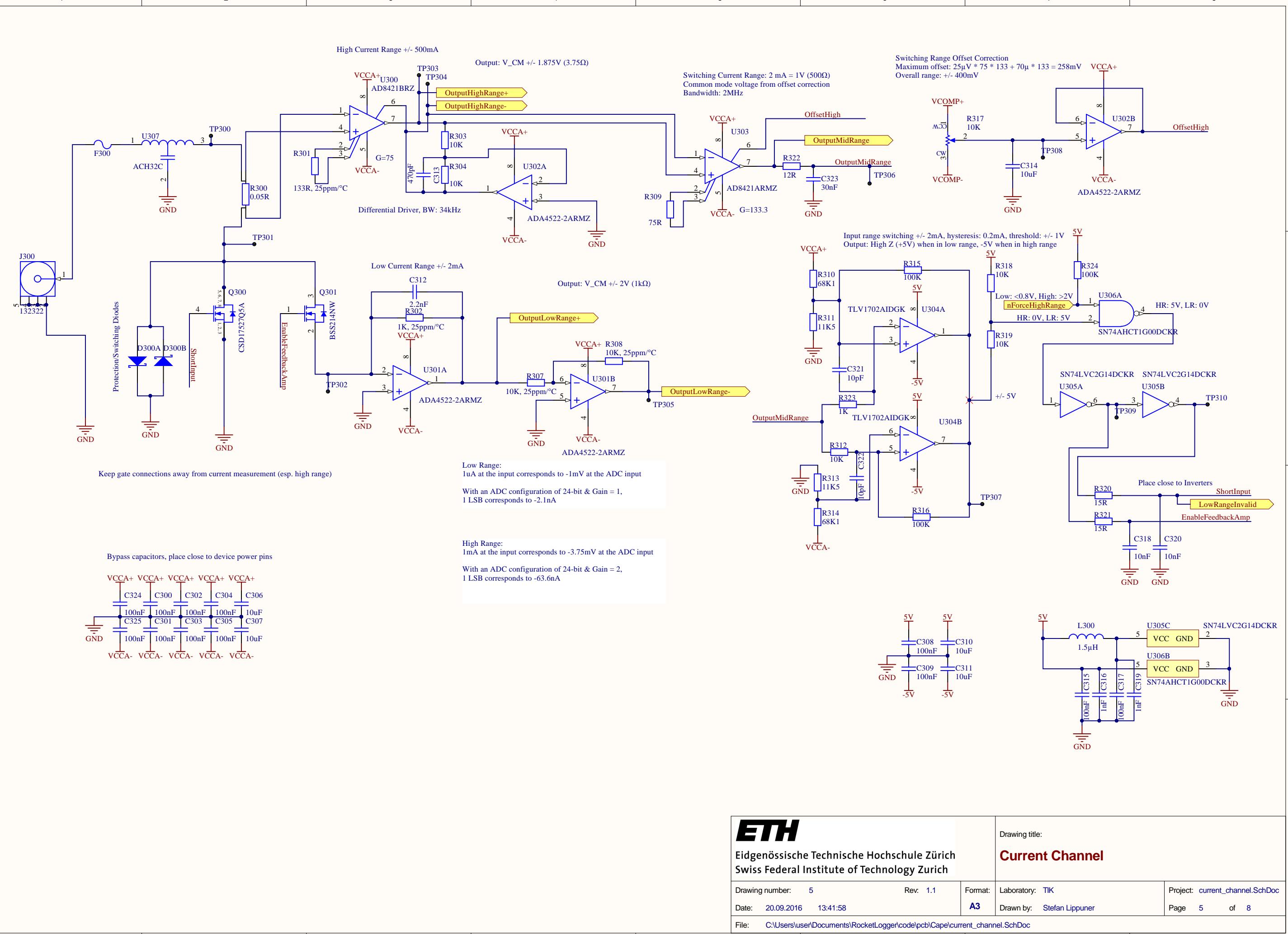


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Drawing title:

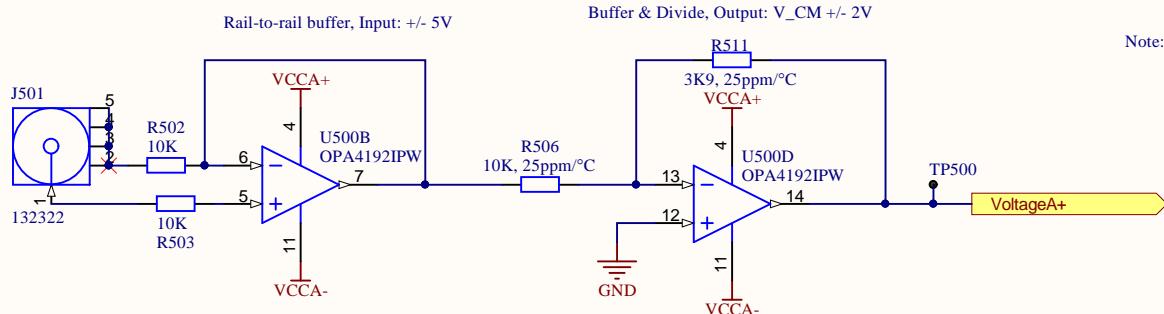
ADC

Drawing number:	4	Rev.	1	Format:	Laboratory:	TIK	Project:	adc.SchDoc
Date:	20.09.2016	13:41:58		A4 Q	Drawn by:	Stefan Lippuner		
File:	C:\Users\user\Documents\RocketLogger\code\pcb\Cape\adc.SchDoc						Page	4 of 8



A

A

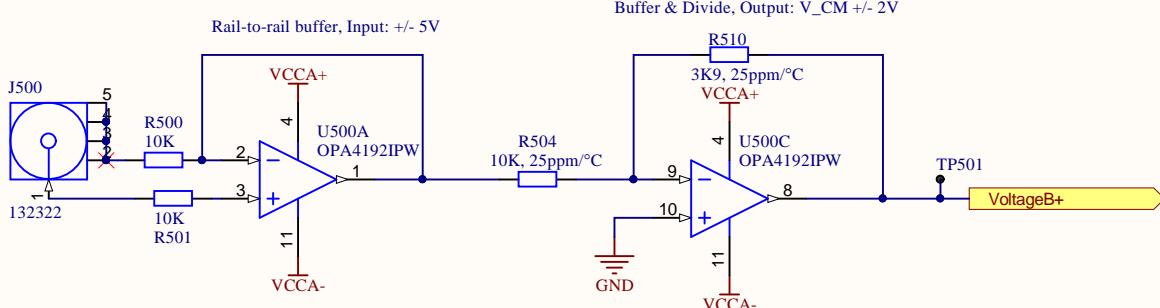


1V at the input corresponds to -390mV at the ADC input

With an ADC configuration of 24-bit & Gain = 1,  
1 LSB corresponds to -1.22uV

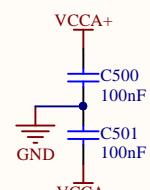
B

B



C

C



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Drawing title:

**Voltage Channel**

Drawing number:	6	Rev.	1	Format:	Laboratory:	TIK	Project:	voltage_channel.SchDoc
Date:	20.09.2016	13:41:58		A4 Q	Drawn by:	Stefan Lippuner		
File:	C:\Users\user\Documents\RocketLogger\code\pcb\Cape\voltage_channel.SchDoc							

A

B

C

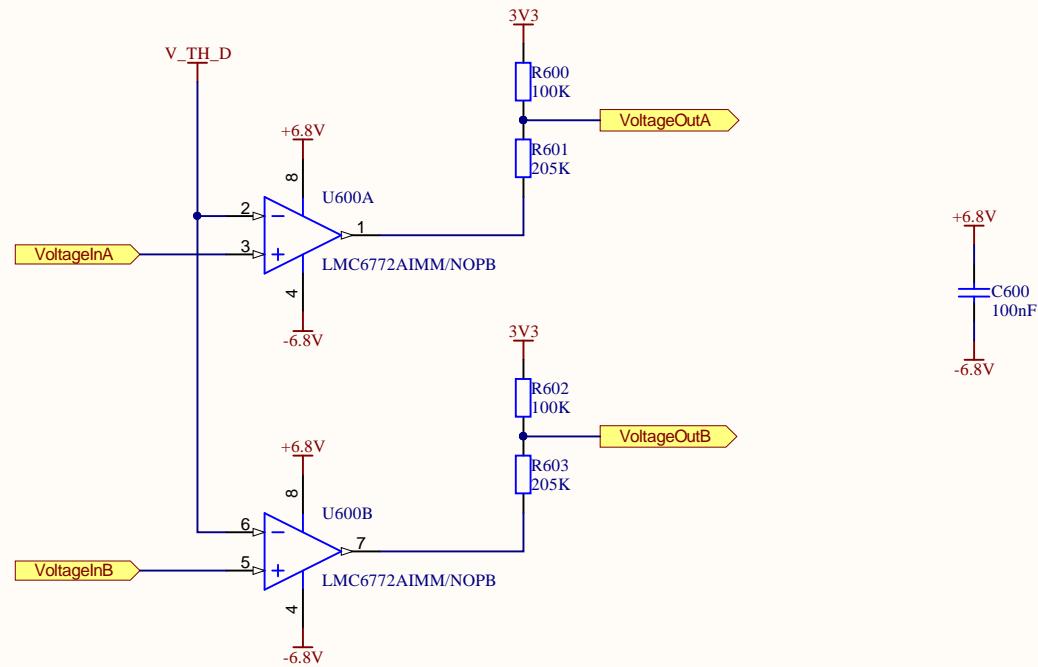
D

A

B

C

D



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Drawing title:

## Digital Voltage Channel

Drawing number: 7 Rev. 1

Date: 20.09.2016 13:41:58

File: C:\Users\user\Documents\RocketLogger\code\pcb\Cape\digital\_voltage\_channel.SchDoc

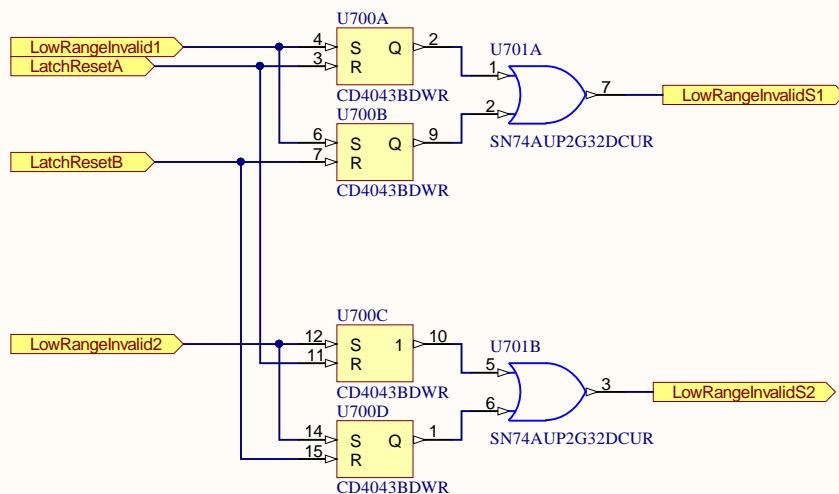
Format: TIK

Laboratory: A4 Q Drawn by: Stefan Lippuner

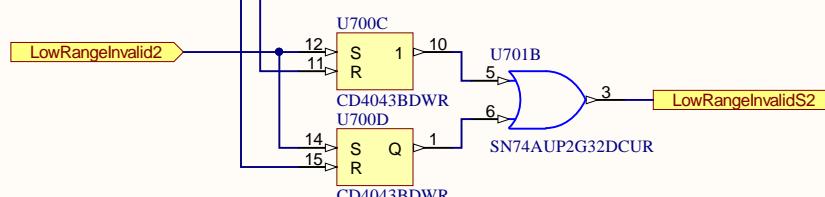
Project: digital\_voltage\_channel.SchDoc

Page 7 of 8

A

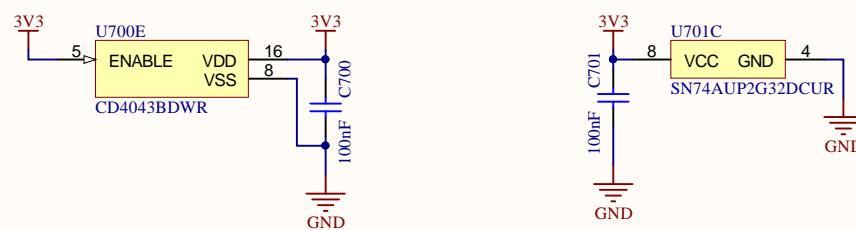


B



C

This circuit stretches the (potentially) short pulses on the LowRangeInvalid signals, such that the ADC can actually detect them. In order to guarantee that, the periods between the non-overlapping reset periods for the two latches must be longer than the sampling period.



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Drawing title:

## Range Valid Signal Stretching

Drawing number:

Rev.

Date: 20.09.2016 13:41:58

Format: Laboratory:

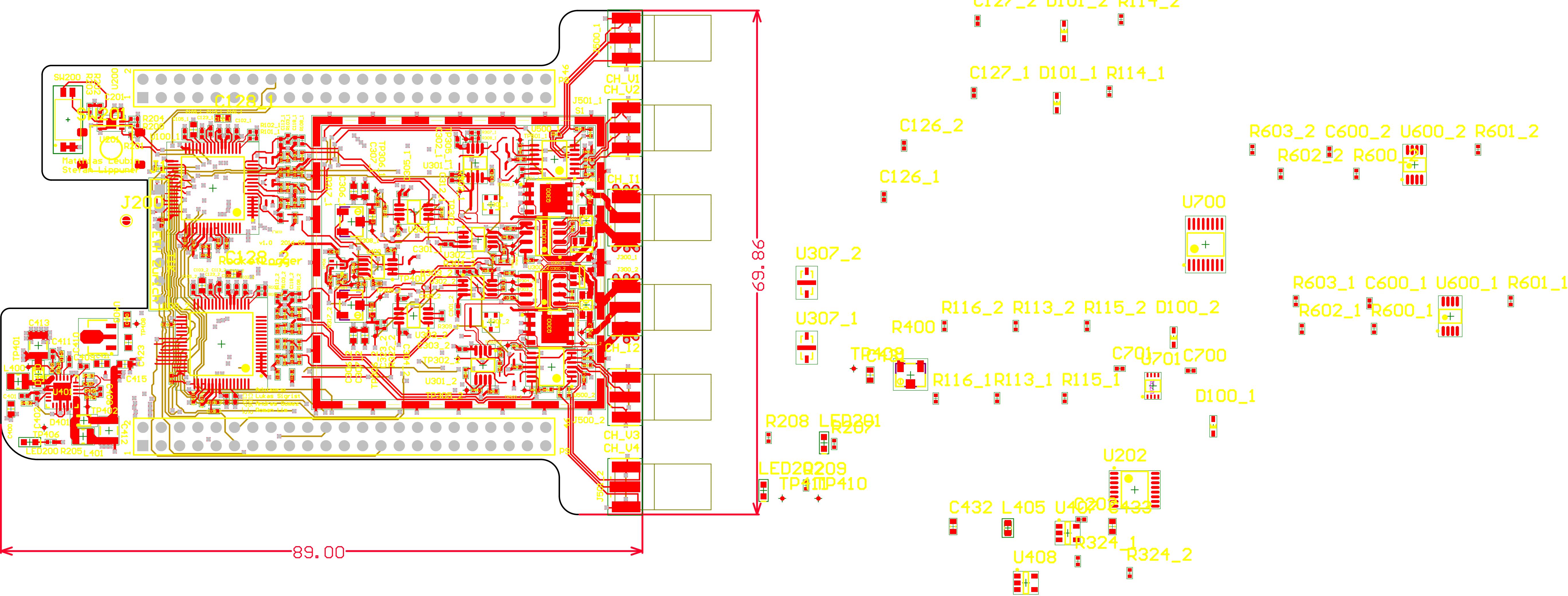
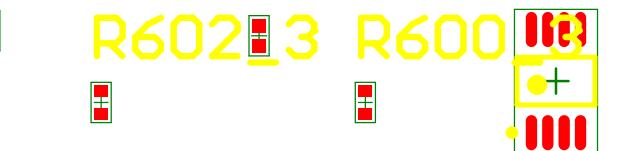
A4 Q TIK  
Drawn by: Stefan Lippuner

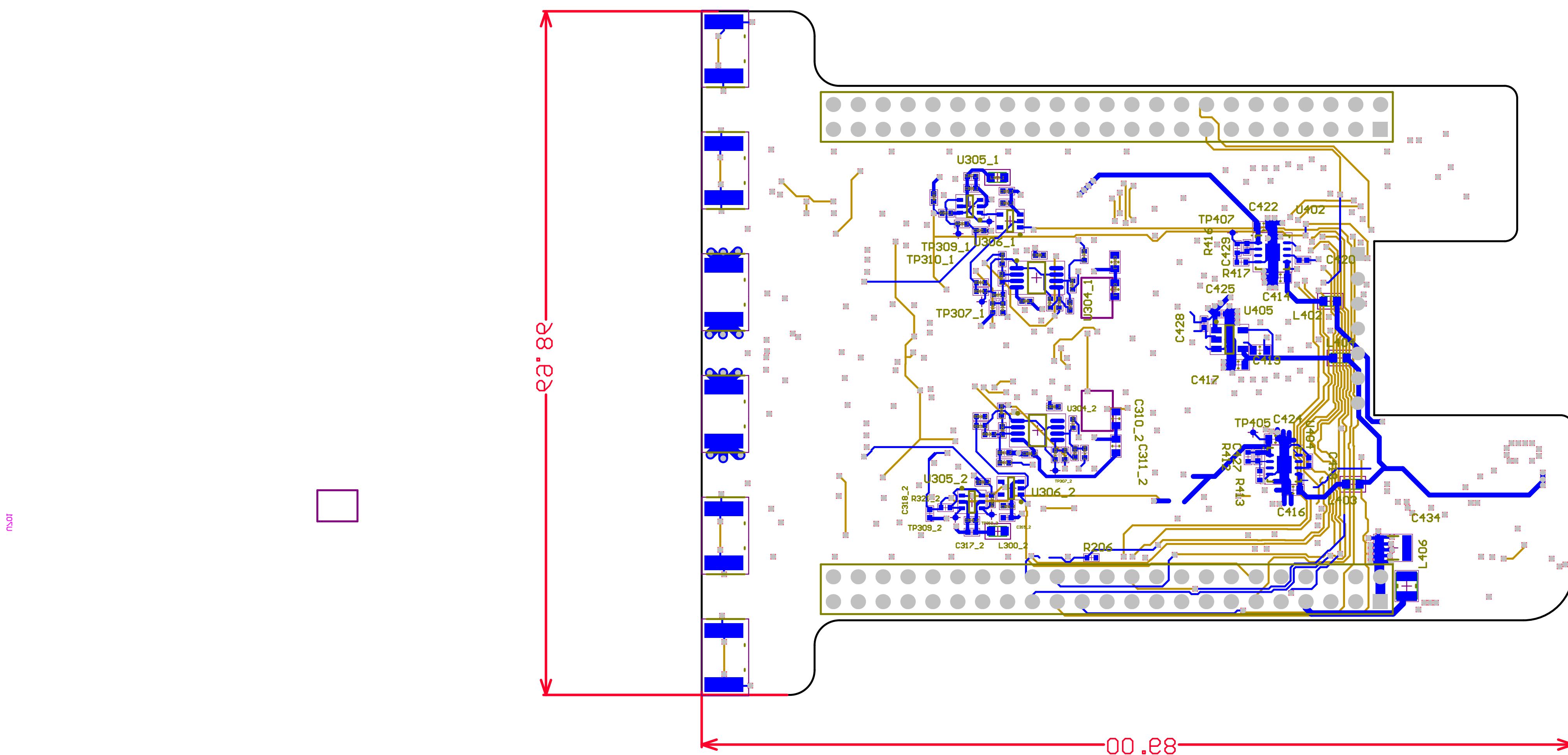
Project: range\_valid\_stretching.SchDoc

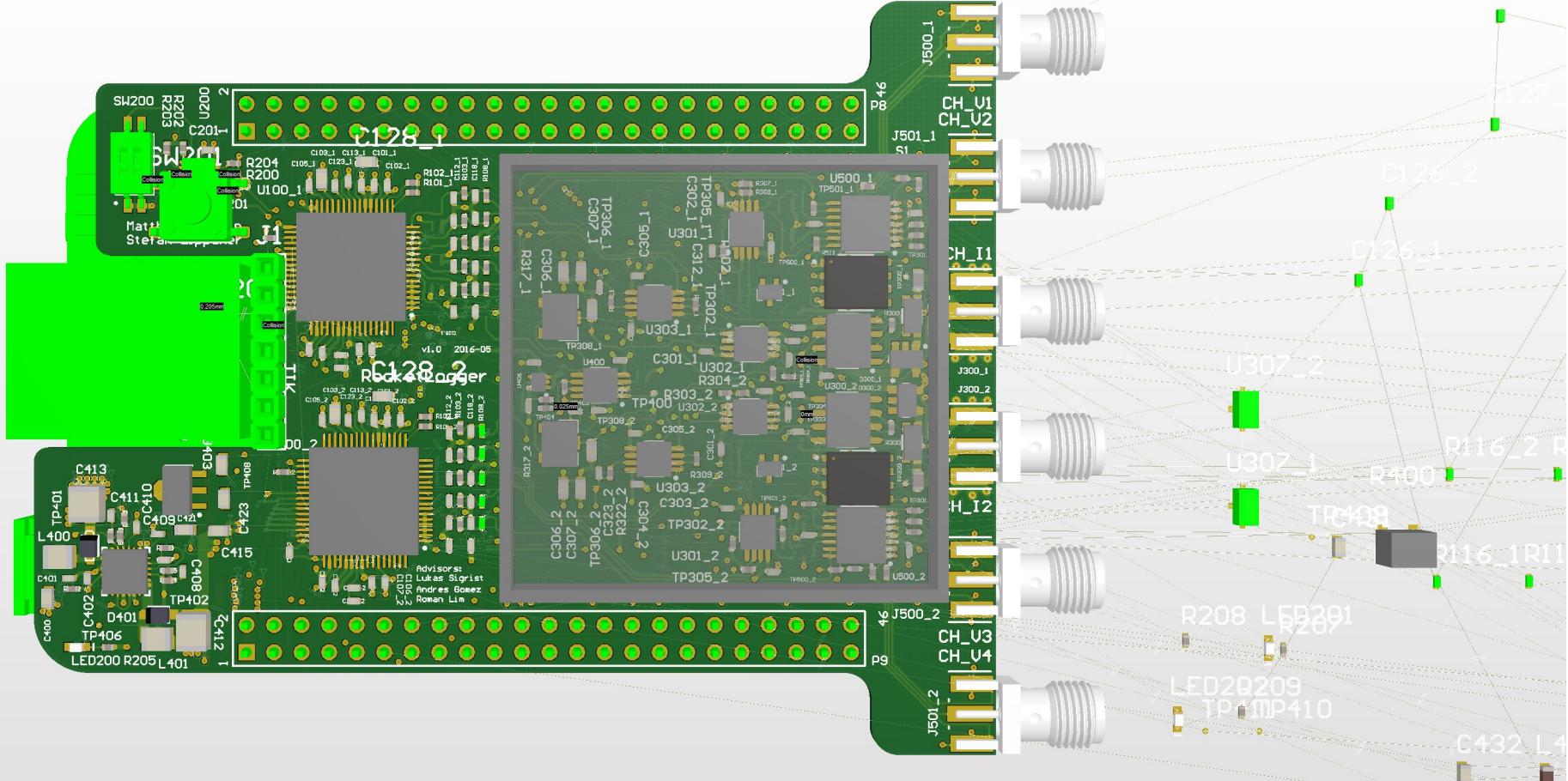
Page 8 of 8

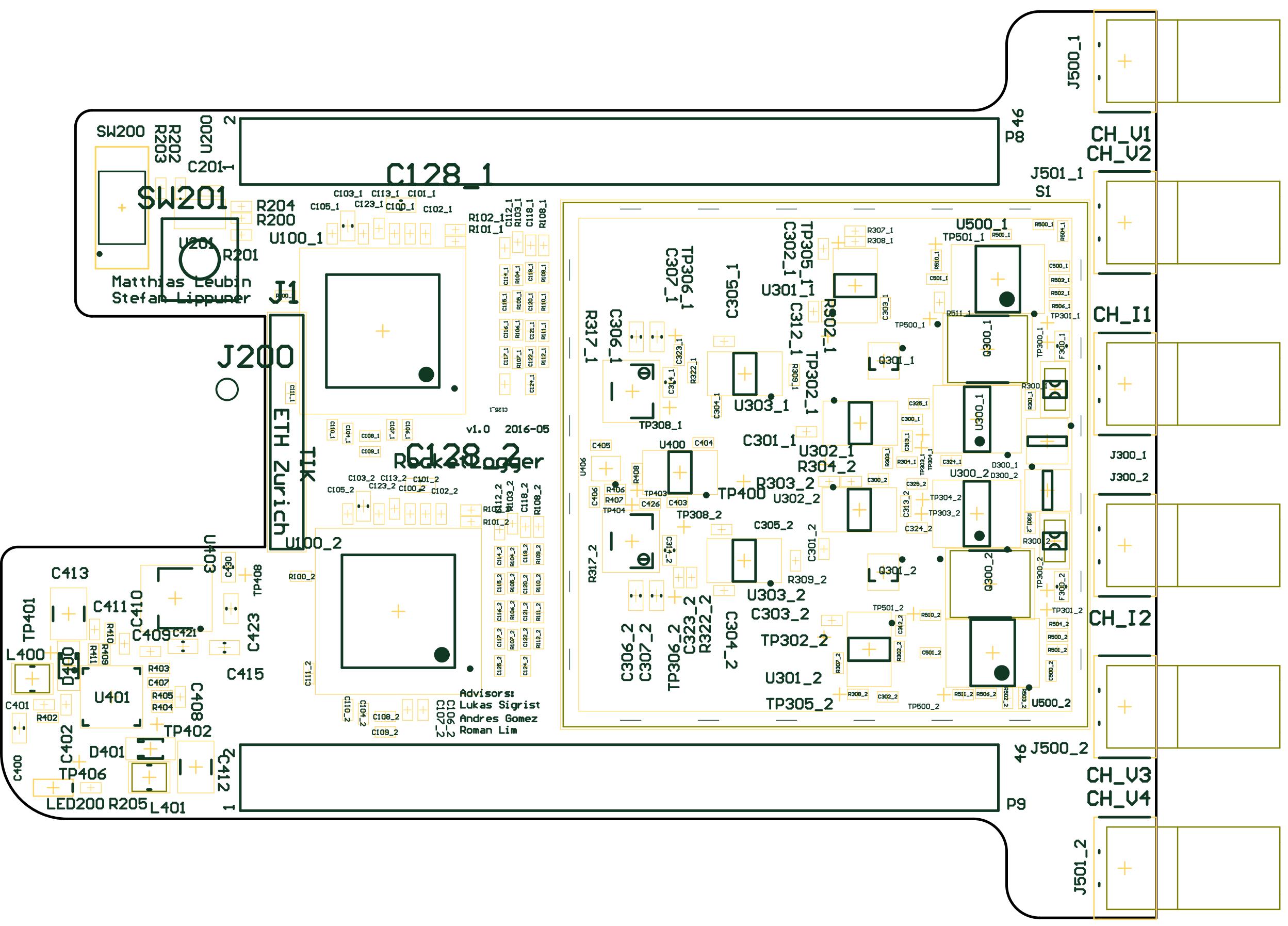
File: C:\Users\user\Documents\RocketLogger\code\pcb\Cape\range\_valid\_stretching.SchDoc

R603\_3 C600\_3 U600\_3 R601\_3  
R602\_3 R600









C127\_2 D101\_2 R114\_2

C127\_1 D101\_1 R114\_1

C126\_2

C126\_

U307\_2

U307\_1

R116\_2 R113\_2 R115\_2 D100\_2

03 C701 C701 C700

**D10**

U202

C432 L405 U40202433

U408 R324\_2

603\_3 C600\_3 U600\_3 R601\_3

R602\_3 R600\_3

