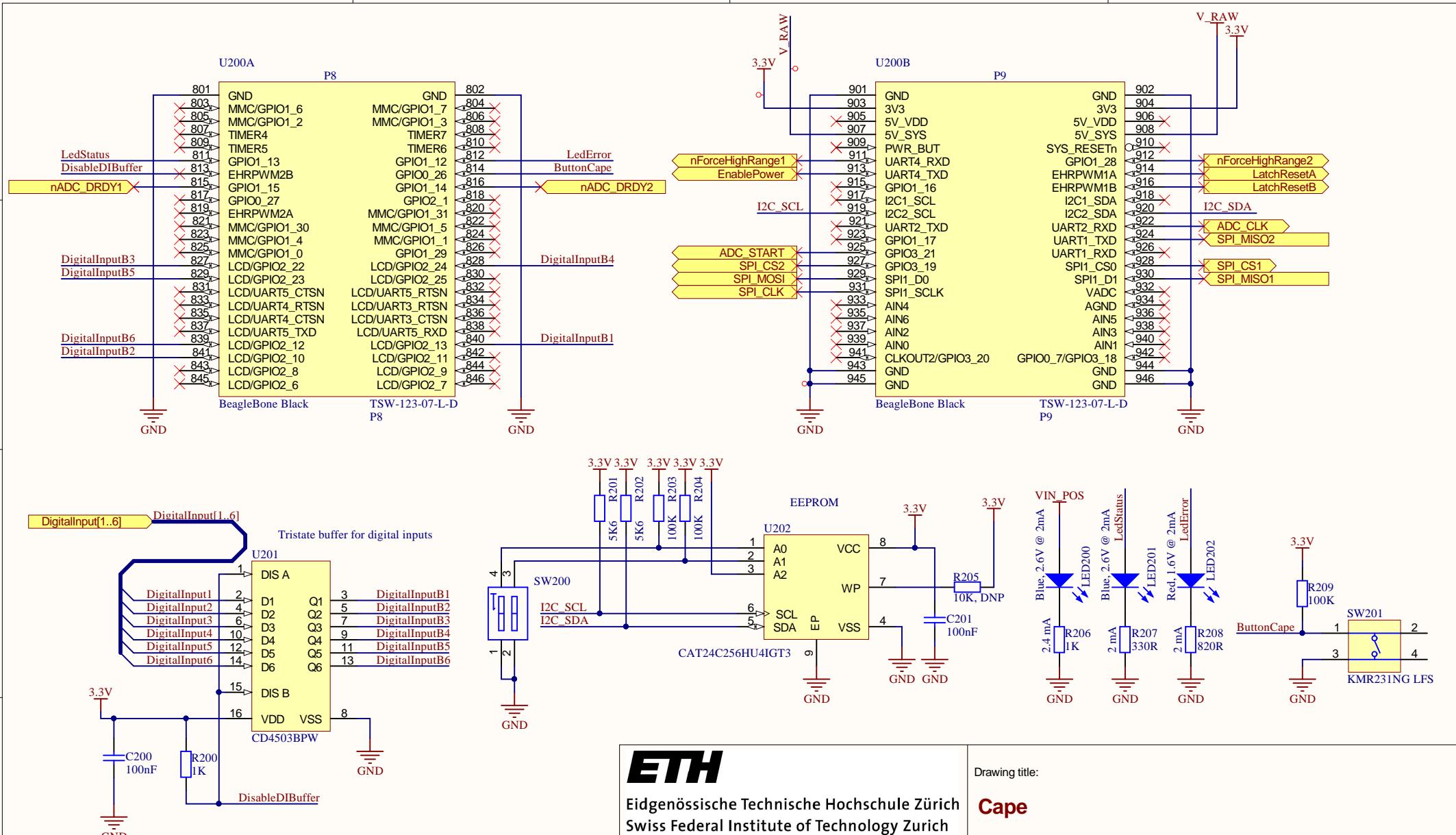


1 2 3 4

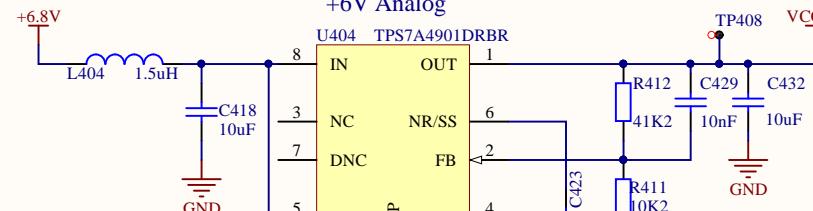
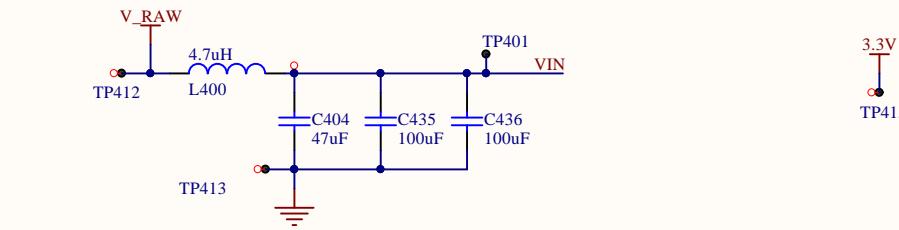
**ETH**Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Drawing title:

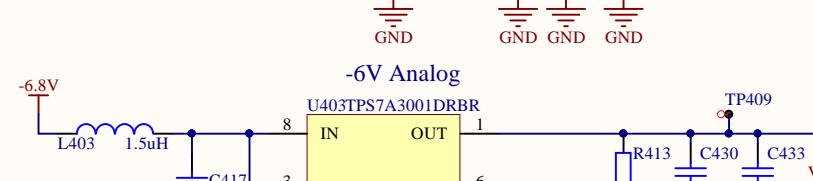
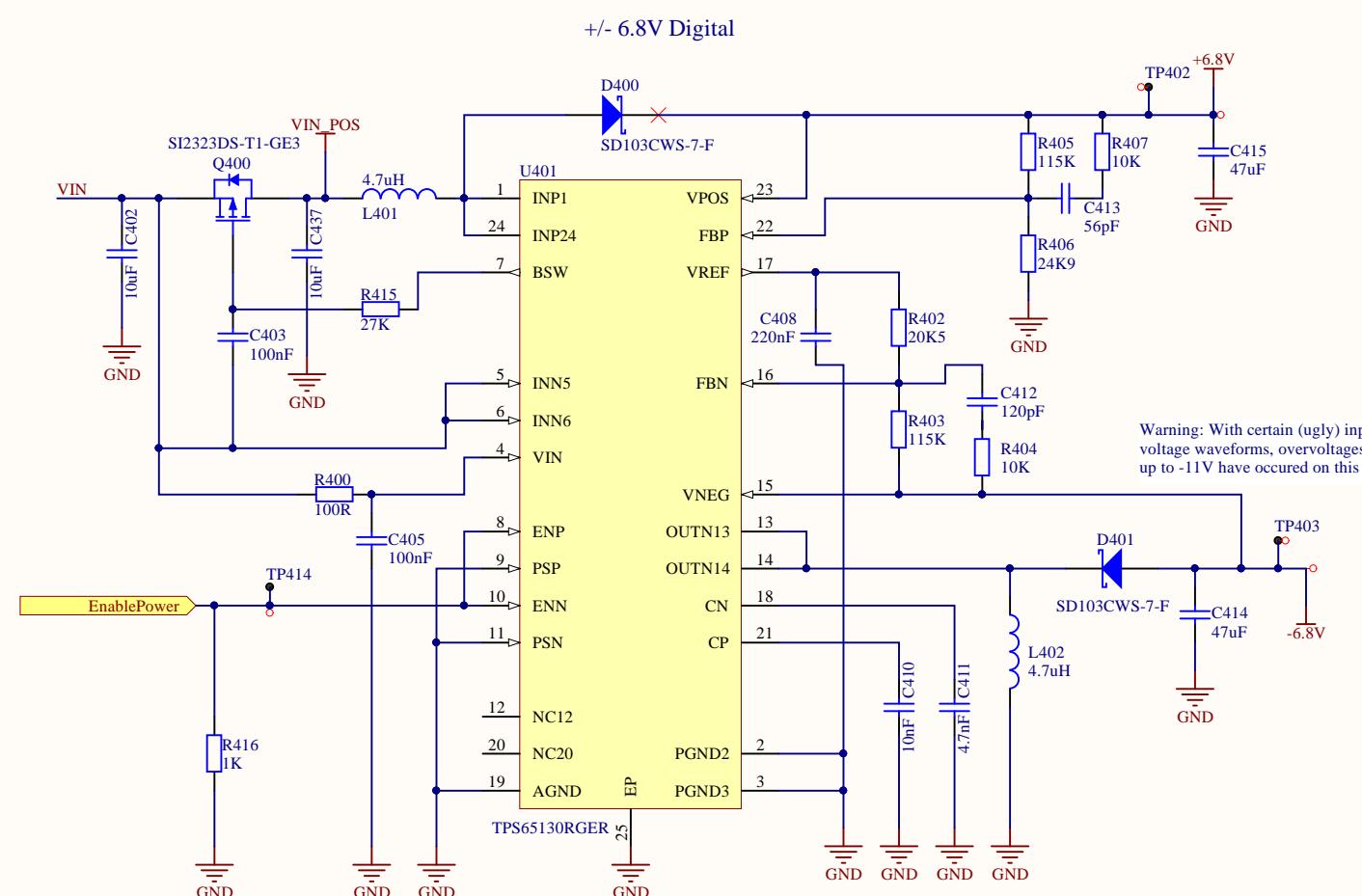
Cape

Drawing number: 2	Rev. 2	Format: A4 Q	Laboratory: TIK	Project: cape.SchDoc
Date: 14.11.2016 14:36:51		Drawn by: Stefan Lippuner		Page 2 of 8
File: C:\Users\user\Documents\Rocketlogger\hardware\pcb\Cape\cape.SchDoc				

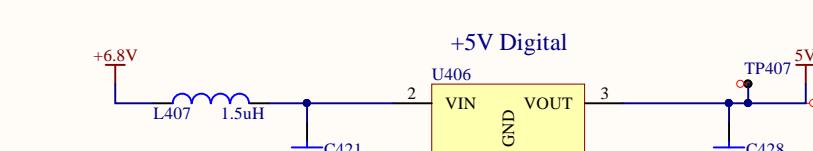
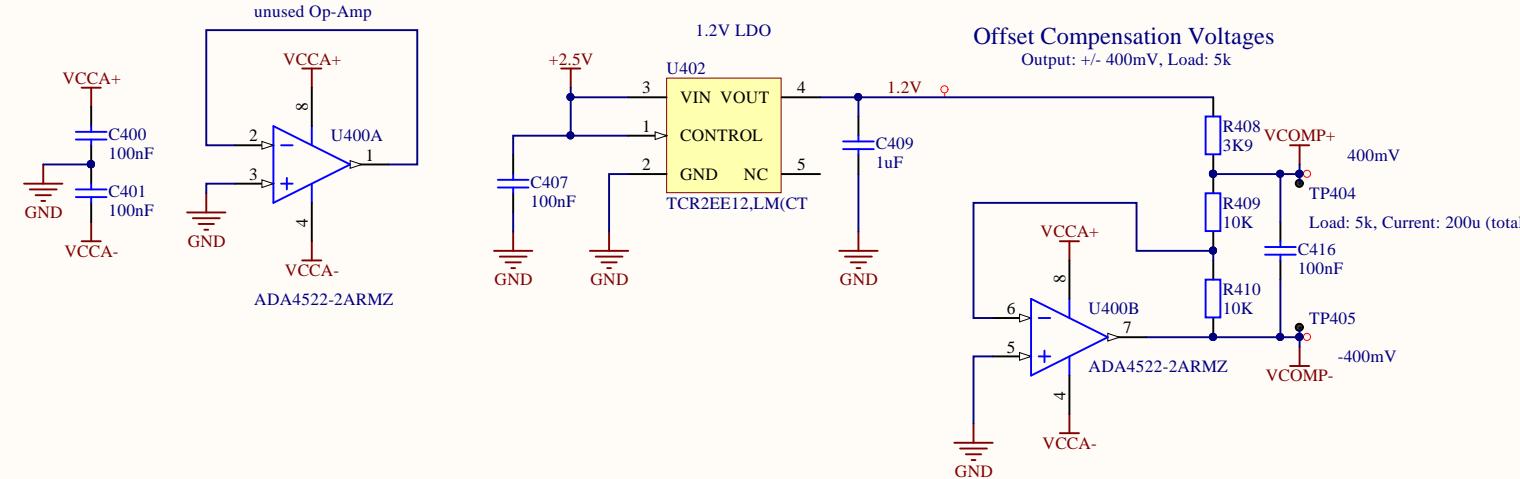
A



B

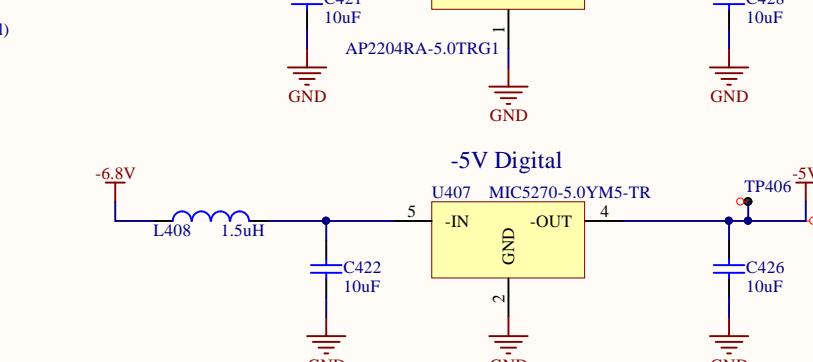
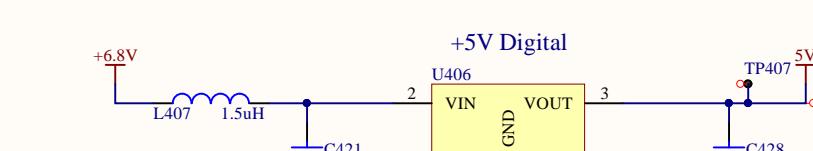
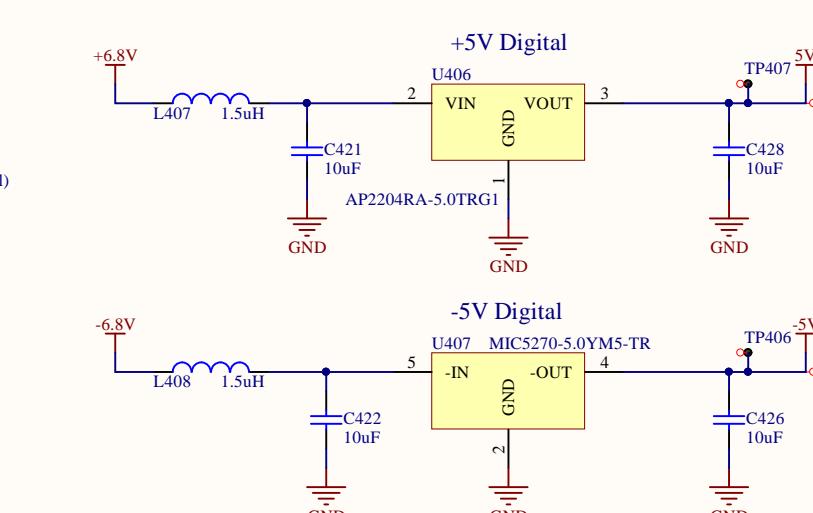
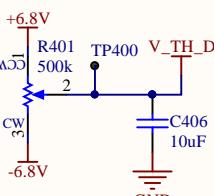


C



D

Digital Input Threshold

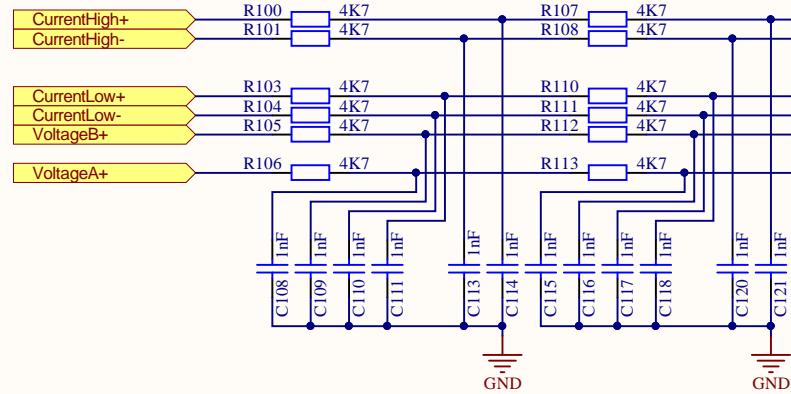
**ETH**Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology ZurichProject:
Power Supplies

Drawing number:	3	Rev.	2	Format:	Laboratory:	TIK
Date:	14.11.2016	14:36:52		A2	Drawn by:	Stefan Lippuner
File:	C:\Users\user\Documents\Rocketlogger\hardware\pcb\psu.SchDoc				Sheet:	psu.SchDoc

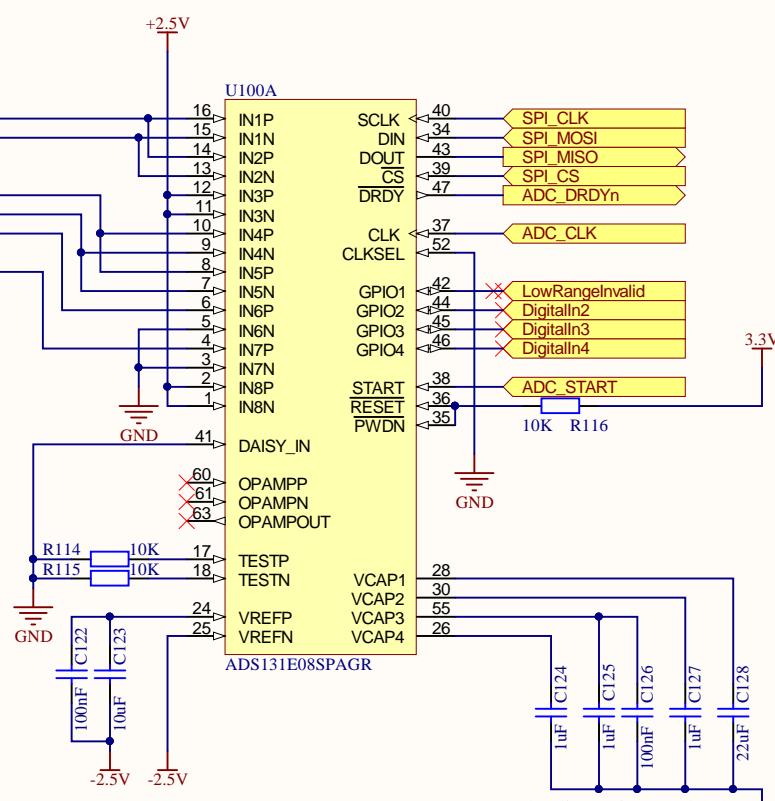
A

Resistors limit input current to 372 uA

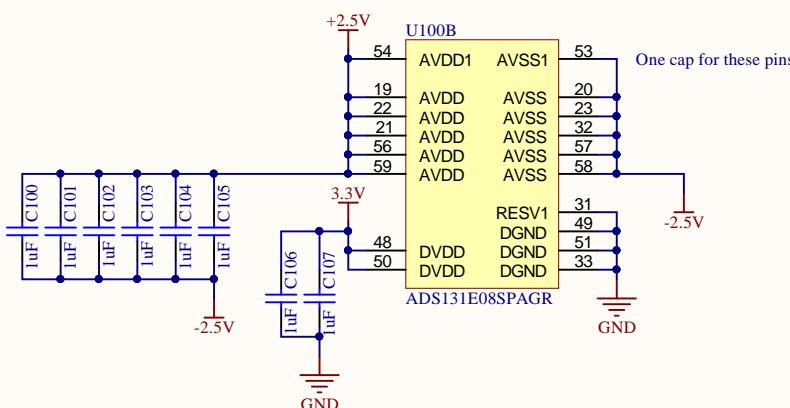
2nd order filter, -3dB @ 21.7kHz



B



C



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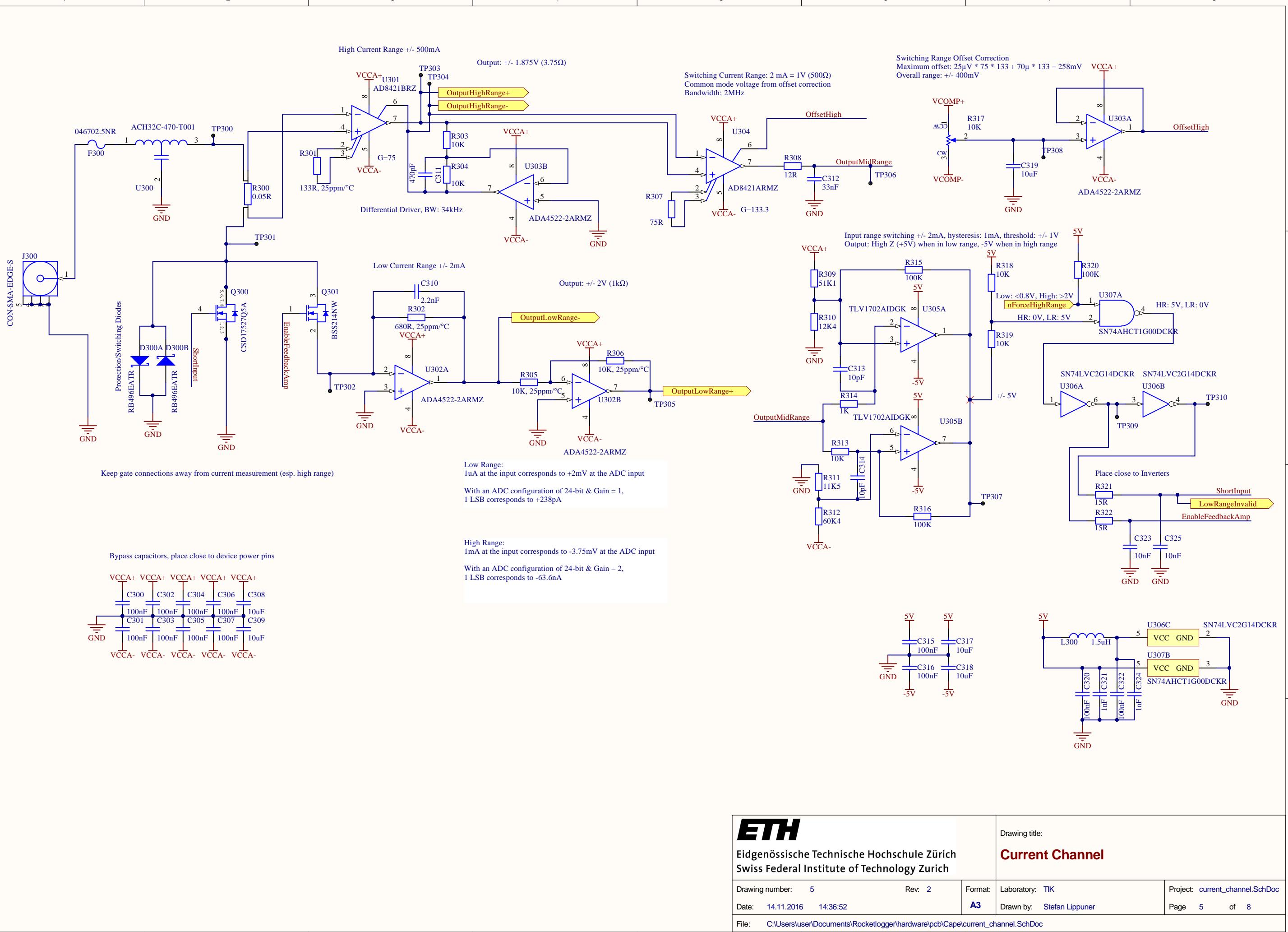
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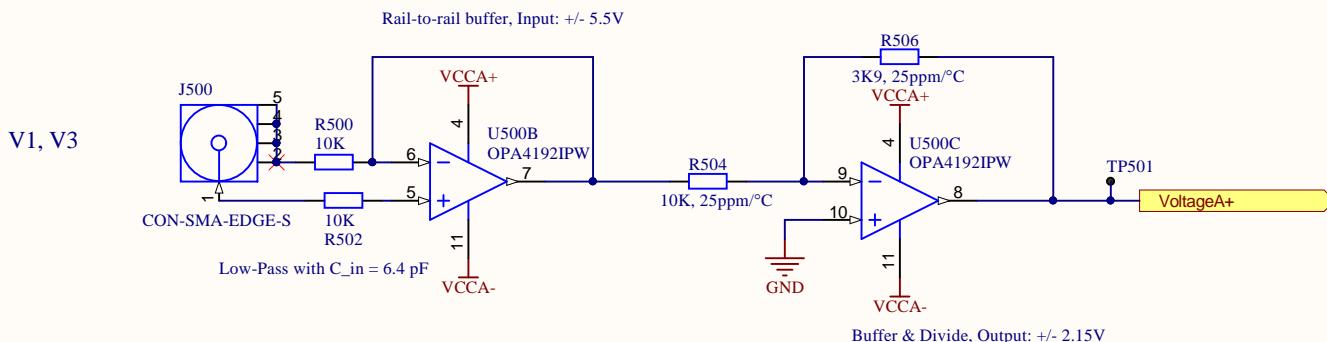
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Drawn by: Stefan Lippuner

Drawing title:

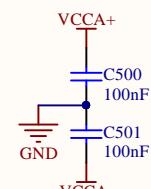
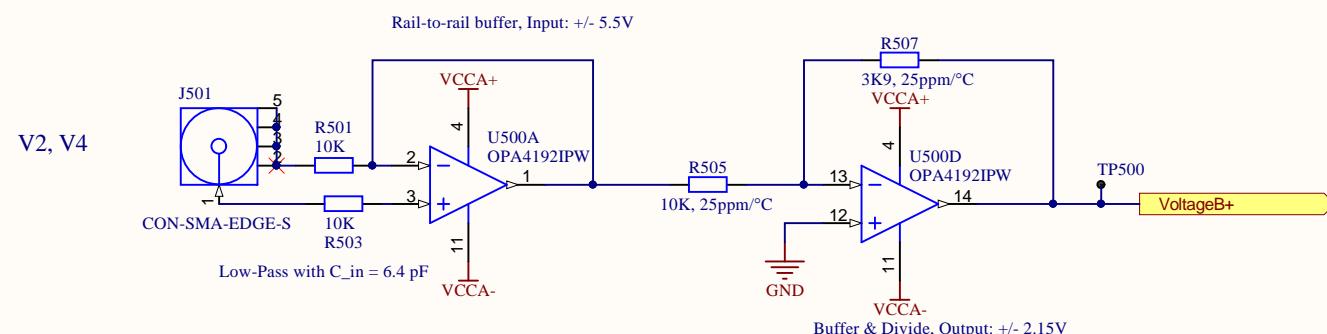
ADC





1V at the input corresponds to -390mV at the ADC input
With an ADC configuration of 24-bit & Gain = 1,
1 LSB corresponds to -1.22uV

Note: For pseudo-differential inputs, the maximum amplitude is +/- 2.2V



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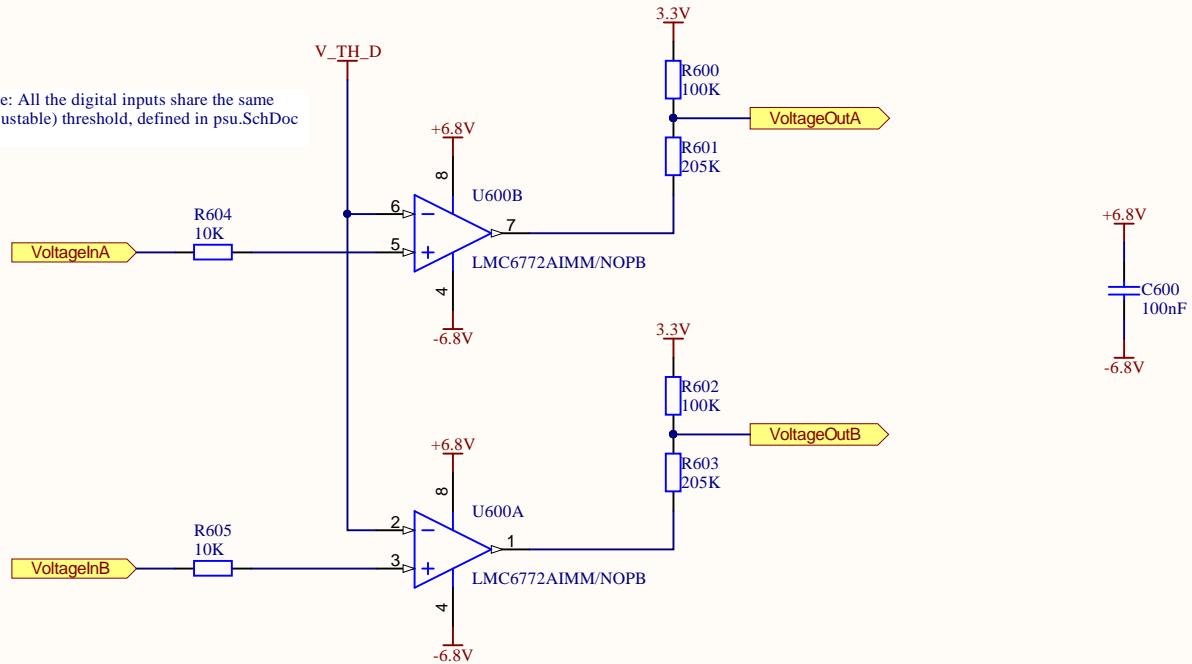
Drawing title:

Voltage Channel

Drawing number:	6	Rev.	2	Format:	Laboratory:	TIK	Project:	voltage_channel.SchDoc
Date:	14.11.2016	14:36:52		A4 Q	Drawn by:	Stefan Lippuner		
File:	C:\Users\user\Documents\Rocketlogger\hardware\pcb\Capel\voltage_channel.SchDoc							

A

Note: All the digital inputs share the same (adjustable) threshold, defined in psu.SchDoc



B

A

B

C

C

D

D



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Drawing title:

Digital Voltage Channel

Drawing number: 7 Rev. 2

Date: 14.11.2016 14:36:52

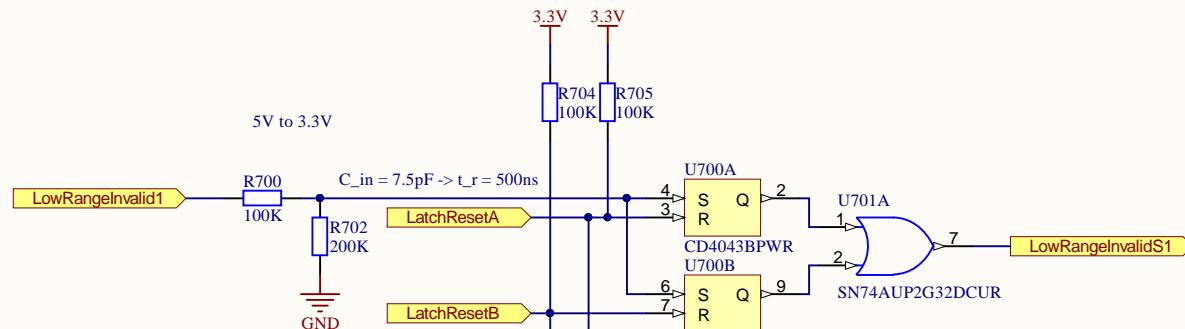
Format: TIK

A4 Q Drawn by: Stefan Lippuner

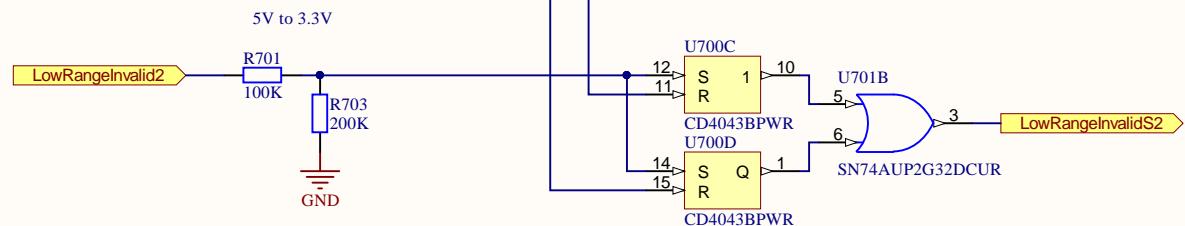
Project: digital_voltage_channel.SchDoc

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A

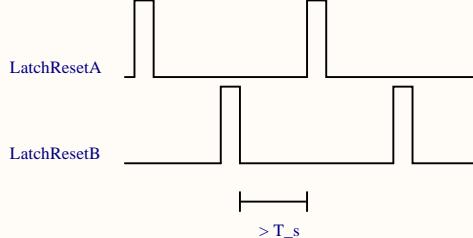
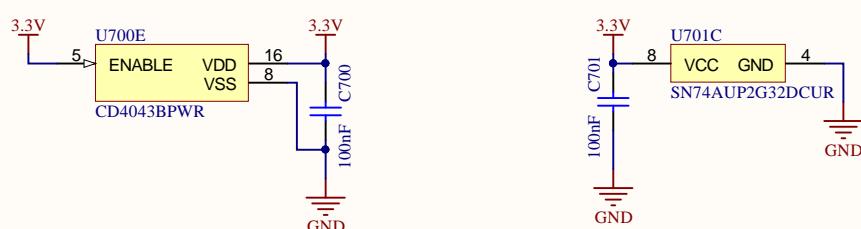


B



C

This circuit stretches the (potentially) short pulses on the LowRangelInvalid signals, such that the ADC can actually detect them. In order to guarantee that, the periods between the non-overlapping reset periods for the two latches must be longer than the sampling period.



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Drawing title:

Range Valid Signal Stretching

Drawing number: 8	Rev. 2	Format: A4 Q	Laboratory: TIK	Project: range_valid_stretching.SchDoc
Date: 14.11.2016 14:36:52		Drawn by: Stefan Lippuner		Page 8 of 8
File: C:\Users\user\Documents\Rocketlogger\hardware\pcb\Cape\range_valid_stretching.SchDoc				

