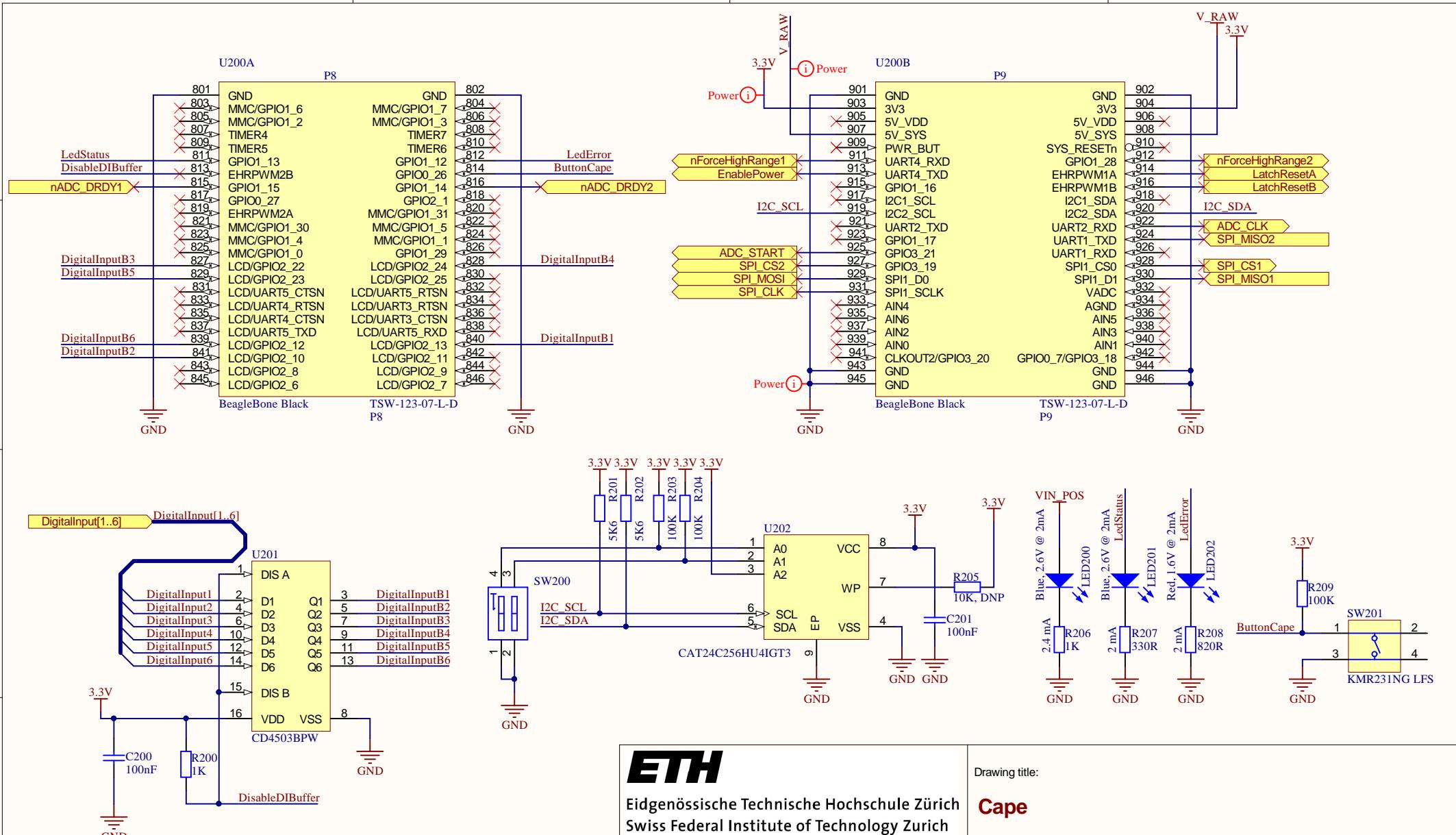


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Project:
Top

Drawing number:	1	Rev:	1	Format:	Laboratory: TIK	Sheet:	top.SchDoc
Date:	14.11.2016	11:17:56		A3	Drawn by:	Stefan Lippuner	
File:	C:\Users\user\Documents\Rocketlogger\hardware\pcb\Cape\top.SchDoc						

1 2 3 4



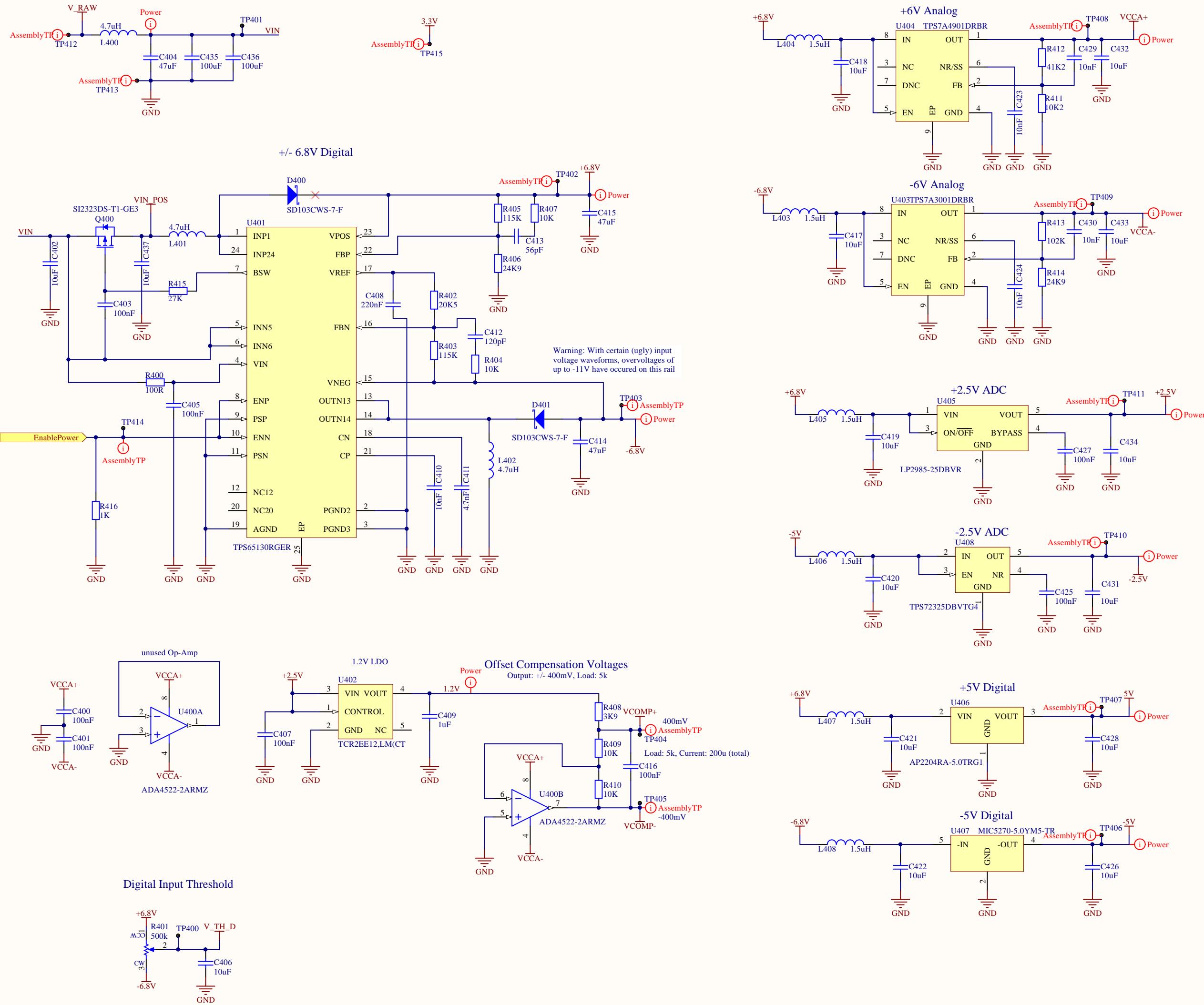
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Drawing number:	2	Rev.	1	Format:	Laboratory:	TIK	Project:	cape.SchDoc
Date:	14.11.2016	11:17:56		A4 Q	Drawn by:	Stefan Lippuner		
File:	C:\Users\user\Documents\Rocketlogger\hardware\pcb\Cape\cape.SchDoc							

Drawing title:

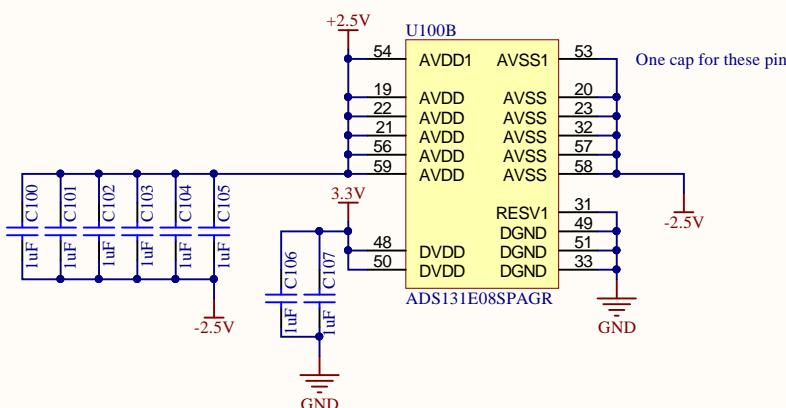
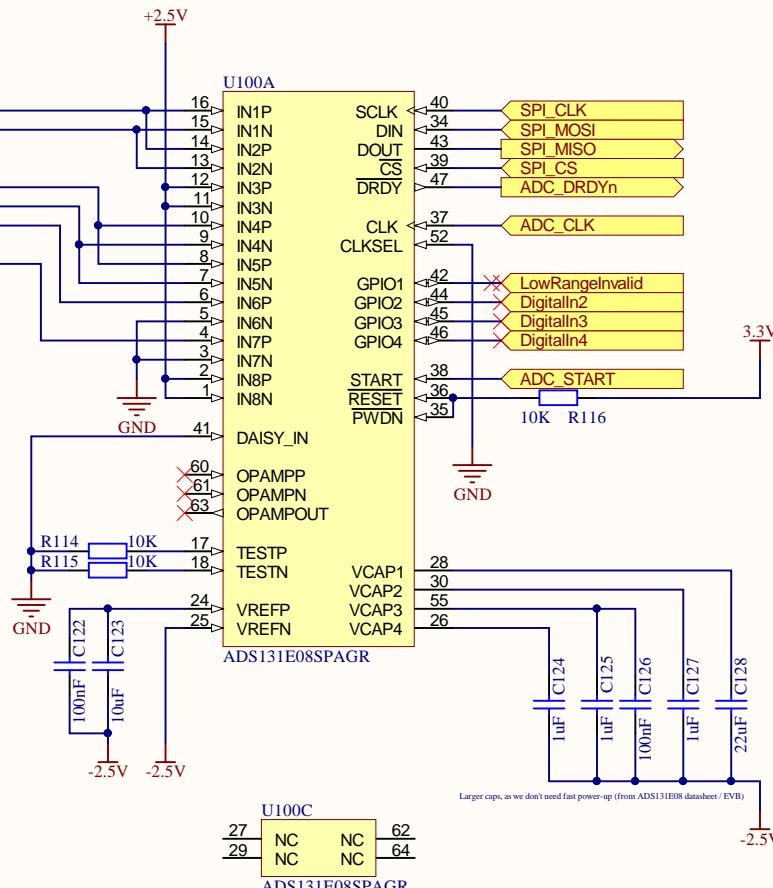
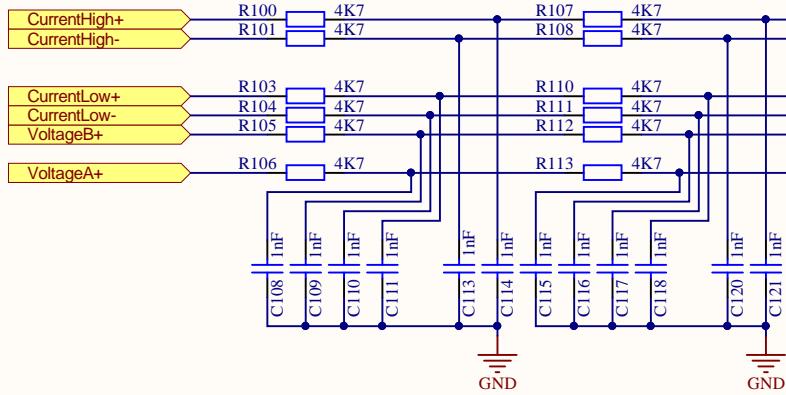
Cape

1 2 3 4



Resistors limit input current to 638uA

2nd order filter, -3dB @ 33.9kHz



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Drawing title

ADC

Drawing number: 4 Rev. 1 Format: Laboratory: TIK

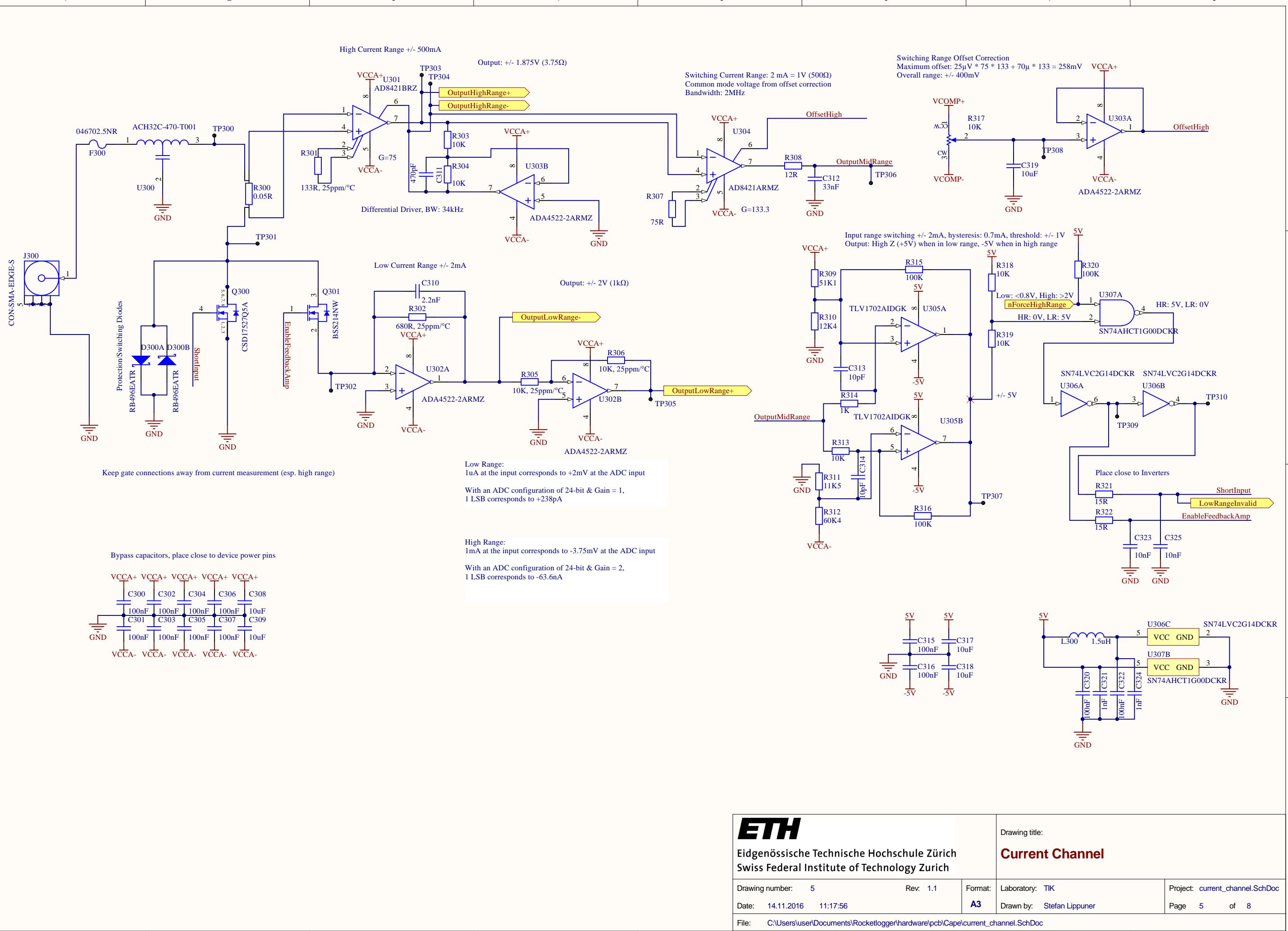
Date: 14.11.2016 11:17:56

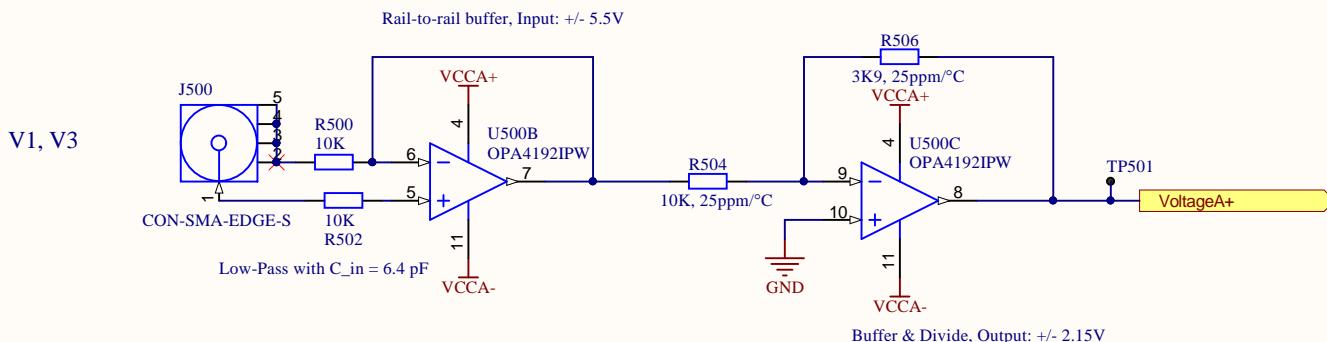
Format: Laboratory: TIK

A4 Q Drawn by: Stefan Lippuner

Project: adc.SchDoc

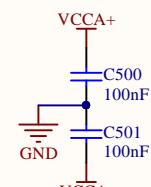
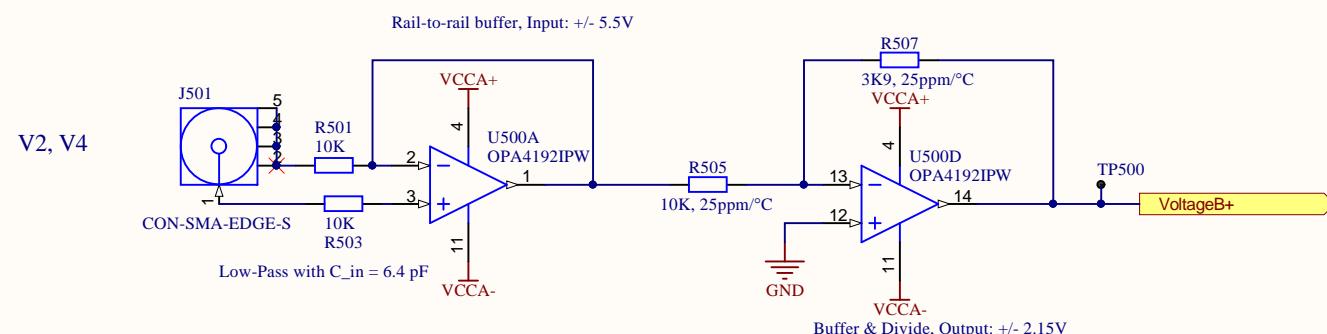
Page 4 of





1V at the input corresponds to -390mV at the ADC input
With an ADC configuration of 24-bit & Gain = 1,
1 LSB corresponds to -1.22uV

Note: For pseudo-differential inputs, the maximum amplitude is +/- 2.2V



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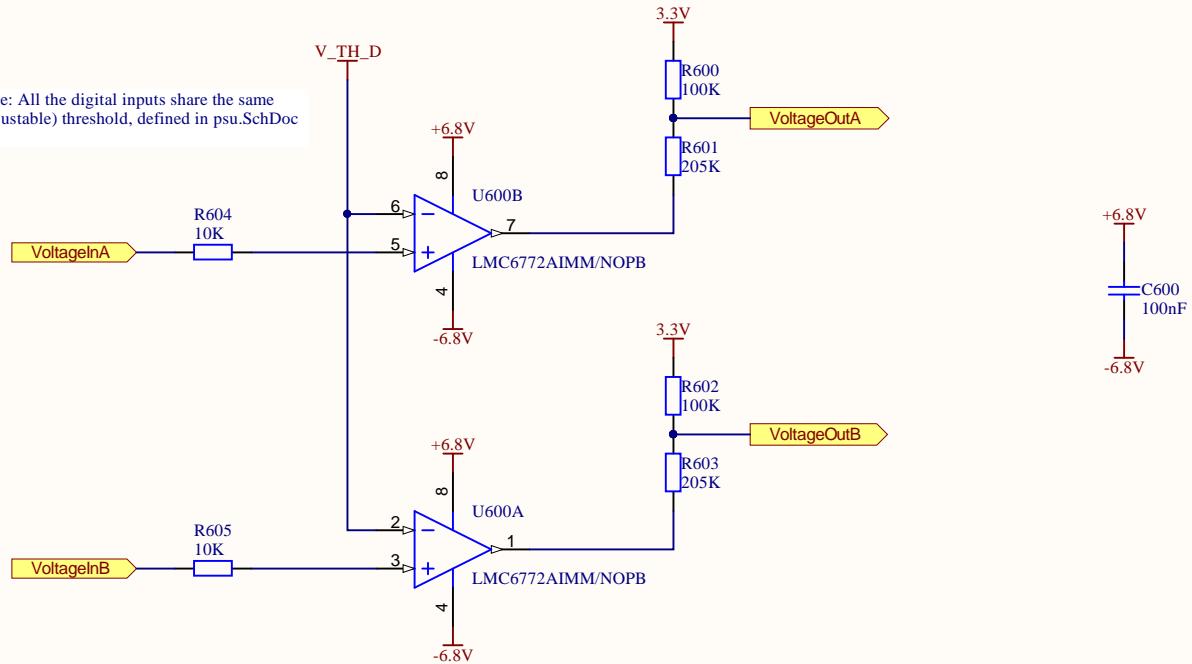
Drawing title:

Voltage Channel

Drawing number:	6	Rev.	1	Format:	Laboratory:	TIK	Project:	voltage_channel.SchDoc
Date:	14.11.2016	11:17:56		A4 Q	Drawn by:	Stefan Lippuner	Page	6 of 8
File:	C:\Users\user\Documents\Rocketlogger\hardware\pcb\Capel\voltage_channel.SchDoc							

A

Note: All the digital inputs share the same (adjustable) threshold, defined in psu.SchDoc



B

A

B

C

C

D

D



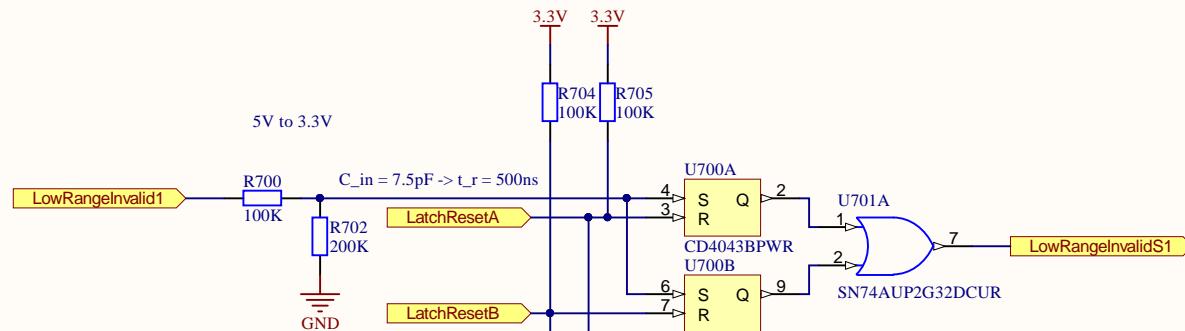
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Drawing title:

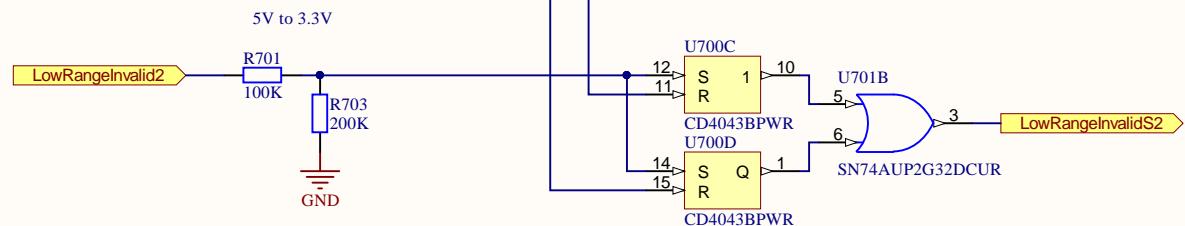
Digital Voltage Channel

Drawing number: 7	Rev. 1	Format: A4 Q	Laboratory: TIK	Project: digital_voltage_channel.SchDoc
Date: 14.11.2016 11:17:56		Drawn by: Stefan Lippuner		Page 7 of 8
File: C:\Users\user\Documents\Rocketlogger\hardware\pcb\Cape\digital_voltage_channel.SchDoc				

A

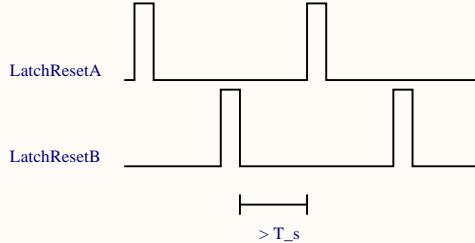
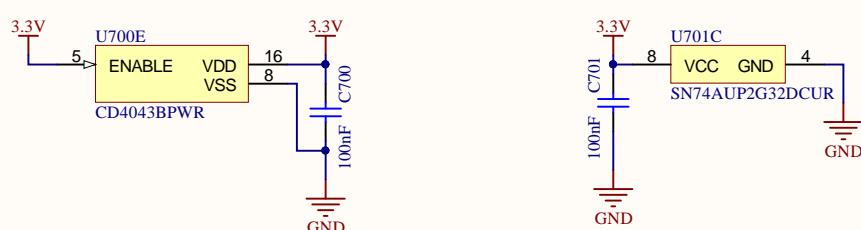


B



C

This circuit stretches the (potentially) short pulses on the LowRangeInvalid signals, such that the ADC can actually detect them. In order to guarantee that, the periods between the non-overlapping reset periods for the two latches must be longer than the sampling period.



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Drawing title:

Range Valid Signal Stretching

Format: A4 Q	Laboratory: TIK	Project: range_valid_stretching.SchDoc
Date: 14.11.2016 11:17:56	Rev. 1	Drawn by: Stefan Lippuner
File: C:\Users\user\Documents\Rocketlogger\hardware\pcb\Cape\range_valid_stretching.SchDoc		

