

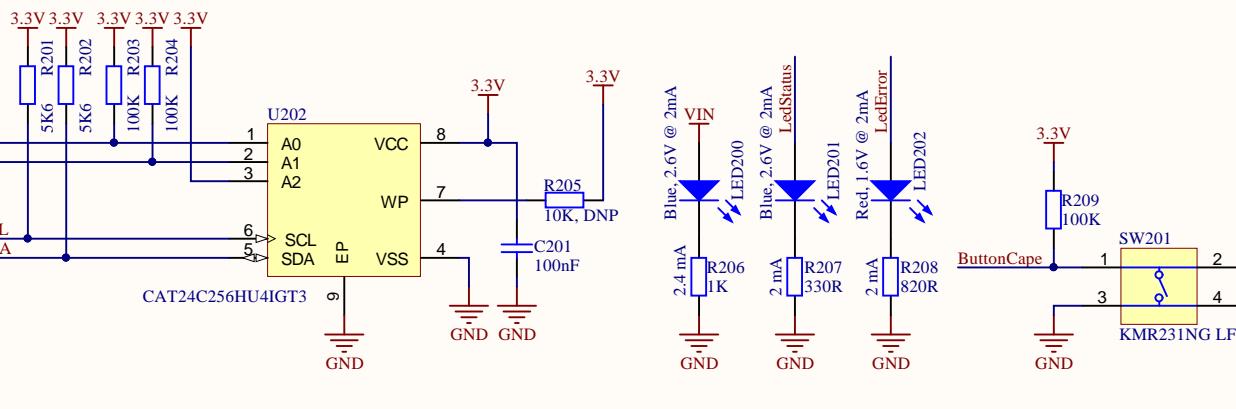
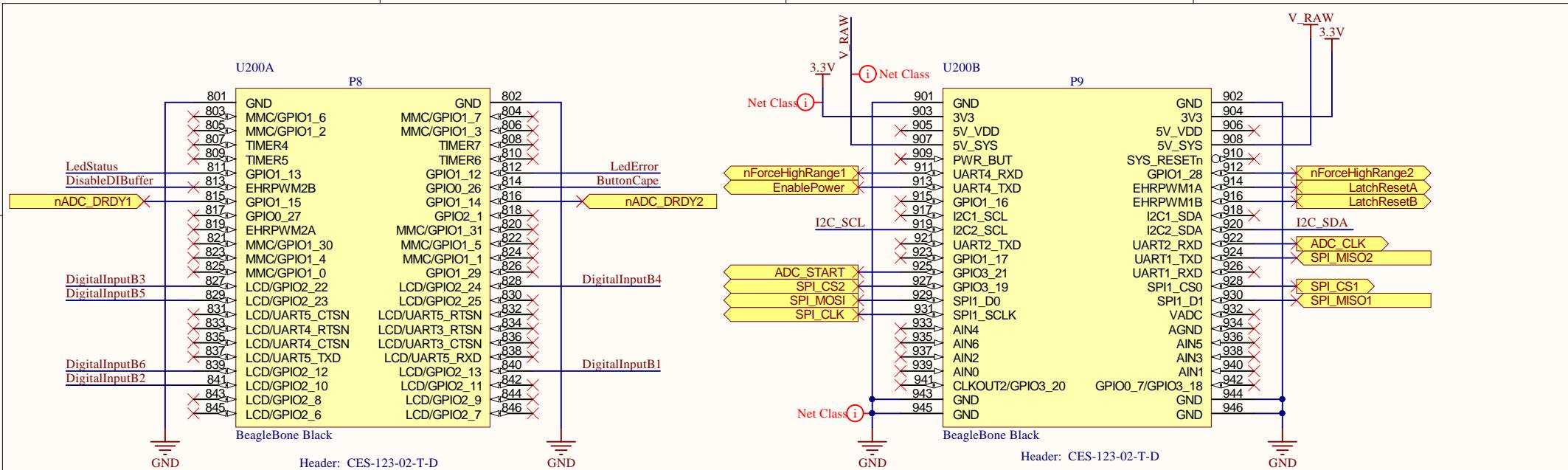
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Swiss Federal Institute of Technology Zurich

Project:

Top

Drawing number:	1	Rev:	1	Format:	Laboratory: TIK	Sheet:	top.SchDoc
Date:	18.10.2016	15:11:15		A3	Drawn by:	Stefan Lippuner	
File:	C:\Users\user\Documents\Rocketlogger\hardware\pcb\Cape\top.SchDoc						

1 2 3 4

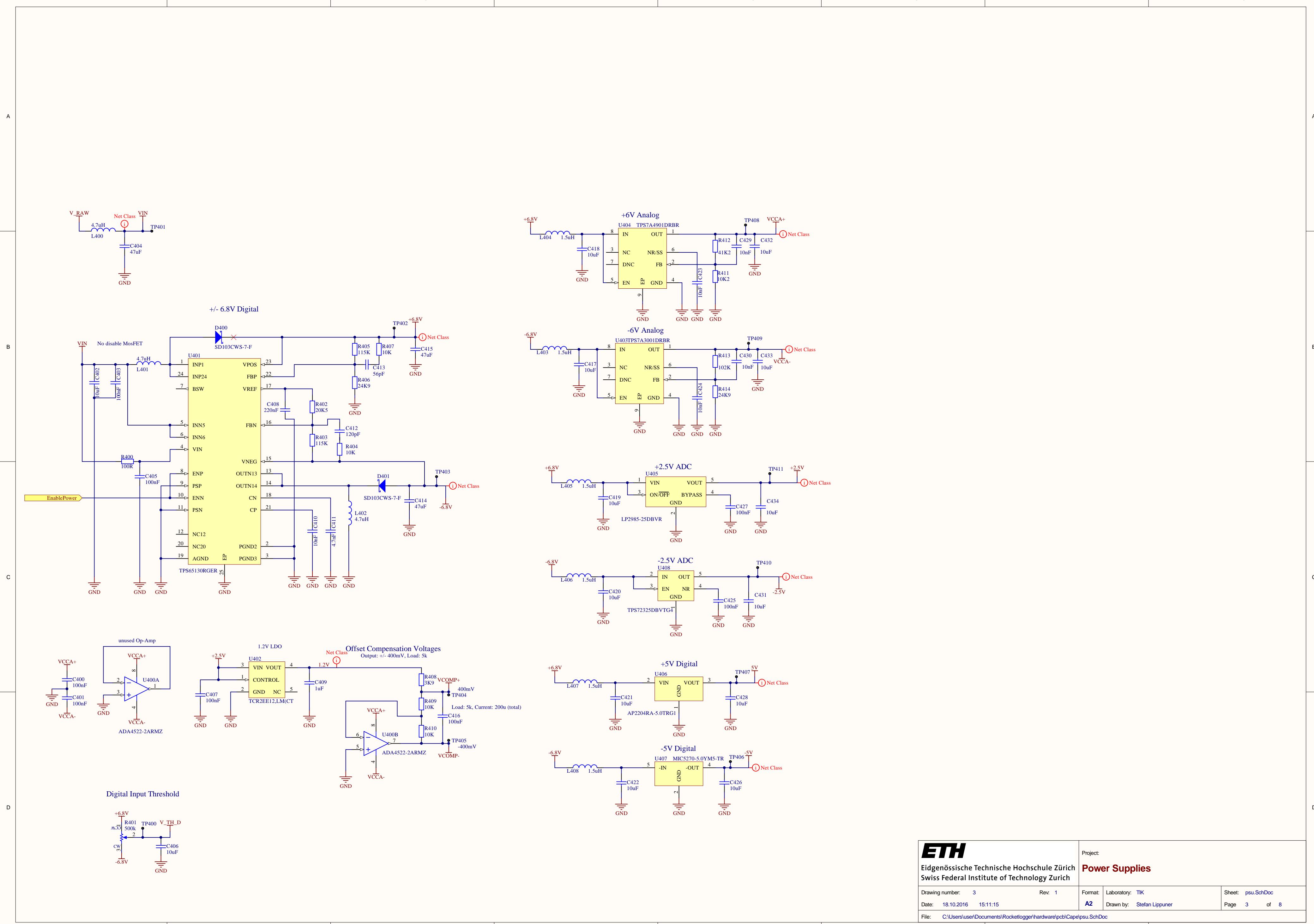


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Drawing title:

Cape

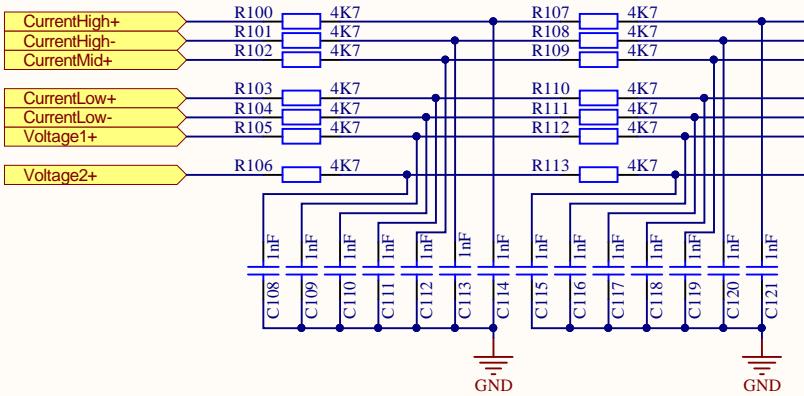
Drawing number:	2	Rev. 1	Format: A4 Q	Laboratory: TIK	Project: cape.SchDoc
Date:	18.10.2016 15:11:15		Drawn by: Stefan Lippuner		Page 2 of 8
File:	C:\Users\user\Documents\Rocketlogger\hardware\pcb\Cape\cape.SchDoc				



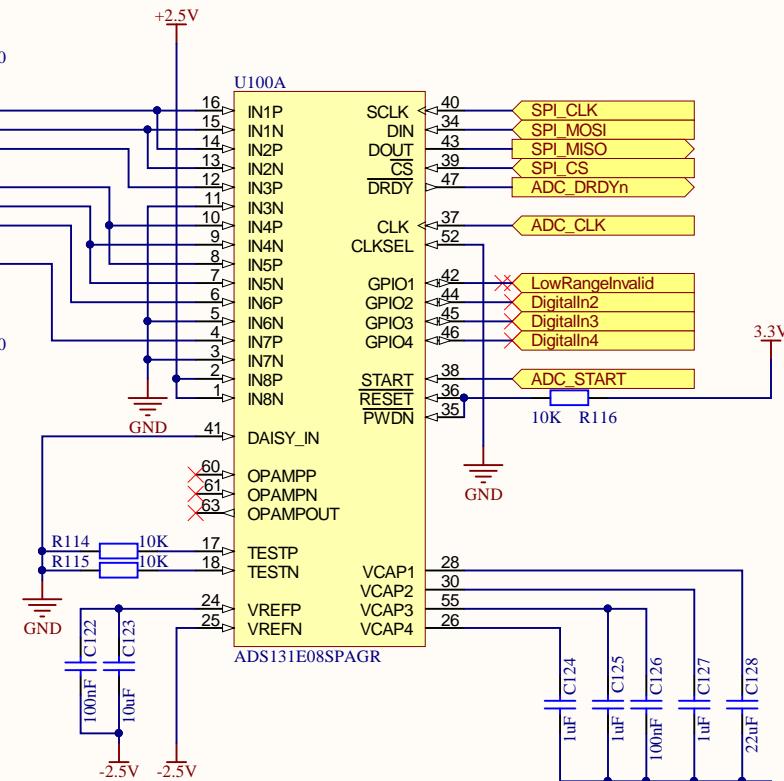
A

Resistors limit input current to 638uA

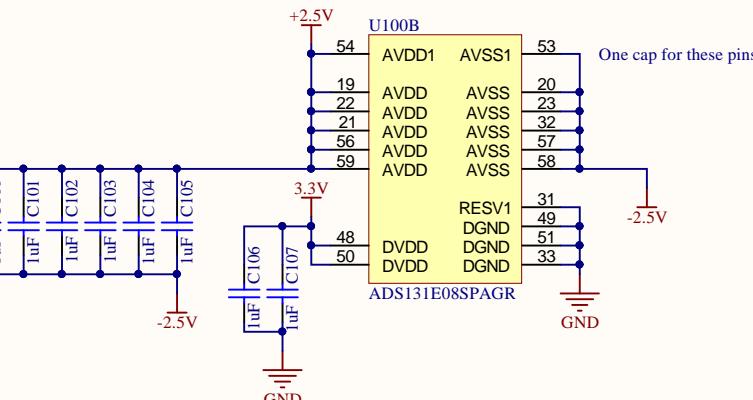
2nd order filter, -3dB @ 33.9kHz



The medium range voltages can exceed the ADC supply during normal operation, we don't want the limiting currents to flow into the ADC



B



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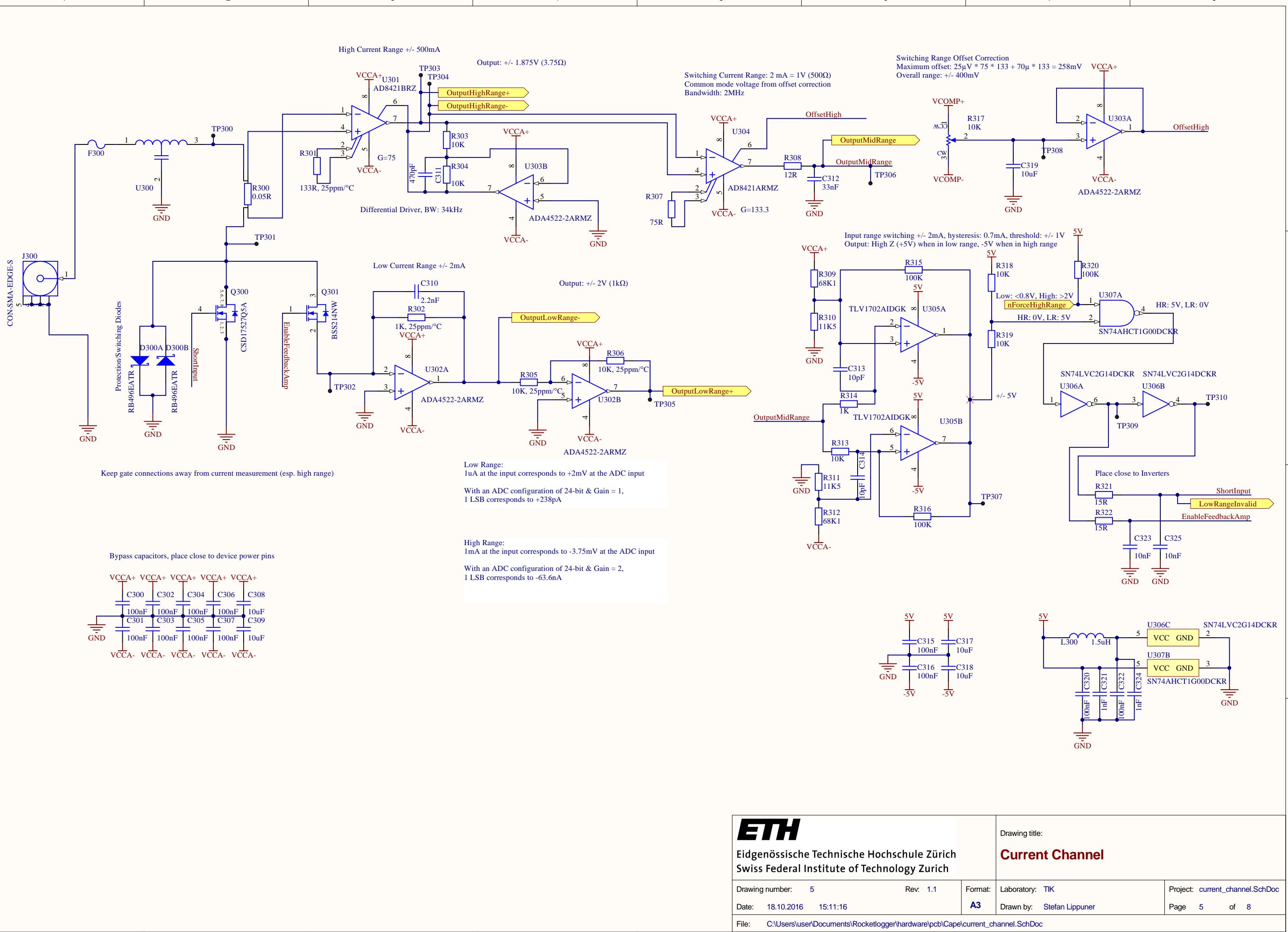
Drawing number: 4 Rev. 1 Format: Laboratory: TIK Project: adc.SchDoc

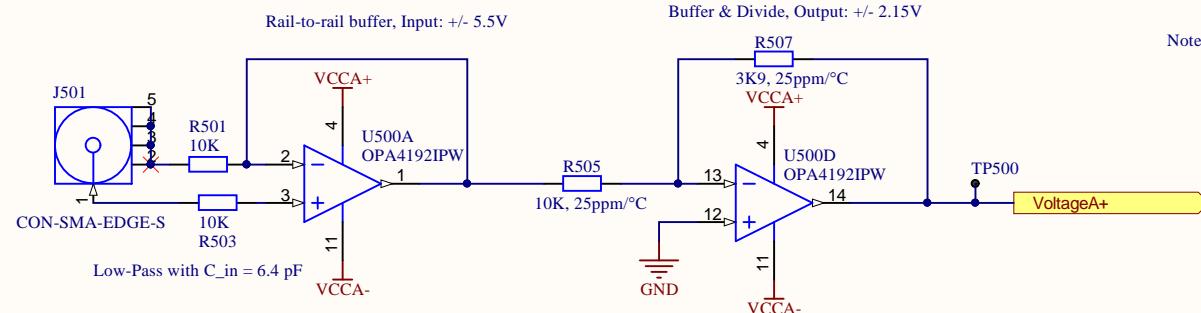
Date: 18.10.2016 15:11:16 Format: A4 Q Drawn by: Stefan Lippuner

File: C:\Users\user\Documents\RocketLogger\hardware\pcb\adc.SchDoc Page 4 of 8

Drawing title:

**ADC**

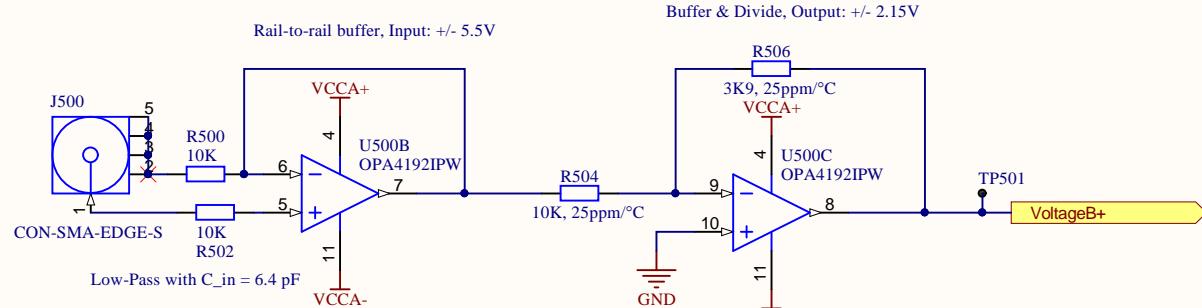




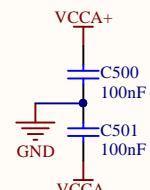
Note: Two channels share an Op Amp

1V at the input corresponds to -390mV at the ADC input

With an ADC configuration of 24-bit & Gain = 1,  
1 LSB corresponds to -1.22 $\mu$ V



Note: For pseudo-differential inputs, the maximum amplitude is +/- 2.2V



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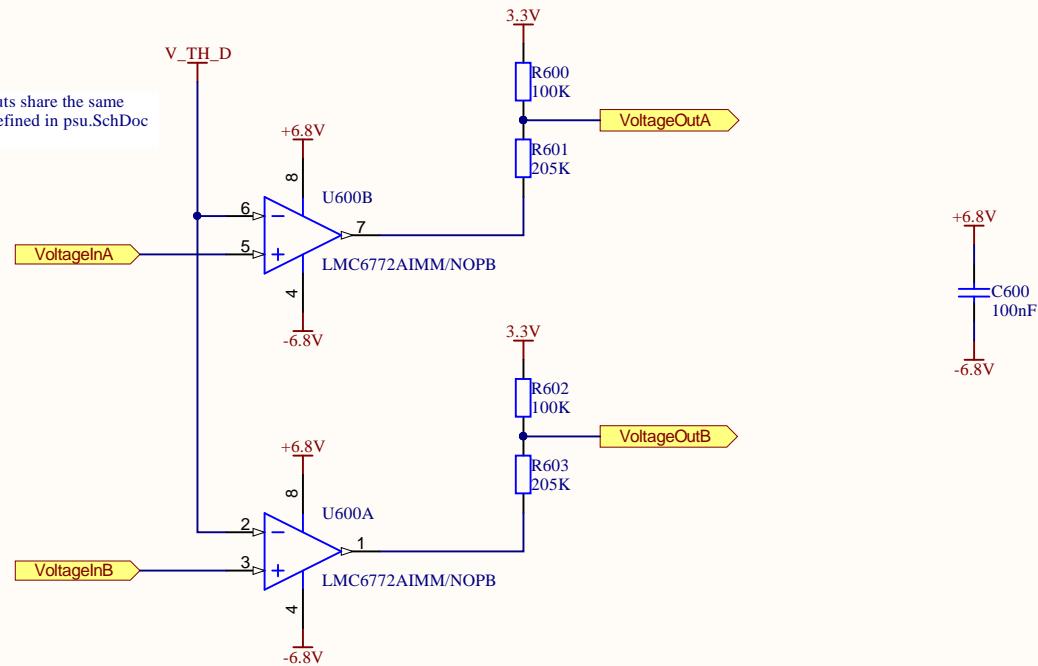
Drawing title:

## Voltage Channel

Drawing number:	6	Rev.	1	Format:	Laboratory:	TIK	Project:	voltage_channel.SchDoc
Date:	18.10.2016	15:11:16		A4 Q	Drawn by:	Stefan Lippuner		
File:	C:\Users\user\Documents\Rocketlogger\hardware\pcb\Capel\voltage_channel.SchDoc							

A

Note: All the digital inputs share the same (adjustable) threshold, defined in psu.SchDoc



B

C

D

A

B

C

D



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Drawing title:

## Digital Voltage Channel

Drawing number: 7 Rev. 1

Date: 18.10.2016 15:11:16

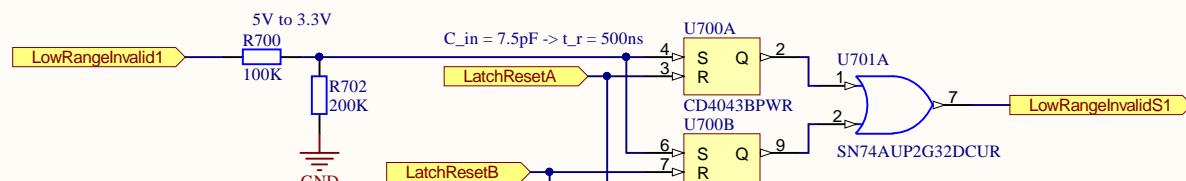
Format: A4 Q Laboratory: TIK

Drawn by: Stefan Lippuner

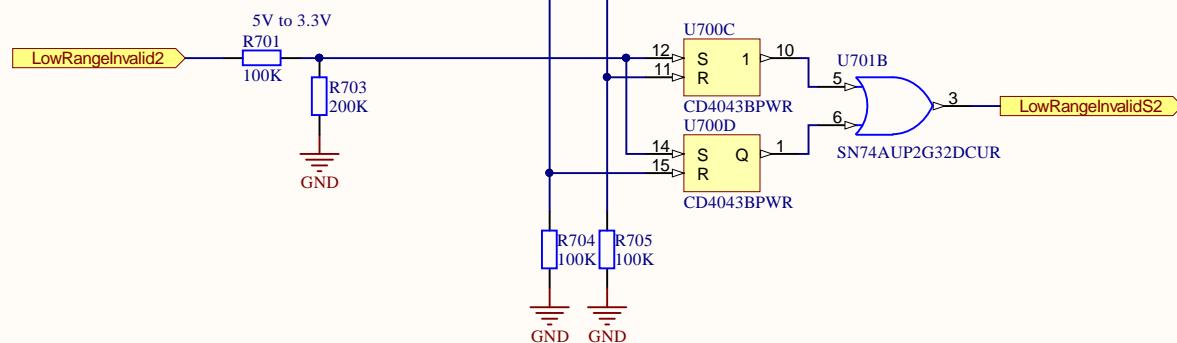
Project: digital\_voltage\_channel.SchDoc

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A

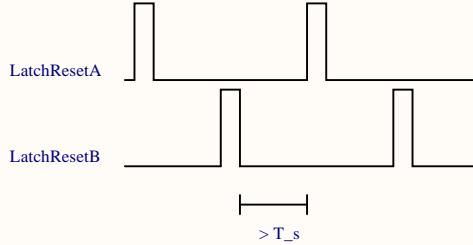
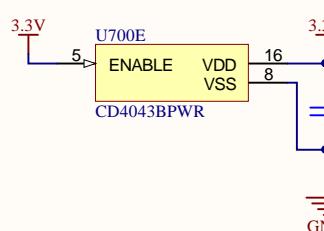


B



C

This circuit stretches the (potentially) short pulses on the LowRangeInvalid signals, such that the ADC can actually detect them. In order to guarantee that, the periods between the non-overlapping reset periods for the two latches must be longer than the sampling period.



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Drawing title:

## Range Valid Signal Stretching

Format: A4 Q	Laboratory: TIK	Project: range_valid_stretching.SchDoc
Date: 18.10.2016 15:11:16	Rev. 1	Drawn by: Stefan Lippuner
File: C:\Users\user\Documents\Rocketlogger\hardware\pcb\Cape\range_valid_stretching.SchDoc		

