

A

A

B

B

C

C

D

D



Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project:

Top

Drawing number: 1 Rev: 1 Format: Laboratory: TIK Sheet: top.SchDoc

Date: 21.09.2016 12:00:01 A3 Drawn by: Stefan Lippuner

File: C:\Users\user\Documents\RocketLogger\code\pcb\Cape\top.SchDoc Page 1 of 8

1

2

3

4

A

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C

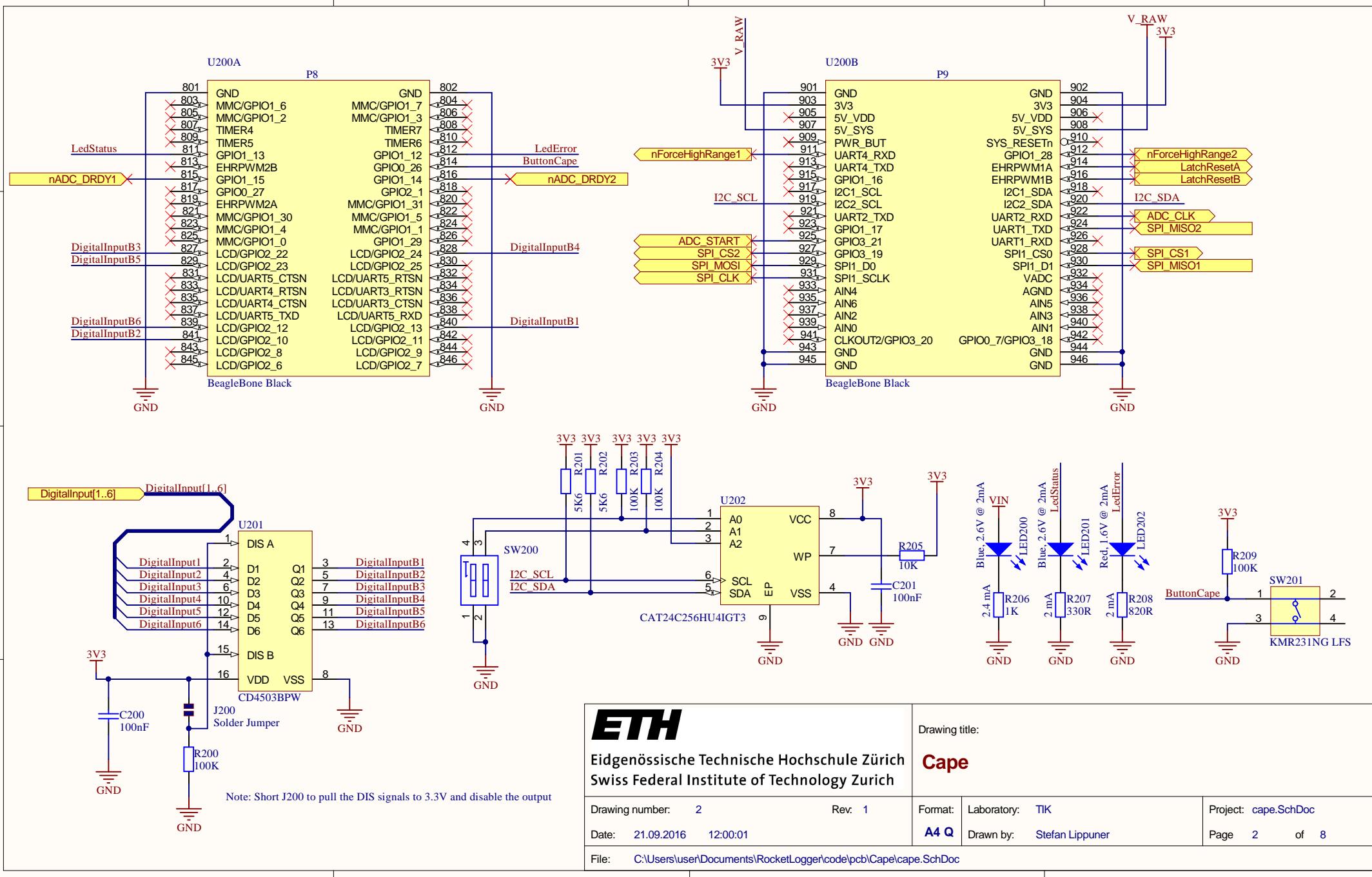
D

A

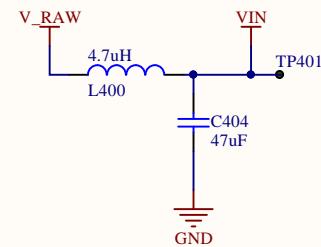
B

C

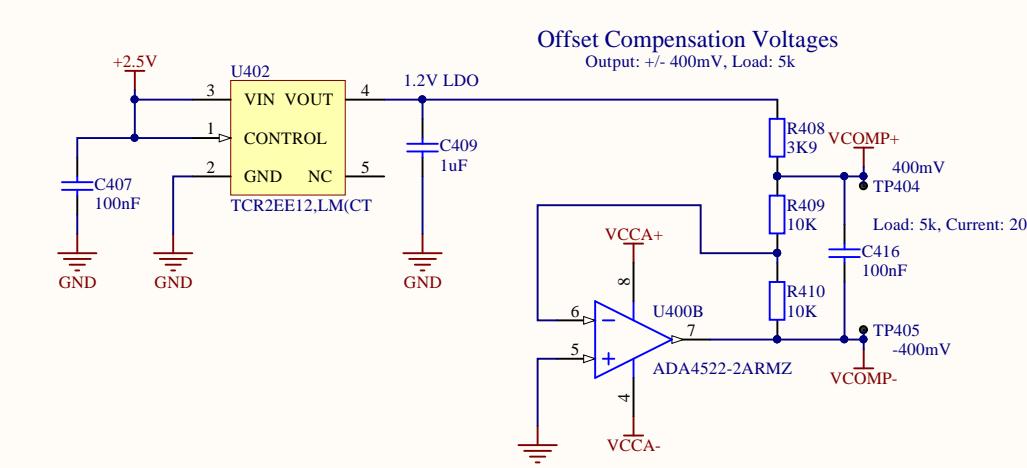
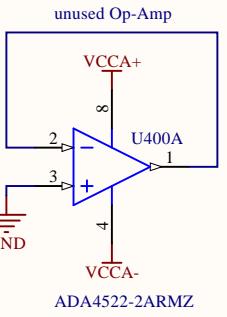
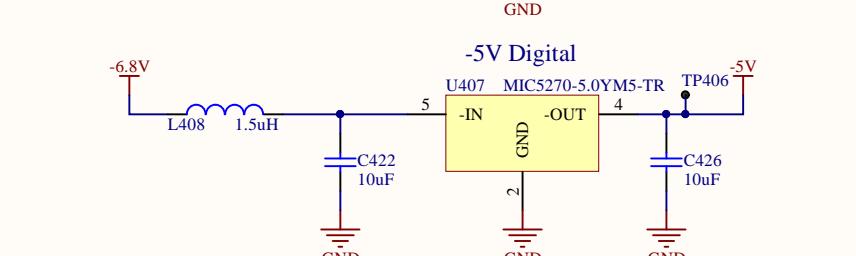
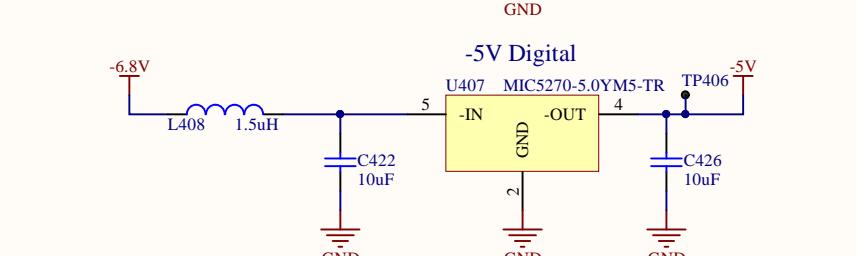
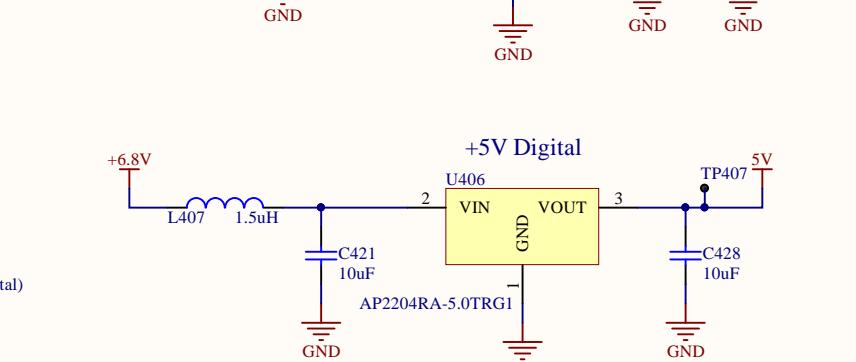
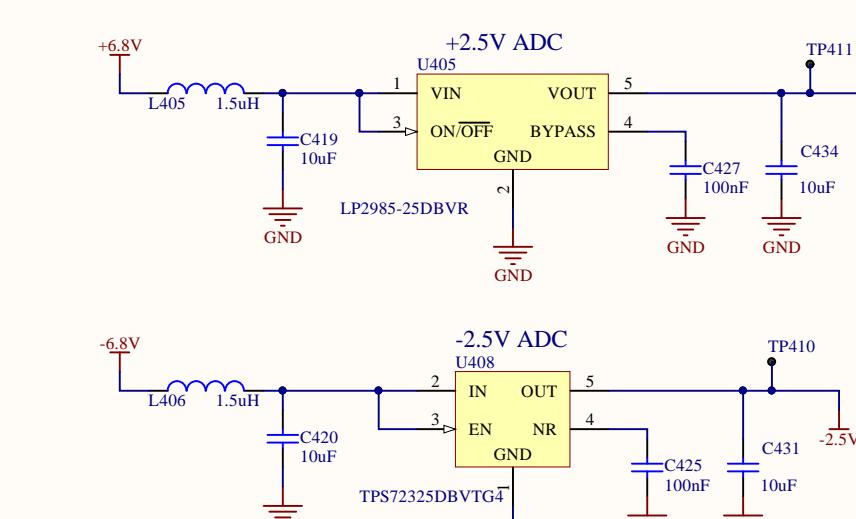
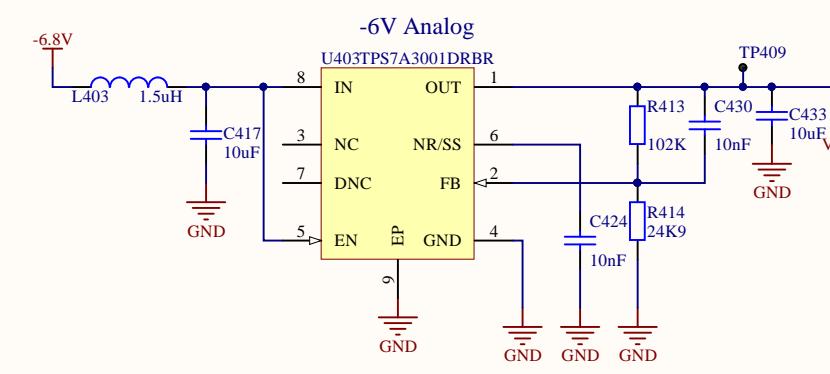
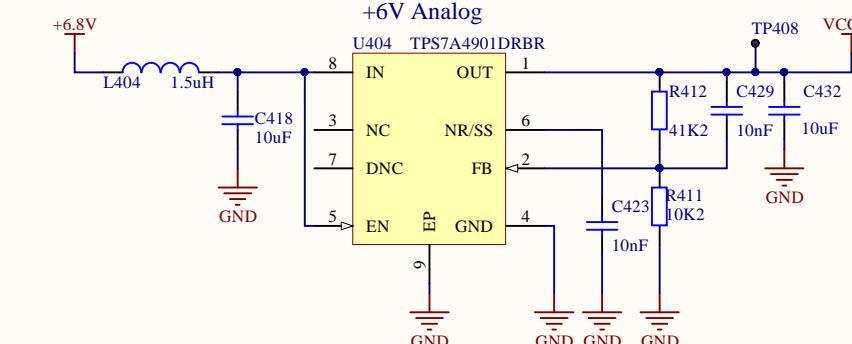
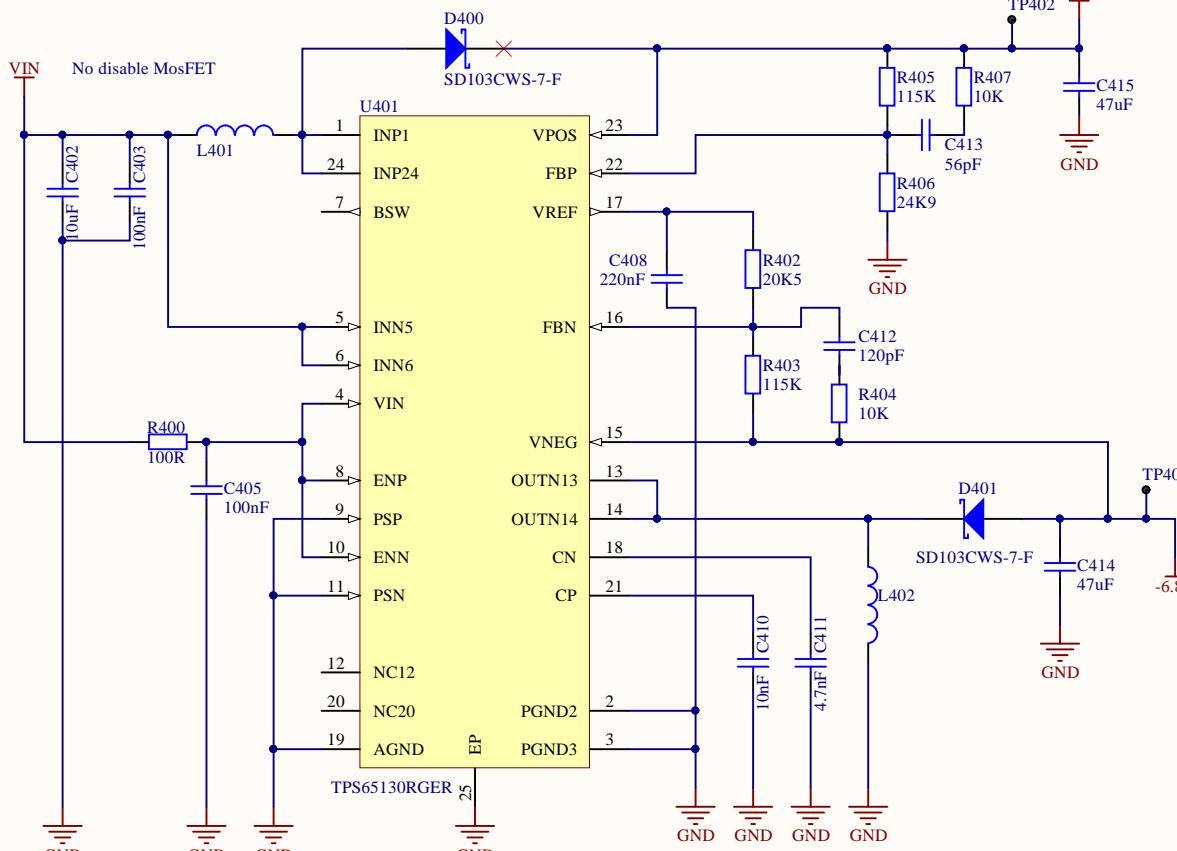
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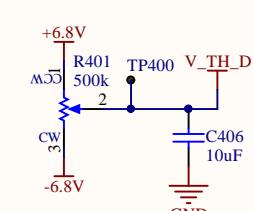
A



+/- 6.8V Digital



Digital Input Threshold



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Project:			
Power Supplies			
Drawing number: 3	Rev. 1	Format: Laboratory: TIK	Sheet: psu.SchDoc
Date: 21.09.2016 12:00:01		A2	Drawn by: Stefan Lippuner
File: C:/Users/user/Documents/RocketLogger/code/pcb/CapeIpsu.SchDoc			Page 3 of 8

A

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A

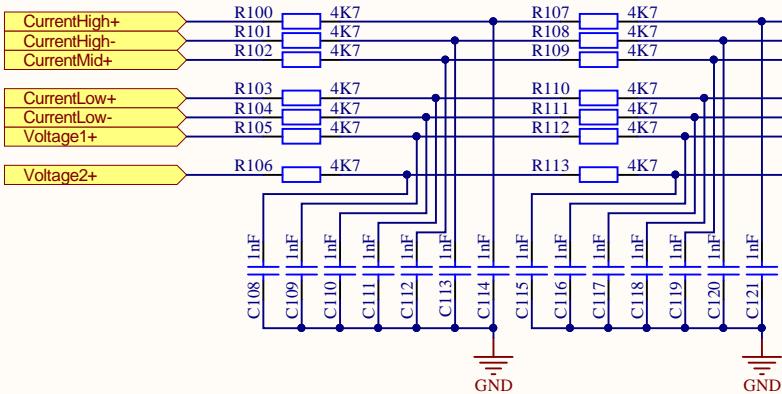
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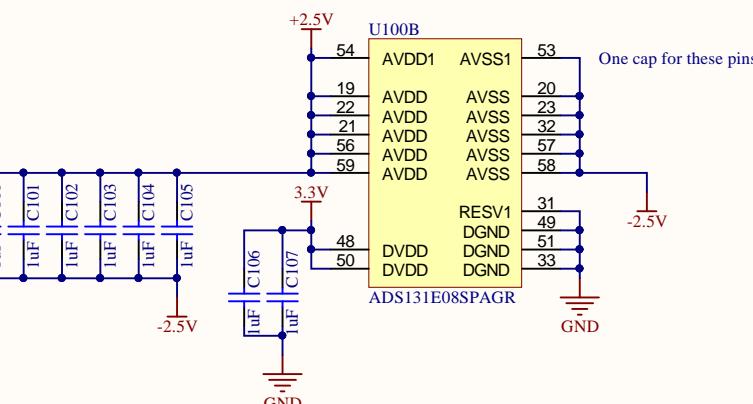
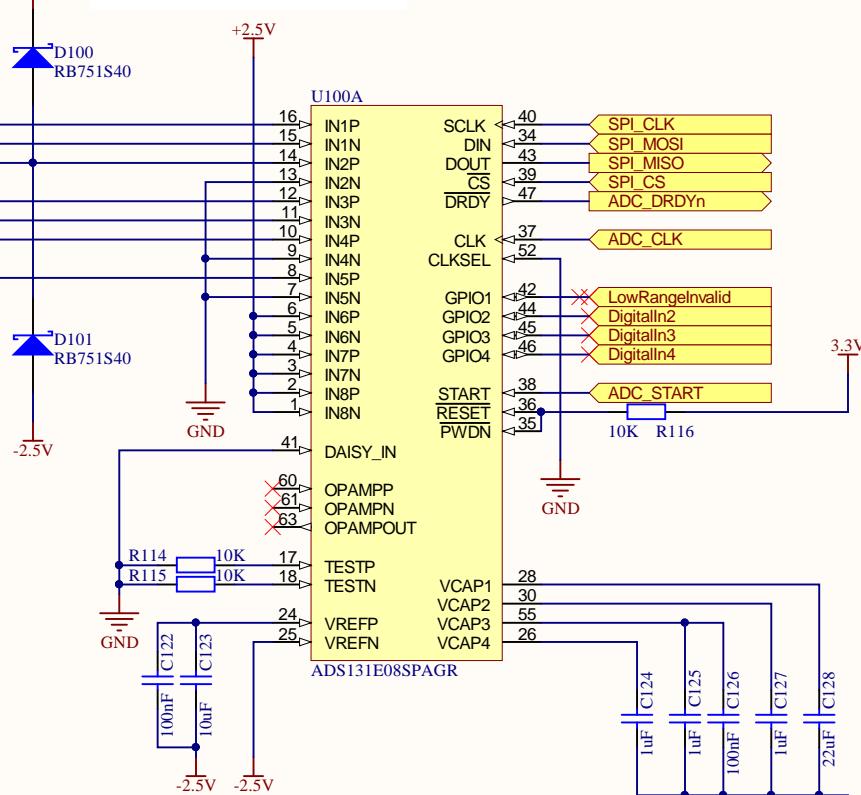
D

Resistors limit input current to 638uA

2nd order filter, -3dB @ 33.9kHz



The medium range voltages can exceed the ADC supply during normal operation, we don't want the limiting currents to flow into the ADC



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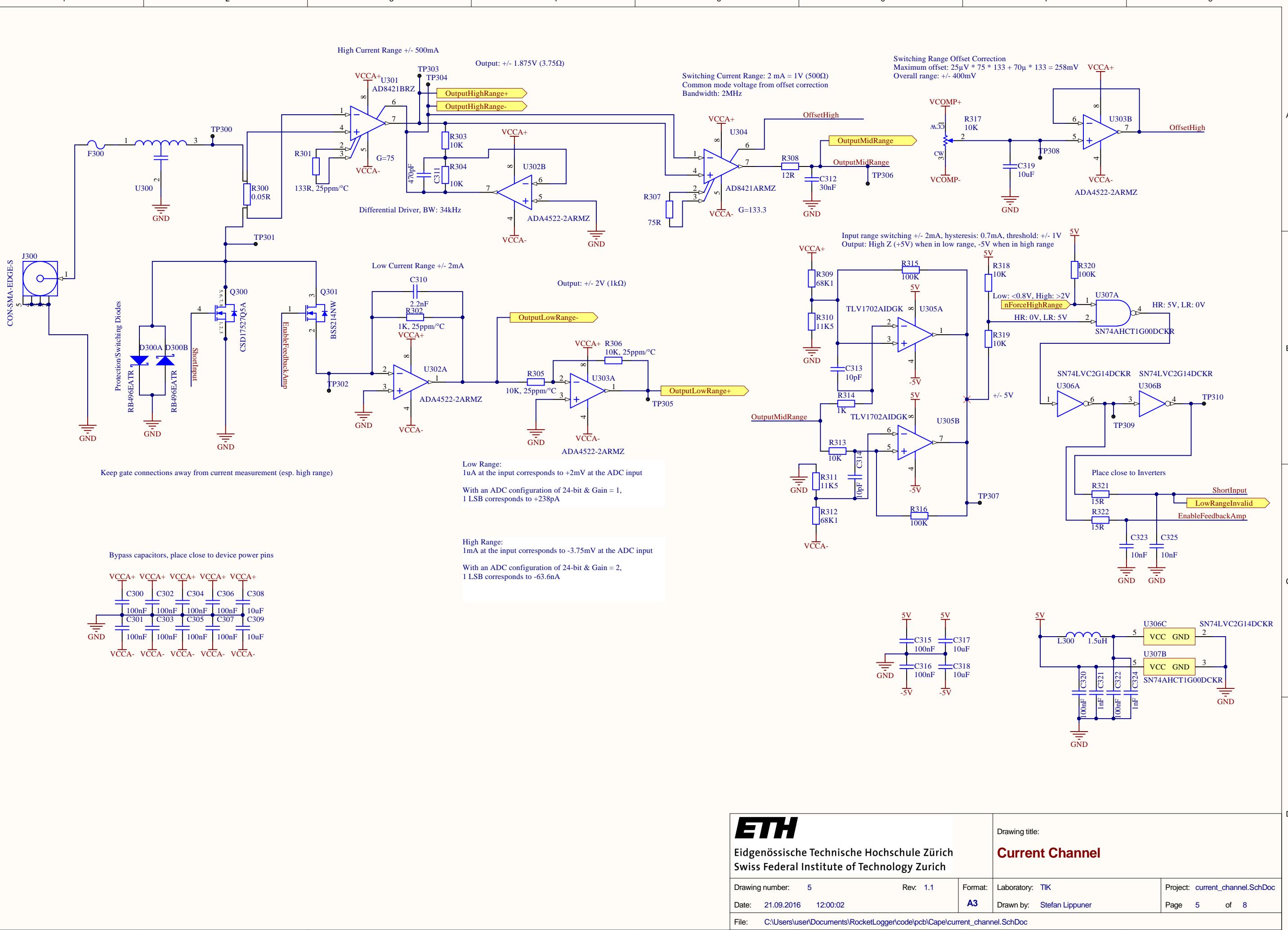
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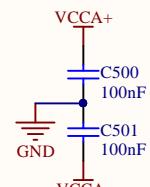
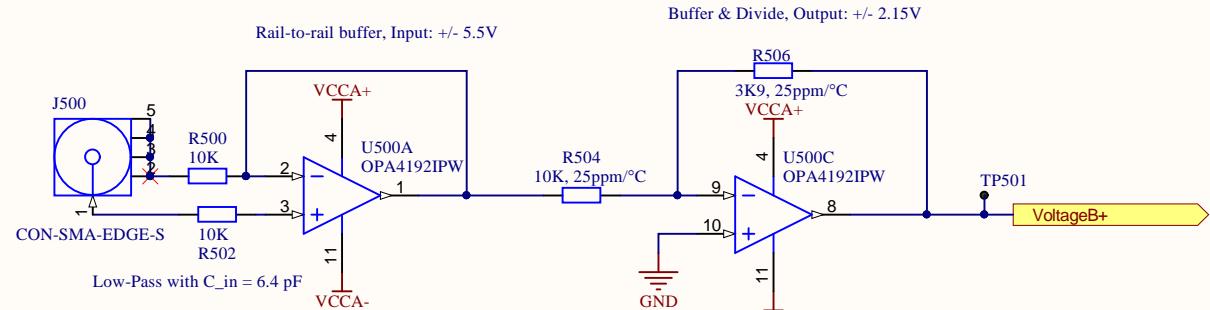
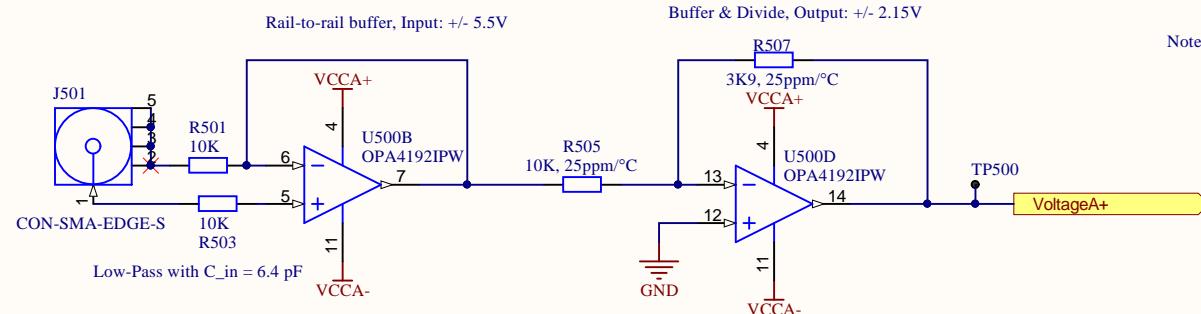
Date: 21.09.2016 12:00:02 Drawn by: Stefan Lippuner

File: C:\Users\user\Documents\RocketLogger\code\pcb\Cape\adc.SchDoc

Drawing title:

ADC





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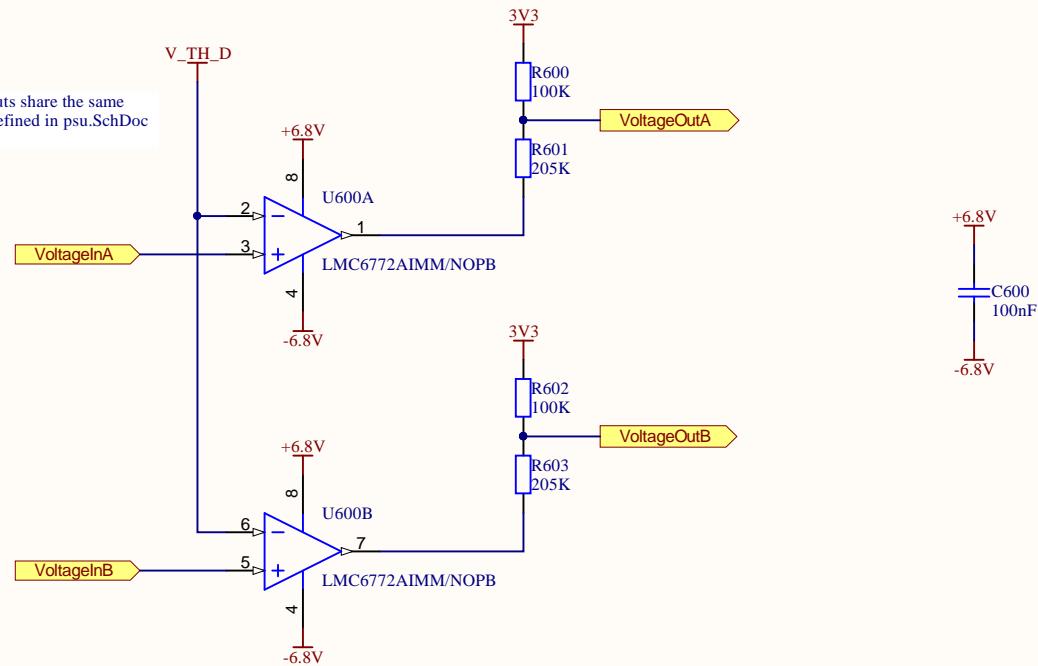
Drawing title:

Voltage Channel

Drawing number:	6	Rev.	1	Format:	Laboratory:	TIK	Project:	voltage_channel.SchDoc
Date:	21.09.2016	12:00:02		A4 Q	Drawn by:	Stefan Lippuner	Page	6 of 8
File:	C:\Users\user\Documents\RocketLogger\code\pcb\Cape\voltage_channel.SchDoc							

A

Note: All the digital inputs share the same (adjustable) threshold, defined in psu.SchDoc



B

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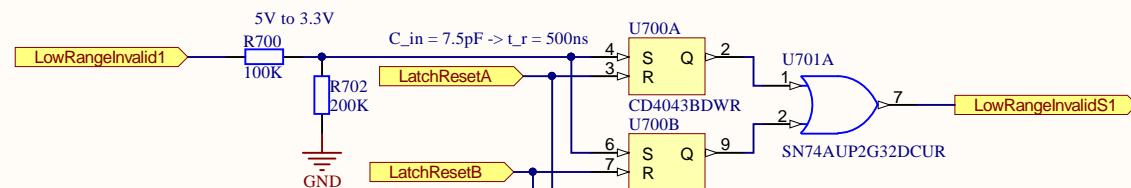
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Drawing title:

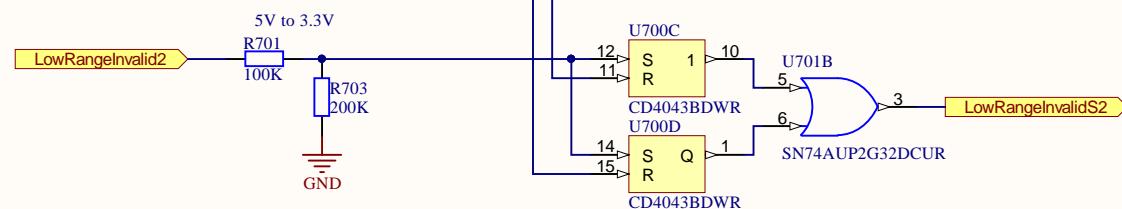
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Drawing number: 7	Rev. 1	Format: A4 Q	Laboratory: TIK	Project: digital_voltage_channel.SchDoc
Date: 21.09.2016 12:00:02		Drawn by: Stefan Lippuner		Page 7 of 8
File: C:\Users\user\Documents\RocketLogger\code\pcb\Cape\digital_voltage_channel.SchDoc				

A

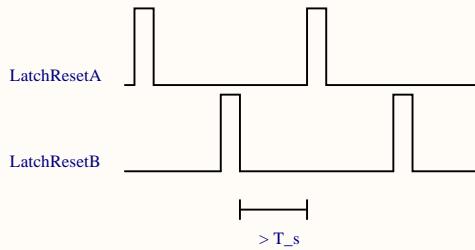
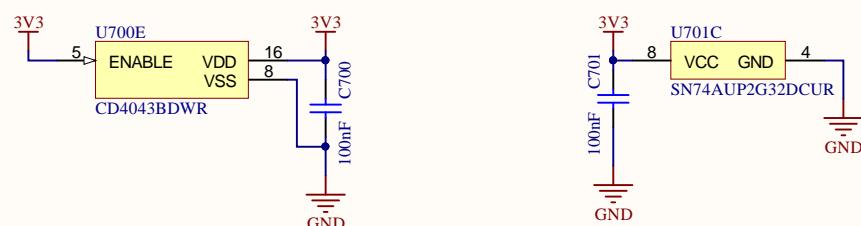


B



C

This circuit stretches the (potentially) short pulses on the LowRangeInvalid signals, such that the ADC can actually detect them. In order to guarantee that, the periods between the non-overlapping reset periods for the two latches must be longer than the sampling period.

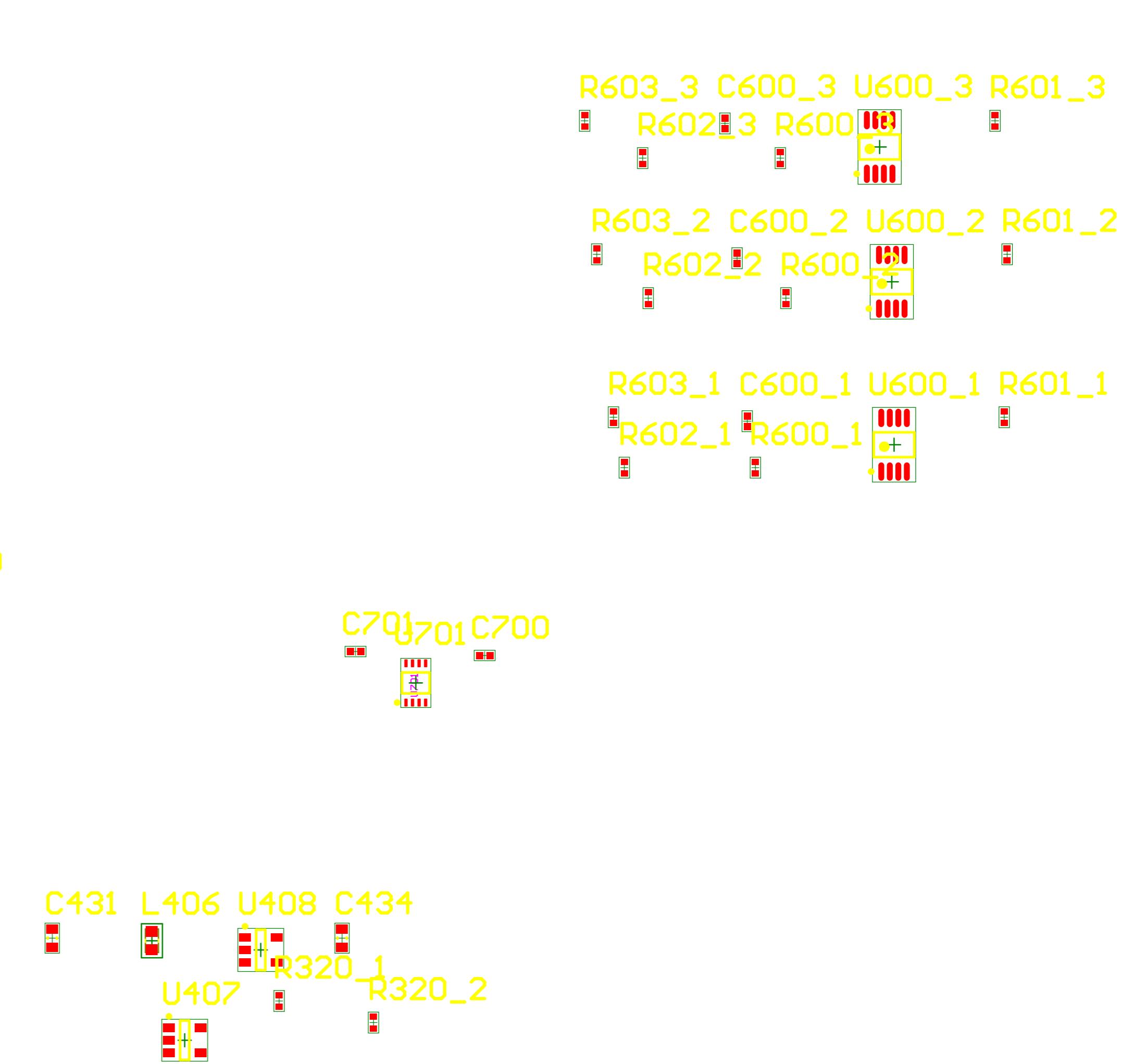
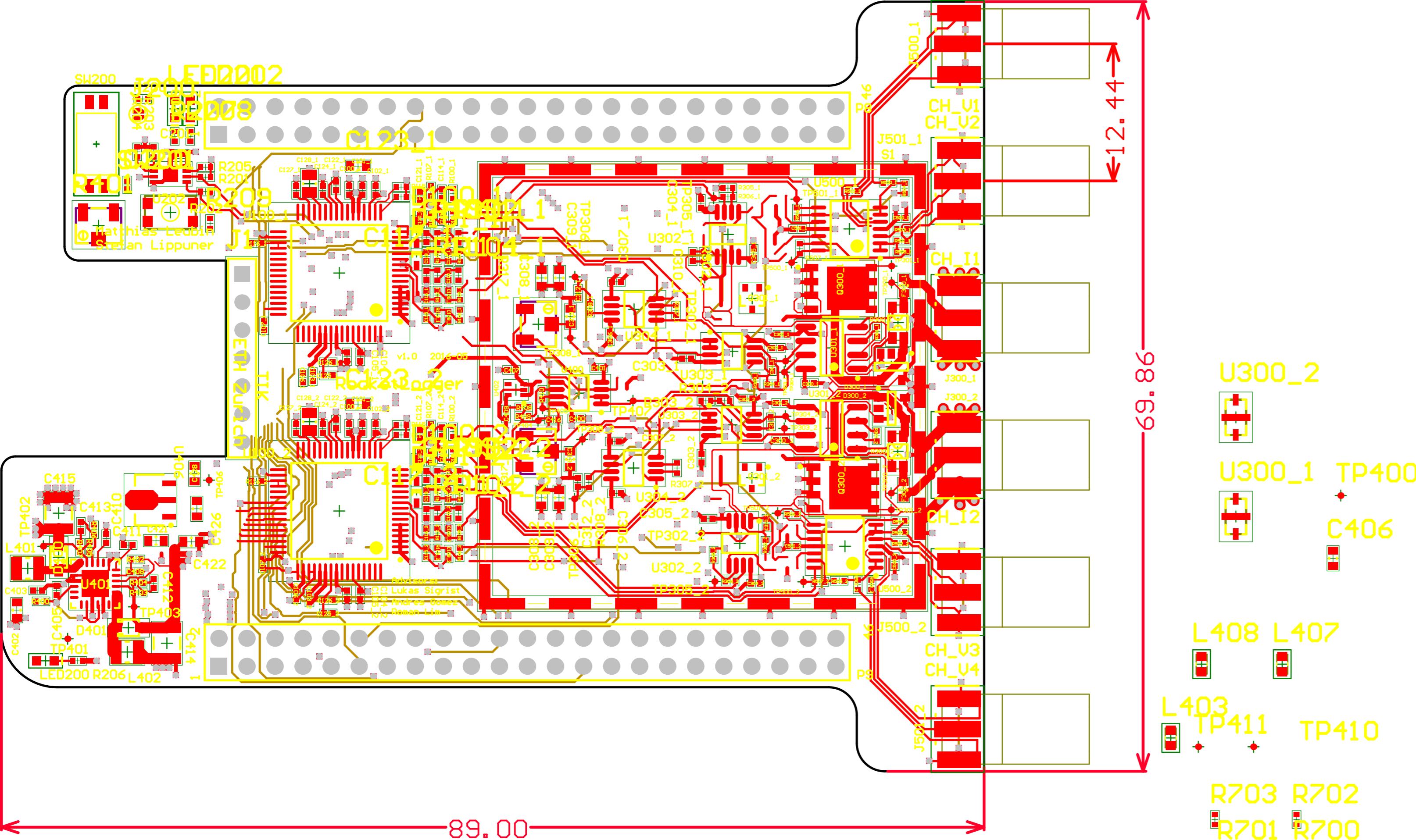


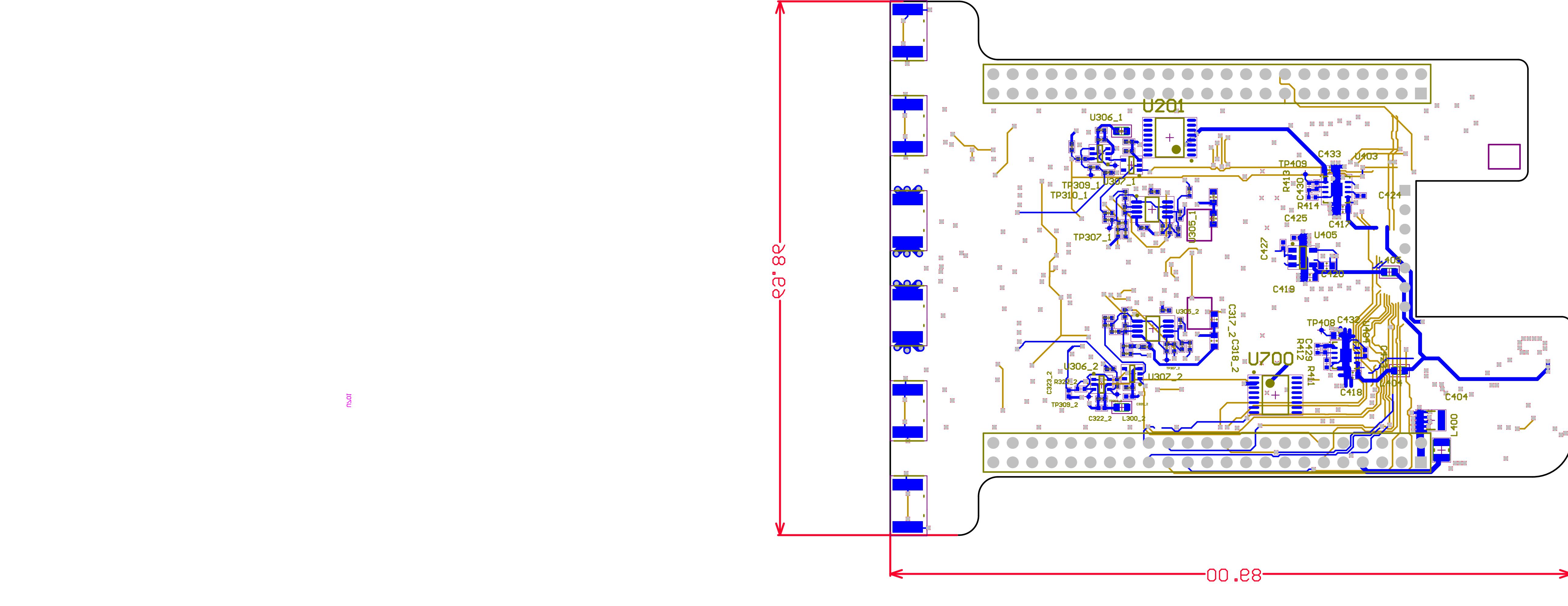
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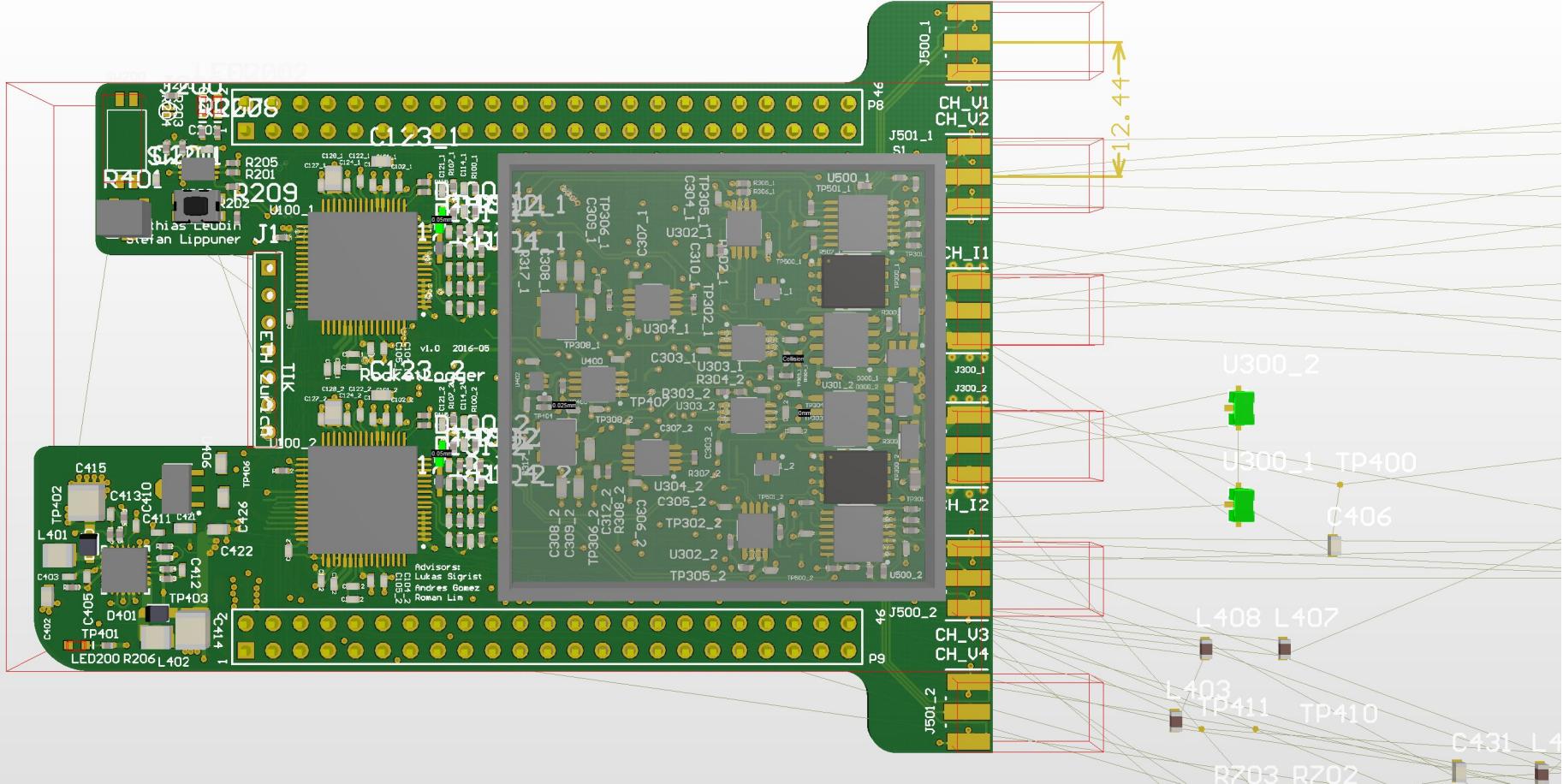
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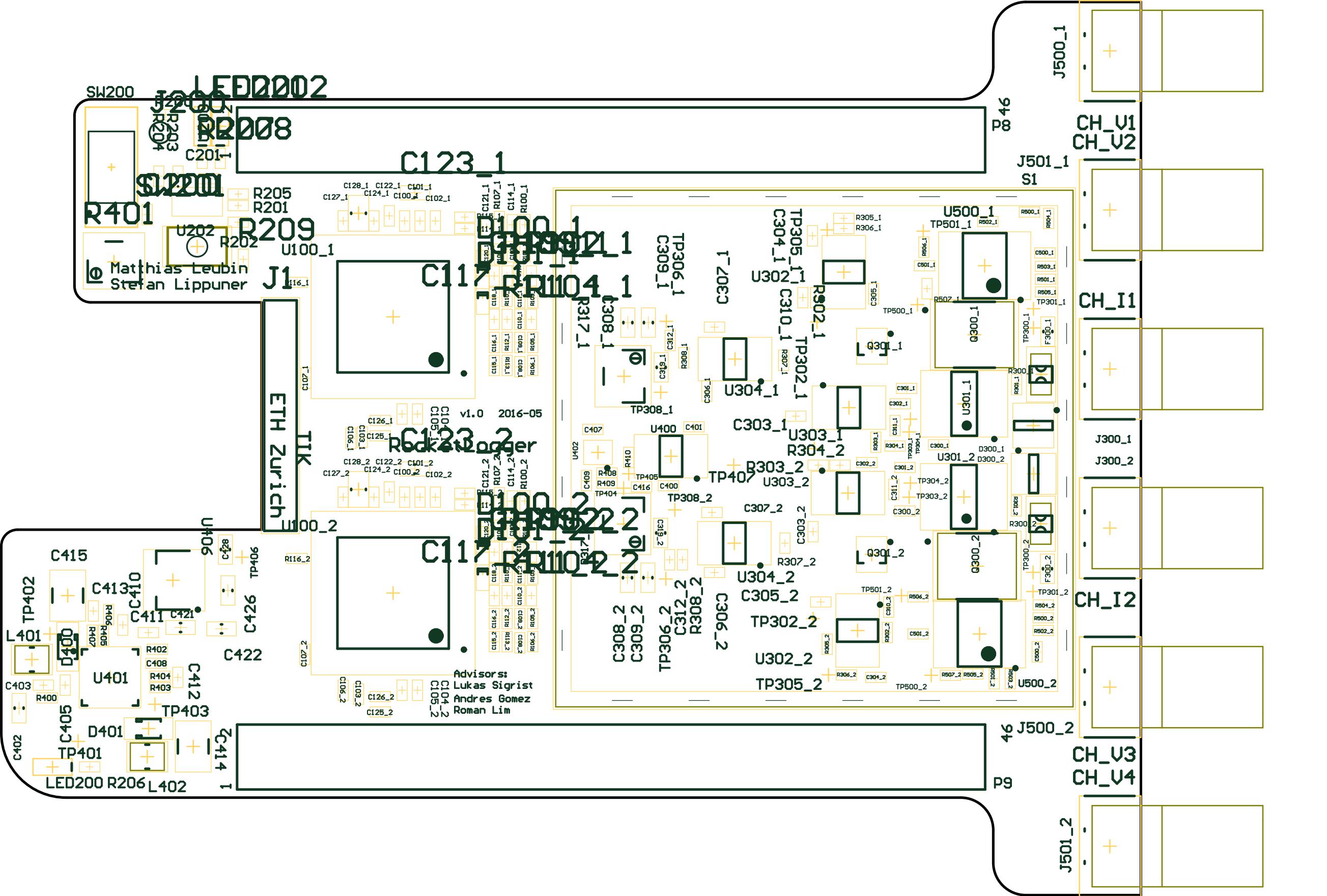
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Date:	21.09.2016	12:00:02		A4 Q	Drawn by:	Stefan Lippuner		
File:	C:\Users\user\Documents\RocketLogger\code\pcb\Cape\range_valid_stretching.SchDoc							









U300_2

U300_1 TP400

C40

L408 L407

403
TP411 TP411

R703 R702

R701 R700

R603_3 C600_3 U600_3 R601_3
R602_3 R600_3

R603_2 C600_2 U600_2 R601_2
R602_2 R600_2

R603_1 C600_1 U600_1 R601_1
R602_1 R600_1

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