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1  /*****
2  MPLAB Harmony System Configuration Header
3
4  File Name:
5      system_config.h
6
7  Summary:
8      Build-time configuration header for the system defined by this MPLAB Harmony
9      project.
10
11  Description:
12      An MPLAB Project may have multiple configurations.  This file defines the
13      build-time options for a single configuration.
14
15  Remarks:
16      This configuration header must not define any prototypes or data
17      definitions (or include any files that do).  It only provides macro
18      definitions for build-time configuration options that are not instantiated
19      until used by another MPLAB Harmony module or application.
20
21      Created with MPLAB Harmony Version 2.06
22  *****/
23
24  // DOM-IGNORE-BEGIN
25  /*****
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27
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44  SUBSTITUTE GOODS, TECHNOLOGY, SERVICES, OR ANY CLAIMS BY THIRD PARTIES
45  (INCLUDING BUT NOT LIMITED TO ANY DEFENSE THEREOF), OR OTHER SIMILAR COSTS.
46  *****/
47  // DOM-IGNORE-END
48
49  #ifndef _SYSTEM_CONFIG_H
50  #define _SYSTEM_CONFIG_H
51
52  // ****
53  // ****
54  // Section: Included Files
55  // ****
56  // ****
57  /* This section Includes other configuration headers necessary to completely
58     define this configuration.
59  */
60
61
62  // DOM-IGNORE-BEGIN
63  #ifdef __cplusplus // Provide C++ Compatibility
64
65  extern "C" {
66
67  #endif
68  // DOM-IGNORE-END
69
70  // ****
71  // ****
72  // Section: System Service Configuration
73  // ****

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74 // *****
75 // *****
76 /* Common System Service Configuration Options
77 */
78 #define SYS_VERSION_STR          "2.06"
79 #define SYS_VERSION              20600
80
81 // *****
82 /* Clock System Service Configuration Options
83 */
84 #define SYS_CLK_FREQ              40000000ul
85 #define SYS_CLK_BUS_PERIPHERAL_1 40000000ul
86 #define SYS_CLK_UPLL_BEFORE_DIV2_FREQ 192000000ul
87 #define SYS_CLK_CONFIG_PRIMARY_XTAL 8000000ul
88 #define SYS_CLK_CONFIG_SECONDARY_XTAL 0ul
89
90 /** Ports System Service Configuration */
91 #define SYS_PORT_A_ANSEL          0xFFFFC
92 #define SYS_PORT_A_TRIS           0xFFFFC
93 #define SYS_PORT_A_LAT            0x0000
94 #define SYS_PORT_A_ODC            0x0000
95 #define SYS_PORT_A_CNPU           0x0000
96 #define SYS_PORT_A_CNPD           0x0000
97 #define SYS_PORT_A_CNEN           0x0000
98
99 #define SYS_PORT_B_ANSEL          0x000B
100 #define SYS_PORT_B_TRIS           0xB7FB
101 #define SYS_PORT_B_LAT            0x0000
102 #define SYS_PORT_B_ODC            0x0000
103 #define SYS_PORT_B_CNPU           0x0000
104 #define SYS_PORT_B_CNPD           0x0000
105 #define SYS_PORT_B_CNEN           0x0080
106
107
108 /** Interrupt System Service Configuration */
109 #define SYS_INT                    true
110
111 // *****
112 // *****
113 // Section: Driver Configuration
114 // *****
115 // *****
116 /** Timer Driver Configuration */
117 #define DRV_TMR_INTERRUPT_MODE      true
118
119 /** Timer Driver 0 Configuration */
120 #define DRV_TMR_PERIPHERAL_ID_IDX0  TMR_ID_1
121 #define DRV_TMR_INTERRUPT_SOURCE_IDX0 INT_SOURCE_TIMER_1
122 #define DRV_TMR_INTERRUPT_VECTOR_IDX0 INT_VECTOR_T1
123 #define DRV_TMR_ISR_VECTOR_IDX0      _TIMER_1_VECTOR
124 #define DRV_TMR_INTERRUPT_PRIORITY_IDX0 INT_PRIORITY_LEVEL1
125 #define DRV_TMR_INTERRUPT_SUB_PRIORITY_IDX0 INT_SUBPRIORITY_LEVEL0
126 #define DRV_TMR_CLOCK_SOURCE_IDX0    DRV_TMR_CLKSOURCE_INTERNAL
127 #define DRV_TMR_PRESCALE_IDX0        TMR_PRESCALE_VALUE_256
128 #define DRV_TMR_OPERATION_MODE_IDX0  DRV_TMR_OPERATION_MODE_16_BIT
129 #define DRV_TMR_ASYNC_WRITE_ENABLE_IDX0 false
130 #define DRV_TMR_POWER_STATE_IDX0
131
132 #define DRV_TMR_PERIPHERAL_ID_IDX1  TMR_ID_2
133 #define DRV_TMR_INTERRUPT_SOURCE_IDX1 INT_SOURCE_TIMER_2
134 #define DRV_TMR_INTERRUPT_VECTOR_IDX1 INT_VECTOR_T2
135 #define DRV_TMR_ISR_VECTOR_IDX1      _TIMER_2_VECTOR
136 #define DRV_TMR_INTERRUPT_PRIORITY_IDX1 INT_PRIORITY_LEVEL1
137 #define DRV_TMR_INTERRUPT_SUB_PRIORITY_IDX1 INT_SUBPRIORITY_LEVEL0
138 #define DRV_TMR_CLOCK_SOURCE_IDX1    DRV_TMR_CLKSOURCE_INTERNAL
139 #define DRV_TMR_PRESCALE_IDX1        TMR_PRESCALE_VALUE_256
140 #define DRV_TMR_OPERATION_MODE_IDX1  DRV_TMR_OPERATION_MODE_16_BIT
141
142 #define DRV_TMR_ASYNC_WRITE_ENABLE_IDX1 false
143 #define DRV_TMR_POWER_STATE_IDX1
144
145 // *****
146 /* USART Driver Configuration Options

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147 */
148 #define DRV_USART_INSTANCES_NUMBER 2
149 #define DRV_USART_CLIENTS_NUMBER 2
150 #define DRV_USART_INTERRUPT_MODE true
151 #define DRV_USART_BYTE_MODEL_SUPPORT true
152 #define DRV_USART_READ_WRITE_MODEL_SUPPORT false
153 #define DRV_USART_BUFFER_QUEUE_SUPPORT false
154
155 // *****
156 // *****
157 // Section: Middleware & Other Library Configuration
158 // *****
159 // *****
160
161
162
163 // *****
164 // *****
165 // Section: Application Configuration
166 // *****
167 // *****
168 /** Application Defined Pins */
169
170 /** Functions for Led_Sended pin */
171 #define Led_SendedToggle() PLIB_PORTS_PinToggle(PORTS_ID_0, PORT_CHANNEL_A,
PORTS_BIT_POS_0)
172 #define Led_SendedOn() PLIB_PORTS_PinSet(PORTS_ID_0, PORT_CHANNEL_A, PORTS_BIT_POS_0)
173 #define Led_SendedOff() PLIB_PORTS_PinClear(PORTS_ID_0, PORT_CHANNEL_A,
PORTS_BIT_POS_0)
174 #define Led_SendedStateGet() PLIB_PORTS_PinGetLatched(PORTS_ID_0, PORT_CHANNEL_A,
PORTS_BIT_POS_0)
175 #define Led_SendedStateSet(Value) PLIB_PORTS_PinWrite(PORTS_ID_0, PORT_CHANNEL_A,
PORTS_BIT_POS_0, Value)
176
177 /** Functions for Led_Ready pin */
178 #define Led_ReadyToggle() PLIB_PORTS_PinToggle(PORTS_ID_0, PORT_CHANNEL_A,
PORTS_BIT_POS_1)
179 #define Led_ReadyOn() PLIB_PORTS_PinSet(PORTS_ID_0, PORT_CHANNEL_A, PORTS_BIT_POS_1)
180 #define Led_ReadyOff() PLIB_PORTS_PinClear(PORTS_ID_0, PORT_CHANNEL_A,
PORTS_BIT_POS_1)
181 #define Led_ReadyStateGet() PLIB_PORTS_PinGetLatched(PORTS_ID_0, PORT_CHANNEL_A,
PORTS_BIT_POS_1)
182 #define Led_ReadyStateSet(Value) PLIB_PORTS_PinWrite(PORTS_ID_0, PORT_CHANNEL_A,
PORTS_BIT_POS_1, Value)
183
184 /** Functions for Rst pin */
185 #define RstToggle() PLIB_PORTS_PinToggle(PORTS_ID_0, PORT_CHANNEL_B, PORTS_BIT_POS_2)
186 #define RstOn() PLIB_PORTS_PinSet(PORTS_ID_0, PORT_CHANNEL_B, PORTS_BIT_POS_2)
187 #define RstOff() PLIB_PORTS_PinClear(PORTS_ID_0, PORT_CHANNEL_B, PORTS_BIT_POS_2)
188 #define RstStateGet() PLIB_PORTS_PinGetLatched(PORTS_ID_0, PORT_CHANNEL_B,
PORTS_BIT_POS_2)
189 #define RstStateSet(Value) PLIB_PORTS_PinWrite(PORTS_ID_0, PORT_CHANNEL_B,
PORTS_BIT_POS_2, Value)
190
191 /** Functions for Xbee_CON pin */
192 #define Xbee_CONToggle() PLIB_PORTS_PinToggle(PORTS_ID_0, PORT_CHANNEL_B,
PORTS_BIT_POS_11)
193 #define Xbee_CONOn() PLIB_PORTS_PinSet(PORTS_ID_0, PORT_CHANNEL_B, PORTS_BIT_POS_11)
194 #define Xbee_CONOff() PLIB_PORTS_PinClear(PORTS_ID_0, PORT_CHANNEL_B,
PORTS_BIT_POS_11)
195 #define Xbee_CONStateGet() PLIB_PORTS_PinGetLatched(PORTS_ID_0, PORT_CHANNEL_B,
PORTS_BIT_POS_11)
196 #define Xbee_CONStateSet(Value) PLIB_PORTS_PinWrite(PORTS_ID_0, PORT_CHANNEL_B,
PORTS_BIT_POS_11, Value)
197
198 /** Functions for Led_Link_Lost pin */
199 #define Led_Link_LostToggle() PLIB_PORTS_PinToggle(PORTS_ID_0, PORT_CHANNEL_B,
PORTS_BIT_POS_14)
200 #define Led_Link_LostOn() PLIB_PORTS_PinSet(PORTS_ID_0, PORT_CHANNEL_B,
PORTS_BIT_POS_14)
201 #define Led_Link_LostOff() PLIB_PORTS_PinClear(PORTS_ID_0, PORT_CHANNEL_B,
PORTS_BIT_POS_14)
202 #define Led_Link_LostStateGet() PLIB_PORTS_PinGetLatched(PORTS_ID_0, PORT_CHANNEL_B,

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203     PORTS_BIT_POS_14)
204     #define Led_Link_LostStateSet(Value) PLIB_PORTS_PinWrite(PORTS_ID_0, PORT_CHANNEL_B,
205     PORTS_BIT_POS_14, Value)
206
207     /** Functions for Button_Send pin */
208     #define Button_SendStateGet() PLIB_PORTS_PinGet(PORTS_ID_0, PORT_CHANNEL_B,
209     PORTS_BIT_POS_7)
210
211     /** Functions for Xbee_LINK pin */
212     #define Xbee_LINKStateGet() PLIB_PORTS_PinGet(PORTS_ID_0, PORT_CHANNEL_B,
213     PORTS_BIT_POS_12)
214
215     /** Application Instance 0 Configuration */
216
217     //DOM-IGNORE-BEGIN
218     #ifndef __cplusplus
219     }
220     #endif
221     //DOM-IGNORE-END
222
223     #endif // _SYSTEM_CONFIG_H
224     /*****
225     End of File
226     */
```