

SPST CMOS ANALOG SWITCHES

FEATURES

- 2-V to 12-V Single-Supply Operation
- Specified ON-State Resistance:
 - 15 Ω Max With 12-V Supply
 - 20 Ω Max With 5-V Supply
 - 50 Ω Max With 3.3-V Supply
- Specified Low OFF-Leakage Currents:
 - 1 nA at 25°C
 - 10 nA at 85°C
- Specified Low ON-Leakage Currents:
 - 1 nA at 25°C
 - 10 nA at 85°C
- Low Charge Injection: 11.5 pC (12-V Supply)
- Fast Switching Speed:
 - $t_{ON} = 80$ ns, $t_{OFF} = 50$ ns (12-V Supply)
- Break-Before-Make Operation ($t_{ON} > t_{OFF}$)
- TTL/CMOS-Logic Compatible With 5-V Supply

DESCRIPTION/ORDERING INFORMATION

The TS12A4514/TS12A4515 are single pole/single throw (SPST), low-voltage, single-supply CMOS analog switches, with very low switch ON-state resistance. The TS12A4514 is normally open (NO). The TS12A4515 is normally closed (NC).

These CMOS switches can operate continuously with a single supply between 2 V and 12 V. Each switch can handle rail-to-rail analog signals. The OFF-leakage current maximum is only 1 nA at 25°C or 10 nA at 85°C.

All digital inputs have 0.8-V to 2.4-V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a 5-V supply.

For pin-compatible parts for use with dual supplies, see the TS12A4516/TS12A4517.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
–40°C to 85°C	PDIP – P	Reel of 1000	TS12A4514P	TS12A4514P
	SOIC – D	Reel of 1500	TS12A4514D	YD514
		Reel of 2500	TS12A4514DR	
	SOP (SOT-23) – DBV	Reel of 3000	TS12A4514DBVR	9CJ_
	PDIP – P	Reel of 1000	TS12A4515P	TS12A4515P
	SOIC – D	Reel of 1500	TS12A4515D	YD515
		Reel of 2500	TS12A4515DR	
	SOP (SOT-23) – DBV	Reel of 3000	TS12A4515DBVR	9CK_

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

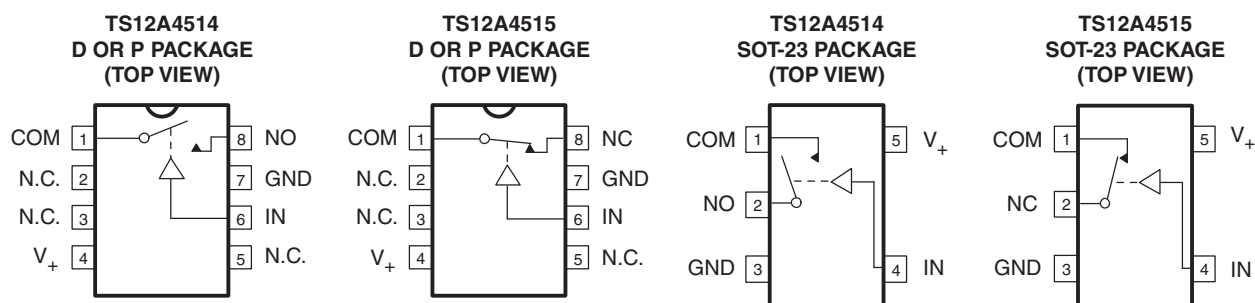
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(3) DBV: The last character designates assembly/test Site




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PIN CONFIGURATIONS



INPUT	SWITCH STATE	
	TS12A4514	TS12A4515
LOW	OFF	ON
HIGH	ON	OFF

MARKING INFORMATION (SOTs only)	
	LOT SPECIFIC CODE
	AE = TS12A4514
	AF = TS12A4515

N.C. – Not internally connected

NO – Normally open

NC – Normally closed

Absolute Minimum and Maximum Ratings⁽¹⁾⁽²⁾

voltages referenced to GND

		MIN	MAX	UNIT
V ₊	Supply voltage range ⁽³⁾	–0.3	13	V
V _{NC} V _{NO} V _{COM}	Analog voltage range ⁽⁴⁾	–0.3	V ₊ + 0.3 or ±20 mA	V
	Continuous current into any terminal		±20	mA
	Peak current, NO or COM (pulsed at 1 ms, 10% duty cycle)		±30	mA
	ESD per method 3015.7		>2000	V
T _A	Continuous power dissipation (T _A = 70°C)	8-pin plastic DIP (derate 9.09 mW/°C above 70°C)		727
		8-pin SOIC (derate 5.88 mW/°C above 70°C)		471
		5-pin SOT-23 (derate 7.1 mW/°C above 70°C)		571
T _A	Operating temperature range	–40	85	°C
T _{stg}	Storage temperature range	–65	150	°C
	Lead temperature (soldering, 10 s)		300	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) Voltages exceeding V₊ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Electrical Characteristics for 5-V Supply⁽¹⁾

 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$, $V_{INH} = 2.4 \text{ V}$, $V_{INL} = 0.8 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A	MIN	TYP ⁽²⁾	MAX	UNIT
Analog Switch							
Analog signal range	V _{COM} , V _{NO} , V _{NC}			0		V ₊	V
ON-state resistance	r _{on}	V ₊ = 4.5 V, V _{COM} = 3.5 V, I _{COM} = 1 mA	25°C	9.5	15	Ω	
			Full		20		
ON-state resistance flatness	r _{on(flat)}	V _{COM} = 1 V, 2 V, 3 V, I _{COM} = 1 mA	25°C	1	3	Ω	
			Full		4		
NO, NC OFF leakage current ⁽³⁾	I _{NO(OFF)} , I _{NC(OFF)}	V ₊ = 5.5 V, V _{COM} = 1 V, V _{NO} or V _{NC} = 4.5 V	25°C		1	nA	
			Full		10		
COM OFF leakage current ⁽³⁾	I _{COM(OFF)}	V ₊ = 5.5 V, V _{COM} = 1 V, V _{NO} or V _{NC} = 4.5 V	25°C		1	nA	
			Full		10		
COM ON leakage current ⁽³⁾	I _{COM(ON)}	V ₊ = 5.5 V, V _{COM} = 4.5 V, V _{NO} or V _{NC} = 4.5 V	25°C		1	nA	
			Full		10		
Digital Control Input (IN)							
Input logic high	V _{IH}		Full	2.4		V ₊	V
Input logic low	V _{IL}		Full	0		0.8	V
Input leakage current	I _{IH} , I _{IL}	V _{IN} = V ₊ , 0 V	Full			0.01	μA
Dynamic							
Turn-on time	t _{ON}	see Figure 2	25°C	32	100	ns	
			Full		125		
Turn-off time	t _{OFF}	see Figure 2	25°C	25	50	ns	
			Full		60		
Charge injection ⁽⁴⁾	Q _C	C _L = 1 nF, V _{NO} = 0 V, R _S = 0 Ω, See Figure 1	25°C		–3		pC
NO, NC OFF capacitance	C _{NO(OFF)} , C _{NC(OFF)}	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM OFF capacitance	C _{COM(OFF)}	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM ON capacitance	C _{COM(ON)}	f = 1 MHz, See Figure 4	25°C		19		pF
Digital input capacitance	C _I	V _{IN} = V ₊ , 0 V	25°C		1.5		pF
Bandwidth	BW	R _L = 50 Ω, C _L = 15 pF, V _{NO} = 1 V _{RMS} , f = 100 kHz	25°C		475		MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, C _L = 15 pF, V _{NO} = 1 V _{RMS} , f = 100 kHz	25°C		–94		dB
Total harmonic distortion	THD	R _L = 50 Ω, C _L = 15 pF, V _{NO} = 1 V _{RMS} , f = 100 kHz	25°C		0.08		%
Supply							
V ₊ supply current	I ₊	V _{IN} = 0 V or V ₊	25°C		0.05	μA	
			Full		0.1		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) Typical values are at $T_A = 25^\circ\text{C}$.

(3) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C .

(4) Specified by design, not production tested

Electrical Characteristics for 12-V Supply⁽¹⁾
 $V_+ = 11.4\text{ V to }12.6\text{ V}$, $V_{\text{INH}} = 5\text{ V}$, $V_{\text{INL}} = 0.8\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A	MIN	TYP ⁽²⁾	MAX	UNIT
Analog Switch							
Analog signal range	V _{COM} , V _{NO} , V _{NC}			0		V ₊	V
ON-state resistance	r _{on}	V ₊ = 11.4 V, V _{COM} = 10 V, I _{COM} = 1 mA	25°C		6.5	10	Ω
			Full			15	
ON-state resistance flatness	r _{on(flat)}	V ₊ = 11.4 V, V _{COM} = 2 V, 5 V, 10 V, I _{COM} = 1 mA	25°C		1.5	3	Ω
			Full			4	
NO, NC OFF leakage current ⁽³⁾	I _{NO(OFF)} , I _{NC(OFF)}	V ₊ = 12.6 V, V _{COM} = 1 V, V _{NO} or V _{NC} = 10 V	25°C			1	nA
			Full			10	
COM OFF leakage current ⁽³⁾	I _{COM(OFF)}	V ₊ = 12.6 V, V _{COM} = 1 V, V _{NO} or V _{NC} = 10 V	25°C			1	nA
			Full			10	
COM ON leakage current ⁽³⁾	I _{COM(ON)}	V ₊ = 12.6 V, V _{COM} = 10 V, V _{NO} or V _{NC} = 10 V	25°C			1	nA
			Full			10	
Digital Control Input (IN)							
Input logic high	V _{IH}		Full	5		V ₊	V
Input logic low	V _{IL}		Full	0		0.8	V
Input leakage current	I _{IH} , I _{IL}	V _{IN} = V ₊ , 0 V	Full			0.01	μA
Dynamic							
Turn-on time	t _{ON}	See Figure 2	25°C		22	75	ns
			Full			80	
Turn-off time	t _{OFF}	See Figure 2	25°C		20	45	ns
			Full			50	
Charge injection ⁽⁴⁾	Q _C	C _L = 1 nF, V _{NO} = 0 V, R _S = 0 Ω, See Figure 1	25°C		−11.5		pC
NO, NC OFF capacitance	C _{NO(OFF)} C _{NC(OFF)}	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM OFF capacitance	C _{COM(OFF)}	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM ON capacitance	C _{COM(ON)}	f = 1 MHz, See Figure 4	25°C		21.5		pF
Digital input capacitance	C _I	V _{IN} = V ₊ , 0 V	25°C		1.5		pF
Bandwidth	BW	R _L = 50 Ω, C _L = 15 pF, V _{NO} = 1 V _{RMS} , f = 100 kHz	25°C		520		MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, C _L = 15 pF, V _{NO} = 1 V _{RMS} , f = 100 kHz	25°C		−95		dB
Total harmonic distortion	THD	R _L = 50 Ω, C _L = 15 pF, V _{NO} = 1 V _{RMS} , f = 100 kHz	25°C		0.07		%
Supply							
V ₊ supply current	I ₊	V _{IN} = 0 V or V ₊	25°C			0.05	μA
			Full			0.2	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) Typical values are at $T_A = 25^\circ\text{C}$.(3) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C .

(4) Specified by design, not production tested

Electrical Characteristics for 3-V Supply⁽¹⁾

 $V_+ = 3\text{ V}$ to 3.6 V , $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A	MIN	TYP ⁽²⁾	MAX	UNIT
Analog Switch							
Analog signal range	V _{COM} , V _{NO} , V _{NC}			0		V ₊	V
ON-state resistance	r _{on}	V ₊ = 3 V, V _{COM} = 1.5 V, I _{NO} = 1 mA,	25°C		18.5	40	Ω
			Full			50	
ON-state resistance flatness	r _{on(flat)}	V ₊ = 3 V, V _{COM} = 1 V, 1.5 V, 2 V, I _{COM} = 1 mA	25°C		1	3	Ω
			Full			4	
NO, NC OFF leakage current ⁽³⁾	I _{NO(OFF)} , I _{NC(OFF)}	V ₊ = 3.6 V, V _{COM} = 1 V, V _{NO} or V _{NC} = 3 V	25°C			1	nA
			Full			10	
COM OFF leakage current ⁽³⁾	I _{COM(OFF)}	V ₊ = 3.6 V, V _{COM} = 1 V, V _{NO} or V _{NC} = 3 V	25°C			1	nA
			Full			10	
COM ON leakage current ⁽³⁾	I _{COM(ON)}	V ₊ = 3.6 V, V _{COM} = 3 V, V _{NO} or V _{NC} = 3 V	25°C			1	nA
			Full			10	
Digital Control Input (IN)							
Input logic high	V _{IH}		Full	2.4		V ₊	V
Input logic low	V _{IL}		Full	0		0.8	V
Input leakage current	I _{IH} , I _{IL}	V _{IN} = V ₊ , 0 V	Full			0.01	μA
Dynamic							
Turn-on time ⁽⁴⁾	t _{ON}	See Figure 2	25°C		63	120	ns
			Full			175	
Turn-off time ⁽⁴⁾	t _{OFF}	See Figure 2	25°C		33	80	ns
			Full			120	
Charge injection ⁽⁴⁾	Q _C	C _L = 1 nF, See Figure 1	25°C		−1.5		pC
NO, NC OFF capacitance	C _{NO(OFF)} , C _{NC(OFF)}	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM OFF capacitance	C _{COM(OFF)}	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM ON capacitance	C _{COM(ON)}	f = 1 MHz, See Figure 4	25°C		17		pF
Digital input capacitance	C _I	V _{IN} = V ₊ , 0 V	25°C		1.5		pF
Bandwidth	BW	R _L = 50 Ω, C _L = 15 pF, V _{NO} = 1 V _{RMS} , f = 100 kHz	25°C		460		MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, C _L = 15 pF, V _{NO} = 1 V _{RMS} , f = 100 kHz	25°C		−94		dB
Total harmonic distortion	THD	R _L = 50 Ω, C _L = 15 pF, V _{NO} = 1 V _{RMS} , f = 100 kHz	25°C		0.15		%
Supply							
V ₊ supply current	I ₊	V _{IN} = 0 V or V ₊	25°C			0.03	μA
			Full			0.05	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) Typical values are at $T_A = 25^\circ\text{C}$.

(3) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C .

(4) Specified by design, not production tested

PIN DESCRIPTION⁽¹⁾

PIN NO.				NAME	DESCRIPTION
TS12A4514		TS12A4515			
D, P	SOT-23	D, P	SOT-23		
1	1	1	1	COM	Common
2, 3, 5	—	2, 3, 5	—	N.C.	No connect (not internally connected)
4	5	4	5	V ₊	Power supply
6	4	6	4	IN	Digital control to connect COM to NO or NC
7	3	7	3	GND	Digital ground
8	2	—	—	NO	Normally open
—	—	8	2	NC	Normally closed

(1) NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass in both directions.

APPLICATION INFORMATION

Power-Supply Considerations

The TS12A4514/TS12A4515 construction is typical of most CMOS analog switches, except that they have only two supply pins: V_+ and GND. V_+ and GND drive the internal CMOS switches and set their analog voltage limits. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V_+ and GND. One of these diodes conducts if any analog signal exceeds V_+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V_+ or GND. Although the ESD diodes on a given signal pin are identical and, therefore, fairly well balanced, they are reverse biased differently. Each is biased by either V_+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V_+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no connection between the analog-signal paths and V_+ or GND.

V_+ and GND also power the internal logic and logic-level translators. The logic-level translators convert the logic levels to switched V_+ and GND signals to drive the analog signal gates.

Logic-Level Thresholds

The logic-level thresholds are CMOS/TTL compatible when V_+ is 5 V. As V_+ is raised, the level threshold increases slightly. When V_+ reaches 12 V, the level threshold is about 3 V – above the TTL-specified high-level minimum of 2.8 V, but still compatible with CMOS outputs.

CAUTION:

If the user is using the TS12A4514 or TS12A4515 with a V_+ supply of 3 V, then the control input (IN) voltage should not exceed V_+ , otherwise the output levels can exceed 3 V and violate the absolute maximum rating, potentially damaging the device.

High-Frequency Performance

In 50- Ω systems, signal response is reasonably flat up to 250 MHz (see *Typical Operating Characteristics*). Above 20 MHz, the on response has several minor peaks that are highly layout dependent. The problem is not in turning the switch on; it is turning it off. The OFF-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10 MHz, OFF isolation is about –45 dB in 50- Ω systems, decreasing (approximately 20 dB per decade) as frequency increases. Higher circuit impedances also make OFF isolation decrease. OFF isolation is about 3 dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Test Circuits/Timing Diagrams

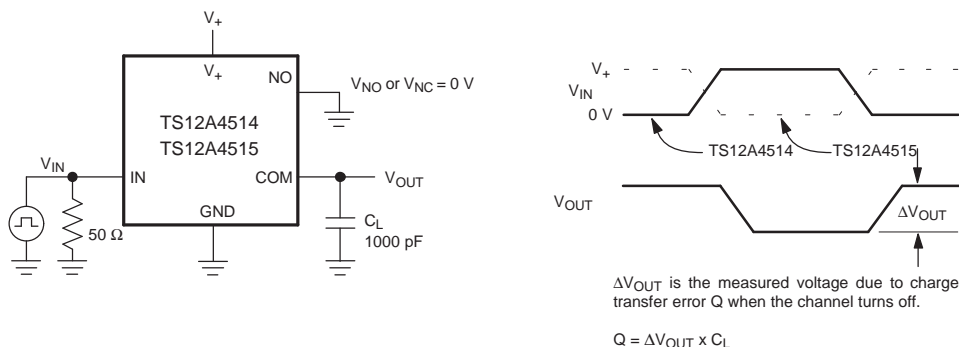


Figure 1. Charge Injection

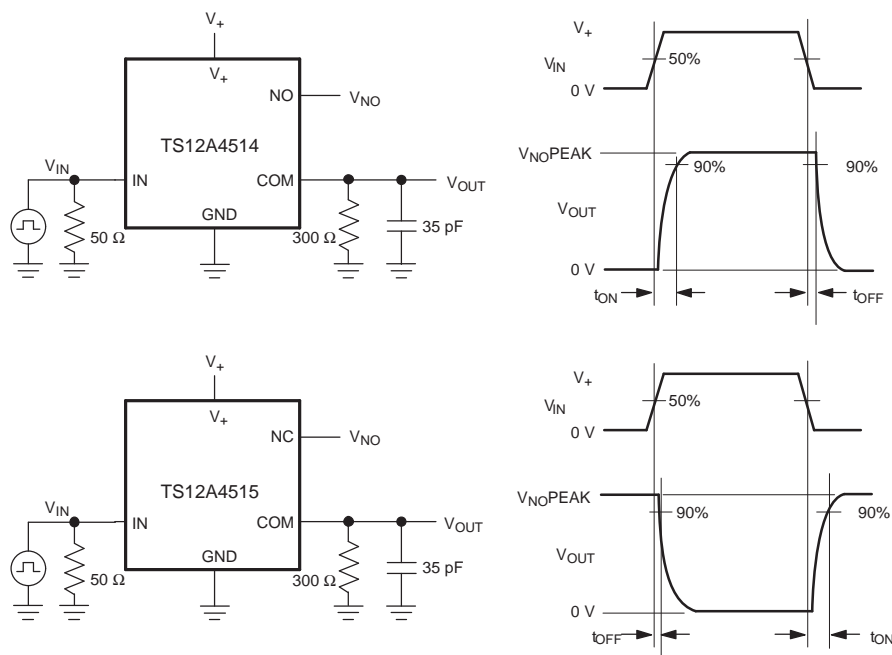
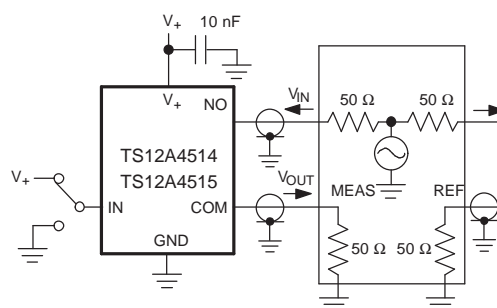


Figure 2. Switching Times



Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. ON loss is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

$$\text{OFF Isolation} = 20 \log \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

$$\text{ON Loss} = 20 \log \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

Figure 3. OFF Isolation and ON Loss

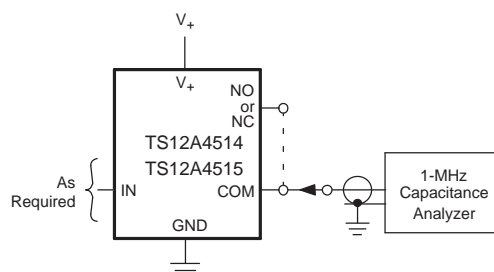


Figure 4. NO, NC, and COM Capacitance

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS12A4514D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD514	Samples
TS12A4514DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	9CJE	Samples
TS12A4514DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD514	Samples
TS12A4514P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TS12A4514P	Samples
TS12A4515D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD515	Samples
TS12A4515DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	9CKE	Samples
TS12A4515DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD515	Samples
TS12A4515DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD515	Samples
TS12A4515P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TS12A4515P	Samples
TS12A4515PE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TS12A4515P	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

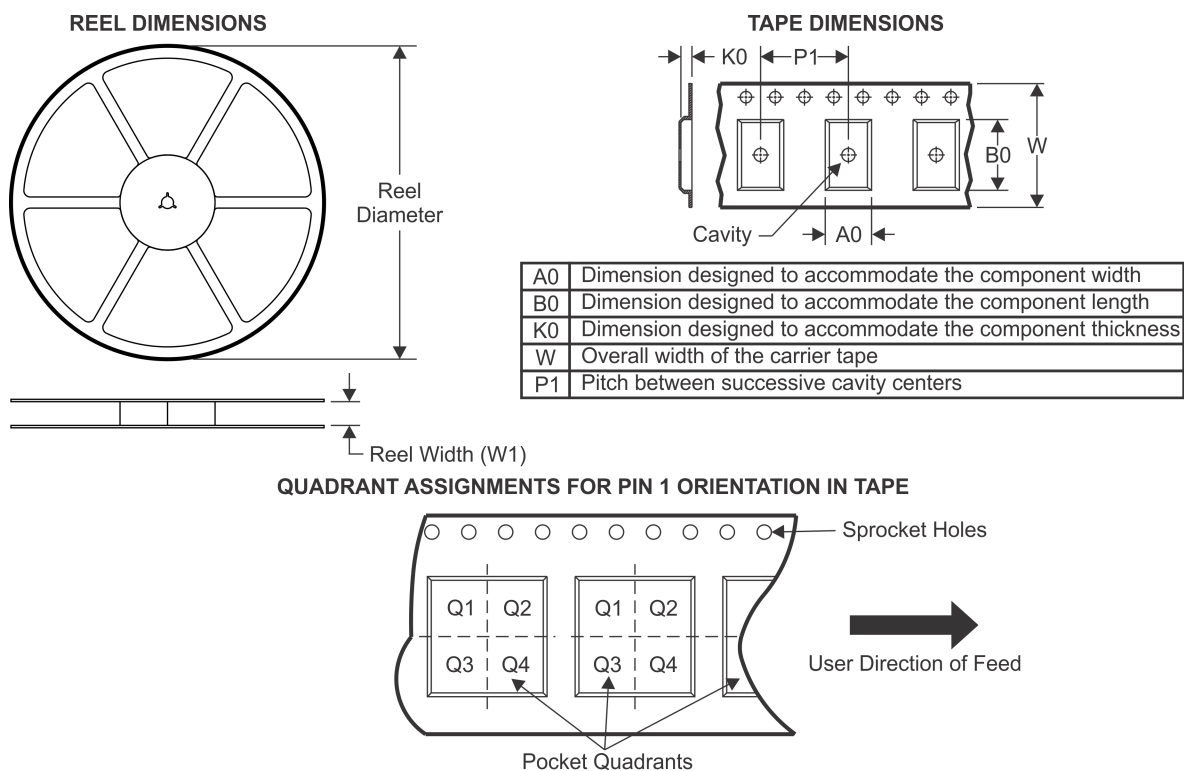
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

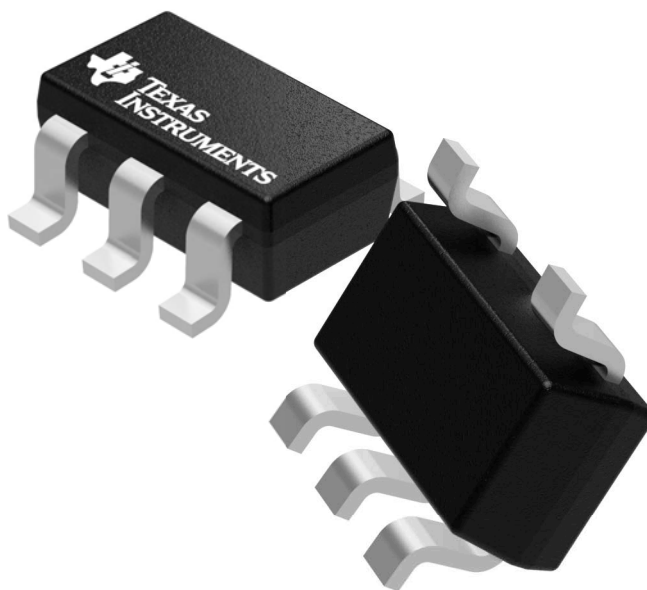
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS12A4514DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TS12A4514DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TS12A4515DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TS12A4515DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS12A4514DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TS12A4514DR	SOIC	D	8	2500	367.0	367.0	35.0
TS12A4515DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TS12A4515DR	SOIC	D	8	2500	367.0	367.0	35.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

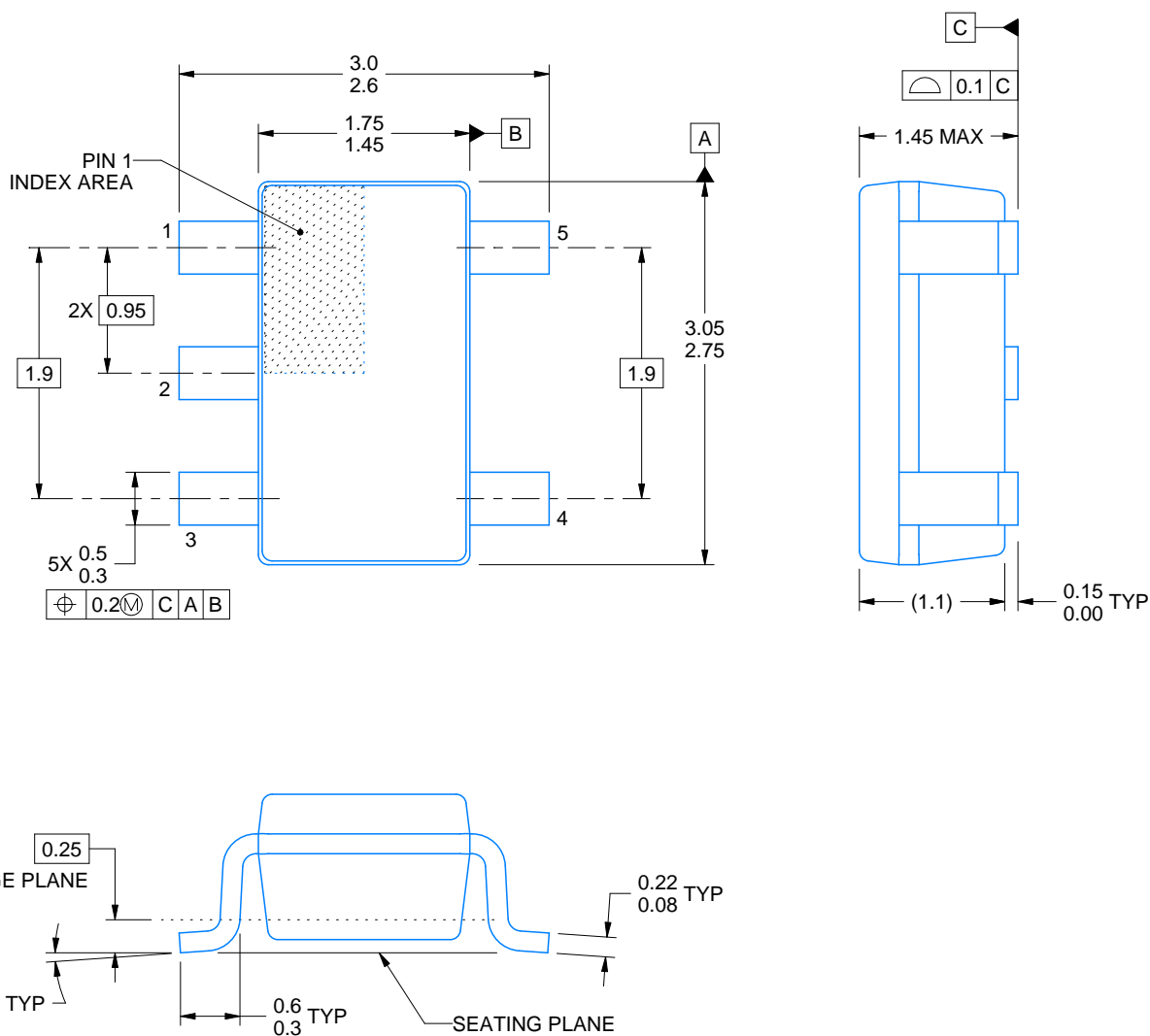


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

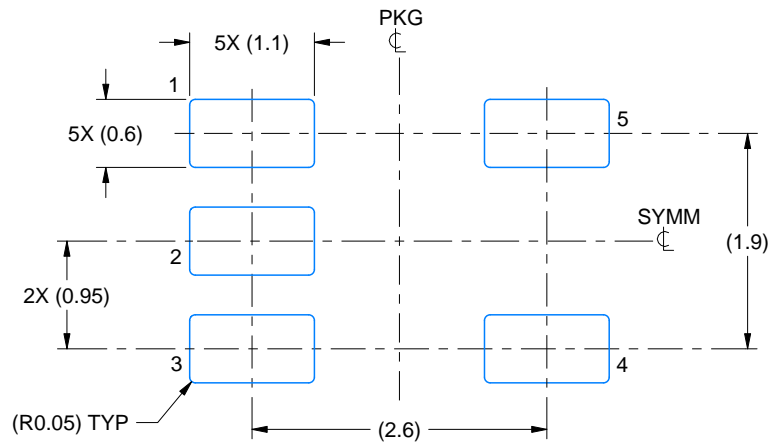
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

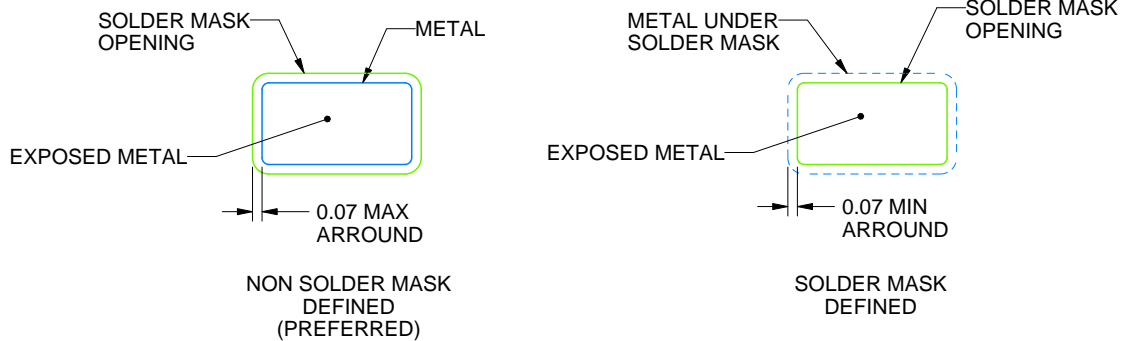
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

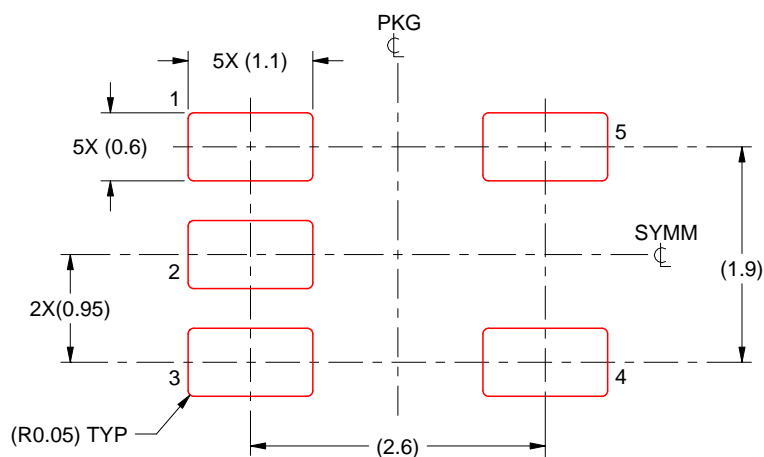
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

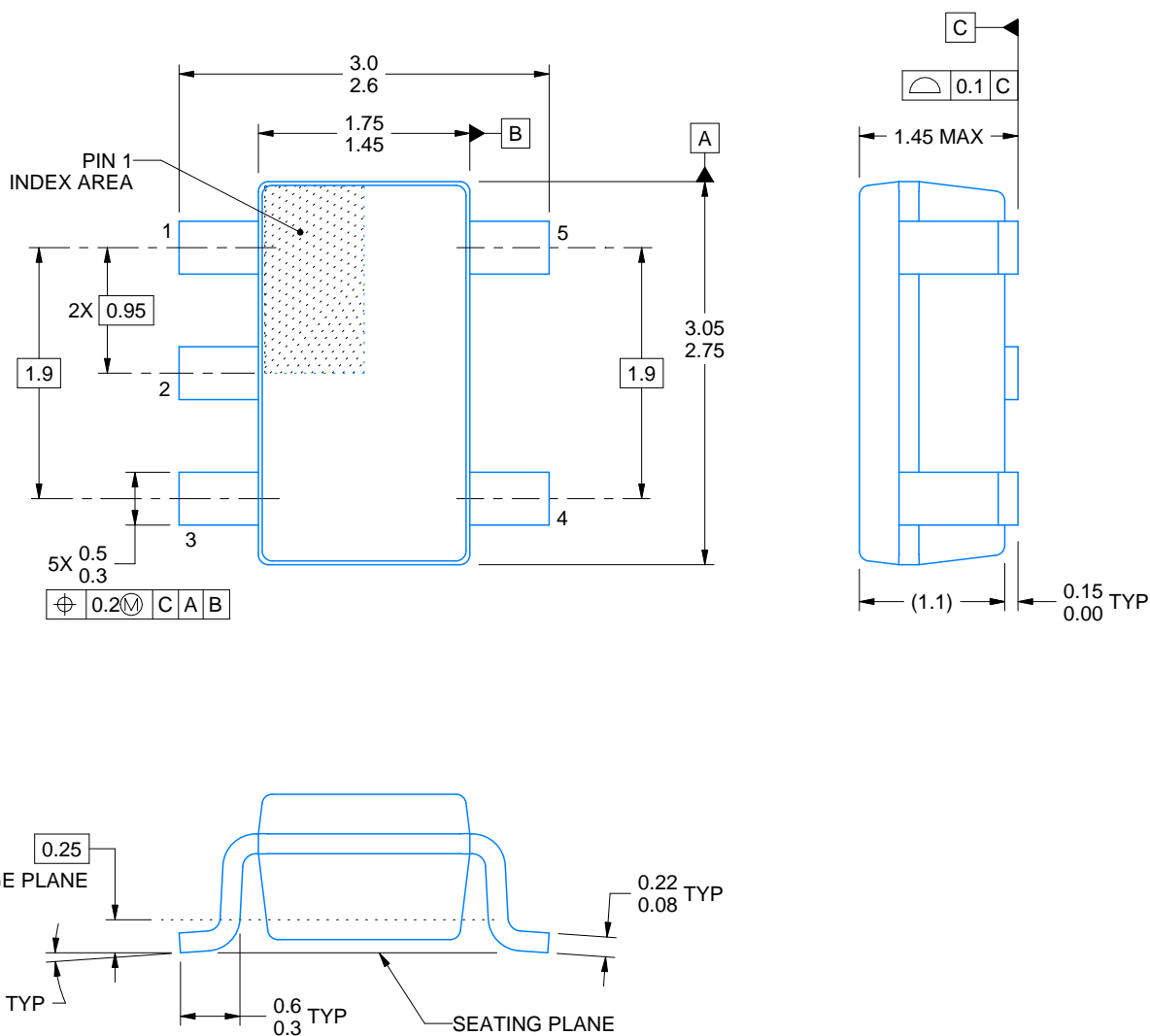


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

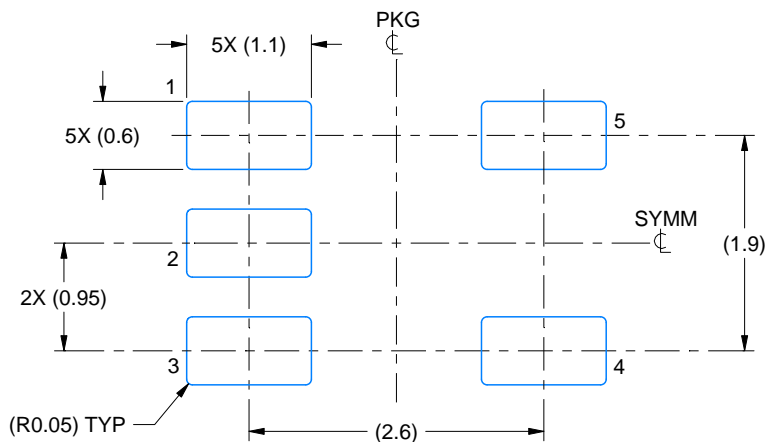
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

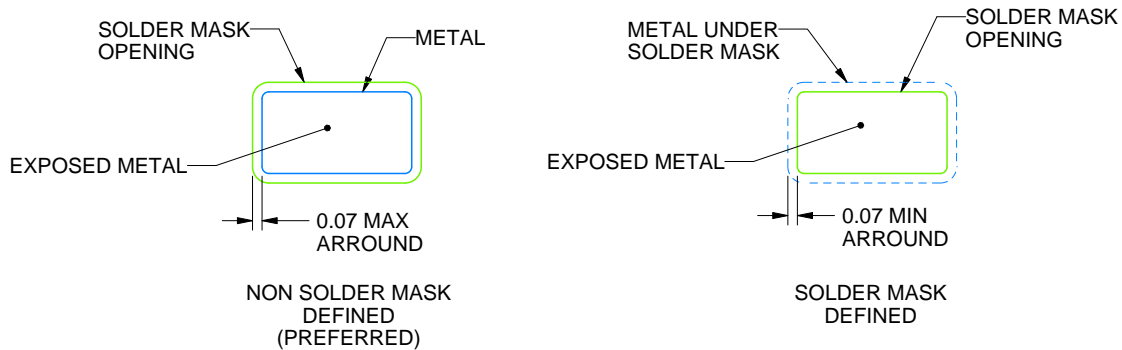
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

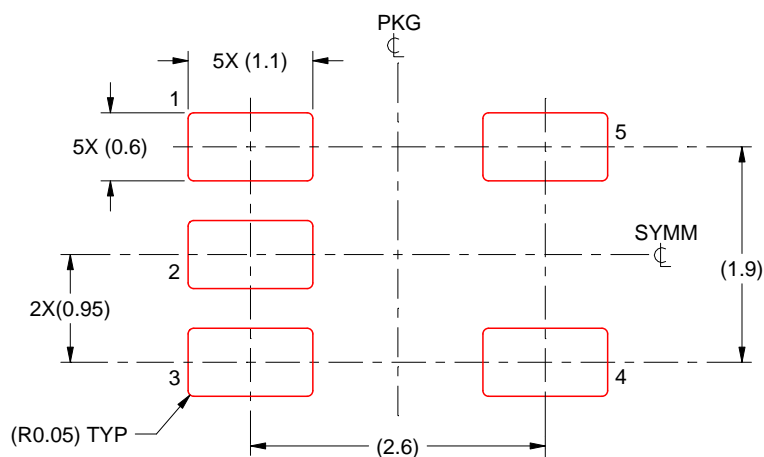
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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