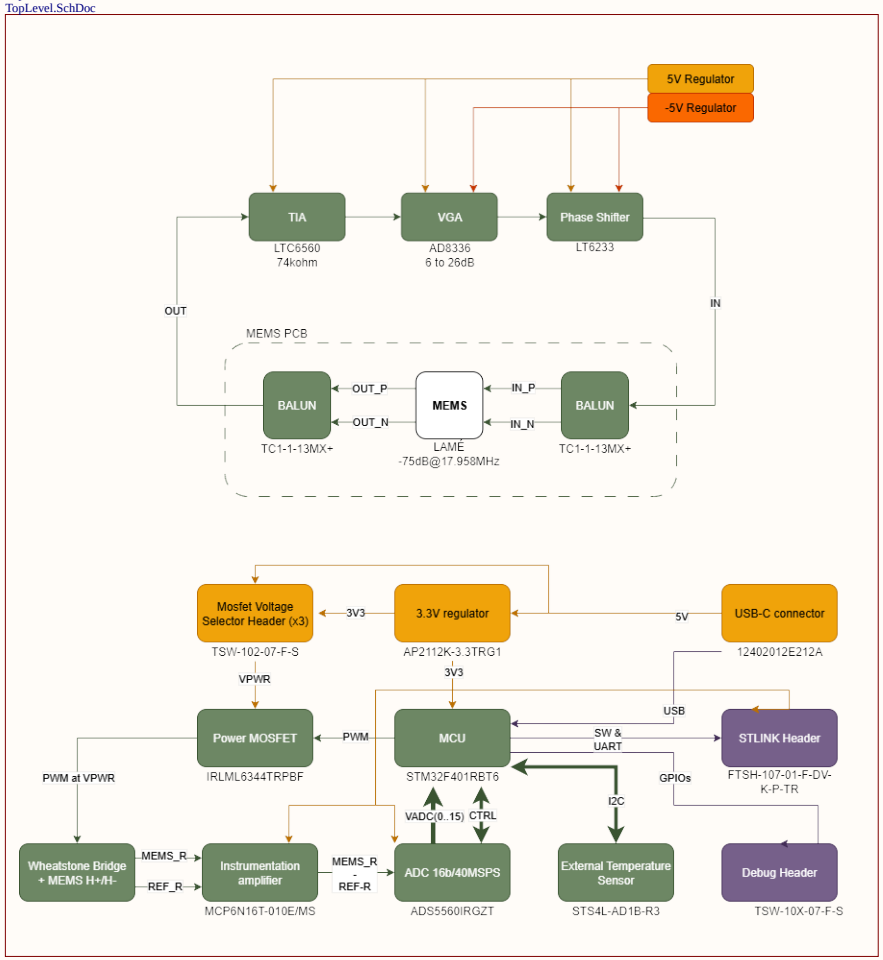
Conditioning and TLL PCB

Top Level
TopLevel.SchDoc



Revision	Description	Date
A	- Initial project	XXX
B	- Correctives: Added voltage, translators, 7 segments, etc.	XXX
C	- Single board conditioning & TLL	Aug 2025

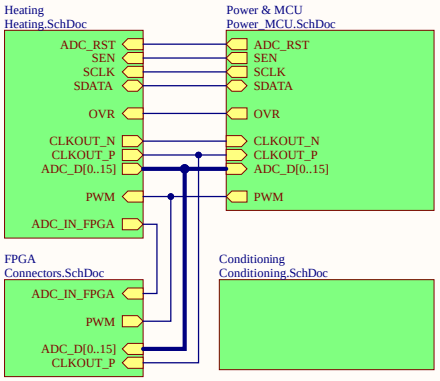
ÉTS

Project: *Conditioning & TLL PCB*

Date: 9/16/2025	Revision:C
File: FrontPage.SchDoc	Sheet 1 of 6

Designed By : Alexis Gagnon
Megane Cyr

Top Level



Project: ***Conditioning & TLL PCB***

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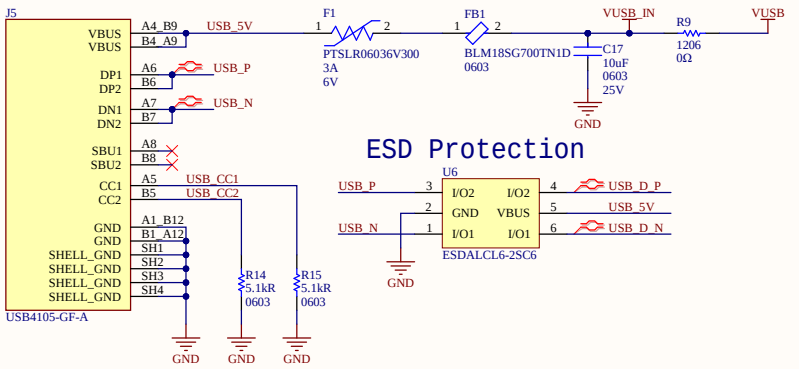
Designed By : Alexis Gagnon
Megane Cyr

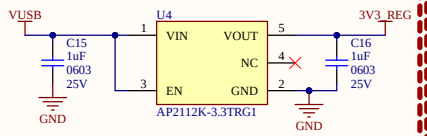
Power & MCU

USB-C Power & Data

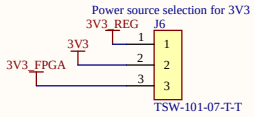


ESD Protection

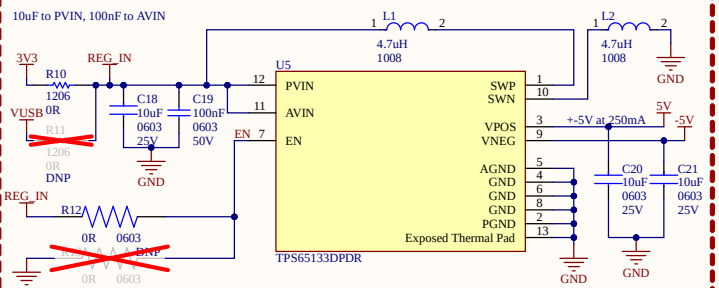
3V3 Regulator



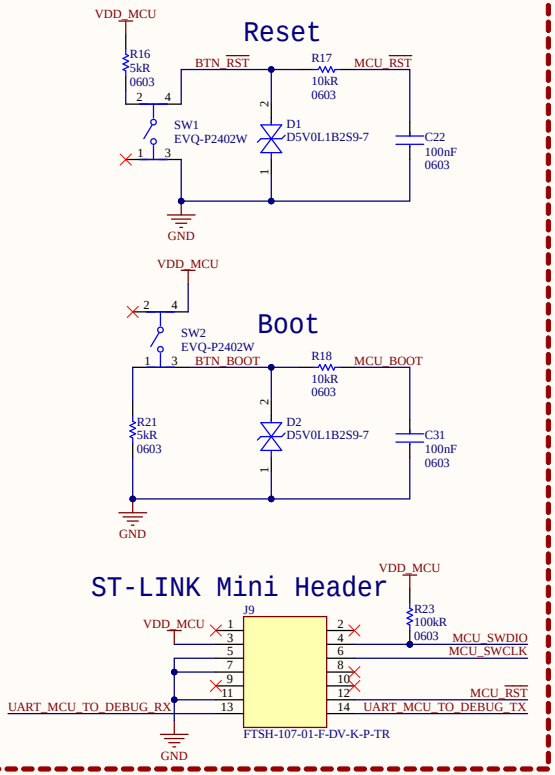
Power source selection for 3V3



+/-5V Regulator

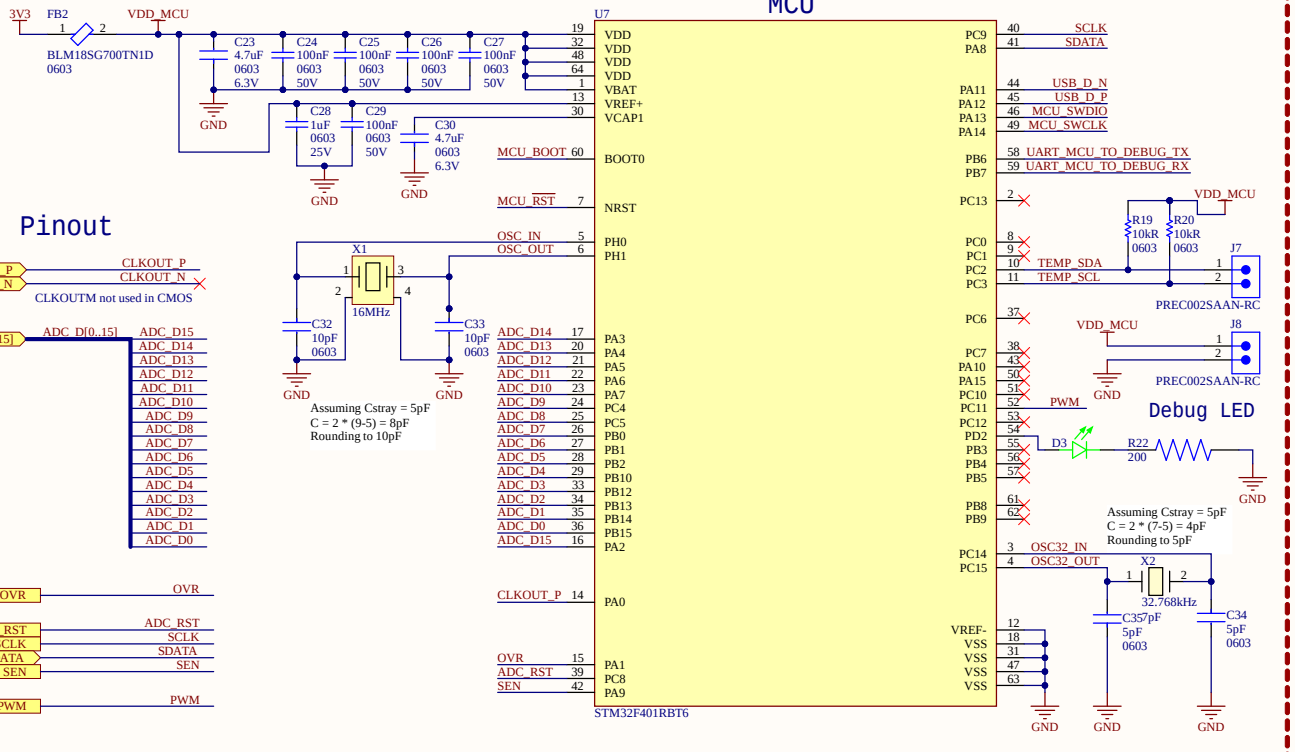


Buttons & ST-LINK Header



MCU & Pinout

MCU



Pinout

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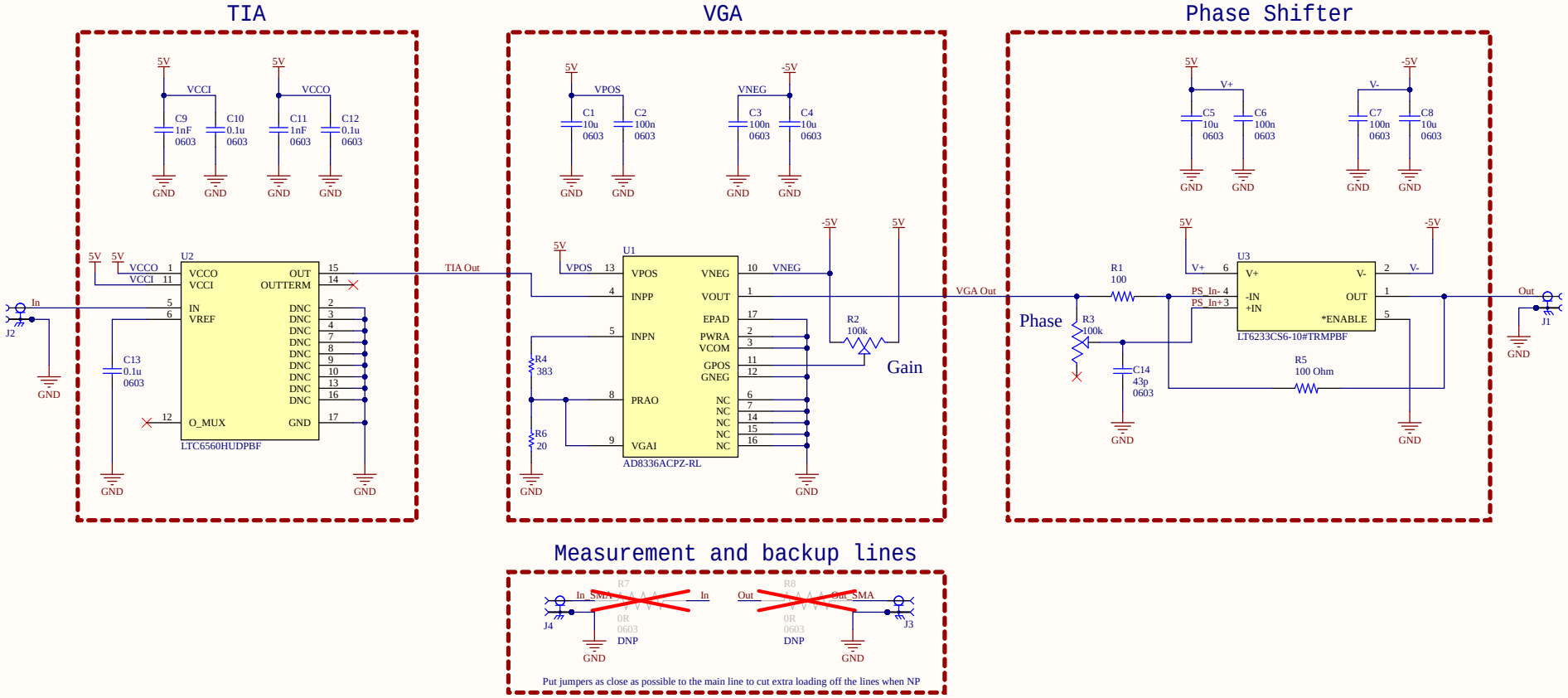
Designed By : Alexis Gagnon
Megane Cyr

Conditioning



Measurement and backup lines

Project:	**Conditioning & TLL PCB**
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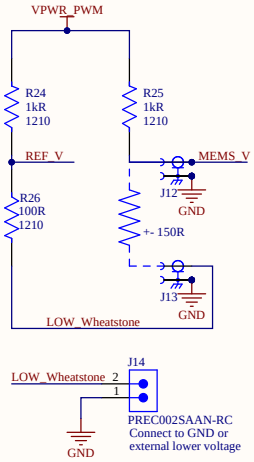
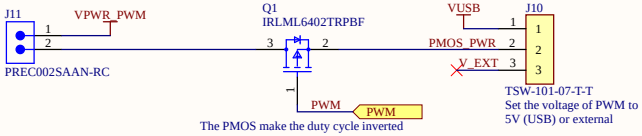
Heating

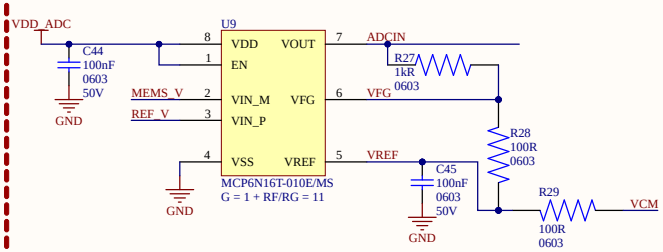
Wheatstone Bridge



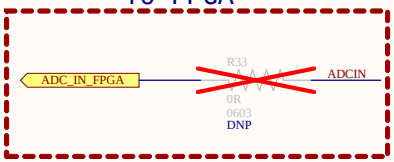
PWM Voltage



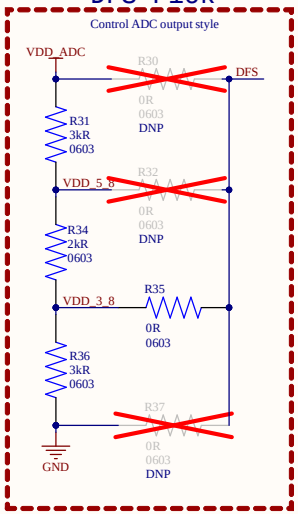
Instrumentation Amplifier



To FPGA

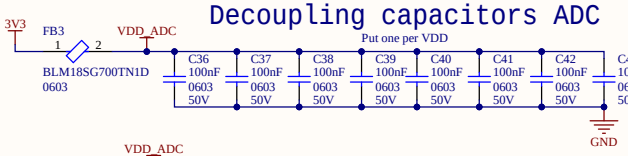


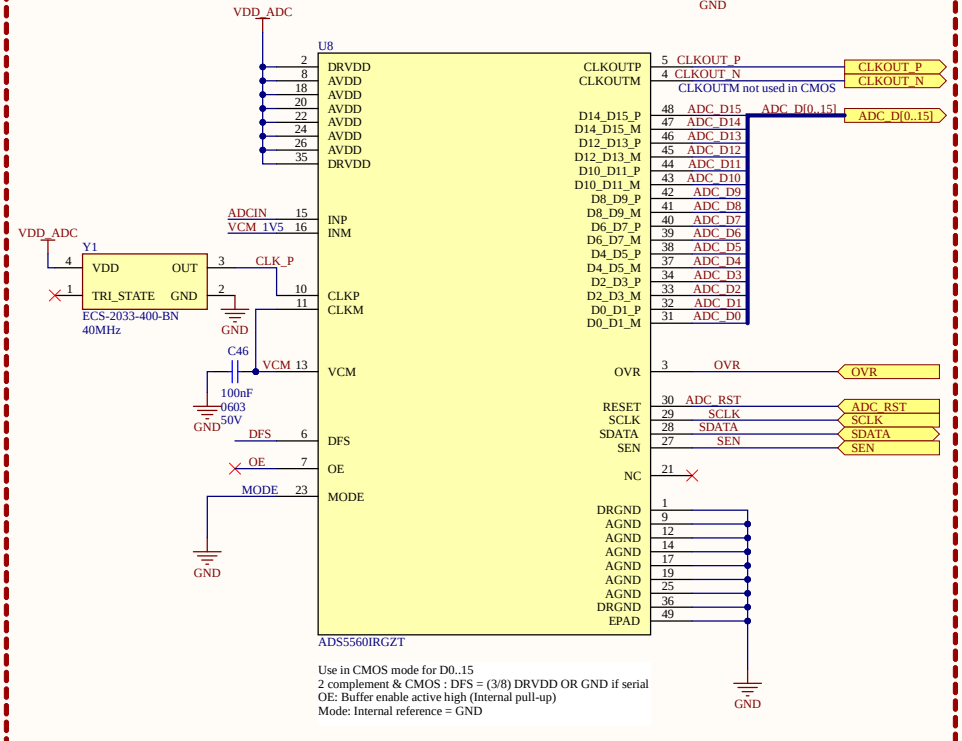
DFS Pick



16 bits ADC

Decoupling capacitors ADC





Project: Conditionning & TLL PCB
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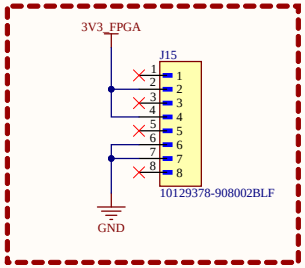
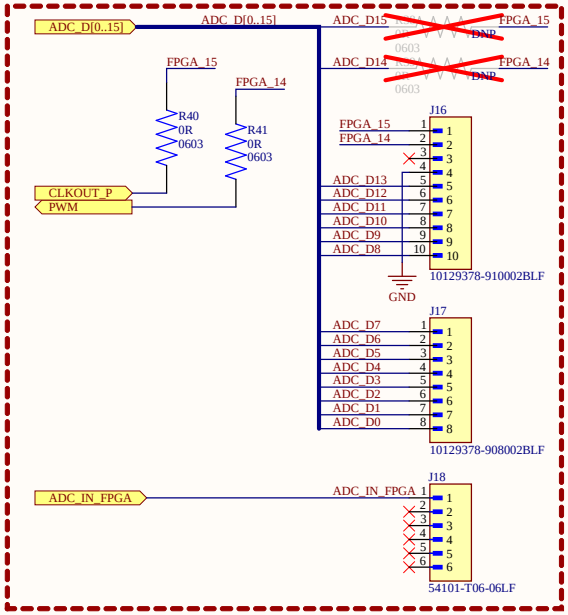
Megane Cyr

Connectors

FPGA Header - Power



FPGA Header - ADC



Project: ***Conditionning & TLL PCB***

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Designed By : Alexis Gagnon
Megane Cyr