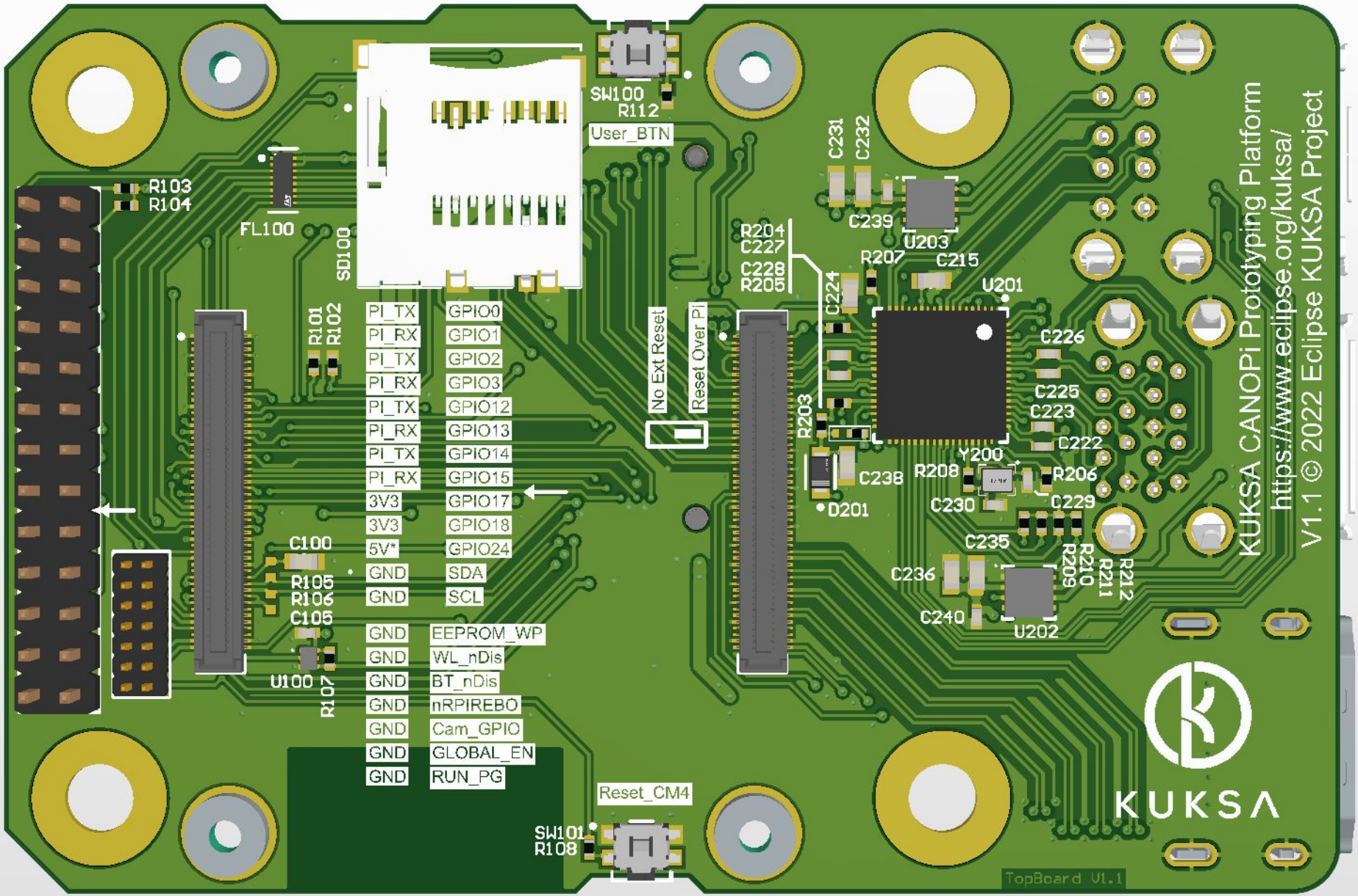
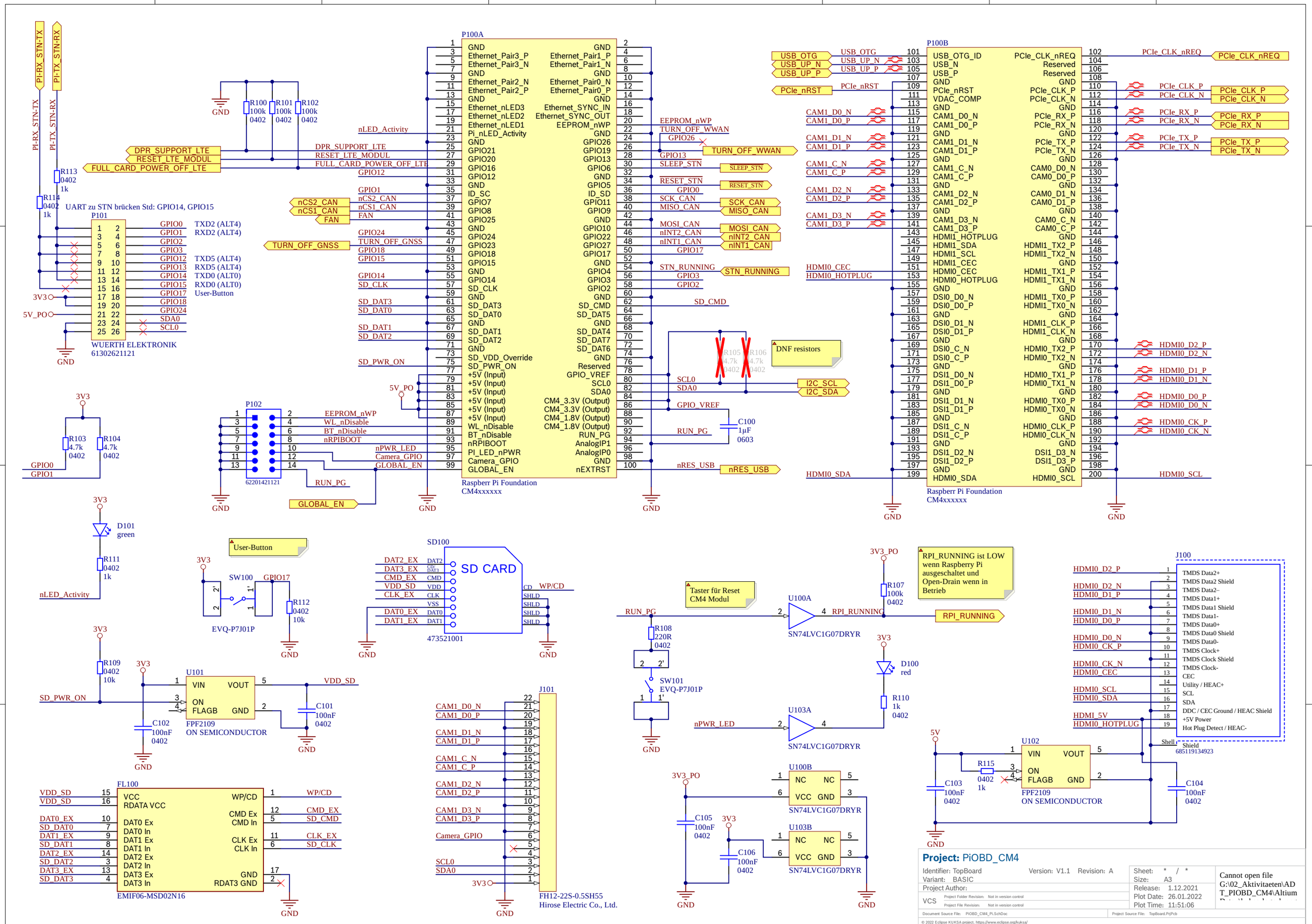

KUKSA CANOPi Prototyping Platform
https://www.eclipse.org/kuksa/
V1.1 © 2022 Eclipse KUKSA Project
KUKSA
TopBoard V1.1
SW100
R112
User_BTN
SW101
R108
Reset_CM4
No Ext Reset
Reset Over Pi
SD100
FL100
R103
R104
R101
R102
C100
R105
R106
C105
U100
R107
PI_TX GPIO0
PI_RX GPIO1
PI_TX GPIO2
PI_RX GPIO3
PI_TX GPIO12
PI_RX GPIO13
PI_TX GPIO14
PI_RX GPIO15
3V3 GPIO17
3V3 GPIO18
5V* GPIO24
GND SDA
GND SCL
GND EEPROM_WP
GND WL_nDis
GND BT_nDis
GND nRPIREBO
GND Cam_GPIO
GND GLOBAL_EN
GND RUN_PG
R204
C227
C228
R205
C224
R203
D201
C238
C231
C232
C239
U203
R207
C215
U201
C226
C225
C223
C222
Y200
R208
R206
C230
C229
C235
C236
C240
U202
R209
R210
R211
R212


P100A
Raspberr Pi Foundation
CM4xxxxxx
P100B
Raspberr Pi Foundation
CM4xxxxxx
P101
WUERTH ELEKTRONIK
61302621121
UART zu STN brücken Std: GPIO14, GPIO15
P102
62201421121
SD100
SD CARD
473521001
J100
TMDS Data2+
TMDS Data2 Shield
TMDS Data2–
TMDS Data1+
TMDS Data1 Shield
TMDS Data1-
TMDS Data0+
TMDS Data0 Shield
TMDS Data0-
TMDS Clock+
TMDS Clock Shield
TMDS Clock-
CEC
Utility / HEAC+
SCL
SDA
DDC / CEC Ground / HEAC Shield
+5V Power
Hot Plug Detect / HEAC-
Shield
685119134923
J101
FH12-22S-0.5SH55
Hirose Electric Co., Ltd.
FL100
EMIF06-MSD02N16
U101
FPF2109
ON SEMICONDUCTOR
U102
FPF2109
ON SEMICONDUCTOR
U100A
SN74LVC1G07DRYR
U100B
SN74LVC1G07DRYR
U103A
SN74LVC1G07DRYR
U103B
SN74LVC1G07DRYR
SW100
EVQ-P7J01P
SW101
EVQ-P7J01P
User-Button
RPI_RUNNING ist LOW wenn Raspberry Pi ausgeschaltet und Open-Drain wenn in Betrieb
Taster für Reset CM4 Modul
DNF resistors
D101 green
D100 red
Project: PiOBD_CM4
Identifier: TopBoard
Variant: BASIC
Project Author:
Version: V1.1
Revision: A
Sheet: * / *
Size: A3
Release: 1.12.2021
Plot Date: 26.01.2022
Plot Time: 11:51:06
Cannot open file G:\02_Aktivitaeten\AD T_PIOBD_CM4\Altium
Document Source File: PiOBD_CM4_Pi.SchDoc
Project Source File: TopBoard.PrjPcb
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Infos druch Rpi 4 Rev 1.2:
USB-Port 3 & USB Port 4 des VL805 sind auf RPi4 nur USB2.0 Ports, kein Routing der RX,TX Leitung

1V05 Regler auf Pi4 Rev 1.2: AP3429

AC-coupling nahe VL805 an 6x PCIe (TX, RX, CLK)
sowie
TX USB-Port 1 und TX USB Port 2

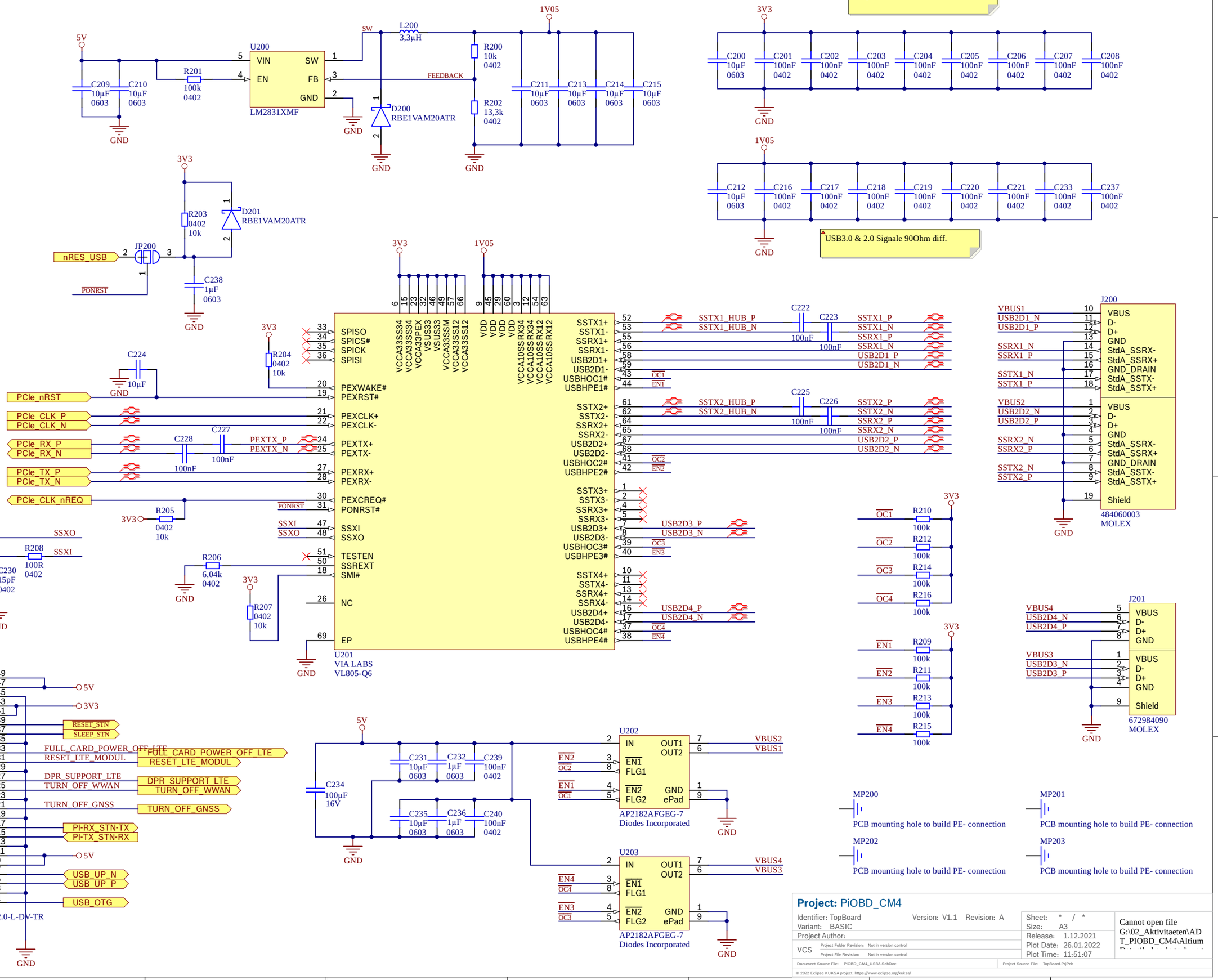
CM4 Datasheet:
"The CM4 has onboard AC coupling capacitors for CLK
and PCIe_TX signals. However the PCIe_RX signals need external coupling capacitors close to the driving source (the
device TX)"

PONRST# an nEXTRST von PI? eventuell triple Jumper R-C oder nEXTRST

PCIe Signale 90Ohm diff.

Waveshare Boards teilw. mit 1µ, 10µ, 100pF

USB3.0 & 2.0 Signale 90Ohm diff.



Project: PiOBD_CM4

Identifier: TopBoard	Version: V1.1	Revision: A	Sheet: * / *
Variant: BASIC			Size: A3
Project Author:			Release: 1.12.2021
VCS	Project Folder Revision: Not in version control		Plot Date: 26.01.2022
	Project File Revision: Not in version control		Plot Time: 11:51:07

Document Source File: PiOBD_CM4_USB3.SchDoc | Project Source File: TopBoard.PrjPcb

Cannot open file G:\02_Aktivitaeten\AD T_PIOBD_CM4\Altium

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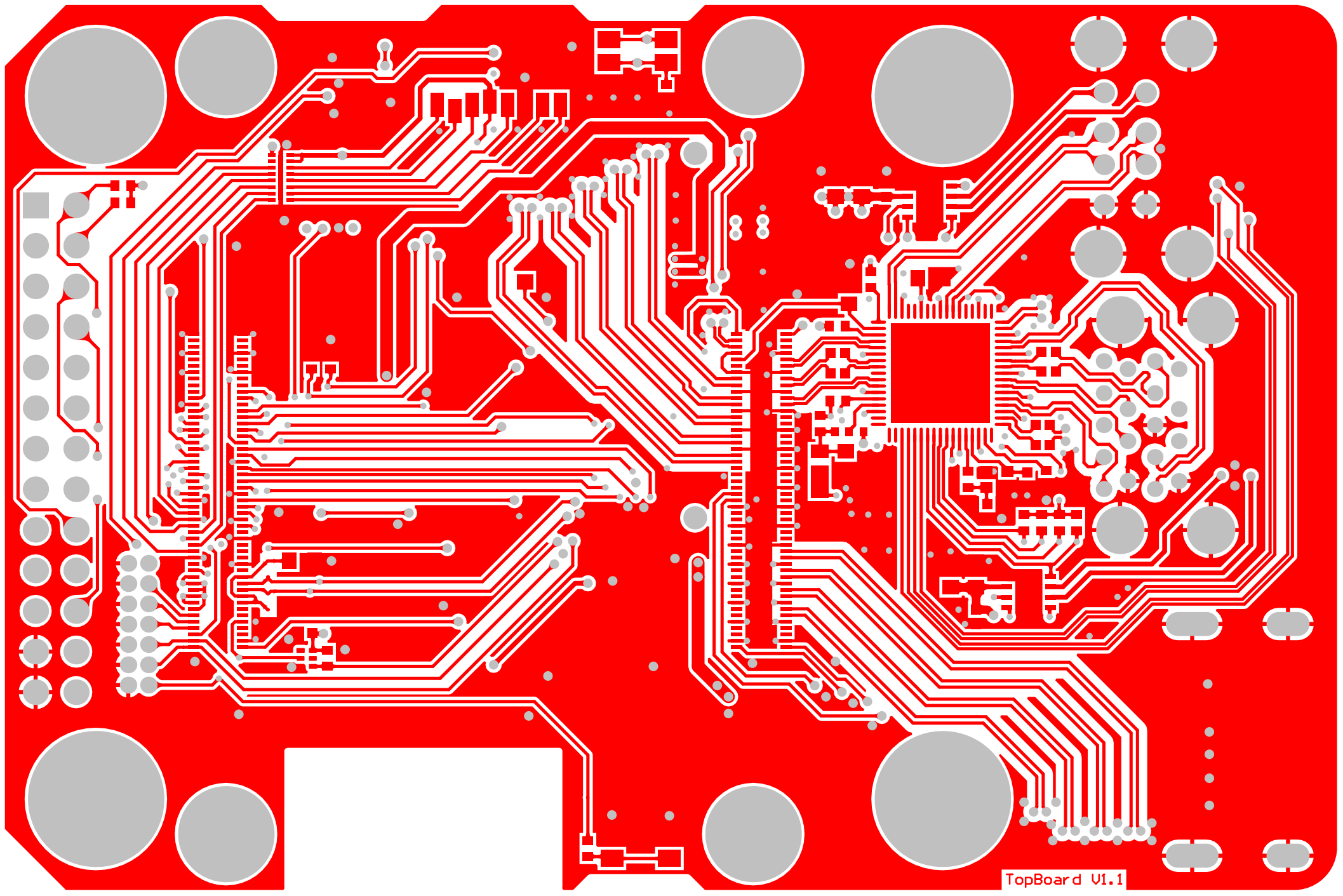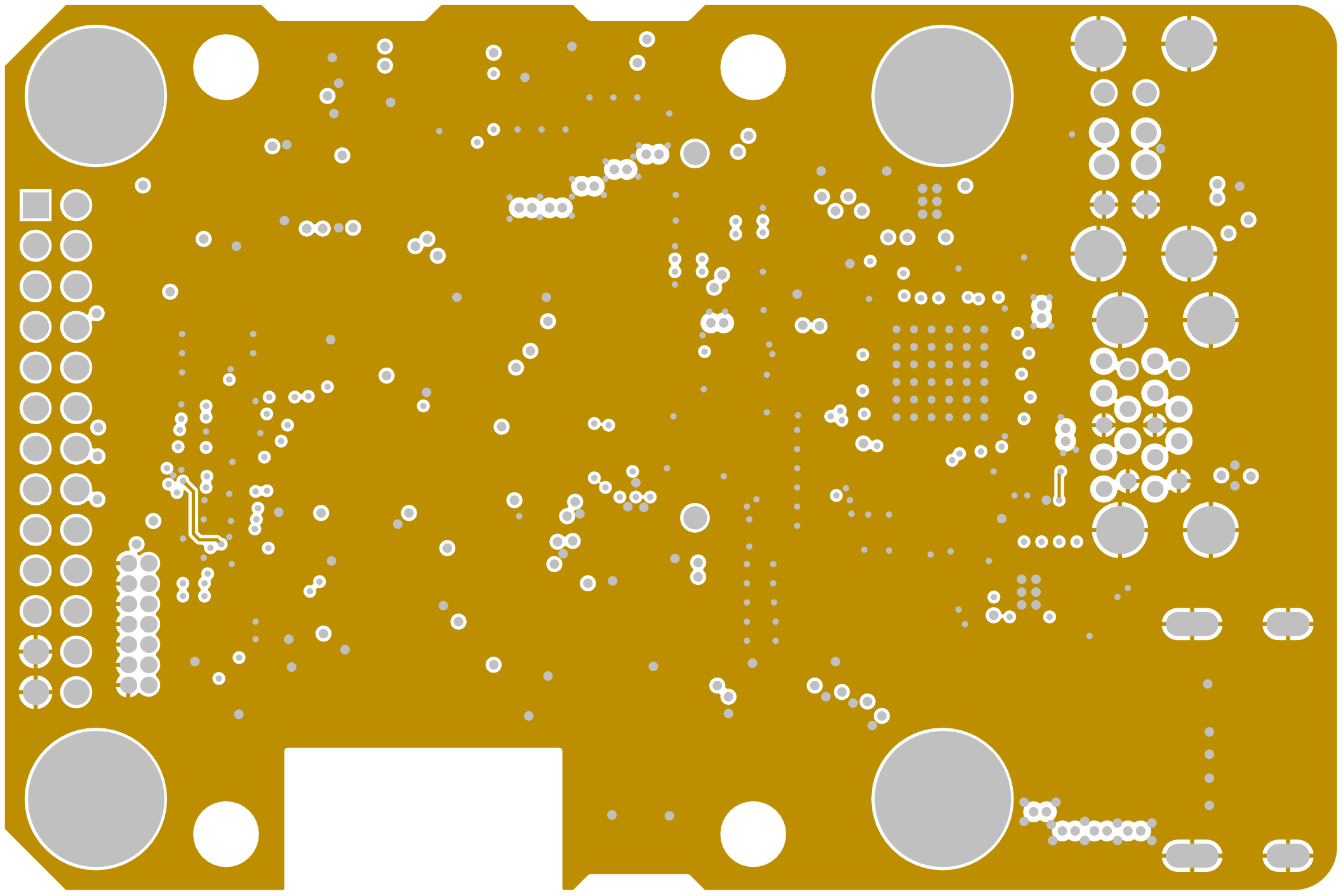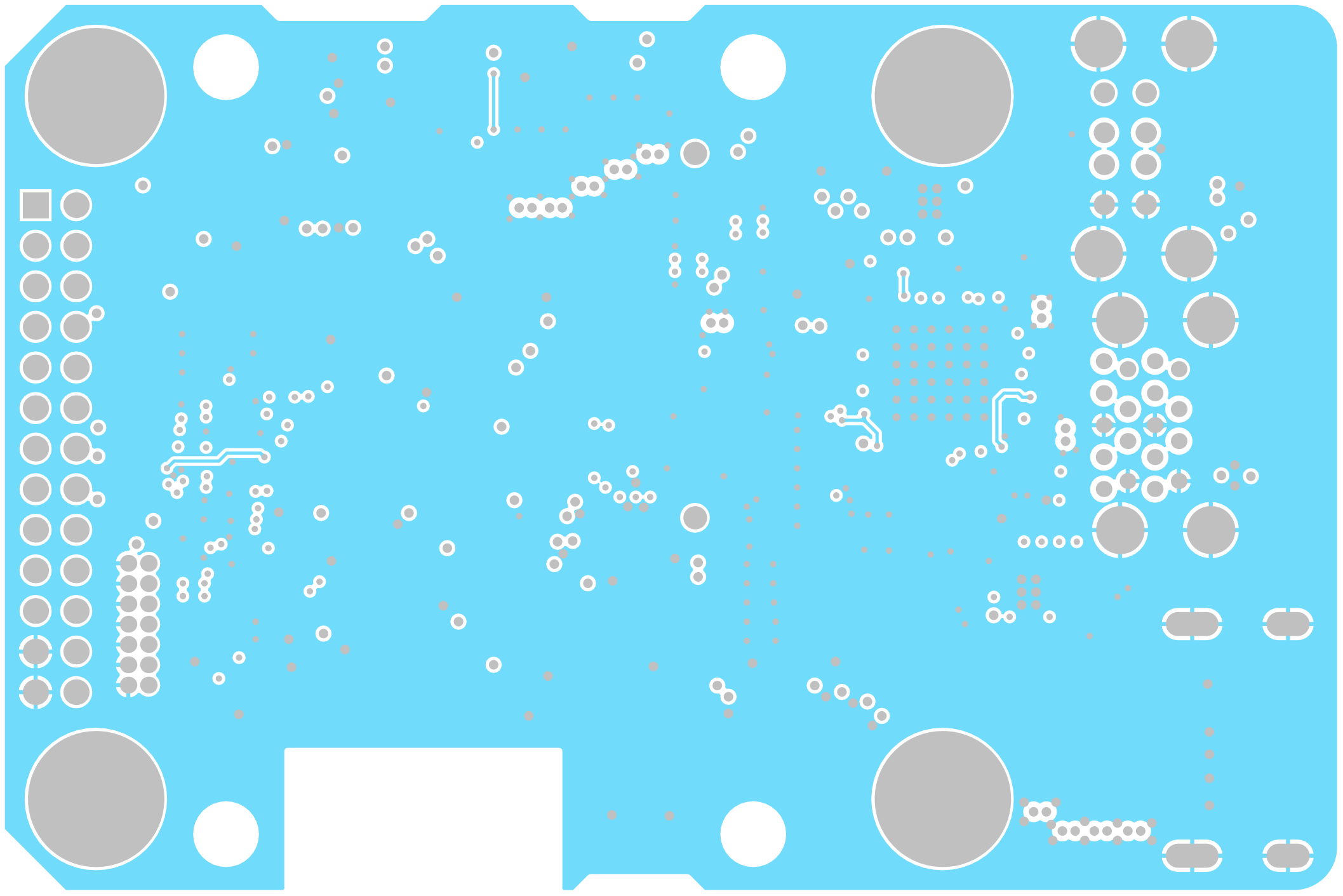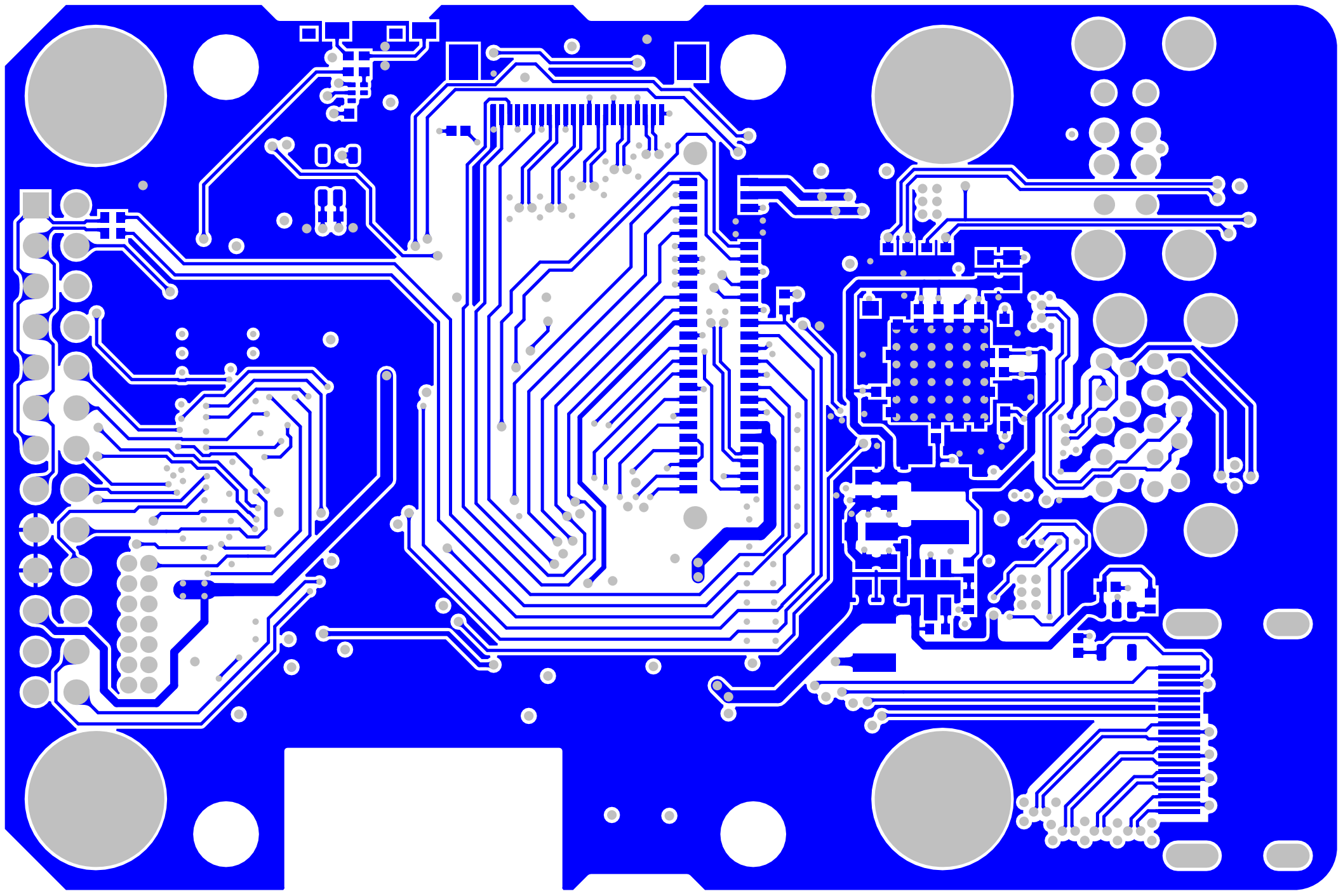
TopBoard V1.1