8.4 Device Functional Modes

8.4.1 Device Interface

8.4.1.1 Digital Pin Description

The digital data interface for the ADS8684A and ADS8688A is shown in Figure 89.

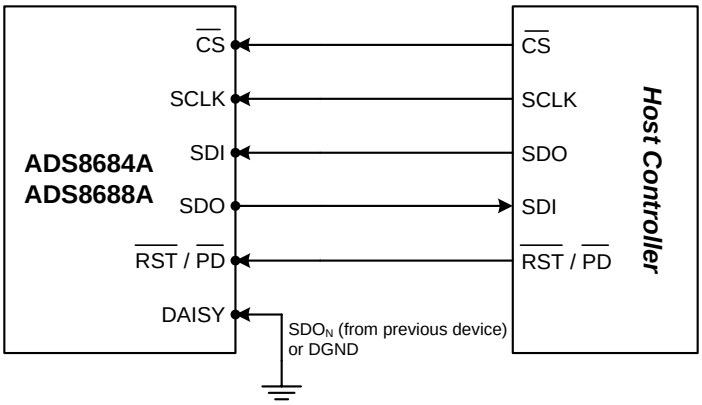

Figure 89. Pin Configuration for the Digital Interface

The signals shown in Figure 89 are summarized as follows:

8.4.1.1.1 $\overline{CS}$ (Input)

$\overline{CS}$ indicates an active-low, chip-select signal. $\overline{CS}$ is also used as a control signal to trigger a conversion on the falling edge. Each data frame begins with the falling edge of the $\overline{CS}$ signal. The analog input channel to be converted during a particular frame is selected in the previous frame. On the $\overline{CS}$ falling edge, the devices sample the input signal from the selected channel and a conversion is initiated using the internal clock. The device settings for the next data frame can be input during this conversion process. When the $\overline{CS}$ signal is high, the ADC is considered to be in an idle state.

8.4.1.1.2 SCLK (Input)

This pin indicates the external clock input for the data interface. All synchronous accesses to the device are timed with respect to the falling edges of the SCLK signal.

8.4.1.1.3 SDI (Input)

SDI is the serial data input line. SDI is used by the host processor to program the internal device registers for device configuration. At the beginning of each data frame, the $\overline{CS}$ signal goes low and the data on the SDI line are read by the device at every falling edge of the SCLK signal for the next 16 SCLK cycles. Any changes made to the device configuration in a particular data frame are applied to the device on the subsequent falling edge of the $\overline{CS}$ signal.

8.4.1.1.4 SDO (Output)

SDO is the serial data output line. SDO is used by the device to output conversion data. The size of the data output frame varies depending on the register setting for the SDO format; see Table 13. A low level on $\overline{CS}$ releases the SDO pin from the Hi-Z state. SDO is kept low for the first 15 SCLK falling edges. The MSB of the output data stream is clocked out on SDO on the 16th SCLK falling edge, followed by the subsequent data bits on every falling edge thereafter. The SDO line goes low after the entire data frame is output and goes to a Hi-Z state when $\overline{CS}$ goes high.

Device Functional Modes (continued)

8.4.1.1.5 DAISY (Input)

DAISY is a serial input pin. When multiple devices are connected in daisy-chain mode, as illustrated in Figure 92, the DAISY pin of the first device in the chain is connected to GND. The DAISY pin of every subsequent device is connected to the SDO output pin of the previous device, and the SDO output of the last device in the chain goes to the SDI of the host processor. If an application uses a stand-alone device, the DAISY pin is connected to GND.

8.4.1.1.6 $\overline{\text{RST}}/\overline{\text{PD}}$ (Input)

$\overline{\text{RST}}/\overline{\text{PD}}$ is a dual-function pin. Figure 90 shows the timing of this pin and Table 5 explains the usage of this pin.

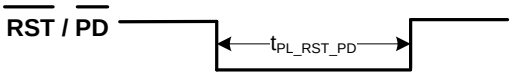

Figure 90. $\overline{\text{RST}}/\overline{\text{PD}}$ Pin Timing

Table 5. $\overline{\text{RST}}/\overline{\text{PD}}$ Pin Functionality

CONDITION	DEVICE MODE
40 ns < $t_{PL\_RST\_PD}$ ≤ 100 ns	The device is in RST mode and does not enter PWR_DN mode.
100 ns < $t_{PL\_RST\_PD}$ < 400 ns	The device is in RST mode and may or may not enter PWR_DN mode. NOTE: This setting is not recommended.
$t_{PL\_RST\_PD}$ ≥ 400 ns	The device enters PWR_DN mode and the program registers are reset to default value.

The devices can be placed into power-down (PWR_DN) mode by pulling the $\overline{\text{RST}}/\overline{\text{PD}}$ pin to a logic low state for at least 400 ns. The $\overline{\text{RST}}/\overline{\text{PD}}$ pin is asynchronous to the clock; thus, $\overline{\text{RST}}/\overline{\text{PD}}$ can be triggered at any time regardless of the status of other pins (including the analog input channels). When the device is in power-down mode, any activity on the digital input pins (apart from the $\overline{\text{RST}}/\overline{\text{PD}}$ pin) is ignored.

The program registers in the device can be reset to their default values (RST) by pulling the $\overline{\text{RST}}/\overline{\text{PD}}$ pin to a logic low state for no longer than 100 ns. This input is asynchronous to the clock. When $\overline{\text{RST}}/\overline{\text{PD}}$ is pulled back to a logic high state, the devices are placed in normal mode. One valid write operation must be executed on the program register in order to configure the device, followed by an appropriate command (AUTO_RST or MAN) to initiate conversions.

When the $\overline{\text{RST}}/\overline{\text{PD}}$ pin is pulled back to a logic high level, the devices wake-up in a default state in which the program registers are reset to their default values.

8.4.1.2 Data Acquisition Example

This section provides an example of how a host processor can use the device interface to configure the device internal registers as well as convert and acquire data for sampling a particular input channel. The timing diagram shown in Figure 91 provides further details.

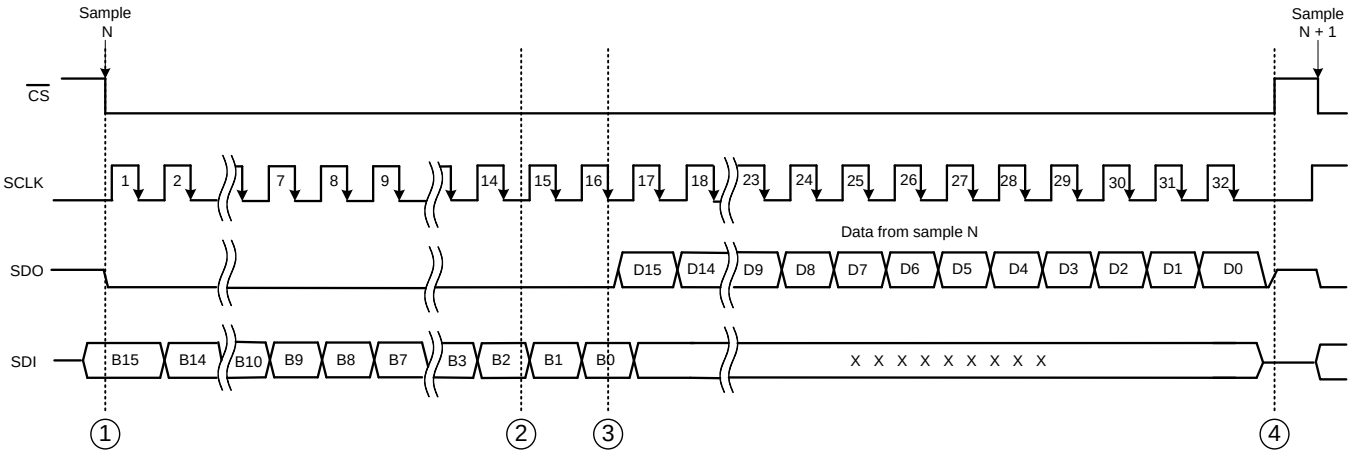

Figure 91. Device Operation Using the Serial Interface Timing Diagram

There are four events shown in Figure 91. These events are described below:

- ***Event 1:*** The host initiates a data conversion frame through a falling edge of the $\overline{CS}$ signal. The analog input signal at the instant of the $\overline{CS}$ falling edge is sampled by the ADC and conversion is performed using an internal oscillator clock. The analog input channel converted during this frame is selected in the previous data frame. The internal register settings of the device for the next conversion can be input during this data frame using the SDI and SCLK inputs. Initiate SCLK at this instant and latch data on the SDI line into the device on every SCLK falling edge for the next 16 SCLK cycles. At this instant, SDO goes low because the device does not output internal conversion data on the SDO line during the first 16 SCLK cycles.
- ***Event 2:*** During the first 16 SCLK cycles, the device completes the internal conversion process and data are now ready within the converter. However, the device does not output data bits on SDO until the 16th falling edge appears on the SCLK input. Because the ADC conversion time is fixed (the maximum value is given in the *Electrical Characteristics* table), the 16th SCLK falling edge must appear after the internal conversion is over, otherwise data output from the device is incorrect. Therefore, the SCLK frequency cannot exceed a maximum value, as provided in the *Timing Requirements: Serial Interface* table.
- ***Event 3:*** At the 16th falling edge of the SCLK signal, the device reads the LSB of the input word on the SDI line. The device does not read anything from the SDI line for the remaining data frame. On the same edge, the MSB of the conversion data is output on the SDO line and can be read by the host processor on the subsequent falling edge of the SCLK signal. For 16 bits of output data, the LSB can be read on the 32nd SCLK falling edge. The SDO outputs 0 on subsequent SCLK falling edges until the next conversion is initiated.
- ***Event 4:*** When the internal data from the device is received, the host terminates the data frame by deactivating the $\overline{CS}$ signal to high. The SDO output goes into a Hi-Z state until the next data frame is initiated, as explained in Event 1.

8.4.1.3 Host-to-Device Connection Topologies

The digital interface of the ADS8684A and ADS8688A offers a lot of flexibility in the ways that a host controller can exchange data or commands with the device. A typical connection between a host controller and a stand-alone device is illustrated in Figure 89. However, there are applications that require multiple ADCs but the host controller has limited interfacing capability. This section describes two connection topologies that can be used to address the requirements of such applications.

8.4.1.3.1 Daisy-Chain Topology

A typical connection diagram showing multiple devices in daisy-chain mode is shown in Figure 92. The $\overline{CS}$, SCLK, and SDI inputs of all devices are connected together and controlled by a single $\overline{CS}$, SCLK, and SDO pin of the host controller, respectively. The $DAISY_1$ input pin of the first ADC in the chain is connected to DGND, the SDO_1 output pin is connected to the $DAISY_2$ input of ADC_2, and so forth. The SDO_N pin of the Nth ADC in the chain is connected to the SDI pin of the host controller. The devices do not require any special hardware or software configuration to enter daisy-chain mode.

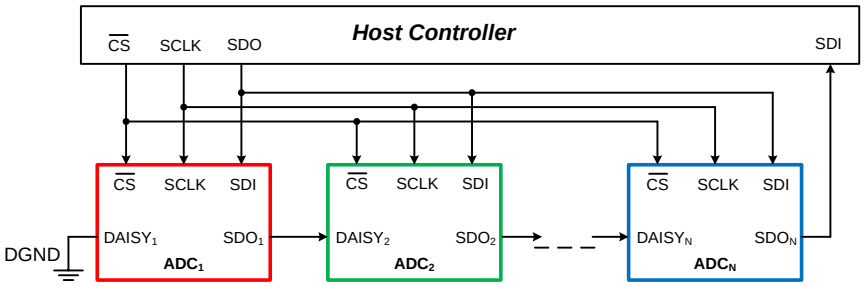

Figure 92. Daisy-Chain Connection Schematic

A typical timing diagram for three devices connected in daisy-chain mode is shown in Figure 93.

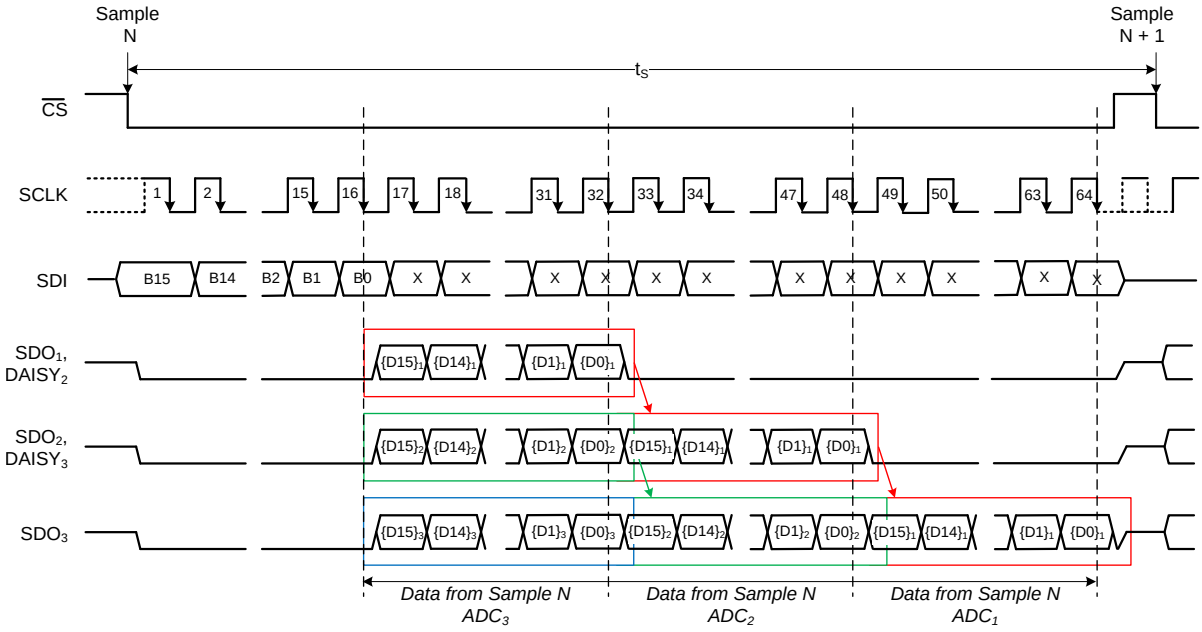

Figure 93. Three Devices Connected in Daisy-Chain Mode Timing Diagram

At the falling edge of the $\overline{CS}$ signal, all devices sample the input signal at their respective selected channels and enter into conversion phase. For the first 16 SCLK cycles, the internal register settings for the next conversion can be entered using the SDI line that is common to all devices in the chain. During this time period, the SDO outputs for all devices remain low. At the end of conversion, every ADC in the chain loads its own conversion result into an internal 16-bit shift register. At the 16th SCLK falling edge, every ADC in the chain outputs the MSB bit on its own SDO output pin. On every subsequent SCLK falling edge, the internal shift register of each ADC latches the data available on its DAISY pin and shifts out the next bit of data on its SDO pin. Therefore, the digital host receives the data of ADC_N, followed by the data of $ADC_{N–1}$, and so forth (in MSB-first fashion). In total, a minimum of 16 × N SCLK falling edges are required to capture the outputs of all N devices in the chain. This example uses three devices in a daisy-chain connection, so 3 × 16 = 48 SCLK cycles are required to capture the outputs of all devices in the chain along with the 16 SCLK cycles to input the register settings for the next conversion, resulting in a total of 64 SCLK cycles for the entire data frame. Note that the overall throughput of the system is proportionally reduced with the number of devices connected in a daisy-chain configuration.

The following points must be noted about the daisy-chain configuration illustrated in Figure 92:

- The SDI pins for all devices are connected together so each device operates with the same internal configuration. This limitation can be overcome by spending additional host controller resources to control the $\overline{CS}$ or SDI input of devices with unique configurations.
- If the number of devices connected in daisy-chain is more than four, loading increases on the shared output lines from the host controller ($\overline{CS}$, SDO, and SCLK). This increased loading can lead to digital timing errors. This limitation can be overcome by using digital buffers on the shared outputs from the host controller before feeding the shared digital lines into additional devices.

8.4.1.3.2 Star Topology

A typical connection diagram showing multiple devices in the star topology is shown in Figure 94. The SDI and SCLK inputs of all devices are connected together and are controlled by a single SDO and SCLK pin of the host controller, respectively. Similarly, the SDO outputs of all devices are tied together and connected to the SDI input pin of the host controller. The $\overline{CS}$ input pin of each device is individually controlled by separate $\overline{CS}$ control lines from the host controller.

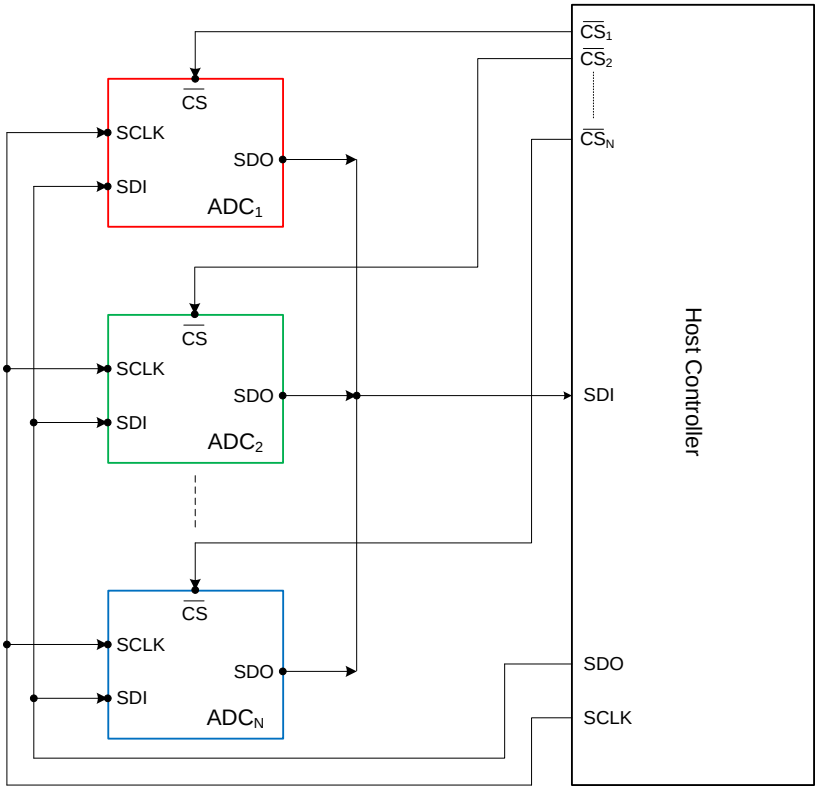

Figure 94. Star Topology Connection Schematic

The timing diagram for a typical data frame in the star topology is the same as in a stand-alone device operation, as illustrated in Figure 91. The data frame for a particular device starts with the falling edge of the $\overline{CS}$ signal and ends when the $\overline{CS}$ signal goes high. Because the host controller provides separate $\overline{CS}$ control signals for each device in this topology, the user can select the devices in any order and initiate a conversion by bringing down the $\overline{CS}$ signal for that particular device. As explained in Figure 91, when $\overline{CS}$ goes high at the end of each data frame, the SDO output of the device is placed into a Hi-Z state. Therefore, the shared SDO line in the star topology is controlled only by the device with an active data frame ($\overline{CS}$ is low). In order to avoid any conflict related to multiple devices driving the SDO line at the same time, ensure that the host controller pulls down the $\overline{CS}$ signal for only one device at any particular time.

TI recommends connecting a maximum of four devices in the star topology. Beyond that, loading may increase on the shared output lines from the host controller (SDO and SCLK). This loading can lead to digital timing errors. This limitation can be overcome by using digital buffers on the shared outputs from the host controller before being fed into additional devices.

8.4.2 Device Modes

The ADS8684A and ADS8688A support multiple modes of operation that are software programmable. After powering up, the device is placed into idle mode and does not perform any function until a command is received from the user. Table 6 lists all commands to enter the different modes of the device. After power-up, the program registers wake up with the default values and require appropriate configuration settings before performing any conversion. The diagram in Figure 95 explains how to switch the device from one mode of operation to another.

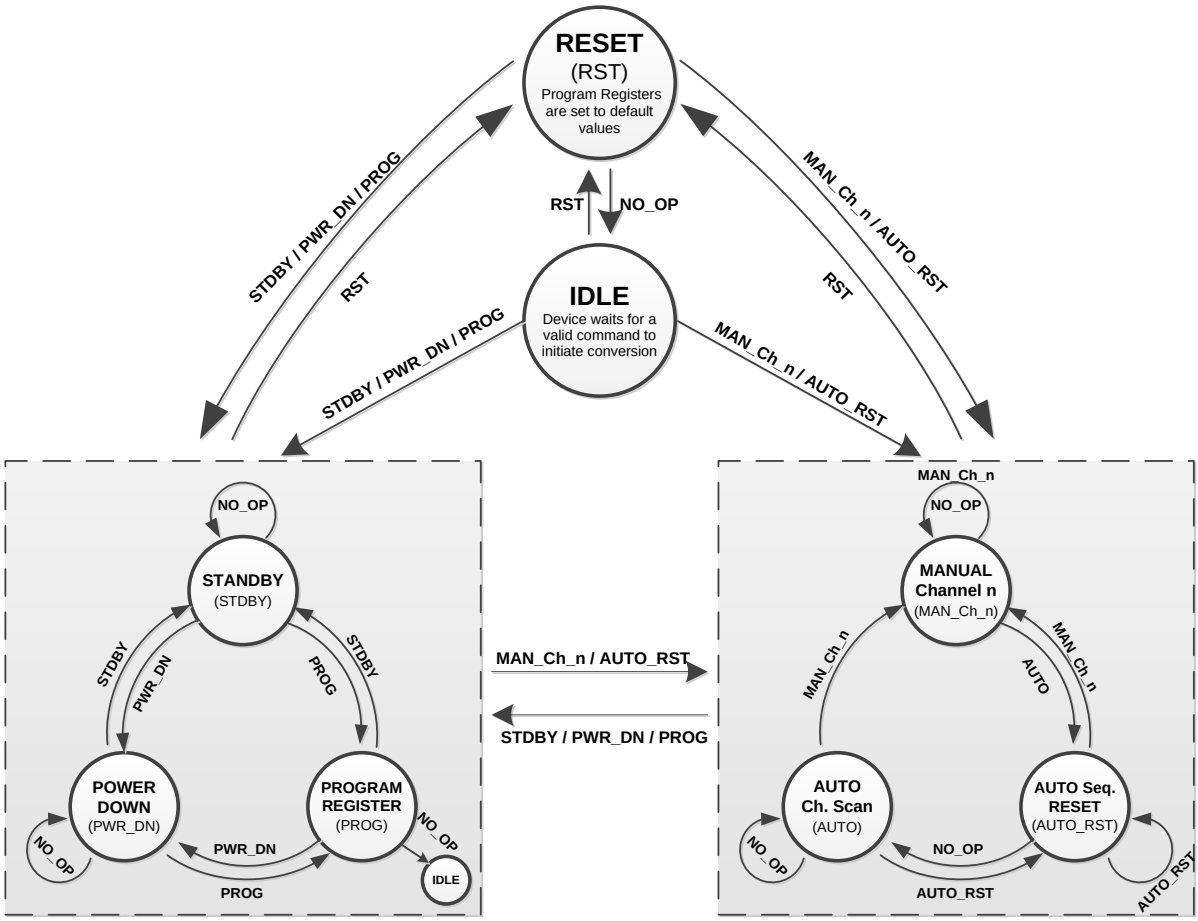

Figure 95. State Transition Diagram

8.4.2.1 Continued Operation in the Selected Mode (NO_OP)

Holding the SDI line low continuously (equivalent to writing a 0 to all 16 bits) during device operation continues device operation in the last selected mode (STDBY, PWR_DN, AUTO_RST, or MAN_Ch_n). In this mode, the device follows the same settings that are already configured in the program registers.

If a NO_OP condition occurs when the device is performing any read or write operation in the program register (PROG mode), then the device retains the current settings of the program registers. The device goes back to IDLE mode and waits for the user to enter a proper command to execute the program register read or write configuration.

8.4.2.2 Frame Abort Condition (FRAME_ABORT)

As explained in the *Data Acquisition Example* section, the device digital interface is designed such that each data frame starts with a falling edge of the $\overline{CS}$ signal. During the first 16 SCLK cycles, the device reads the 16-bit command word on the SDI line. The device waits to execute the command until the last bit of the command is received, which is latched on the 16th SCLK falling edge. During this operation, the $\overline{CS}$ signal must stay low. If the $\overline{CS}$ signal goes high for any reason before the data transmission is complete, the device goes into an INVALID state and waits for a proper command to be written. This condition is called the FRAME_ABORT condition. When the device is operating in this INVALID mode, any read operation on the device returns invalid data on the SDO line. The output of the ALARM pin will continue to reflect the status of input signal on the previously selected channel.

8.4.2.3 STANDBY Mode (STDBY)

The devices support a low-power standby mode (STDBY) in which only part of the circuit is powered down. The internal reference and buffer is not powered down, and therefore, the devices can be quickly powered up in 20 µs on exiting the STDBY mode. When the device comes out of STDBY mode, the program registers are not reset to the default values.

To enter STDBY mode, execute a valid write operation to the command register with a STDBY command of 8200h, as shown in Figure 96. The command is executed and the device enters STDBY mode on the next $\overline{CS}$ rising edge following this write operation. The device remains in STDBY mode if no valid conversion command (AUTO_RST or MAN_Ch_n) is executed and SDI remains low (see the *Continued Operation in the Selected Mode* section) during the subsequent data frames. When the device operates in STDBY mode, the program register settings can be updated (as explained in the *Program Register Read/Write Operation* section) using 16 SCLK cycles. However, if 32 complete SCLK cycles are provided, then the device returns invalid data on the SDO line because there is no ongoing conversion in STDBY mode. The program register read operation can take place normally during this mode.

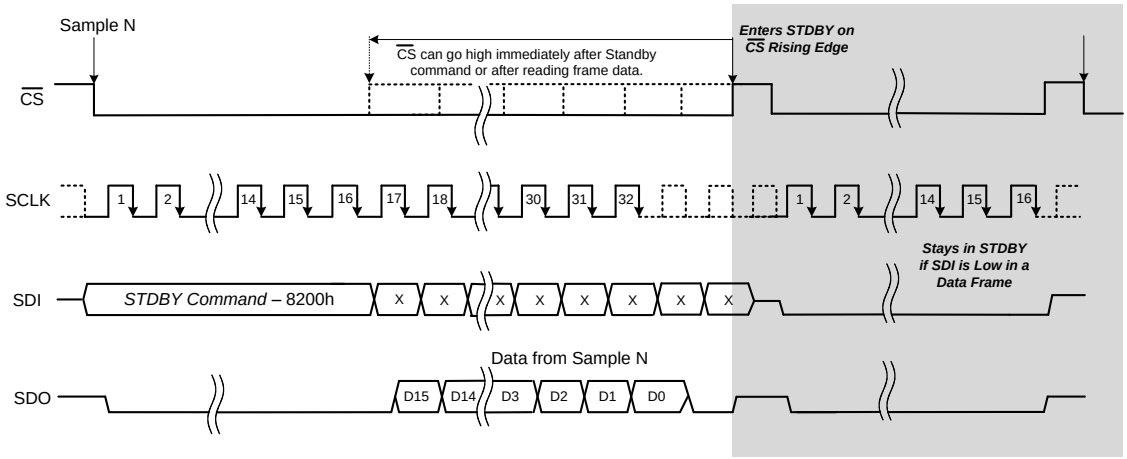

Figure 96. Enter and Remain in STDBY Mode Timing Diagram

In order to exit STDBY mode a valid 16-bit write command must be executed to enter auto (AUTO_RST) or manual (MAN_CH_n) scan mode, as shown in Figure 97. The device starts exiting STDBY mode on the next $\overline{CS}$ rising edge. At the next $\overline{CS}$ falling edge, the device samples the analog input at the channel selected by the MAN_CH_n command or the first channel of the AUTO_RST mode sequence. To ensure that the input signal is sampled correctly, keep the minimum width of the $\overline{CS}$ signal at 20 µs after exiting STDBY mode so the device internal circuitry can be fully powered up and biased properly before taking the sample. The data output for the selected channel can be read during the same data frame, as explained in Figure 91.

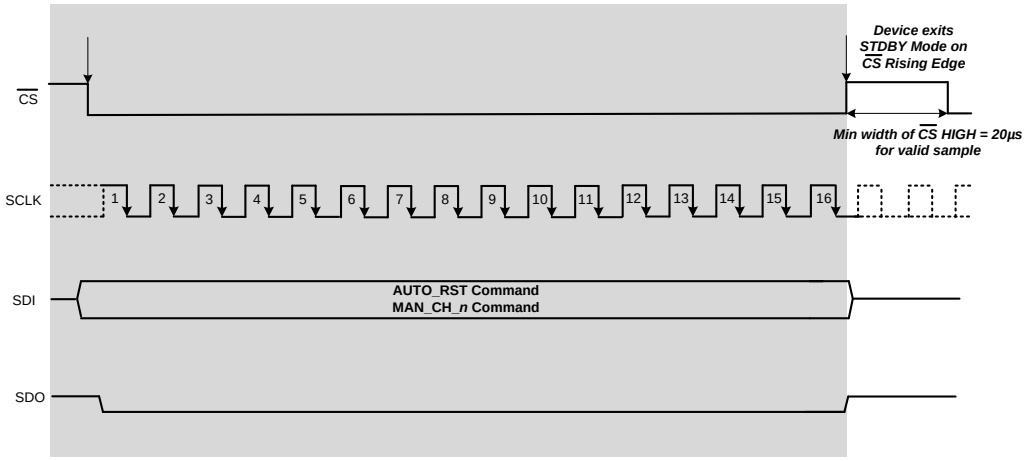

Figure 97. Exit STDBY Mode Timing Diagram

8.4.2.4 Power-Down Mode (PWR_DN)

The devices support a hardware and software power-down mode (PWR_DN) in which all internal circuitry is powered down, including the internal reference and buffer. A minimum time of 15 ms is required for the device to power up and convert the selected analog input channel after exiting PWR_DN mode, if the device is operating in the internal reference mode ($\overline{\text{REFSEL}}$ = 0). The hardware power mode for the device is explained in the ***RST/PD (Input)*** section. The primary difference between the hardware and software power-down modes is that the program registers are reset to default values when the devices wake up from hardware power-down, but the previous settings of the program registers are retained when the devices wake up from software power-down.

To enter PWR_DN mode using software, execute a valid write operation on the command register with a software PWR_DN command of 8300h, as shown in Figure 98. The command is executed and the device enters PWR_DN mode on the next $\overline{\text{CS}}$ rising edge following this write operation. The device remains in PWR_DN mode if no valid conversion command (AUTO_RST or MAN_Ch_n) is executed and SDI remains low (see the *Continued Operation in the Selected Mode* section) during the subsequent data frames. When the device operates in PWR_DN mode, the program register settings can be updated (as explained in the *Program Register Read/Write Operation* section) using 16 SCLK cycles. However, if 32 complete SCLK cycles are provided, then the device returns invalid data on the SDO line because there is no ongoing conversion in PWR_DN mode. The program register read operation can take place normally during this mode.

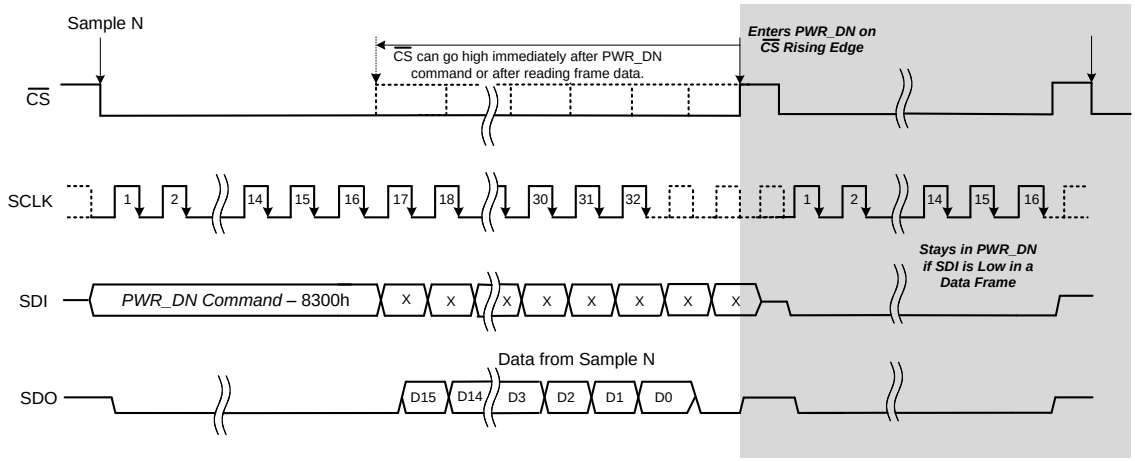

Figure 98. Enter and Remain in PWR_DN Mode Timing Diagram

In order to exit from PWR_DN mode a valid 16-bit write command must be executed, as shown in Figure 99. The device comes out of PWR_DN mode on the next $\overline{\text{CS}}$ rising edge. For operation in internal reference mode ($\overline{\text{REFSEL}}$ = 0), 15 ms are required for the device to power-up the reference and other internal circuits and settle to the required accuracy before valid conversion data are output for the selected input channel.

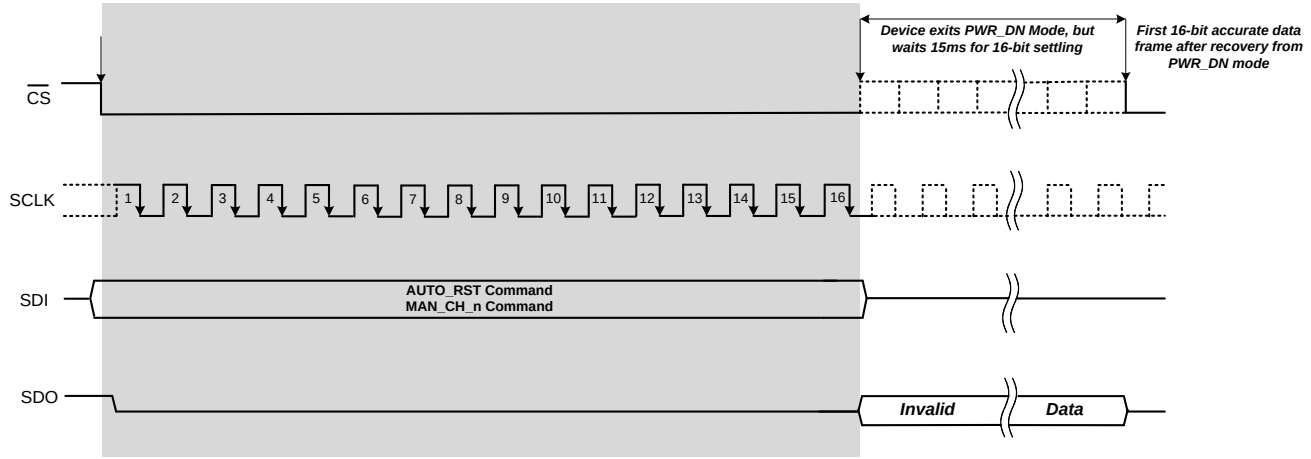

Figure 99. Exit PWR_DN Mode Timing Diagram

8.4.2.5 Auto Channel Enable with Reset (AUTO_RST)

The devices can be programmed to scan the input signal on all analog channels automatically by writing a valid auto channel sequence with a reset (AUTO_RST, A000h) command in the command register, as explained in Figure 100. As shown in Figure 100, the $\overline{CS}$ signal can be pulled high immediately after the AUTO_RST command or after reading the output data of the frame. However, in order to accurately acquire and convert the input signal on the first selected channel in the next data frame, the command frame must be a complete frame of 32 SCLK cycles.

The sequence of channels for the automatic scan can be configured by the AUTO SCAN sequencing control register (01h to 02h) in the program register; see the *Program Register Map* section. In this mode, the devices continuously cycle through the selected channels in ascending order, beginning with the lowest channel and converting all channels selected in the program register. On completion of the sequence, the devices return to the lowest count channel in the program register and repeat the sequence. The input voltage range for each channel in the auto-scan sequence can be configured by setting the *Range Select Registers* of the program registers.

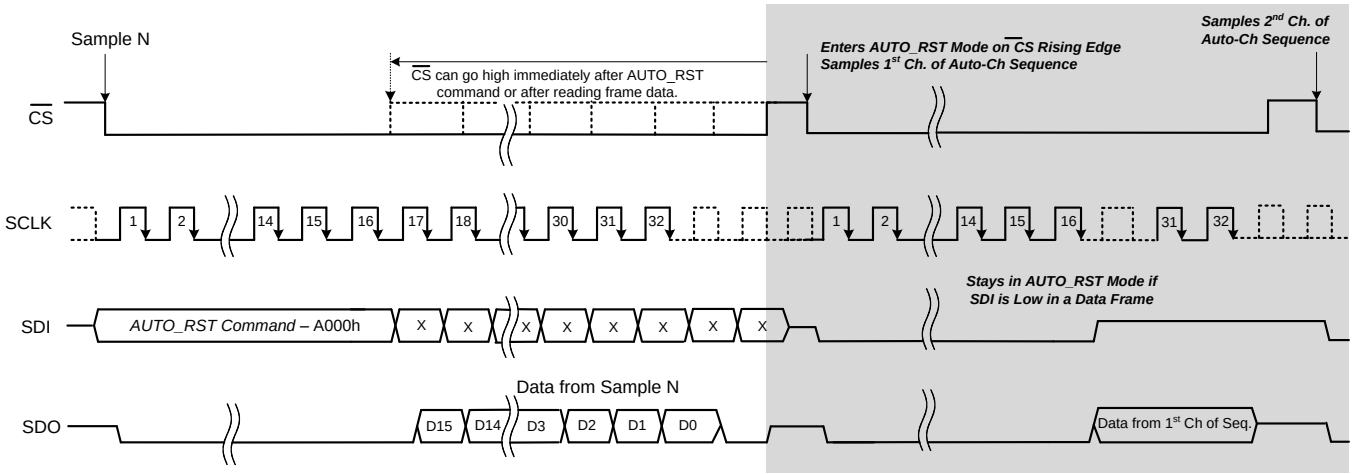

Figure 100. Enter AUTO_RST Mode Timing Diagram

The devices remain in AUTO_RST mode if no other valid command is executed and SDI is kept low (see the *Continued Operation in the Selected Mode (NO_OP)* section) during subsequent data frames. If the AUTO_RST command is executed again at any time during this mode of operation, then the sequence of the scanned channels is reset. The devices return to the lowest count channel of the auto-scan sequence in the program register and repeat the sequence. The timing diagram in Figure 101 shows this behavior using an example in which channels 0 to 2 are selected in the auto sequence. For switching between AUTO_RST mode and MAN_Ch_n mode; see the *Channel Sequencing Modes* section.

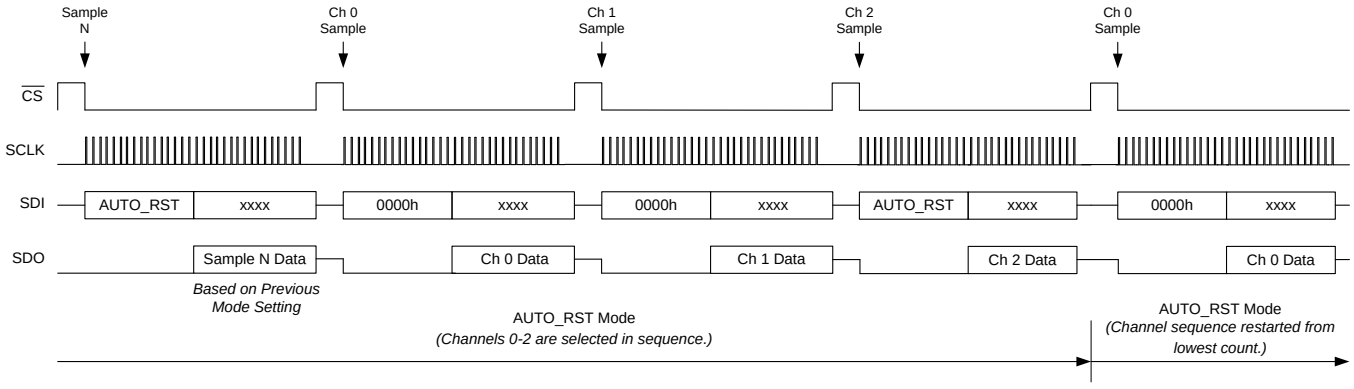

Figure 101. Device Operation Example in AUTO_RST Mode

8.4.2.6 Manual Channel n Select (MAN_Ch_n)

The devices can be programmed to convert a particular analog input channel by operating in manual channel *n* scan mode (MAN_Ch_n). This programming is done by writing a valid manual channel *n* select command (MAN_Ch_n) in the command register, as shown in Figure 102. As shown in Figure 102, the $\overline{CS}$ signal can be pulled high immediately after the MAN_Ch_n command or after reading the output data of the frame. However, in order to accurately acquire and convert the input signal on the next channel, the command frame must be a complete frame of 32 SCLK cycles. See Table 6 for a list of commands to select individual channels during MAN_Ch_n mode.

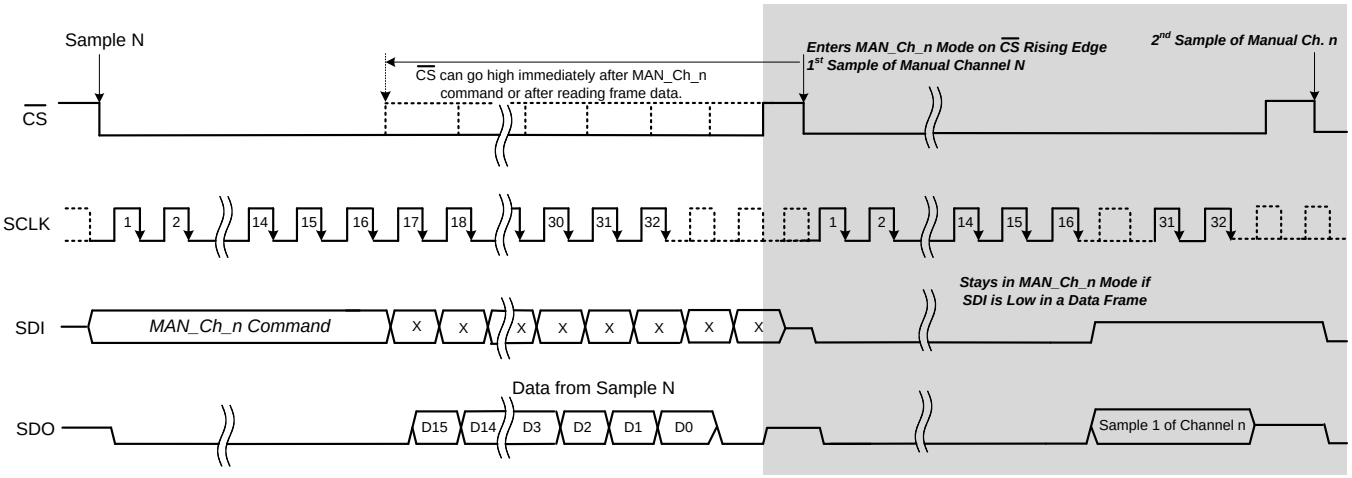

Figure 102. Enter MAN_Ch_*n* Scan Mode Timing Diagram

The manual channel *n* select command (MAN_Ch_n) is executed and the devices sample the analog input on the selected channel on the $\overline{CS}$ falling edge of the next data frame following this write operation. The input voltage range for each channel in the MAN_Ch_n mode can be configured by setting the *Range Select Registers* in the program registers. The device continues to sample the analog input on the same channel if no other valid command is executed and SDI is kept low (see the *Continued Operation in the Selected Mode (NO_OP)* section) during subsequent data frames. The timing diagram in Figure 103 shows this behavior using an example in which channel 1 is selected in the manual sequencing mode. For switching between MAN_Ch_n mode and AUTO_RST mode; see the *Channel Sequencing Modes* section.

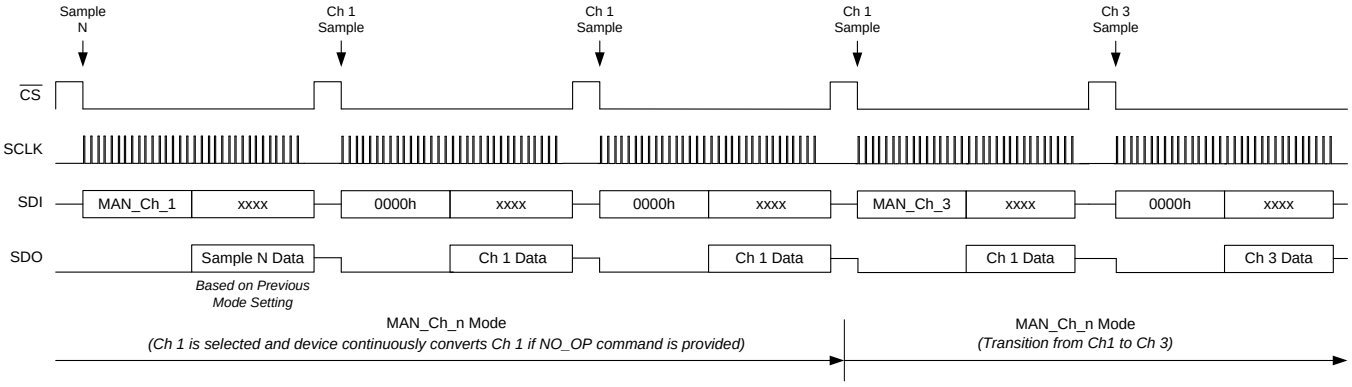

Figure 103. Device Operation in MAN_Ch_n Mode

8.4.2.7 Channel Sequencing Modes

The devices offer two channel sequencing modes: AUTO_RST and MAN_Ch_n.

In AUTO_RST mode, the channel number automatically increments in every subsequent frame. As explained in the *Auto-Scan Sequencing Control Registers* section, the analog inputs can be selected for an automatic scan with a register setting. The device automatically scans only the selected analog inputs in ascending order. The unselected analog input channels can also be powered down for optimizing power consumption in this mode of operation. The auto-mode sequence can be reset at any time during an automatic scan (using the AUTO_RST command). When the reset command is received, the ongoing auto-mode sequence is reset and restarts from the lowest selected channel in the sequence.

In MAN_Ch_n mode, the same input channel is selected during every data conversion frame. The input command words to select individual analog channels in MAN_Ch_n mode are listed in Table 6. If a particular input channel is selected during a data frame, then the analog inputs on the same channel are sampled during the next data frame. Figure 104 shows the SDI command sequence for transitions from AUTO_RST to MAN_Ch_n mode.

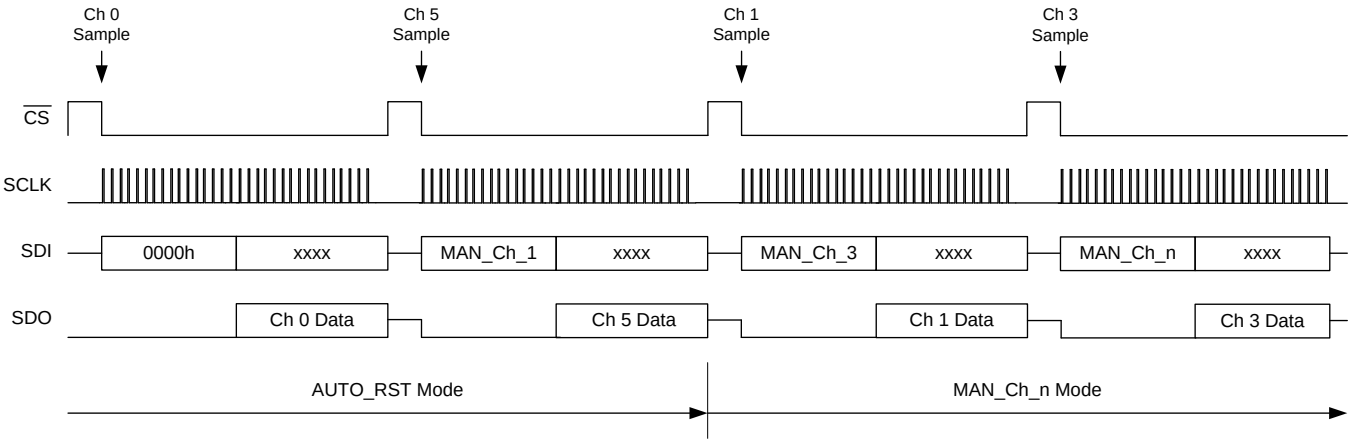

Figure 104. Transitioning from AUTO_RST to MAN_Ch_n Mode (Channels 0 and 5 are Selected for Auto Sequence)

Figure 105 shows the SDI command sequence for transitions from MAN_Ch_n to AUTO_RST mode. Note that each SDI command is executed on the next $\overline{CS}$ falling edge. A RST command can be issued at any instant during any channel sequencing mode, after which the device is placed into a default power-up state in the next data frame.

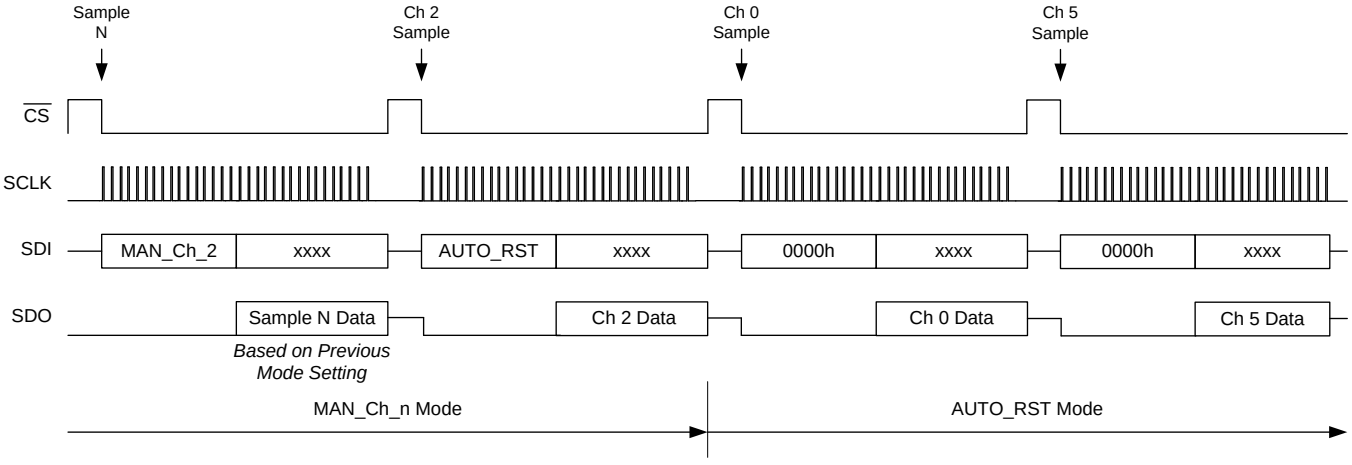

Figure 105. Transitioning from MAN_Ch_n to AUTO_RST Mode (Channels 0 and 5 are Selected for Auto Sequence)

8.4.2.8 Reset Program Registers (RST)

The devices support a hardware and software reset (RST) mode in which all program registers are reset to their default values. The devices can be put into RST mode using a hardware pin, as explained in the ***RST/PD (Input)*** section.

The device program registers can be reset to their default values during any data frame by executing a valid write operation on the command register with a RST command of 8500h, as shown in Figure 106. The device remains in RST mode if no valid conversion command (AUTO_RST or MAN_Ch_n) is executed and SDI remains low (see the *Continued Operation in the Selected Mode (NO_OP)* section) during the subsequent data frames. When the device operates in RST mode, the program register settings can be updated (as explained in the *Program Register Read/Write Operation* section) using 16 SCLK cycles. However, if 32 complete SCLK cycles are provided, then the device returns invalid data on the SDO line because there is no ongoing conversion in RST mode. The values of the program register can be read normally during this mode. A valid AUTO_RST or MAN_CH_n channel selection command must be executed for initiating a conversion on a particular analog channel using the default program register settings.

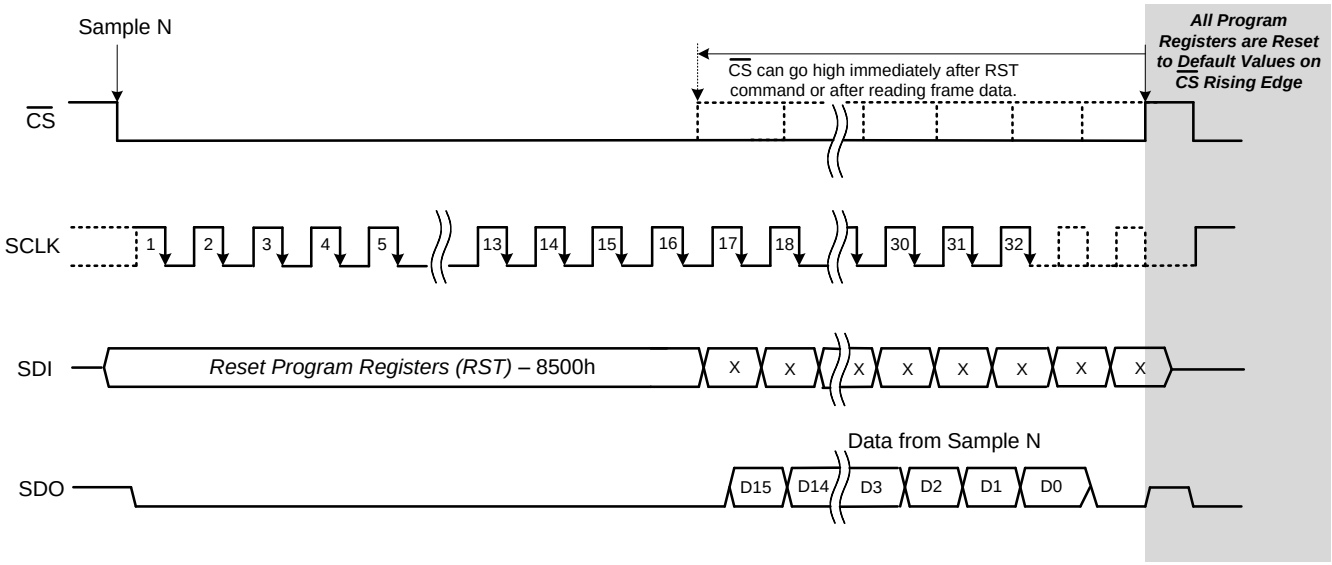

Figure 106. Reset Program Registers (RST) Timing Diagram

8.5 Register Maps

The internal registers of the ADS8684A and ADS8688A are categorized into two categories: command registers and program registers.

The command registers are used to select the channel sequencing mode (AUTO_RST or MAN_Ch_n), configure the device in standby (STDBY) or power-down (PWR_DN) mode, and reset (RST) the program registers to their default values.

The program registers are used to select the sequence of channels for AUTO_RST mode, select the SDO output format, control input range settings for individual channels, control the ALARM feature, reading the alarm flags, and programming the alarm thresholds for each channel.

8.5.1 Command Register Description

The command register is a 16-bit, write-only register that is used to set the operating modes of the ADS8684A and ADS8688A. The settings in this register are used to select the channel sequencing mode (AUTO_RST or MAN_Ch_n), configure the device in standby (STDBY) or power-down (PWR_DN) mode, and reset (RST) the program registers to their default values. All command settings for this register are listed in Table 6. During power-up or reset, the default content of the command register is all 0's and the device waits for a command to be written before being placed into any mode of operation. See Figure 1 for a typical timing diagram for writing a 16-bit command into the device. The device executes the command at the end of this particular data frame when the $\overline{CS}$ signal goes high.

Table 6. Command Register Map

REGISTER	MSB BYTE								LSB BYTE	COMMAND (Hex)	OPERATION IN NEXT FRAME
	B15	B14	B13	B12	B11	B10	B9	B8	B[7:0]		
Continued Operation (NO_OP)	0	0	0	0	0	0	0	0	0000 0000	0000h	Continue operation in previous mode
Standby (STDBY)	1	0	0	0	0	0	1	0	0000 0000	8200h	Device is placed into standby mode
Power Down (PWR_DN)	1	0	0	0	0	0	1	1	0000 0000	8300h	Device is powered down
Reset program registers (RST)	1	0	0	0	0	1	0	1	0000 0000	8500h	Program register is reset to default
Auto Ch. Sequence with Reset (AUTO_RST)	1	0	1	0	0	0	0	0	0000 0000	A000h	Auto mode enabled following a reset
Manual Ch 0 Selection (MAN_Ch_0)	1	1	0	0	0	0	0	0	0000 0000	C000h	Channel 0 input is selected
Manual Ch 1 Selection (MAN_Ch_1)	1	1	0	0	0	1	0	0	0000 0000	C400h	Channel 1 input is selected
Manual Ch 2 Selection (MAN_Ch_2)	1	1	0	0	1	0	0	0	0000 0000	C800h	Channel 2 input is selected
Manual Ch 3 Selection (MAN_Ch_3)	1	1	0	0	1	1	0	0	0000 0000	CC00h	Channel 3 input is selected
Manual Ch 4 Selection (MAN_Ch_4)(1)	1	1	0	1	0	0	0	0	0000 0000	D000h	Channel 4 input is selected
Manual Ch 5 Selection (MAN_Ch_5)	1	1	0	1	0	1	0	0	0000 0000	D400h	Channel 5 input is selected
Manual Ch 6 Selection (MAN_Ch_6)	1	1	0	1	1	0	0	0	0000 0000	D800h	Channel 6 input is selected
Manual Ch 7 Selection (MAN_Ch_7)	1	1	0	1	1	1	0	0	0000 0000	DC00h	Channel 7 input is selected
Manual AUX Selection (MAN_AUX)	1	1	1	0	0	0	0	0	0000 0000	E000h	AUX channel input is selected

(1) Shading indicates bits or registers not included in the 4-channel version of the device.

8.5.2 Program Register Description

The program register is a 16-bit register used to set the operating modes of the ADS8684A and ADS8688A. The settings in this register are used to select the channel sequence for AUTO_RST mode, configure the device ID in daisy-chain mode, select the SDO output format, control input range settings for individual channels, control the ALARM feature, reading the alarm flags, and programming the alarm thresholds for each channel. All program settings for this register are listed in Table 9. During power-up or reset, the different program registers in the device wake up with their default values and the device waits for a command to be written before being placed into any mode of operation.

8.5.2.1 Program Register Read/Write Operation

The program register is a 16-bit read or write register. There must be a minimum of 24 SCLKs after the $\overline{CS}$ falling edge for any read or write operation to the program registers. When $\overline{CS}$ goes low, the SDO line goes low as well. The device receives the command (see Table 7 and Table 8) through SDI where the first seven bits (bits 15-9) represent the register address and the eighth bit (bit 8) is the write or read instruction.

For a write cycle, the next eight bits (bits 7-0) on SDI are the desired data for the addressed register. Over the next eight SCLK cycles, the device outputs this 8-bit data that is written into the register. This data readback allows verification to determine if the correct data are entered into the device. A typical timing diagram for a program register write cycle is shown in Figure 107.

Table 7. Write Cycle Command Word

PIN	REGISTER ADDRESS (Bits 15-9)	WR/$\overline{RD}$ (Bit 8)	DATA (Bits 7-0)
SDI	ADDR[6:0]	1	DIN[7:0]

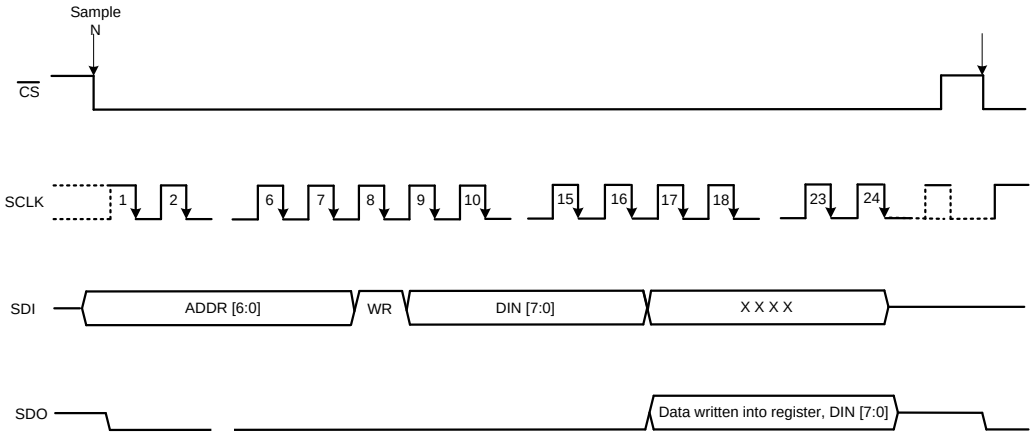

Figure 107. Program Register Write Cycle Timing Diagram

For a read cycle, the next eight bits (bits 7-0) on SDI are *don't care* bits and SDO stays low. From the 16th SCLK falling edge and onwards, SDO outputs the 8-bit data from the addressed register during the next eight clocks, in MSB-first fashion. A typical timing diagram for a program register read cycle is shown in Figure 108.

Table 8. Read Cycle Command Word

PIN	REGISTER ADDRESS (Bits 15-9)	WR/$\overline{RD}$ (Bit 8)	DATA (Bits 7-0)
SDI	ADDR[6:0]	0	XXXXX
SDO	0000 000	0	DOUT[7:0]

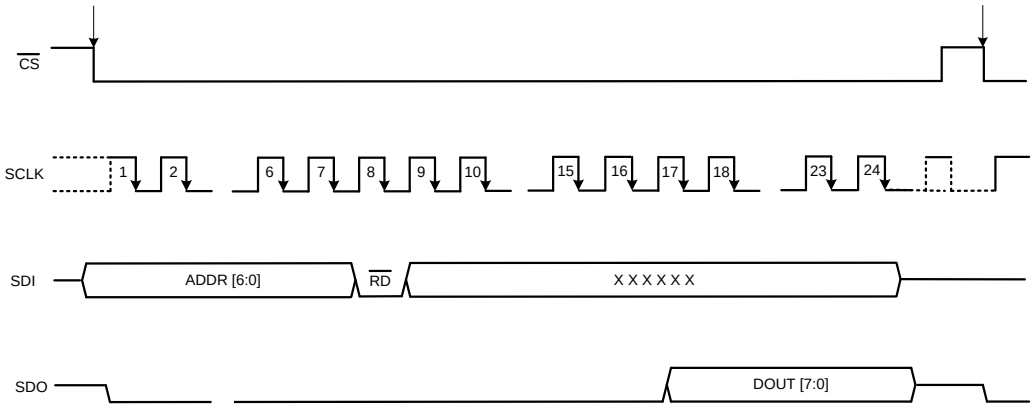

Figure 108. Program Register Read Cycle Timing Diagram

8.5.2.2 Program Register Map

This section provides a bit-by-bit description of each program register.

Table 9. Program Register Map

REGISTER	REGISTER ADDRESS BITS[15:9]	DEFAULT VALUE(1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AUTO SCAN SEQUENCING CONTROL										
AUTO_SEQ_EN	01h	FFh	CH7_EN(2)	CH6_EN	CH5_EN	CH4_EN	CH3_EN	CH2_EN	CH1_EN	CH0_EN
Channel Power Down	02h	00h	CH7_PD	CH6_PD	CH5_PD	CH4_PD	CH3_PD	CH2_PD	CH1_PD	CH0_PD
DEVICE FEATURES SELECTION CONTROL										
Feature Select	03h	00h	DEV[1:0]		0	ALARM_EN0	0	SDO [2:0]		
RANGE SELECT REGISTERS										
Channel 0 Input Range	05h	00h	0	0	0	0	Range Select Channel 0[3:0]			
Channel 1 Input Range	06h	00h	0	0	0	0	Range Select Channel 1[3:0]			
Channel 2 Input Range	07h	00h	0	0	0	0	Range Select Channel 2[3:0]			
Channel 3 Input Range	08h	00h	0	0	0	0	Range Select Channel 3[3:0]			
Channel 4 Input Range	09h	00h	0	0	0	0	Range Select Channel 4[3:0]			
Channel 5 Input Range	0Ah	00h	0	0	0	0	Range Select Channel 5[3:0]			
Channel 6 Input Range	0Bh	00h	0	0	0	0	Range Select Channel 6[3:0]			
Channel 7 Input Range	0Ch	00h	0	0	0	0	Range Select Channel 7[3:0]			
ALARM FLAG REGISTERS (Read-Only)										
ALARM Overview Tripped-Flag	10h	00h	Tripped Alarm Flag Ch7	Tripped Alarm Flag Ch6	Tripped Alarm Flag Ch5	Tripped Alarm Flag Ch4	Tripped Alarm Flag Ch3	Tripped Alarm Flag Ch2	Tripped Alarm Flag Ch1	Tripped Alarm Flag Ch0
ALARM Ch 0-3 Tripped-Flag	11h	00h	Tripped Alarm Flag Ch0 Low	Tripped Alarm Flag Ch0 High	Tripped Alarm Flag Ch1 Low	Tripped Alarm Flag Ch1 High	Tripped Alarm Flag Ch2 Low	Tripped Alarm Flag Ch2 High	Tripped Alarm Flag Ch3 Low	Tripped Alarm Flag Ch3 High
ALARM Ch 0-3 Active-Flag	12h	00h	Active Alarm Flag Ch0 Low	Active Alarm Flag Ch0 High	Active Alarm Flag Ch1 Low	Active Alarm Flag Ch1 High	Active Alarm Flag Ch2 Low	Active Alarm Flag Ch2 High	Active Alarm Flag Ch3 Low	Active Alarm Flag Ch3 High
ALARM Ch 4-7 Tripped-Flag	13h	00h	Tripped Alarm Flag Ch4 Low	Tripped Alarm Flag Ch4 High	Tripped Alarm Flag Ch5 Low	Tripped Alarm Flag Ch5 High	Tripped Alarm Flag Ch6 Low	Tripped Alarm Flag Ch6 High	Tripped Alarm Flag Ch7 Low	Tripped Alarm Flag Ch7 High
ALARM Ch 4-7 Active-Flag	14h	00h	Active Alarm Flag Ch4 Low	Active Alarm Flag Ch4 High	Active Alarm Flag Ch5 Low	Active Alarm Flag Ch5 High	Active Alarm Flag Ch6 Low	Active Alarm Flag Ch6 High	Active Alarm Flag Ch7 Low	Active Alarm Flag Ch7 High

(1) All registers are reset to the default values at power-on or at device reset using the register settings method.
(2) Shading indicates bits or registers that are not included in the 4-channel version of the device. A write operation on any of these bits or registers has no effect on device behavior. A read operation on any of these bits or registers outputs all 1's on the SDO line.

Table 9. Program Register Map (continued)

REGISTER	REGISTER ADDRESS BITS[15:9]	DEFAULT VALUE(1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ALARM THRESHOLD REGISTERS										
Ch 0 Hysteresis	15h	00h	CH0_HYST[7:0]							
Ch 0 High Threshold MSB	16h	FFh	CH0_HT[15:8]							
Ch 0 High Threshold LSB	17h	FFh	CH0_HT[7:0]							
Ch 0 Low Threshold MSB	18h	00h	CH0_LT[15:8]							
Ch 0 Low Threshold LSB	19h	00h	CH0_LT[7:0]							
…	…	…	… See the *Alarm Threshold Setting Registers* for details regarding the ALARM threshold settings registers. …							
Ch 7 Hysteresis	38h	00h	CH7_HYST[7:0]							
Ch 7 High Threshold MSB	39h	FFh	CH7_HT[15:8]							
Ch 7 High Threshold LSB	3Ah	FFh	CH7_HT[7:0]							
Ch 7 Low Threshold MSB	3Bh	00h	CH7_LT[15:8]							
Ch 7 Low Threshold LSB	3Ch	00h	CH7_LT[7:0]							
COMMAND READ BACK (Read-Only)										
Command Read Back	3Fh	00h	COMMAND_WORD[7:0]							

8.5.2.3 Program Register Descriptions

8.5.2.3.1 Auto-Scan Sequencing Control Registers

In AUTO_RST mode, the device automatically scans the preselected channels in ascending order with a new channel selected for every conversion. Each individual channel can be selectively included in the auto channel sequencing. For channels not selected for auto sequencing, the analog front-end circuitry can be individually powered down.

8.5.2.3.1.1 Auto-Scan Sequence Enable Register (address = 01h)

This register selects individual channels for sequencing in AUTO_RST mode. The default value for this register is FFh, which implies that in default condition all channels are included in the auto-scan sequence. If no channels are included in the auto sequence (that is, the value for this register is 00h), then channel 0 is selected for conversion by default.

Figure 109. AUTO_SEQ_EN Register

7	6	5	4	3	2	1	0
CH7_EN(1)	CH6_EN	CH5_EN	CH4_EN	CH3_EN	CH2_EN	CH1_EN	CH0_EN
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

(1) Shading indicates bits or registers that are not included in the 4-channel version of the device. A write operation on any of these bits or registers has no effect on device behavior. A read operation on any of these bits or registers outputs all 1's on the SDO line.

Table 10. AUTO_SEQ_EN Field Descriptions

Bit	Field	Type	Reset	Description
7	CH7_EN	R/W	1h	Channel 7 enable. 0 = Channel 7 is not selected for sequencing in AUTO_RST mode 1 = Channel 7 is selected for sequencing in AUTO_RST mode
6	CH6_EN	R/W	1h	Channel 6 enable. 0 = Channel 6 is not selected for sequencing in AUTO_RST mode 1 = Channel 6 is selected for sequencing in AUTO_RST mode
5	CH5_EN	R/W	1h	Channel 5 enable. 0 = Channel 5 is not selected for sequencing in AUTO_RST mode 1 = Channel 5 is selected for sequencing in AUTO_RST mode
4	CH4_EN	R/W	1h	Channel 4 enable. 0 = Channel 4 is not selected for sequencing in AUTO_RST mode 1 = Channel 4 is selected for sequencing in AUTO_RST mode
3	CH3_EN	R/W	1h	Channel 3 enable. 0 = Channel 3 is not selected for sequencing in AUTO_RST mode 1 = Channel 3 is selected for sequencing in AUTO_RST mode
2	CH2_EN	R/W	1h	Channel 2 enable. 0 = Channel 2 is not selected for sequencing in AUTO_RST mode 1 = Channel 2 is selected for sequencing in AUTO_RST mode
1	CH1_EN	R/W	1h	Channel 1 enable. 0 = Channel 1 is not selected for sequencing in AUTO_RST mode 1 = Channel 1 is selected for sequencing in AUTO_RST mode
0	CH0_EN	R/W	1h	Channel 0 enable. 0 = Channel 0 is not selected for sequencing in AUTO_RST mode 1 = Channel 0 is selected for sequencing in AUTO_RST mode

8.5.2.3.1.2 Channel Power Down Register (address = 02h)

This register powers down individual channels that are not included for sequencing in AUTO_RST mode. The default value for this register is 00h, which implies that in default condition all channels are powered up. If all channels are powered down (that is, the value for this register is FFh), then the analog front-end circuits for all channels are powered down and the output of the ADC contains invalid data. If the device is in MAN-Ch_n mode and the selected channel is powered down, then the device yields invalid output that can also trigger a false alarm condition.

Figure 110. Channel Power Down Register

7	6	5	4	3	2	1	0
CH7_PD(1)	CH6_PD	CH5_PD	CH4_PD	CH3_PD	CH2_PD	CH1_PD	CH0_PD
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

(1) Shading indicates bits or registers that are not included in the 4-channel version of the device. A write operation on any of these bits or registers has no effect on device behavior. A read operation on any of these bits or registers outputs all 1's on the SDO line.

Table 11. Channel Power Down Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH7_PD	R/W	0h	Channel 7 power-down. 0 = The analog front-end on channel 7 is powered up and channel 7 can be included in the AUTO_RST sequence 1 = The analog front-end on channel 7 is powered down and channel 7 cannot be included in the AUTO_RST sequence
6	CH6_PD	R/W	0h	Channel 6 power-down. 0 = The analog front-end on channel 6 is powered up and channel 6 can be included in the AUTO_RST sequence 1 = The analog front-end on channel 6 is powered down and channel 6 cannot be included in the AUTO_RST sequence
5	CH5_PD	R/W	0h	Channel 5 power-down. 0 = The analog front-end on channel 5 is powered up and channel 5 can be included in the AUTO_RST sequence 1 = The analog front-end on channel 5 is powered down and channel 5 cannot be included in the AUTO_RST sequence
4	CH4_PD	R/W	0h	Channel 4 power-down. 0 = The analog front-end on channel 4 is powered up and channel 4 can be included in the AUTO_RST sequence 1 = The analog front-end on channel 4 is powered down and channel 4 cannot be included in the AUTO_RST sequence
3	CH3_PD	R/W	0h	Channel 3 power-down. 0 = The analog front-end on channel 3 is powered up and channel 3 can be included in the AUTO_RST sequence 1 = The analog front end on channel 3 is powered down and channel 3 cannot be included in the AUTO_RST sequence
2	CH2_PD	R/W	0h	Channel 2 power-down. 0 = The analog front end on channel 2 is powered up and channel 2 can be included in the AUTO_RST sequence 1 = The analog front end on channel 2 is powered down and channel 2 cannot be included in the AUTO_RST sequence
1	CH1_PD	R/W	0h	Channel 1 power-down. 0 = The analog front end on channel 1 is powered up and channel 1 can be included in the AUTO_RST sequence 1 = The analog front end on channel 1 is powered down and channel 1 cannot be included in the AUTO_RST sequence
0	CH0_PD	R/W	0h	Channel 0 power-down. 0 = The analog front end on channel 0 is powered up and channel 0 can be included in the AUTO_RST sequence 1 = The analog front end on channel 0 is powered down and channel 0 cannot be included in the AUTO_RST sequence

8.5.2.3.2 Device Features Selection Control Register (address = 03h)

The bits in this register can be used to configure the device ID for daisy-chain operation, enable the ALARM feature, and configure the output bit format on SDO.

Figure 111. Feature Select Register

7	6	5	4	3	2	1	0
DEV[1:0]		0	ALARM_EN	0	SDO[2:0]		
R/W-0h		R-0h	R/W-0h	R-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. Feature Select Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DEV[1:0]	R/W	0h	Device ID bits. 00 = ID for device 0 in daisy-chain mode 01 = ID for device 1 in daisy-chain mode 10 = ID for device 2 in daisy-chain mode 11 = ID for device 3 in daisy-chain mode
5	0	R	0h	Must always be set to 0
4	0	R/W	0h	ALARM feature enable. 0 = ALARM feature is disabled 1 = ALARM feature is enabled
3	0	R	0h	Must always be set to 0
2-0	SDO[2:0]	R/W	0h	SDO data format bits (see Table 13).

Table 13. Description of Program Register Bits for SDO Data Format

SDO FORMAT SDO[2:0]	BEGINNING OF THE OUTPUT BIT STREAM	OUTPUT FORMAT			
		BITS 24-9	BITS 8-5	BITS 4-3	BITS 2-0
000	16th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	SDO pulled low		
001	16th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	Channel address(1)	SDO pulled low	
010	16th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	Channel address(1)	Device address(1)	SDO pulled low
011	16th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	Channel address(1)	Device address(1)	Input range(1)

(1) Table 14 lists the bit descriptions for these channel addresses, device addresses, and input range.

Table 14. Bit Description for the SDO Data

BIT	BIT DESCRIPTION
24-9	16 bits of conversion result for the channel represented in MSB-first format.
8-5	Four bits of channel address. 0000 = Channel 0 0001 = Channel 1 0010 = Channel 2 0011 = Channel 3 0100 = Channel 4 (valid only for the ADS8688A) 0101 = Channel 5 (valid only for the ADS8688A) 0110 = Channel 6 (valid only for the ADS8688A) 0111 = Channel 7 (valid only for the ADS8688A)
4-3	Two bits of device address (mainly useful in daisy-chain mode).
2-0	Three LSB bits of input voltage range (see the *Range Select Registers* section).

8.5.2.3.3 Range Select Registers (addresses 05h-0Ch)

Address 05h corresponds to channel 0, address 06h corresponds to channel 1, address 07h corresponds to channel 2, address 08h corresponds to channel 3, address 09h corresponds to channel 4, address 0Ah corresponds to channel 5, address 0Bh corresponds to channel 6, and address 0Ch corresponds to channel 7.

These registers allow the selection of input ranges for all individual channels (n = 0 to 3 for the ADS8684A and n = 0 to 7 for the ADS8688A). The default value for these registers is 00h.

Figure 112. Channel *n* Input Range Registers

7	6	5	4	3	2	1	0
0	0	0	0	Range_CH*n*[3:0]			
R-0h	R-0h	R-0h	R-0h	R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. Channel *n* Input Range Registers Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R	0h	Must always be set to 0
3-0	Range_CH*n*[3:0]	R/W	0h	Input range selection bits for channel n (n = 0 to 3 for the ADS8684A and n = 0 to 7 for the ADS8688A). 0000 = Input range is set to ±2.5 x V_{REF} 0001 = Input range is set to ±1.25 x V_{REF} 0010 = Input range is set to ±0.625 x V_{REF} 0011 = Input range is set to ±0.3125 x V_{REF} 1011 = Input range is set to ±0.15625 x V_{REF} 0101 = Input range is set to 0 to 2.5 x V_{REF} 0110 = Input range is set to 0 to 1.25 x V_{REF} 0111 = Input range is set to 0 to 0.625 x V_{REF} 1111 = Input range is set to 0 to 0.3125 x V_{REF}

8.5.2.3.4 Alarm Flag Registers (Read-Only)

The alarm conditions related to individual channels are stored in these registers. The flags can be read when an alarm interrupt is received on the ALARM pin. There are two types of flag for every alarm: active and tripped. The active flag is set to 1 under the alarm condition (when data cross the alarm limit) and remains so as long as the alarm condition persists. The tripped flag turns on the alarm condition similar to the active flag, but remains set until read. This feature relieves the device from having to track alarms.

8.5.2.3.4.1 ALARM Overview Tripped-Flag Register (address = 10h)

The ALARM overview tripper-flags register contains the logical OR of high or low tripped alarm flags for all eight channels.

Figure 113. ALARM Overview Tripped-Flag Register

7	6	5	4	3	2	1	0
Tripped Alarm Flag Ch7(1)	Tripped Alarm Flag Ch6	Tripped Alarm Flag Ch5	Tripped Alarm Flag Ch4	Tripped Alarm Flag Ch3	Tripped Alarm Flag Ch2	Tripped Alarm Flag Ch1	Tripped Alarm Flag Ch0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

(1) Shading indicates bits or registers that are not included in the 4-channel version of the device. A write operation on any of these bits or registers has no effect on device behavior. A read operation on any of these bits or registers outputs all 1's on the SDO line.

Table 16. ALARM Overview Tripped-Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Tripped Alarm Flag Ch7	R	0h	Tripped alarm flag for all analog channels at a glance. Each individual bit indicates a tripped alarm flag status for each channel, as per the alarm flags register for channels 7 to 0, respectively. 0 = No alarm detected 1 = Alarm detected
6	Tripped Alarm Flag Ch6	R	0h	
5	Tripped Alarm Flag Ch5	R	0h	
4	Tripped Alarm Flag Ch4	R	0h	
3	Tripped Alarm Flag Ch3	R	0h	
2	Tripped Alarm Flag Ch2	R	0h	
1	Tripped Alarm Flag Ch1	R	0h	
0	Tripped Alarm Flag Ch0	R	0h	

8.5.2.3.4.2 Alarm Flag Registers: Tripped and Active (address = 11h to 14h)

There are two alarm thresholds (high and low) per channel, with two flags for each threshold. An active alarm flag is enabled when an alarm is triggered (when data cross the alarm threshold) and remains enabled as long as the alarm condition persists. A tripped alarm flag is enabled in the same manner as an active alarm flag, but remains latched until read. Registers 11h to 14h in the program registers store the active and tripped alarm flags for all individual eight channels.

Figure 114. ALARM Ch0-3 Tripped-Flag Register (address = 11h)

7	6	5	4	3	2	1	0
Tripped Alarm Flag Ch0 Low	Tripped Alarm Flag Ch0 High	Tripped Alarm Flag Ch1 Low	Tripped Alarm Flag Ch1 High	Tripped Alarm Flag Ch2 Low	Tripped Alarm Flag Ch2 High	Tripped Alarm Flag Ch3 Low	Tripped Alarm Flag Ch3 High
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

Table 17. ALARM Ch0-3 Tripped-Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Tripped Alarm Flag Ch n Low or High (n = 0 to 3)	R	0h	Tripped alarm flag high, low for channel n (n = 0 to 3) Each individual bit indicates an active high or low alarm flag status for each channel, as per the alarm flags register for channels 0 to 7. 0 = No alarm detected 1 = Alarm detected

Figure 115. ALARM Ch0-3 Active-Flag Register (address = 12h)

7	6	5	4	3	2	1	0
Active Alarm Flag Ch0 Low	Active Alarm Flag Ch0 High	Active Alarm Flag Ch1 Low	Active Alarm Flag Ch1 High	Active Alarm Flag Ch2 Low	Active Alarm Flag Ch2 High	Active Alarm Flag Ch3 Low	Active Alarm Flag Ch3 High
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

Table 18. ALARM Ch0-3 Active-Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Active Alarm Flag Ch n Low or High (n = 0 to 3)	R	0h	Active alarm flag high, low for channel n (n = 0 to 3) Each individual bit indicates an active high or low alarm flag status for each channel, as per the alarm flags register for channels 0 to 7. 0 = No alarm detected 1 = Alarm detected

Figure 116. ALARM Ch4-7 Tripped-Flag Register (address = 13h)(1)

7	6	5	4	3	2	1	0
Tripped Alarm Flag Ch4 Low	Tripped Alarm Flag Ch4 High	Tripped Alarm Flag Ch5 Low	Tripped Alarm Flag Ch5 High	Tripped Alarm Flag Ch6 Low	Tripped Alarm Flag Ch6 High	Tripped Alarm Flag Ch7 Low	Tripped Alarm Flag Ch7 High
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

(1) This register is not included in the 4-channel version of the device. A write operation on this register has no effect on device behavior. A read operation on this register outputs all 1's on the SDO line.

Table 19. ALARM Ch4-7 Tripped-Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Tripped Alarm Flag Ch n Low or High (n = 4 to 7)	R	0h	Tripped alarm flag high, low for channel n (n = 4 to 7). Each individual bit indicates an active high or low alarm flag status for each channel, as per the alarm flags register for channels 0 to 7. 0 = No alarm detected 1 = Alarm detected

Figure 117. ALARM Ch4-7 Active-Flag Register (address = 14h)(1)

7	6	5	4	3	2	1	0
Active Alarm Flag Ch4 Low	Active Alarm Flag Ch4 High	Active Alarm Flag Ch5 Low	Active Alarm Flag Ch5 High	Active Alarm Flag Ch6 Low	Active Alarm Flag Ch6 High	Active Alarm Flag Ch7 Low	Active Alarm Flag Ch7 High
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

(1) This register is not included in the 4-channel version of the device. A write operation on this register has no effect on device behavior. A read operation on this register outputs all 1's on the SDO line.

Table 20. ALARM Ch4-7 Active-Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Active Alarm Flag Ch n Low or High (n = 4 to 7)	R	0h	Active alarm flag high, low for channel n (n = 4 to 7). Each individual bit indicates an active high or low alarm flag status for each channel, as per the alarm flags register for channels 0 to 7. 0 = No alarm detected 1 = Alarm detected

8.5.2.3.5 Alarm Threshold Setting Registers

The ADS8684A and ADS8688A feature individual high and low alarm threshold settings for each channel. Each alarm threshold is 16 bits wide with 8-bit hysteresis, which is the same for both high and low threshold settings. This 40-bit setting is accomplished through five 8-bit registers associated with every high and low alarm.

NAME	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Ch 0 Hysteresis	15h	CH0_HYST[7:0]							
Ch 0 High Threshold MSB	16h	CH0_HT[15:8]							
Ch 0 High Threshold LSB	17h	CH0_HT[7:0]							
Ch 0 Low Threshold MSB	18h	CH0_LT[15:8]							
Ch 0 Low Threshold LSB	19h	CH0_LT[7:0]							
Ch 1 Hysteresis	1Ah	CH1_HYST[7:0]							
Ch 1 High Threshold MSB	1Bh	CH1_HT[15:8]							
Ch 1 High Threshold LSB	1Ch	CH1_HT[7:0]							
Ch 1 Low Threshold MSB	1Dh	CH1_LT[15:8]							
Ch 1 Low Threshold LSB	1Eh	CH1_LT[7:0]							
Ch 2 Hysteresis	1Fh	CH2_HYST[7:0]							
Ch 2 High Threshold MSB	20h	CH2_HT[15:8]							
Ch 2 High Threshold LSB	21h	CH2_HT[7:0]							
Ch 2 Low Threshold MSB	22h	CH2_LT[15:8]							
Ch 2 Low Threshold LSB	23h	CH2_LT[7:0]							
Ch 3 Hysteresis	24h	CH3_HYST[7:0]							
Ch 3 High Threshold MSB	25h	CH3_HT[15:8]							
Ch 3 High Threshold LSB	26h	CH3_HT[7:0]							
Ch 3 Low Threshold MSB	27h	CH3_LT[15:8]							
Ch 3 Low Threshold LSB	28h	CH3_LT[7:0]							
Ch 4 Hysteresis(1)	29h	CH4_HYST[7:0]							
Ch 4 High Threshold MSB	2Ah	CH4_HT[15:8]							
Ch 4 High Threshold LSB	2Bh	CH4_HT[7:0]							
Ch 4 Low Threshold MSB	2Ch	CH4_LT[15:8]							
Ch 4 Low Threshold LSB	2Dh	CH4_LT[7:0]							
Ch 5 Hysteresis	2Eh	CH5_HYST[7:0]							
Ch 5 High Threshold MSB	2Fh	CH5_HT[15:8]							
Ch 5 High Threshold LSB	30h	CH5_HT[7:0]							
Ch 5 Low Threshold MSB	31h	CH5_LT[15:8]							
Ch 5 Low Threshold LSB	32h	CH5_LT[7:0]							
Ch 6 Hysteresis	33h	CH6_HYST[7:0]							
Ch 6 High Threshold MSB	34h	CH6_HT[15:8]							
Ch 6 High Threshold LSB	35h	CH6_HT[7:0]							
Ch 6 Low Threshold MSB	36h	CH6_LT[15:8]							
Ch 6 Low Threshold LSB	37h	CH6_LT[7:0]							
Ch 7 Hysteresis	38h	CH7_HYST[7:0]							
Ch 7 High Threshold MSB	39h	CH7_HT[15:8]							
Ch 7 High Threshold LSB	3Ah	CH7_HT[7:0]							
Ch 7 Low Threshold MSB	3Bh	CH7_LT[15:8]							
Ch 7 Low Threshold LSB	3Ch	CH7_LT[7:0]							

(1) Shading indicates bits or registers not included in the 4-channel version of the device.

Figure 118. Ch n Hysteresis Registers

7	6	5	4	3	2	1	0
CHn_HYST[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. Channel *n* Hysteresis Register Field Descriptions (n = 0 to 7 for the ADS8688A; n = 0 to 3 for the ADS8684A)

Bit	Field	Type	Reset	Description
7-0	Channel *n* Hysteresis[7-0] (n = 0 to 7 for the ADS8688A; n = 0 to 3 for the ADS8684A)	R/W	0h	These bits set the channel high and low alarm hysteresis for channel *n (n = 0 to 7 for the ADS8688A; n = 0 to 3 for the ADS8684A)* For example, bits 7-0 of the channel 0 register (address 15h) set the channel 0 alarm hysteresis. 00000000 = No hysteresis 00000001 = ±1-LSB hysteresis 00000010 to 11111110 = ±2-LSB to ±254-LSB hysteresis 11111111 = ±255-LSB hysteresis

Figure 119. Ch n High Threshold MSB Registers

7	6	5	4	3	2	1	0
CHn_HT[15:8]							
R/W-1h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 22. Channel *n* High Threshold MSB Register Field Descriptions (n = 0 to 7 for the ADS8688A; n = 0 to 3 for the ADS8684A)

Bit	Field	Type	Reset	Description
7-0	CH*n*_HT[15:8] (n = 0 to 7 for the ADS8688A; n = 0 to 3 for the ADS8684A)	R/W	1h	These bits set the MSB byte for the 16-bit channel *n* high alarm. For example, bits 7-0 of the channel 0 register (address 16h) set the MSB byte for the channel 0 high alarm threshold. The channel 0 high alarm threshold is AAFFh when bits 7-0 of the ch 0 high threshold MSB register (address 16h) are set to AAh and bits 7-0 of the ch 0 high threshold LSB register (address 17h) are set to FFh. 0000 0000 = MSB byte is 00h 0000 0001 = MSB byte is 01h 0000 0010 to 1110 1111 = MSB byte is 02h to FEh 1111 1111 = MSB byte is FFh

Figure 120. Ch n High Threshold LSB Registers

7	6	5	4	3	2	1	0
CHn_HT[7:0]							
R/W-1h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. Channel *n* High Threshold LSB Register Field Descriptions (n = 0 to 7 for the ADS8688A; n = 0 to 3 for the ADS8684A)

Bit	Field	Type	Reset	Description
7-0	CH*n*_HT[7-0] (n = 0 to 7 for the ADS8688A; n = 0 to 3 for the ADS8684A)	R/W	1h	These bits set the LSB for the 16-bit channel *n* high alarm. For example, bits 7-0 of the channel 0 register (address 17h) set the LSB for the channel 0 high alarm threshold. The channel 0 high alarm threshold is AAFFh when bits 7-0 of the ch 0 high threshold MSB register (address 16h) are set to AAh and bits 7-0 of the ch 0 high threshold LSB register (address 17h) are set to FFh. 0000 0000 = LSB byte is 00h 0000 0001 = LSB byte is 01h 0000 0010 to 1111 1110 = LSB byte is 02h to FEh 1111 1111 = LSB byte is FFh

Figure 121. Ch n Low Threshold MSB Registers

7	6	5	4	3	2	1	0
CHn_LT[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 24. Channel *n* Low Threshold MSB Register Field Descriptions (n = 0 to 7 for the ADS8688A; n = 0 to 3 for the ADS8684A)

Bit	Field	Type	Reset	Description
7-0	CH*n*_LT[15:8] (n = 0 to 7 for the ADS8688A; n = 0 to 3 for the ADS8684A)	R/W	0h	These bits set the MSB byte for the 16-bit channel *n* low alarm. For example, bits 7-0 of the channel 0 register (address 18h) set the MSB byte for the channel 0 low alarm threshold. The channel 0 low alarm threshold is AAFFh when bits 7-0 of the ch 0 low threshold MSB register (address 18h) are set to AAh and bits 7-0 of the ch 0 low threshold LSB register (address 19h) are set to FFh. 0000 0000 = MSB byte is 00h 0000 0001 = MSB byte is 01h 0000 0010 to 1110 1111 = MSB byte is 02h to FEh 1111 1111 = MSB byte is FFh

Figure 122. Ch n Low Threshold LSB Registers

7	6	5	4	3	2	1	0
CHn_LT[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. Channel *n* Low Threshold MSB Register Field Descriptions (n = 0 to 7 for the ADS8688A; n = 0 to 3 for the ADS8684A)

Bit	Field	Type	Reset	Description
7-0	CH*n*_LT[7-0] (n = 0 to 7 for the ADS8688A; n = 0 to 3 for the ADS8684A)	R/W	0h	These bits set the LSB for the 16-bit channel *n* low alarm. For example, bits 7-0 of the channel 0 register (address 19h) set the LSB for the channel 0 low alarm threshold. The channel 0 low alarm threshold is AAFFh when bits 7-0 of the ch 0 low threshold MSB register (address 18h) are set to AAh and bits 7-0 of the ch 0 low threshold LSB register (address 19h) are set to FFh. 0000 0000 = LSB byte is 00h 0000 0001 = LSB byte is 01h 0000 0010 to 1110 1111 = LSB byte is 02h to FEh 1111 1111 = LSB byte is FFh

8.5.2.3.6 Command Read-Back Register (address = 3Fh)

This register allows the device mode of operation to be read. On execution of this command, the device outputs the command word executed in the previous data frame. The output of the command register appears on SDO from the 16th falling edge onwards in an MSB-first format. All information regarding the command register is contained in the first eight bits and the last eight bits are 0 (see Table 6), thus the command read-back operation can be stopped after the 24th SCLK cycle.

Figure 123. Command Read-Back Register

7	6	5	4	3	2	1	0
COMMAND_WORD[15:8]							
R-0h							

LEGEND: R = Read only; -n = value after reset

Table 26. Command Read-Back Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	COMMAND_WORD[15:8]	R	0h	Command executed in previous data frame.