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ECE 5780
Post Questions Lab 2

1. Why can't you use both pins PA0 and PC0 for external interrupts at the same time?

Both PA0 and PC0 share the same mux/ EXTI line, so they cannot operate the interrupts at the same time.

2. What software priority level gives the highest priority? What level gives the lowest?

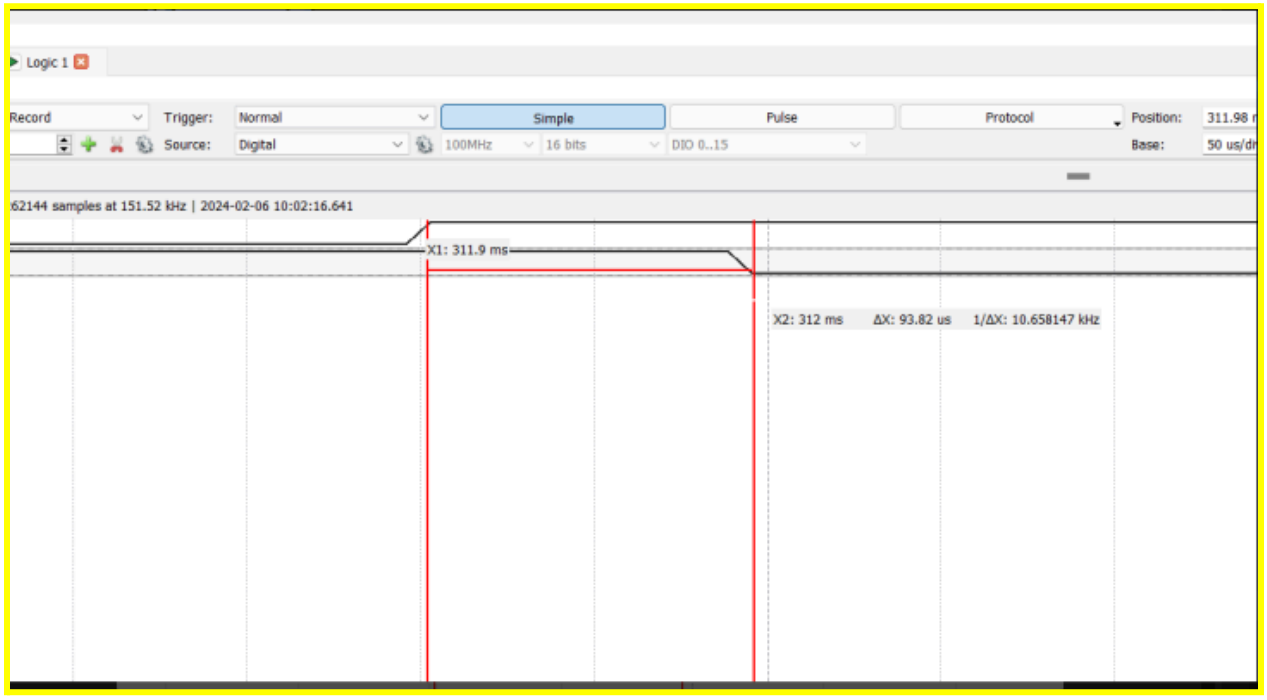
For the software priority level, 0 gives the highest priority, while 3 is the lowest priority.

3. How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? Which bits in the group are implemented?

EAch IPR Register has four 8-bit regions that the NVIC have reserved in its priority registers for each interrupt. The NVIC within the STM32F0 only has the uppermost two bits from these regions implemented, giving four possible configurable priority levels (0-3).

4. What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.

The latency between pushing the Discovery board button and the LED change is 93.82 µs, this was measured with the logic analyzer.



5. Why do you need to clear status flag bits in peripherals when servicing their interrupts?

The handlers will keep running and looping until the flag is notified where to finish, which is why we need to clear the status flag bits. If the status flag bit was not cleared, then the request would never be acknowledged as done.