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ECE 5780

Post Lab 3 - Timers Post-Lab Questions

1. Using a timer clock source of 8 MHz, calculate PSC and ARR values to get a 60 Hz interrupt. • This is tricky because precisely 60 Hz is impossible with our system; instead, think about the process and minimize the error. Many combinations of PSC and ARR values work—not just one!

Using the Arr = fclk/((PSC+1)*Ftarget) function, I was able to interpret the PSC value to be 59, which I chose because it was a value close to 60 that gives me a better estimate of being precise. The outcome gave me an ARR value of around 2222. We also experimented with other PSC and ARR values to better understand the correlation of the timers and notice how one LED can start getting dimmer and the other could get brighter.

2. Look through the Table 13 "STM32F072x8/xB pin definitions" in the chip datasheet and list all pins that can have the timer 3 capture/compare channel 1 alternate function. • If the pin is included on the LQFP64 package that we are using, list the alternate function number that you would use to select it.

The pines that can have the timer 3 capture/compare chanel 1 alternate function is:

- PE3, which doesn’t have an alternation function number

- PA6, which is AF1
- PC6, which is AF0
- PB4, which is AF1

3. List your measured value of the timer UEV interrupt period from first experiment.

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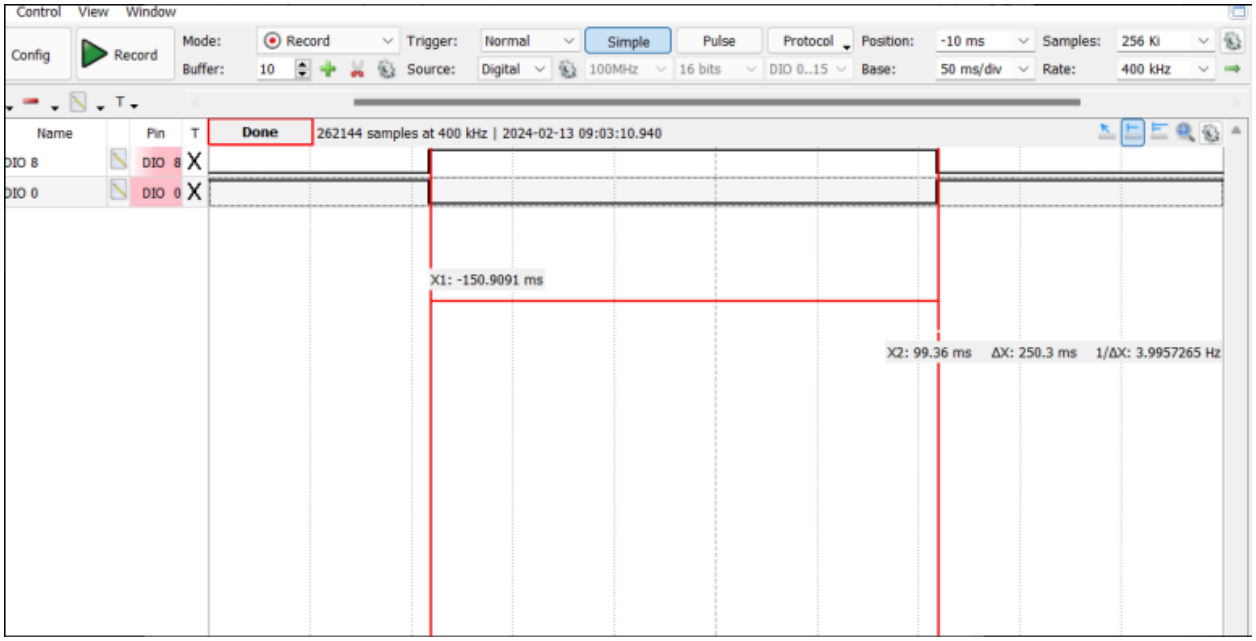
In this screenshot, it shows our measured value of the timer UEV interrupt period from the 1st experiment, I also verified with Christian and he says that the screenshot was good.



4. Describe what happened to the measured duty-cycle as the CCRx value increased in PWM mode 1.

In PWM mode 1, elevating the CCRx value leads to an increase in the duty cycle, as the CCRx value directly influences the width of the PWM signal's pulse. Consequently, a higher CCRx

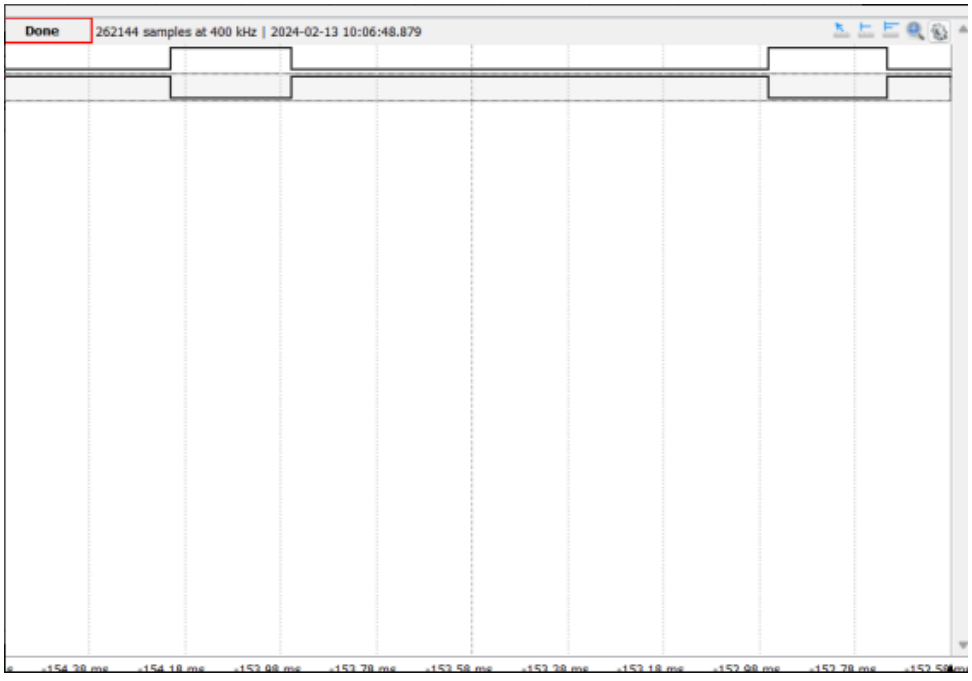
value results in an extended pulse width, thereby augmenting the duty cycle. This can be shown as a brighter LED was lighted up for the Red led.

5. Describe what happened to the measured duty-cycle as the CCRx value increased in PWM mode 2.

In PWM mode 2, the duty cycle is determined by the value of the CCRx register. As the CCRx value increases, the duty cycle also increases. This is because the CCRx register determines the point at which the PWM signal goes high. A higher CCRx value means that the PWM signal will go high later in the period, which results in a higher duty cycle. This is shown in a brighter blue led during the experiment.

6. Include at least one logic analyzer screenshot of a PWM capture.

We also verified with Christian about this screenshot and he said it was good.



7. What PWM mode is shown in figure 3.6 of the lab manual (PWM mode 1 or 2)?

The PWM mode that is shown in figure 3.6 is showing PWM mode 2.