Project 4 Switch Queueing Scheme

Yifan Li yifanl 18-756

Design

Input Queueing Scheme

In implementation of input queueing, the size of input nic's buffer is set to be N, the size of output nic's buffer is set to be 1. The packet will only be dropped when the input buffer is full. If the output buffer size is full, it means there is already an input port destined to the target output. In this case, the packet has wait in the queue until next tock. Inside each tock, the sending inside the switch begins from a random input queue to keep fair for each port. Then, the next input queue of the starting queue will be served.

Output Queueing Scheme

In implementation of input queueing, the size of input nic's buffer is set to be 1, the size of output nic's buffer is set to be N. For each tock, all of the input queues will be served. This implies the switch speed should be faster than the input queueing scheme. The output queue size N is set to be a large number to ensure the high throughput of the scheme. However, if the queue is full, the packet would be dropped.

The testing packets generating scheme

The packets are generated before starting to send. For each source computer, there will be one packet destined to a random destination computer. The number_packets_per_nic specifies the number of packets that will be generated on each computer. Since the line speed of between nics is one packet per tock. So, these packets will be sent to the switch at the rate of 1 packet per tock per computer.

Analysis

The overall performance of Input and Output Queueing

I set the input queue size to be 10 and the number of computers to be 32, the performance of the input queueing is shown in the figure 1. When the number of the input packets becomes larger and larger, the throughput converged to somewhere around 59.40% and the average delay converges to 16.82 tocks.

I set the output queue size to be 100 and the number of computers to be 32, the performance of the output queueing is shown in the figure 2. The figure shows that the throughput of the output queueing scheme is very close to the 100%. Even though when number of packets become very big, the throughput falls a little bit, it is fair to say output queueing will have a very high throughput at very large traffic. However, the average delay of the output queueing tempts to grow very fast. When the number of packets is big enough, the output queuing delay is longer than input queueing.

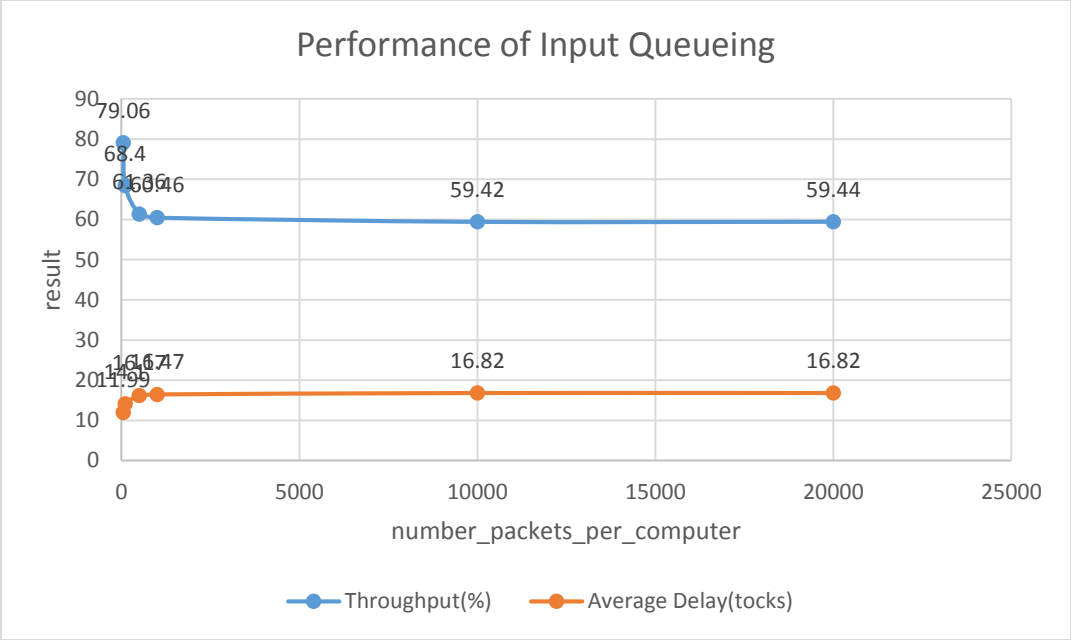

Figure 1

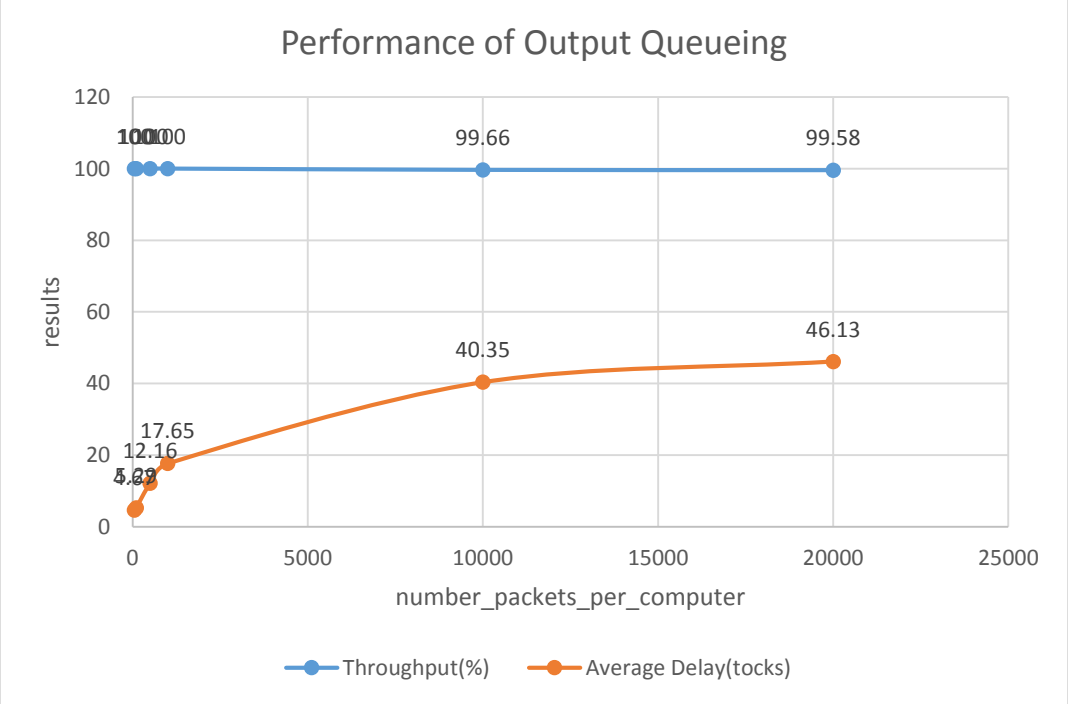

Figure 2

The impact of switch size

As we can see in the figure 3 and figure 4, the switch size won't affect the performance of the output queueing. However, as switch size increases, the performance of the input queueing will drop and finally get around 59%.

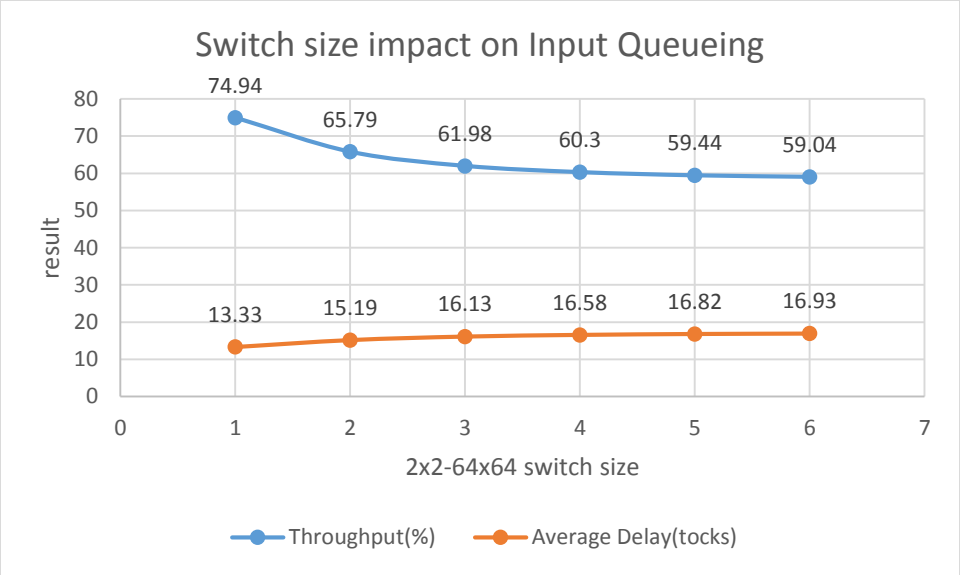

Figure 3

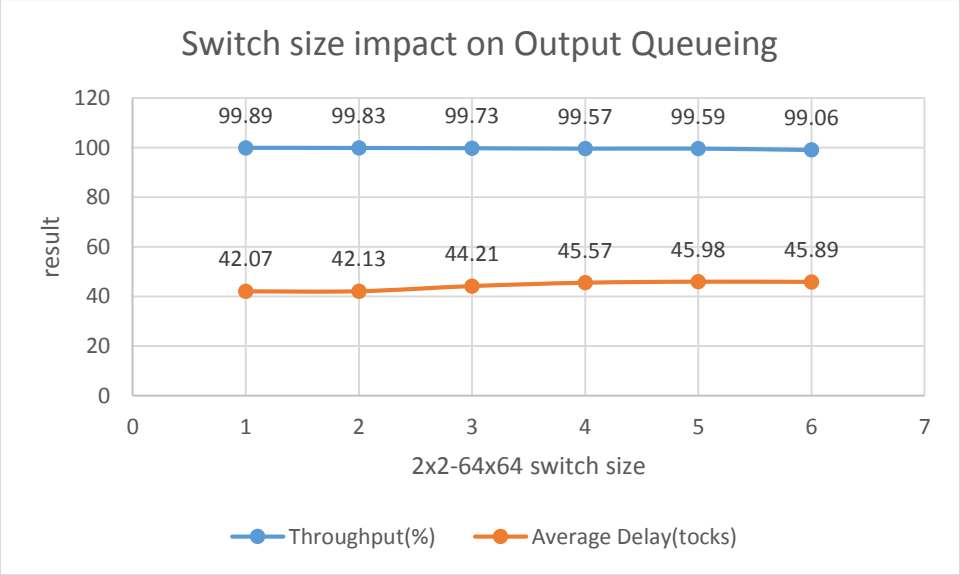

Figure 4

The impact of distribution of packets

The distribution will absolutely impact the performance of the input and output queueing. This is mainly due to the contention situation is very different on different distribution of packets.

Let's generate a packet traffic in which every source computer wants to go the same destination. For output queuing which only has the size of 100, the throughput would be very low, actually in one of my experiment it is just 3.15%. But previously in the traffic where the destination computer would be random, it is around 100%.