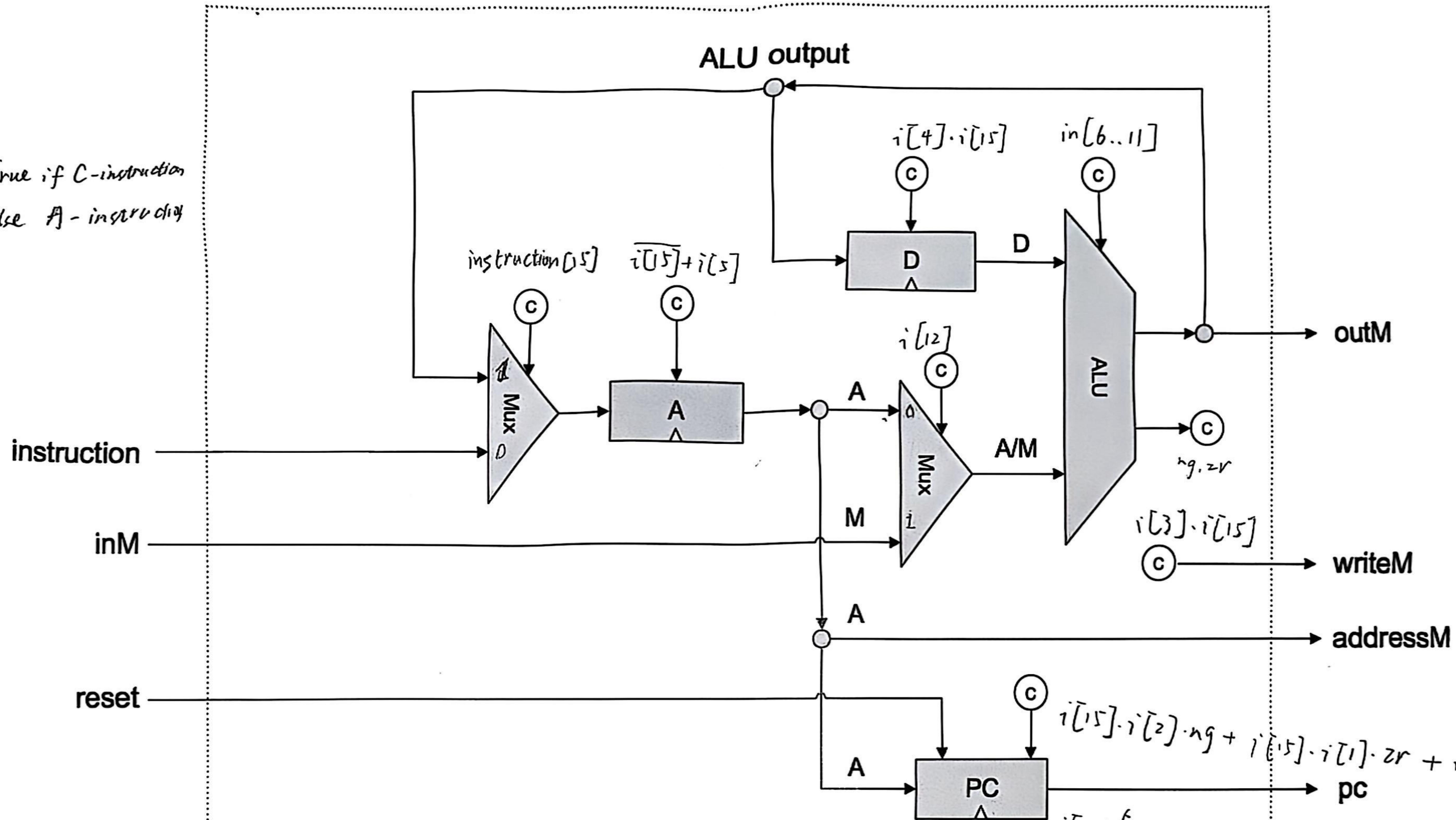


@16

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CPU Design

instruction[15]: True if C-instruction
else A-instruction



	comp										dest			jump		
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary:	1	1	1	a	c1	c2	c3	c4	c5	c6	d1	d2	d3	j1	j2	j3
				zx	nx	zy	ny	f	no	A	D	M	<	=	>	

$a=0$
 A, D, 其他寄存器
 $a=1$
 M, D 和 M
 f: 1=add, 0=and

$$i[15] \cdot i[12] \cdot ng + i[15] \cdot i[11] \cdot zr + i[15] \cdot i[10] \cdot \bar{zr} \cdot ng$$

$$i[15] \cdot ((in[12] \cdot ng) + (i[11] \cdot zr) + (i[10] \cdot \bar{zr} \cdot ng)) + (i[11] \cdot zr) + (i[10] \cdot \bar{zr} \cdot ng)$$

input inc, output reset