Project1 for Intro to Computer Systems 2025 spring

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File Structure:

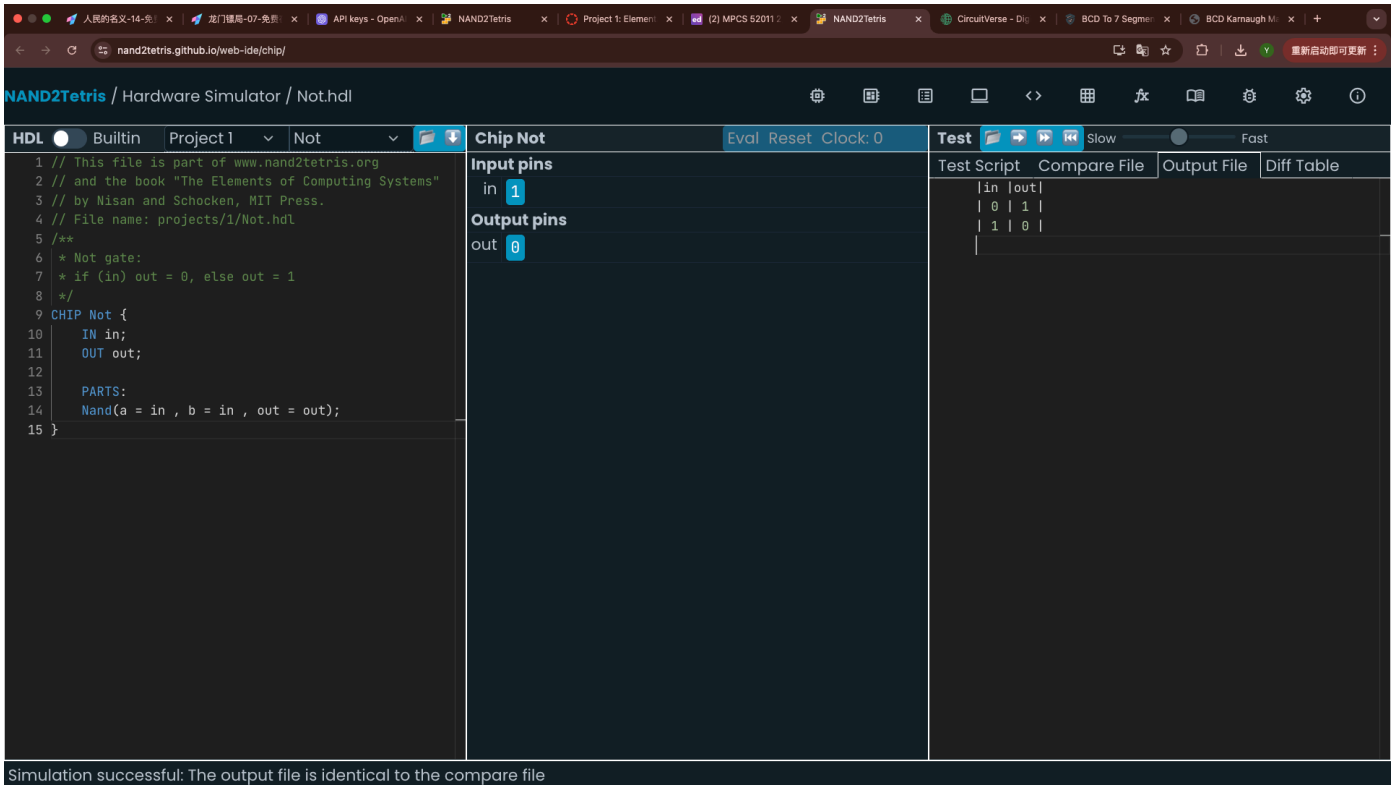
Result:

1. Not : $\boxed{work}$
2. And $\boxed{work}$
3. Or $\boxed{work}$
4. Xor $\boxed{work}$
5. Not16 $\boxed{work}$

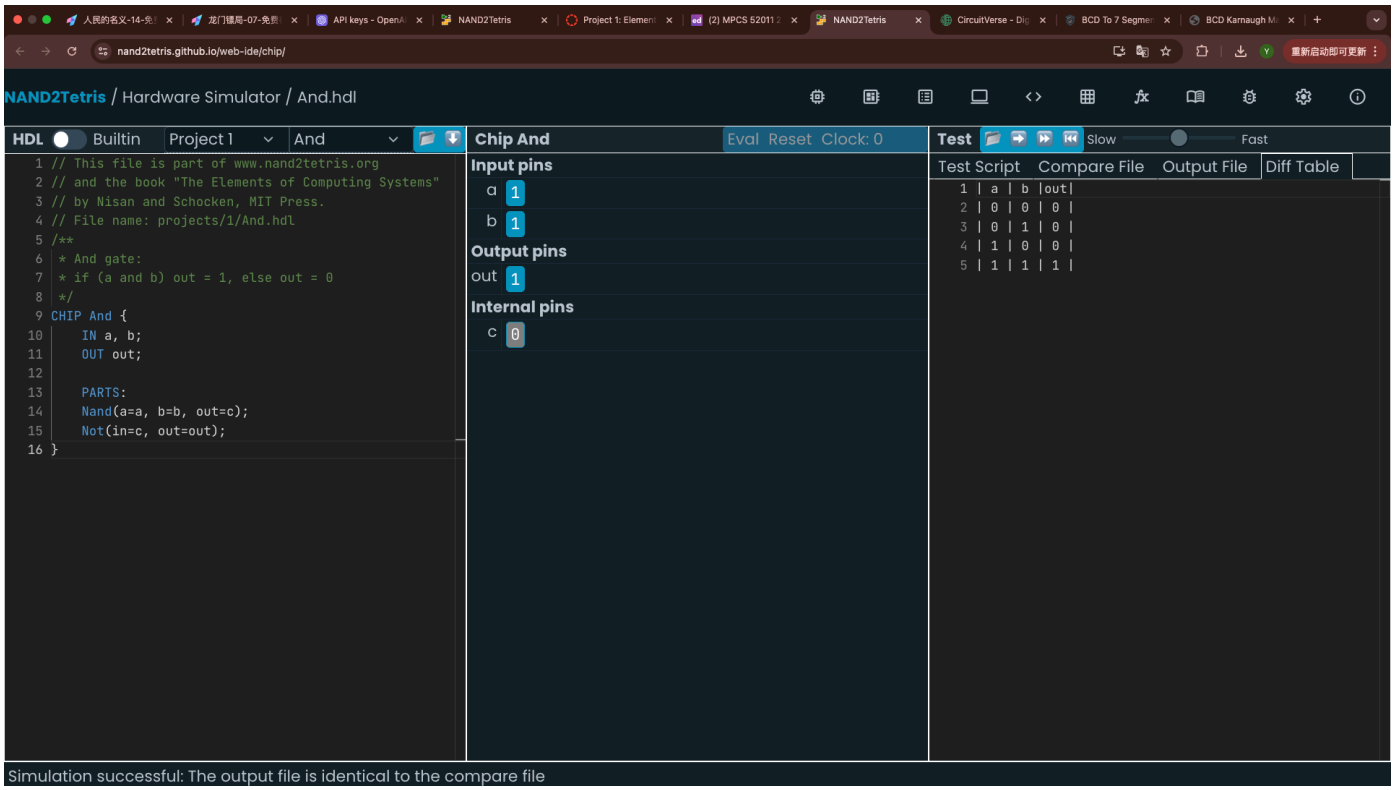
6. And16 $\boxed{work}$
7. Or16 $\boxed{work}$
8. Or8Way $\boxed{work}$
9. Mux $\boxed{work}$
0. DMux $\boxed{work}$
1. Mux16 $\boxed{work}$
2. Mux4Way16 $\boxed{work}$
3. Mux8Way16 $\boxed{work}$
4. DMux4Way $\boxed{work}$
5. DMux8Way $\boxed{work}$

Details:

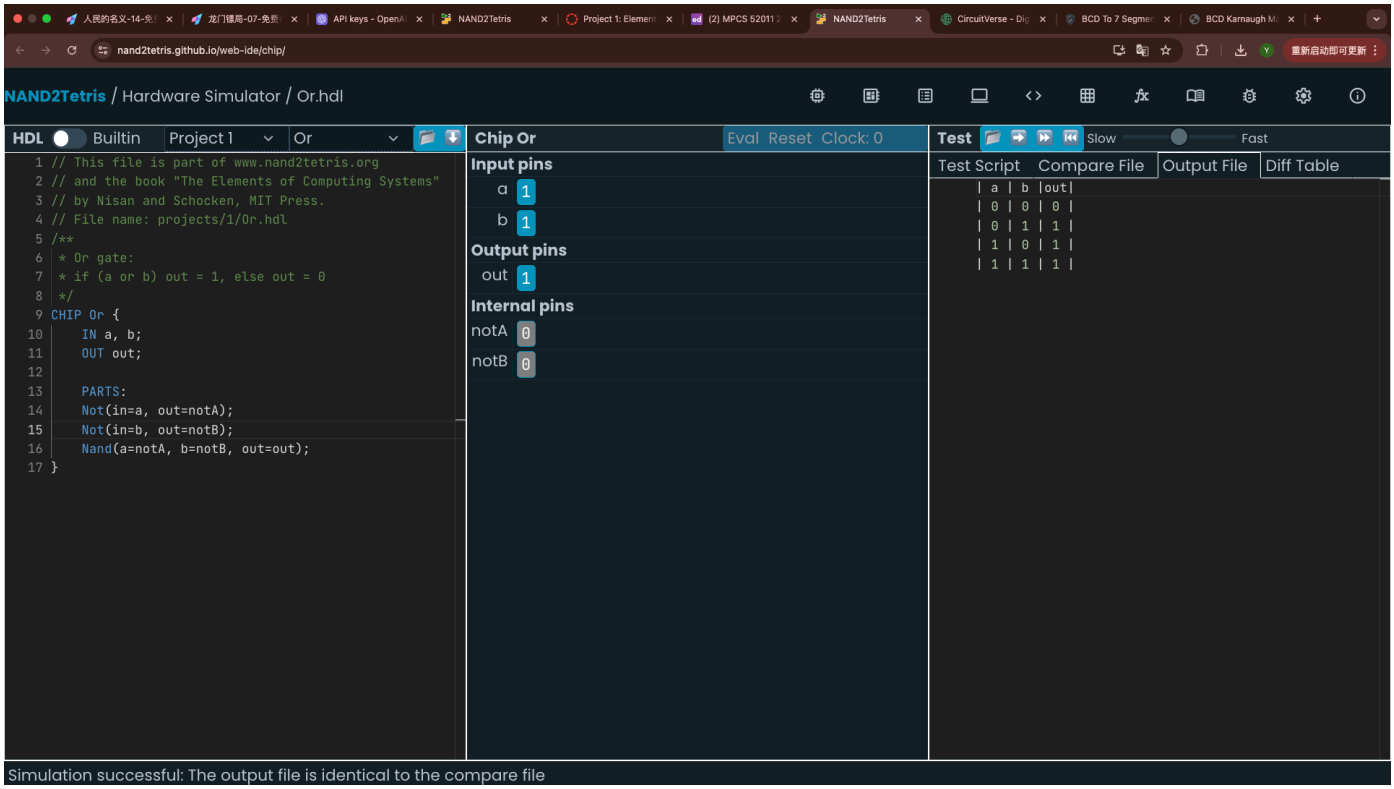
1. Not


nand2tetris.github.io/web-ide/chip/
NAND2Tetris / Hardware Simulator / Not.hdl
HDL Builtin Project 1 Not
// This file is part of www.nand2tetris.org
// and the book "The Elements of Computing Systems"
// by Nisan and Schocken, MIT Press.
// File name: projects/1/Not.hdl
/**
* Not gate:
* if (in) out = 0, else out = 1
*/
CHIP Not {
IN in;
OUT out;
PARTS:
Nand(a = in , b = in , out = out);
}
Chip Not
Eval Reset Clock: 0
Input pins
in 1
Output pins
out 0
Test
Slow
Fast
Test Script
Compare File
Output File
Diff Table
in	out
0	1
1	0
Simulation successful: The output file is identical to the compare file

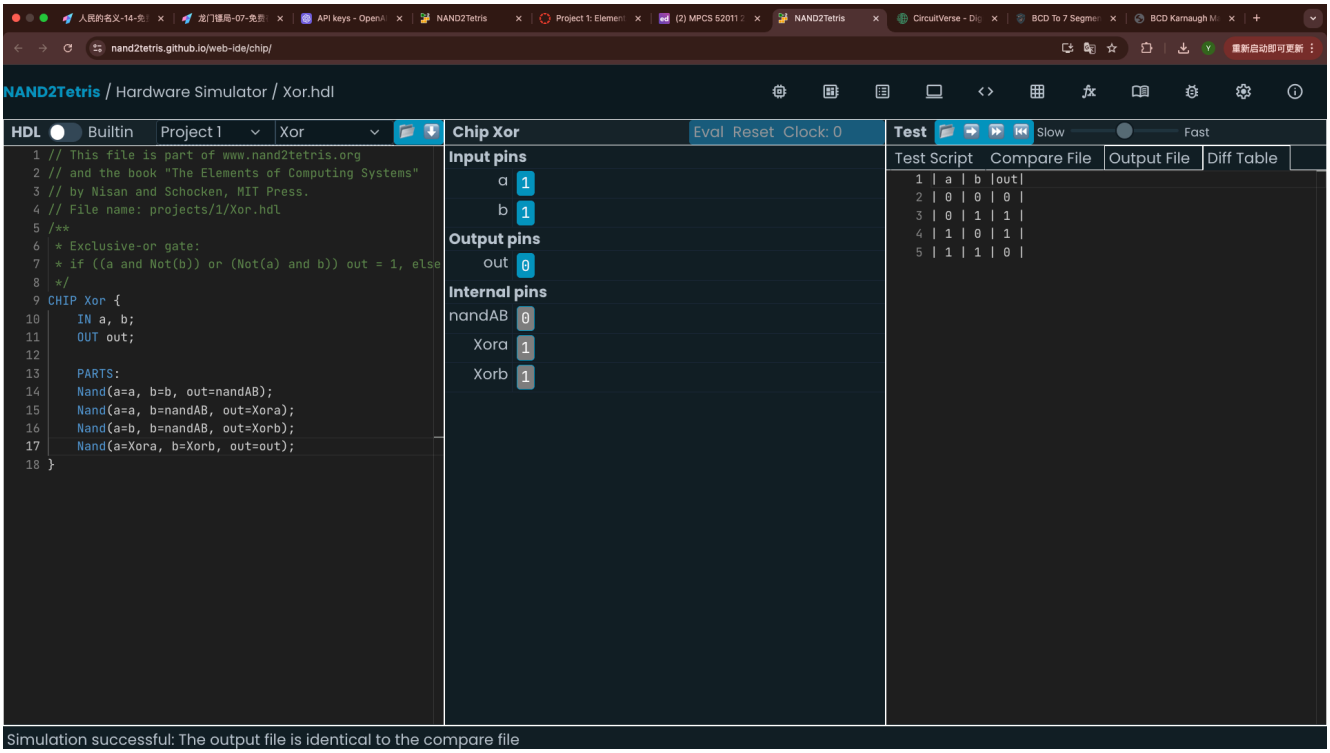
2. And


nand2tetris.github.io/web-ide/chip/
NAND2Tetris / Hardware Simulator / And.hdl
HDL Builtin Project 1 And
// This file is part of www.nand2tetris.org
// and the book "The Elements of Computing Systems"
// by Nisan and Schocken, MIT Press.
// File name: projects/1/And.hdl
/**
* And gate:
* if (a and b) out = 1, else out = 0
*/
CHIP And {
IN a, b;
OUT out;
PARTS:
Nand(a=a, b=b, out=c);
Not(in=c, out=out);
}
Chip And
Eval Reset Clock: 0
Input pins
a 1
b 1
Output pins
out 1
Internal pins
c 0
Test
Slow
Fast
Test Script
Compare File
Output File
Diff Table
1 | a | b |out|
2 | 0 | 0 | 0 |
3 | 0 | 1 | 0 |
4 | 1 | 0 | 0 |
5 | 1 | 1 | 1 |
Simulation successful: The output file is identical to the compare file

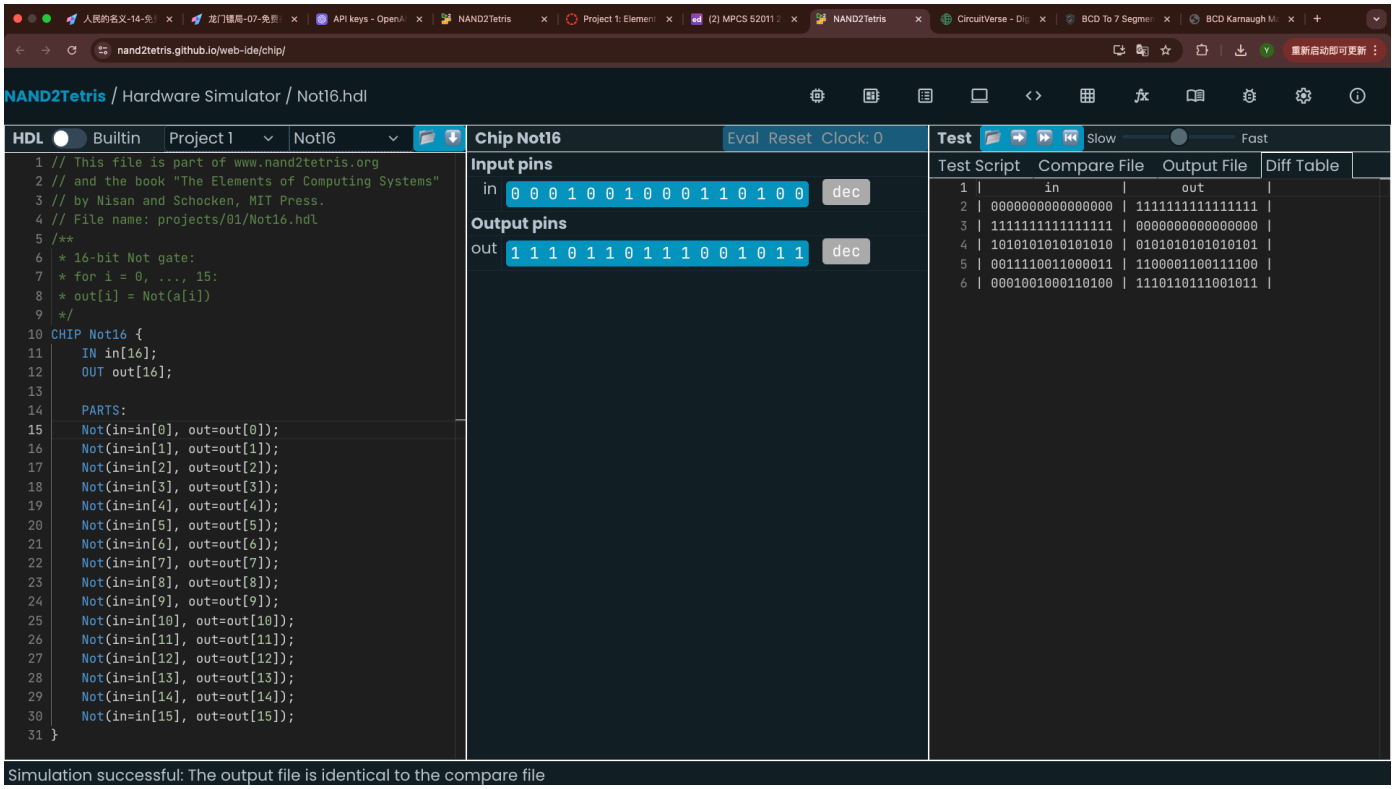
3. Or


NAND2Tetris / Hardware Simulator / Or.hdl
HDL Builtin Project 1 Or
// This file is part of www.nand2tetris.org
// and the book "The Elements of Computing Systems"
// by Nisan and Schocken, MIT Press.
// File name: projects/1/Or.hdl
/**
* Or gate:
* if (a or b) out = 1, else out = 0
*/
CHIP Or {
IN a, b;
OUT out;
PARTS:
Not(in=a, out=notA);
Not(in=b, out=notB);
Nand(a=notA, b=notB, out=out);
}
Chip Or
Eval Reset Clock: 0
Input pins
a 1
b 1
Output pins
out 1
Internal pins
notA 0
notB 0
Test
Slow
Fast
Test Script
Compare File
Output File
Diff Table
a	b	out
0	0	0
0	1	1
1	0	1
1	1	1
Simulation successful: The output file is identical to the compare file

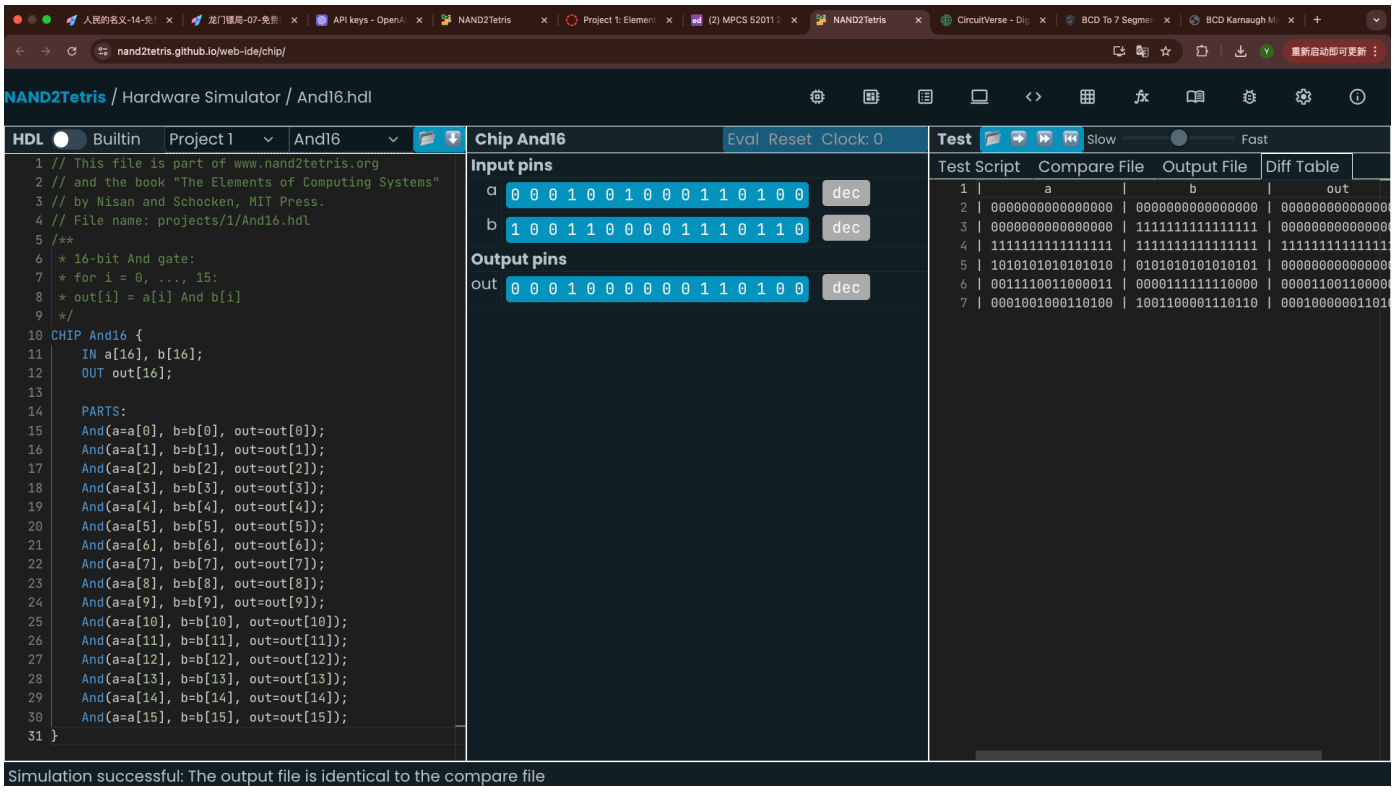
4. Xor


NAND2Tetris / Hardware Simulator / Xor.hdl
HDL Builtin Project 1 Xor
// This file is part of www.nand2tetris.org
// and the book "The Elements of Computing Systems"
// by Nisan and Schocken, MIT Press.
// File name: projects/1/Xor.hdl
/**
* Exclusive-or gate:
* if ((a and Not(b)) or (Not(a) and b)) out = 1, else
*/
CHIP Xor {
IN a, b;
OUT out;
PARTS:
Nand(a=a, b=b, out=nandAB);
Nand(a=a, b=nandAB, out=Xora);
Nand(a=b, b=nandAB, out=Xorb);
Nand(a=Xora, b=Xorb, out=out);
}
Chip Xor
Eval Reset Clock: 0
Input pins
a 1
b 1
Output pins
out 0
Internal pins
nandAB 0
Xora 1
Xorb 1
Test
Slow
Fast
Test Script
Compare File
Output File
Diff Table
a	b	out
0	0	0
0	1	1
1	0	1
1	1	0
Simulation successful: The output file is identical to the compare file

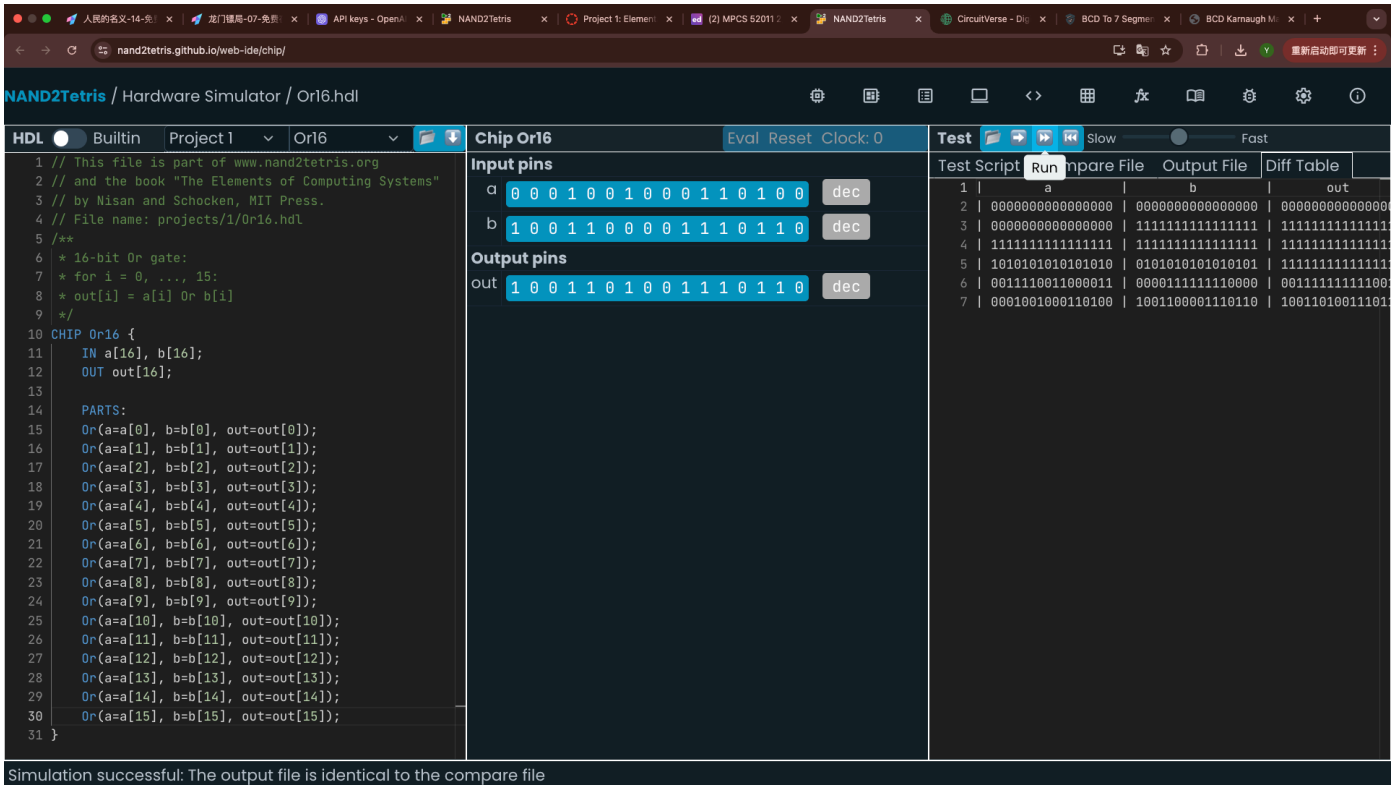
5. Not16



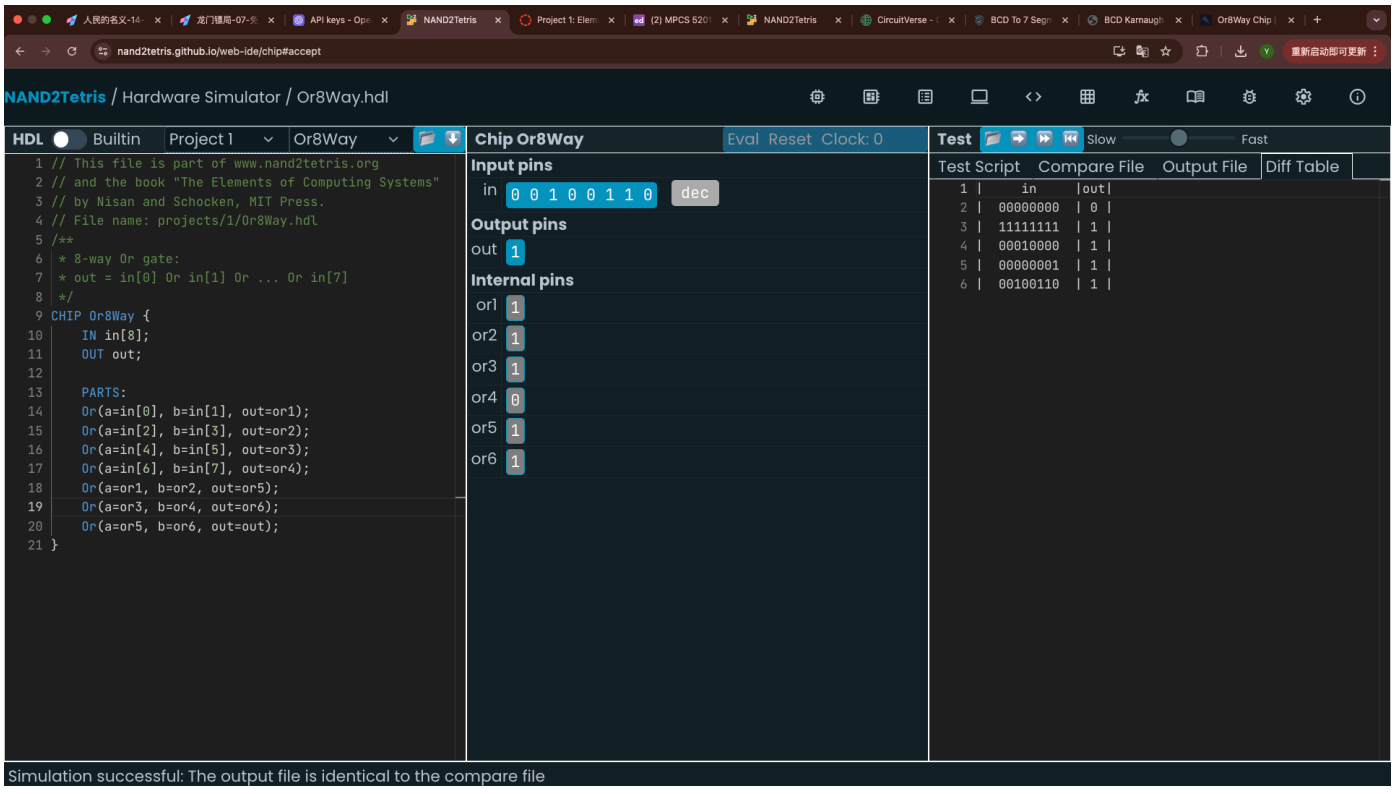
6. And16



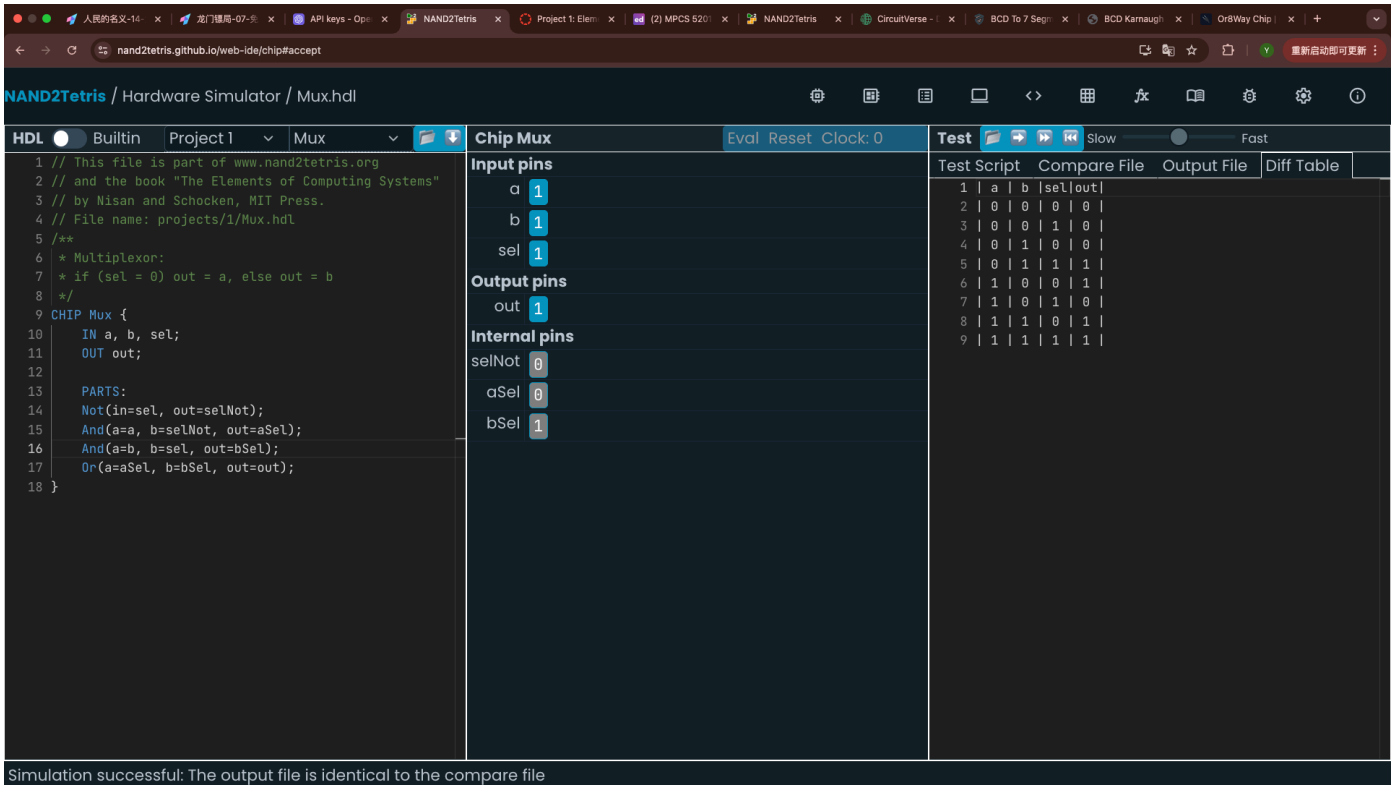
7. Or16



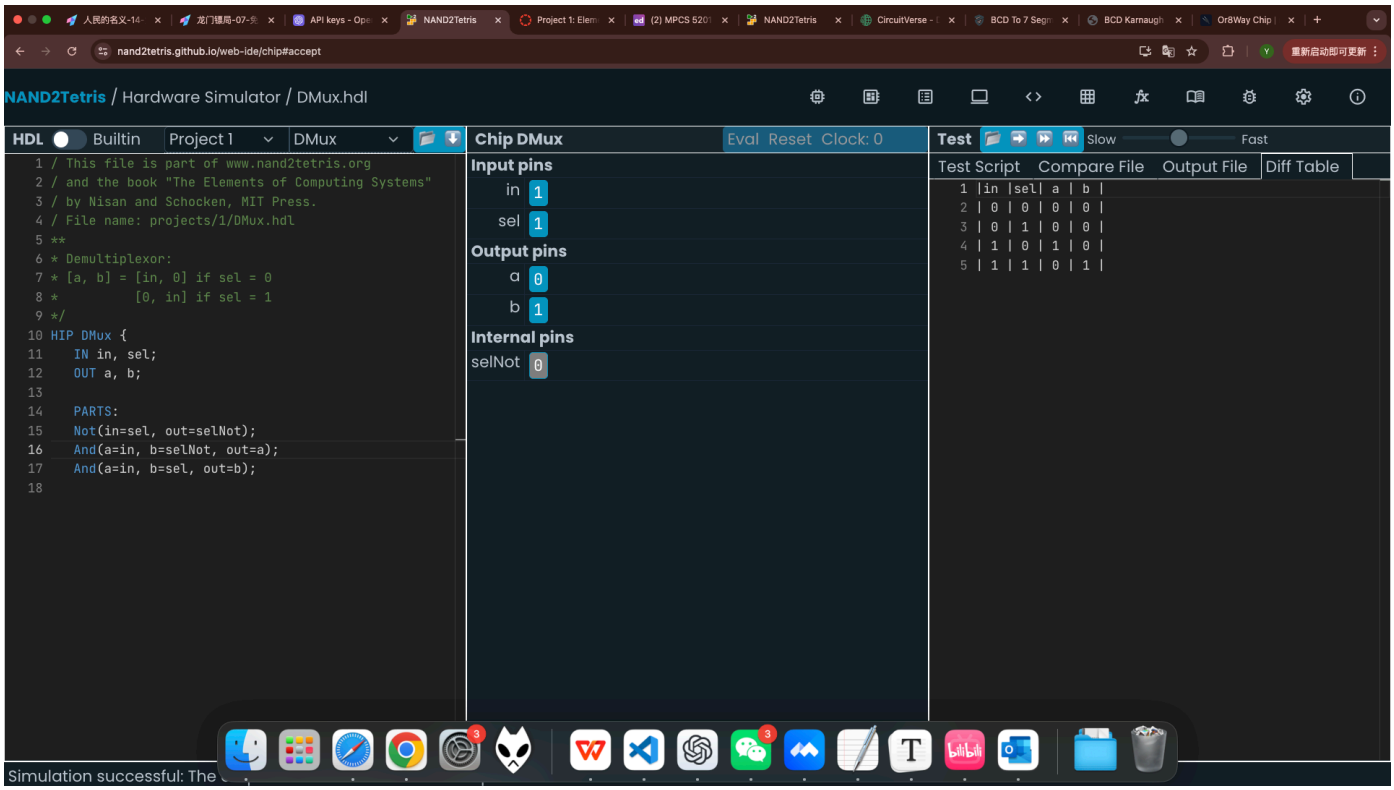
8. Or8Way



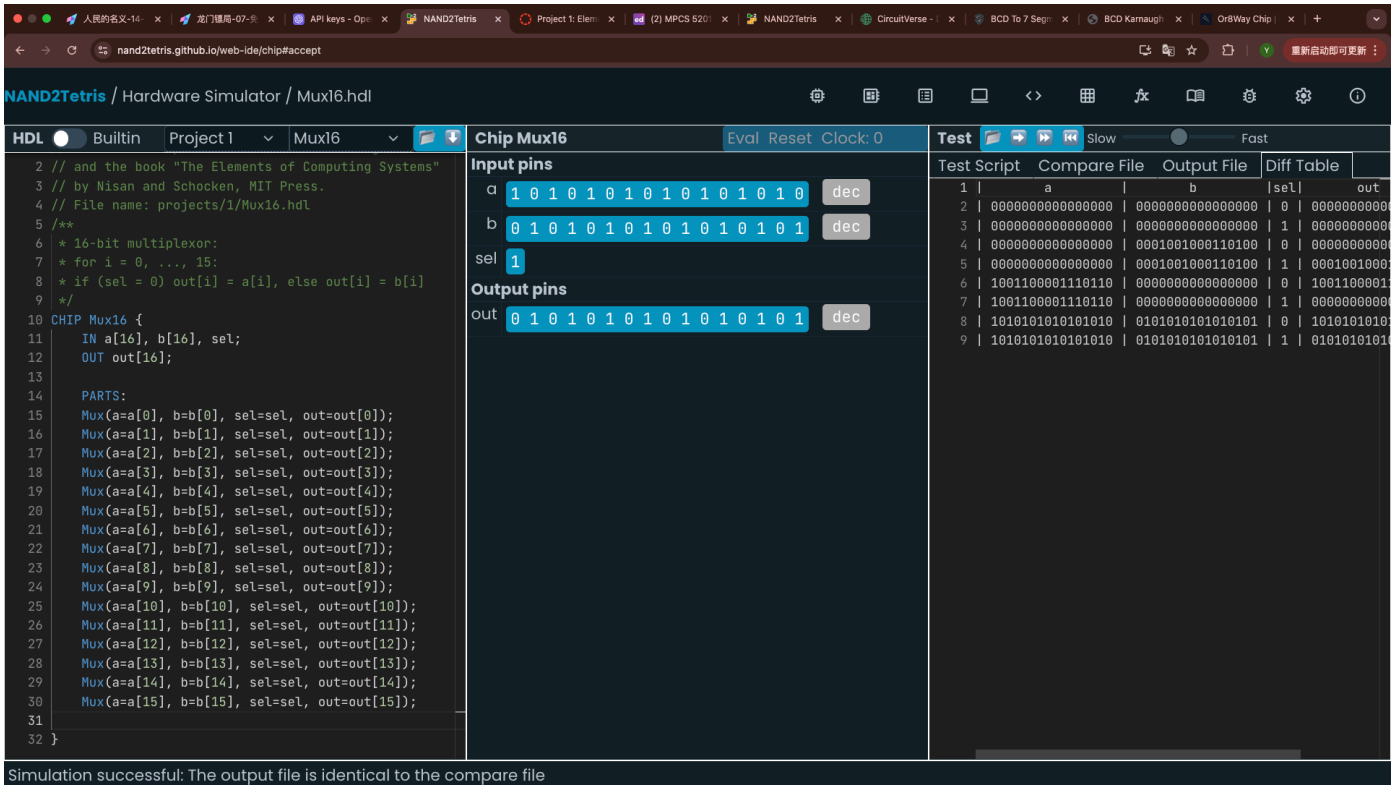
9. Mux



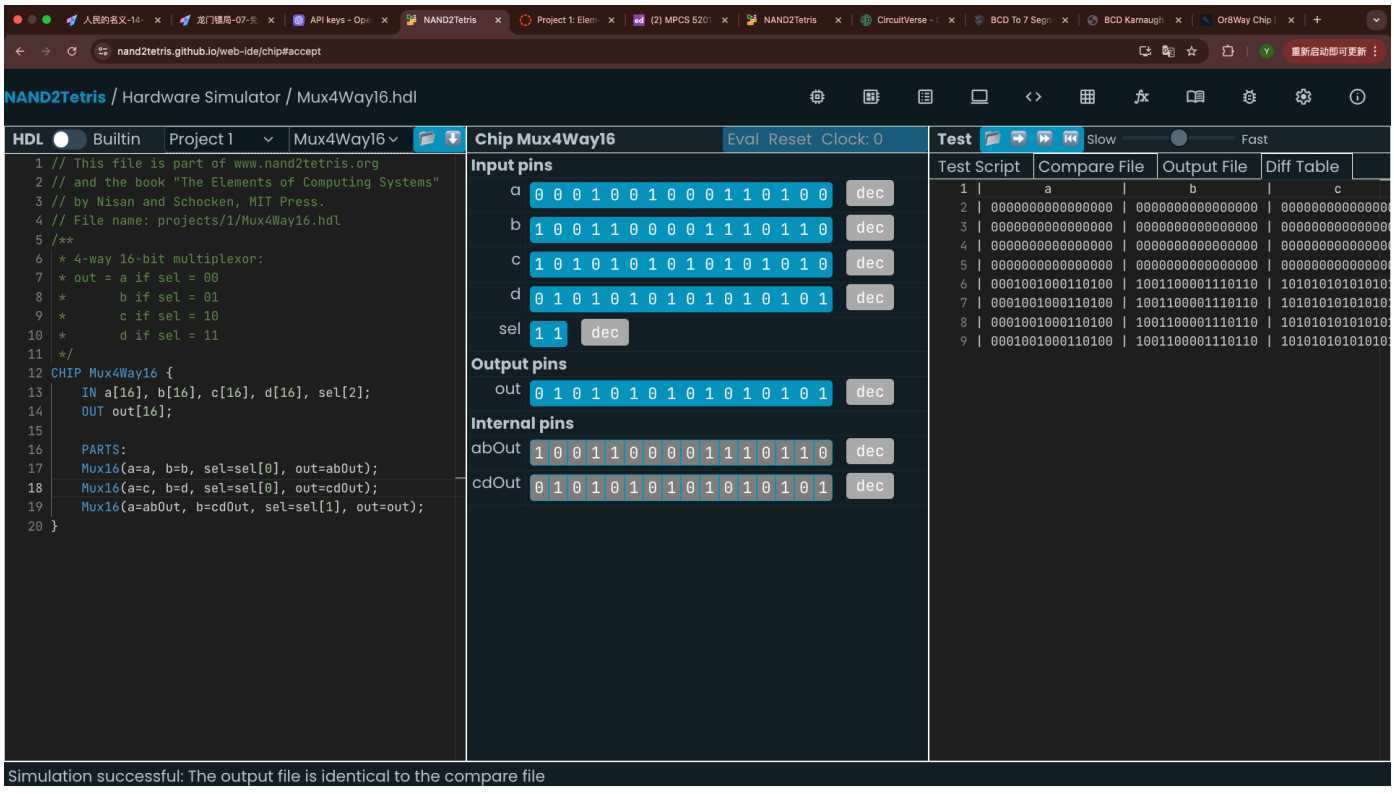
0. DMux



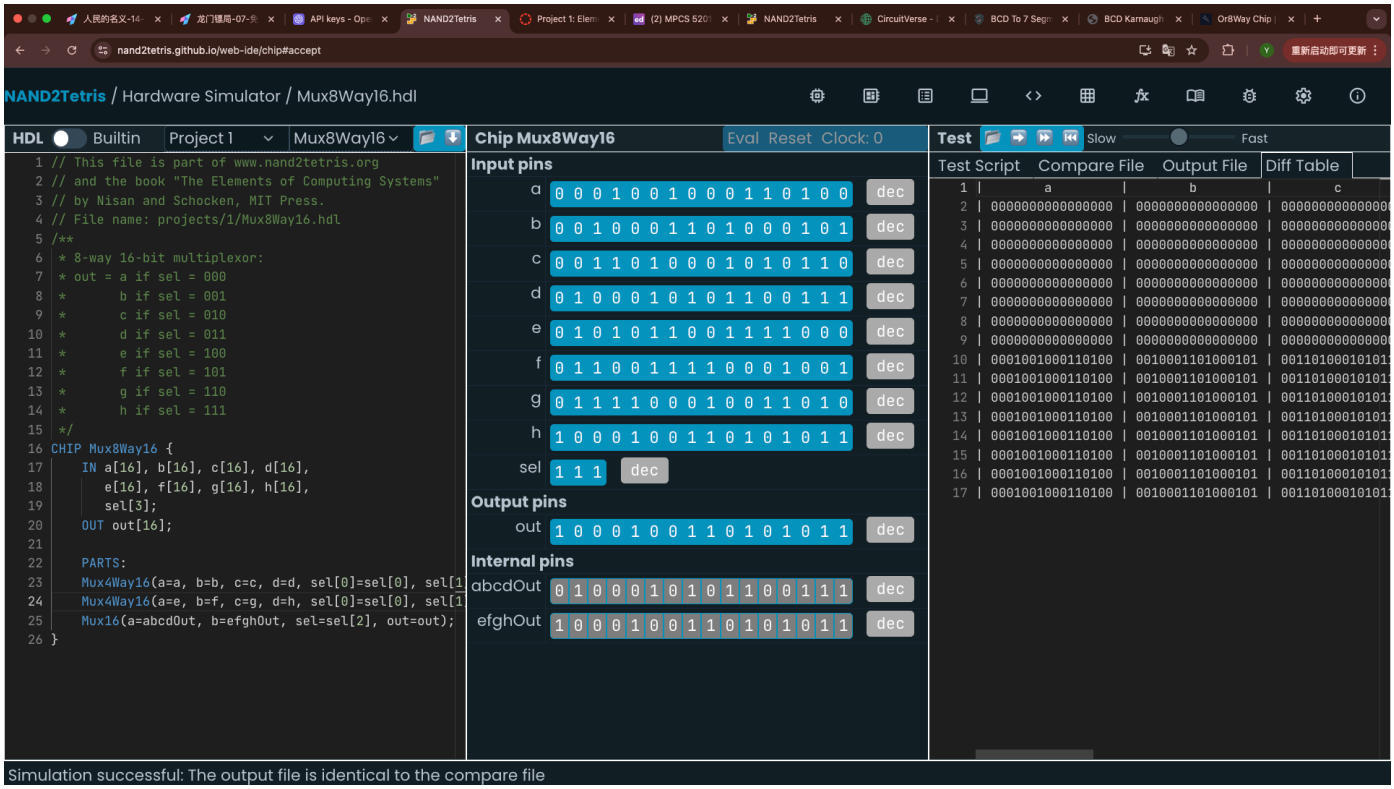
1. Mux16



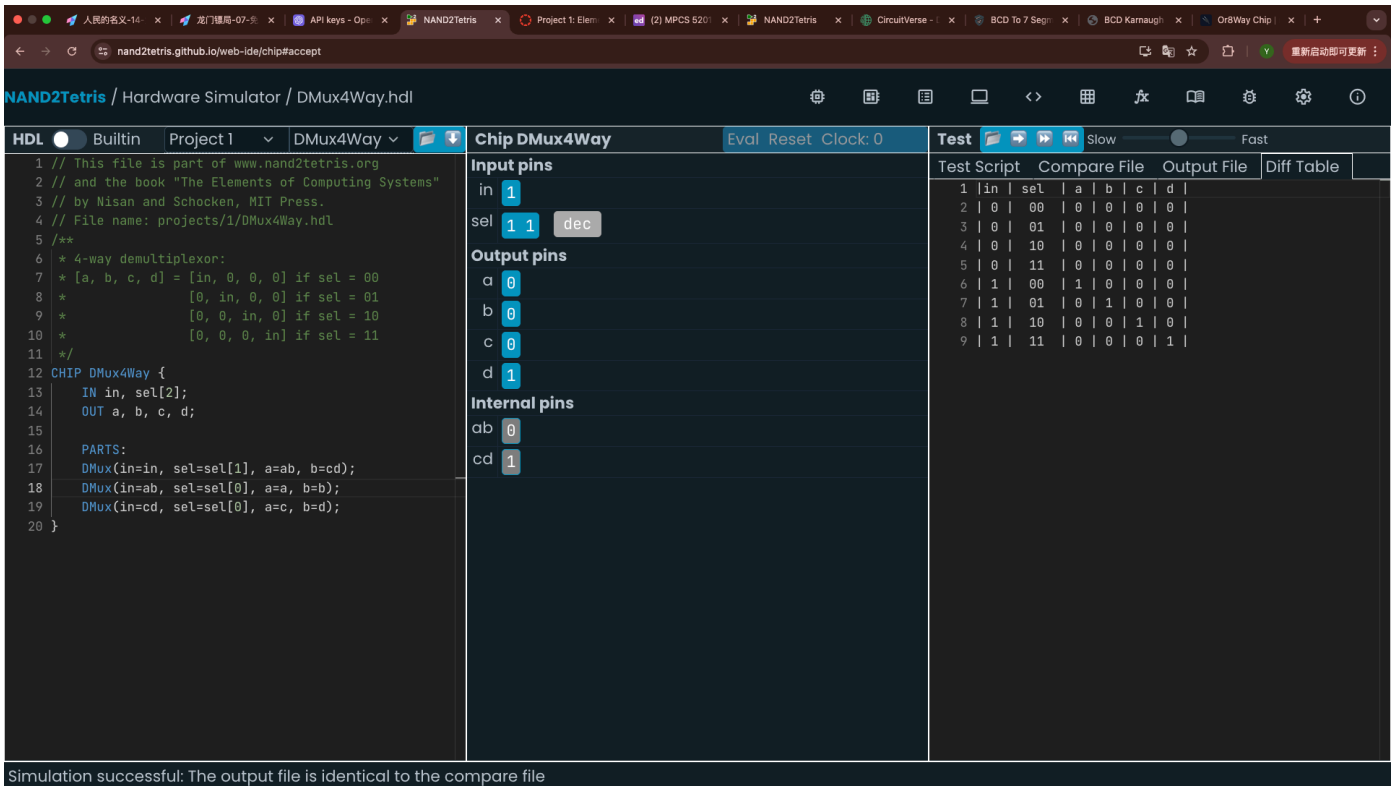
2. Mux4Way16



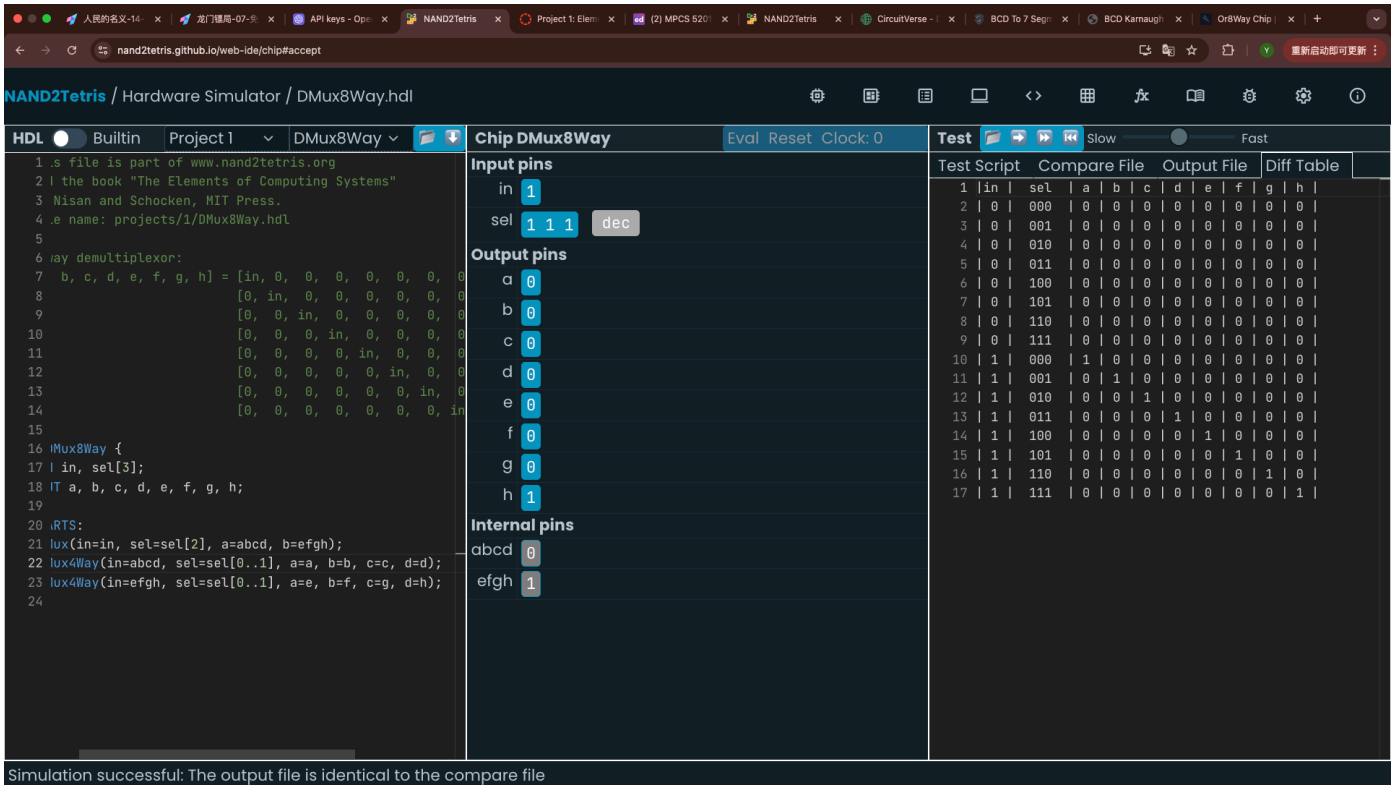
3. Mux8Way16



4. DMux4Way



15 /. DMux8Way


nand2tetris.github.io/web-ide/chip#accept
NAND2Tetris / Hardware Simulator / DMux8Way.hdl
HDL
Builtin
Project 1
DMux8Way
.s file is part of www.nand2tetris.org
l the book "The Elements of Computing Systems"
Nisan and Schocken, MIT Press.
.e name: projects/1/DMux8Way.hdl
ay demultiplexor:
b, c, d, e, f, g, h] = [in, 0, 0, 0, 0, 0, 0, 0
[0, in, 0, 0, 0, 0, 0, 0
[0, 0, in, 0, 0, 0, 0, 0
[0, 0, 0, in, 0, 0, 0, 0
[0, 0, 0, 0, in, 0, 0, 0
[0, 0, 0, 0, 0, in, 0, 0
[0, 0, 0, 0, 0, 0, in, 0
[0, 0, 0, 0, 0, 0, 0, in
Mux8Way {
in, sel[3];
T a, b, c, d, e, f, g, h;
RTS:
ux(in=in, sel=sel[2], a=abcd, b=efgh);
ux4Way(in=abcd, sel=sel[0..1], a=a, b=b, c=c, d=d);
ux4Way(in=efgh, sel=sel[0..1], a=e, b=f, c=g, d=h);
Chip DMux8Way
Eval Reset Clock: 0
Input pins
in 1
sel 1 1 1 dec
Output pins
a 0
b 0
c 0
d 0
e 0
f 0
g 0
h 1
Internal pins
abcd 0
efgh 1
Test
Slow
Fast
Test Script
Compare File
Output File
Diff Table
in	sel	a	b	c	d	e	f	g	h
0	000	0	0	0	0	0	0	0	0
0	001	0	0	0	0	0	0	0	0
0	010	0	0	0	0	0	0	0	0
0	011	0	0	0	0	0	0	0	0
0	100	0	0	0	0	0	0	0	0
0	101	0	0	0	0	0	0	0	0
0	110	0	0	0	0	0	0	0	0
0	111	0	0	0	0	0	0	0	0
1	000	1	0	0	0	0	0	0	0
1	001	0	1	0	0	0	0	0	0
1	010	0	0	1	0	0	0	0	0
1	011	0	0	0	1	0	0	0	0
1	100	0	0	0	0	1	0	0	0
1	101	0	0	0	0	0	1	0	0
1	110	0	0	0	0	0	0	1	0
1	111	0	0	0	0	0	0	0	1
Simulation successful: The output file is identical to the compare file