

Project1 for Intro to Computer Systems 2025 spring

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[Project1 for Intro to Computer Systems 2025 spring](#)

[File Structure:](#)

[Result:](#)

[Details:](#)

File Structure:

Result:

1. Not : *work*
2. And *work*
3. Or *work*
4. Xor *work*
5. Not16 *work*

- 6. And16 *work*
- 7. Or16 *work*
- 8. Or8Way *work*
- 9. Mux *work*
- 0. DMux *work*
- 1. Mux16 *work*
- 2. Mux4Way16 *work*
- 3. Mux8Way16 *work*
- 4. DMux4Way *work*
- 5. DMux8Way *work*

Details:

- 1. Not

NAND2Tetris / Hardware Simulator / Not.hdl

HDL Built-in Project 1 Not Chip Not Eval Reset Clock: 0 Test Test Script Compare File Output File Diff Table

```
1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/1/Not.hdl
5 /**
6  * Not gate:
7  * if (in) out = 0, else out = 1
8  */
9 CHIP Not {
10     IN in;
11     OUT out;
12
13     PARTS:
14         Nand(a = in , b = in , out = out);
15 }
```

Input pins
in 1

Output pins
out 0

in	out
0	1
1	0

Simulation successful: The output file is identical to the compare file

2. And

NAND2Tetris / Hardware Simulator / And.hdl

HDL Built-in Project 1 And Chip And Eval Reset Clock: 0 Test Test Script Compare File Output File Diff Table

```
1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/1/And.hdl
5 /**
6  * And gate:
7  * if (a and b) out = 1, else out = 0
8  */
9 CHIP And {
10     IN a, b;
11     OUT out;
12
13     PARTS:
14         Nand(a=a, b=b, out=c);
15         Not(in=c, out=out);
16 }
```

Input pins
a 1
b 1

Output pins
out 1

Internal pins
c 0

	a	b	out
1	0	0	0
2	0	1	0
3	1	0	0
4	1	1	1

Simulation successful: The output file is identical to the compare file

3. Or

NAND2Tetris / Hardware Simulator / Or.hdl

HDL Built-in Project 1 Or

```
1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/1/Or.hdl
5 /**
6  * Or gate:
7  * if (a or b) out = 1, else out = 0
8  */
9 CHIP Or {
10     IN a, b;
11     OUT out;
12
13     PARTS:
14     Not(in=a, out=notA);
15     Not(in=b, out=notB);
16     Nand(a=notA, b=notB, out=out);
17 }
```

Chip Or

Input pins

a 1

b 1

Output pins

out 1

Internal pins

notA 0

notB 0

Test

Test Script Compare File Output File Diff Table

	a	b	out
1	0	0	0
2	0	1	1
3	1	0	1
4	1	1	1

Simulation successful: The output file is identical to the compare file

4. Xor

NAND2Tetris / Hardware Simulator / Xor.hdl

HDL Built-in Project 1 Xor

```
1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/1/Xor.hdl
5 /**
6  * Exclusive-or gate:
7  * if ((a and Not(b)) or (Not(a) and b)) out = 1, else
8  */
9 CHIP Xor {
10     IN a, b;
11     OUT out;
12
13     PARTS:
14     Nand(a=a, b=b, out=nandAB);
15     Nand(a=a, b=nandAB, out=Xora);
16     Nand(a=b, b=nandAB, out=Xorb);
17     Nand(a=Xora, b=Xorb, out=out);
18 }
```

Chip Xor

Input pins

a 1

b 1

Output pins

out 0

Internal pins

nandAB 0

Xora 1

Xorb 1

Test

Test Script Compare File Output File Diff Table

	a	b	out
1	0	0	0
2	0	1	1
3	1	0	1
4	1	1	0

Simulation successful: The output file is identical to the compare file

5. Not16

NAND2Tetris / Hardware Simulator / Not16.hdl

HDL Builtin Project1 Not16

```

1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/01/Not16.hdl
5 /**
6  * 16-bit Not gate:
7  * for i = 0, ..., 15:
8  *   out[i] = Not(a[i])
9  */
10 CHIP Not16 {
11     IN in[16];
12     OUT out[16];
13
14     PARTS:
15     Not(in=in[0], out=out[0]);
16     Not(in=in[1], out=out[1]);
17     Not(in=in[2], out=out[2]);
18     Not(in=in[3], out=out[3]);
19     Not(in=in[4], out=out[4]);
20     Not(in=in[5], out=out[5]);
21     Not(in=in[6], out=out[6]);
22     Not(in=in[7], out=out[7]);
23     Not(in=in[8], out=out[8]);
24     Not(in=in[9], out=out[9]);
25     Not(in=in[10], out=out[10]);
26     Not(in=in[11], out=out[11]);
27     Not(in=in[12], out=out[12]);
28     Not(in=in[13], out=out[13]);
29     Not(in=in[14], out=out[14]);
30     Not(in=in[15], out=out[15]);
31 }

```

Chip Not16

Input pins

in 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 dec

Output pins

out 1 1 1 0 1 1 0 1 1 1 0 0 1 0 1 1 dec

Test

Test Script	Compare File	Output File	Diff Table
1 in		out	
2 0000000000000000	1111111111111111		
3 1111111111111111	0000000000000000		
4 1010101010101010	0101010101010101		
5 0011110011000011	1100001100111100		
6 0001001000110100	1110110111001011		

Simulation successful: The output file is identical to the compare file

6. And16

NAND2Tetris / Hardware Simulator / And16.hdl

HDL Builtin Project1 And16

```

1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/1/And16.hdl
5 /**
6  * 16-bit And gate:
7  * for i = 0, ..., 15:
8  *   out[i] = a[i] And b[i]
9  */
10 CHIP And16 {
11     IN a[16], b[16];
12     OUT out[16];
13
14     PARTS:
15     And(a=a[0], b=b[0], out=out[0]);
16     And(a=a[1], b=b[1], out=out[1]);
17     And(a=a[2], b=b[2], out=out[2]);
18     And(a=a[3], b=b[3], out=out[3]);
19     And(a=a[4], b=b[4], out=out[4]);
20     And(a=a[5], b=b[5], out=out[5]);
21     And(a=a[6], b=b[6], out=out[6]);
22     And(a=a[7], b=b[7], out=out[7]);
23     And(a=a[8], b=b[8], out=out[8]);
24     And(a=a[9], b=b[9], out=out[9]);
25     And(a=a[10], b=b[10], out=out[10]);
26     And(a=a[11], b=b[11], out=out[11]);
27     And(a=a[12], b=b[12], out=out[12]);
28     And(a=a[13], b=b[13], out=out[13]);
29     And(a=a[14], b=b[14], out=out[14]);
30     And(a=a[15], b=b[15], out=out[15]);
31 }

```

Chip And16

Input pins

a 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 dec

b 1 0 0 1 1 0 0 0 0 0 1 1 1 0 1 0 dec

Output pins

out 0 0 0 1 0 0 0 0 0 0 1 1 0 1 0 0 dec

Test

Test Script	Compare File	Output File	Diff Table
1 a	b	out	
2 0000000000000000	0000000000000000	0000000000000000	
3 0000000000000000	1111111111111111	0000000000000000	
4 1111111111111111	1111111111111111	1111111111111111	
5 1010101010101010	0101010101010101	0000000000000000	
6 0011110011000011	0000111111111000	0000110011000000	
7 0001001000110100	1001100001110110	0001000001101000	

Simulation successful: The output file is identical to the compare file

7. Or16

NAND2Tetris / Hardware Simulator / Or16.hdl

HDL Builtin Project1 Or16 Chip Or16 Eval Reset Clock: 0 Test Run Compare File Output File Diff Table

```

1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/1/Or16.hdl
5 /**
6  * 16-bit Or gate:
7  * for i = 0, ..., 15:
8  * out[i] = a[i] Or b[i]
9  */
10 CHIP Or16 {
11     IN a[16], b[16];
12     OUT out[16];
13
14     PARTS:
15     Or(a=a[0], b=b[0], out=out[0]);
16     Or(a=a[1], b=b[1], out=out[1]);
17     Or(a=a[2], b=b[2], out=out[2]);
18     Or(a=a[3], b=b[3], out=out[3]);
19     Or(a=a[4], b=b[4], out=out[4]);
20     Or(a=a[5], b=b[5], out=out[5]);
21     Or(a=a[6], b=b[6], out=out[6]);
22     Or(a=a[7], b=b[7], out=out[7]);
23     Or(a=a[8], b=b[8], out=out[8]);
24     Or(a=a[9], b=b[9], out=out[9]);
25     Or(a=a[10], b=b[10], out=out[10]);
26     Or(a=a[11], b=b[11], out=out[11]);
27     Or(a=a[12], b=b[12], out=out[12]);
28     Or(a=a[13], b=b[13], out=out[13]);
29     Or(a=a[14], b=b[14], out=out[14]);
30     Or(a=a[15], b=b[15], out=out[15]);
31 }

```

Input pins

a 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 dec

b 1 0 0 1 1 0 0 0 0 1 1 1 0 1 1 0 dec

Output pins

out 1 0 0 1 1 0 1 0 0 1 1 1 0 1 1 0 dec

Test Script Run Compare File Output File Diff Table

	a	b	out
1			
2	0000000000000000	0000000000000000	0000000000000000
3	0000000000000000	1111111111111111	1111111111111111
4	1111111111111111	1111111111111111	1111111111111111
5	1010101010101010	0101010101010101	1111111111111111
6	0011110011000011	0000111111110000	0011111111111001
7	0001001000110100	1001100001110110	100110100111011

Simulation successful: The output file is identical to the compare file

8. Or8Way

NAND2Tetris / Hardware Simulator / Or8Way.hdl

HDL Builtin Project1 Or8Way Chip Or8Way Eval Reset Clock: 0 Test Run Compare File Output File Diff Table

```

1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/1/Or8Way.hdl
5 /**
6  * 8-way Or gate:
7  * out = in[0] Or in[1] Or ... Or in[7]
8  */
9 CHIP Or8Way {
10     IN in[8];
11     OUT out;
12
13     PARTS:
14     Or(a=in[0], b=in[1], out=or1);
15     Or(a=in[2], b=in[3], out=or2);
16     Or(a=in[4], b=in[5], out=or3);
17     Or(a=in[6], b=in[7], out=or4);
18     Or(a=or1, b=or2, out=or5);
19     Or(a=or3, b=or4, out=or6);
20     Or(a=or5, b=or6, out=out);
21 }

```

Input pins

in 0 0 1 0 0 1 1 0 dec

Output pins

out 1

Internal pins

or1 1

or2 1

or3 1

or4 0

or5 1

or6 1

Test Script Run Compare File Output File Diff Table

	in	out
1		
2	00000000	0
3	11111111	1
4	00010000	1
5	00000001	1
6	00100110	1

Simulation successful: The output file is identical to the compare file

9. Mux

NAND2Tetris / Hardware Simulator / Mux.hdl

HDL Built-in Project1 Mux Chip Mux Eval Reset Clock: 0 Test

```
1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/1/Mux.hdl
5 /**
6  * Multiplexor:
7  * if (sel = 0) out = a, else out = b
8  */
9 CHIP Mux {
10     IN a, b, sel;
11     OUT out;
12
13     PARTS:
14     Not(in=sel, out=selNot);
15     And(a=a, b=selNot, out=aSel);
16     And(a=b, b=sel, out=bSel);
17     Or(a=aSel, b=bSel, out=out);
18 }
```

Input pins

a 1

b 1

sel 1

Output pins

out 1

Internal pins

selNot 0

aSel 0

bSel 1

Test Script Compare File Output File Diff Table

1	a	b	sel	out
2	0	0	0	0
3	0	0	1	0
4	0	1	0	0
5	0	1	1	1
6	1	0	0	1
7	1	0	1	0
8	1	1	0	1
9	1	1	1	1

Simulation successful: The output file is identical to the compare file

0. DMux

NAND2Tetris / Hardware Simulator / DMux.hdl

HDL Built-in Project1 DMux Chip DMux Eval Reset Clock: 0 Test

```
1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/1/DMux.hdl
5 /**
6  * Demultiplexor:
7  * [a, b] = [in, 0] if sel = 0
8  *         [0, in] if sel = 1
9  */
10 CHIP DMux {
11     IN in, sel;
12     OUT a, b;
13
14     PARTS:
15     Not(in=sel, out=selNot);
16     And(a=in, b=selNot, out=a);
17     And(a=in, b=sel, out=b);
18 }
```

Input pins

in 1

sel 1

Output pins

a 0

b 1

Internal pins

selNot 0

Test Script Compare File Output File Diff Table

1	in	sel	a	b
2	0	0	0	0
3	0	1	0	0
4	1	0	1	0
5	1	1	0	1

Simulation successful: The output file is identical to the compare file

1. Mux16

NAND2Tetris / Hardware Simulator / Mux16.hdl

HDL Built-in Project1 Mux16

```
1 // and the book "The Elements of Computing Systems"
2 // by Nisan and Schocken, MIT Press.
3 // File name: projects/1/Mux16.hdl
4 /**
5  * 16-bit multiplexor:
6  * for i = 0, ..., 15:
7  * if (sel = 0) out[i] = a[i], else out[i] = b[i]
8  */
9
10 CHIP Mux16 {
11     IN a[16], b[16], sel;
12     OUT out[16];
13
14     PARTS:
15     Mux(a=a[0], b=b[0], sel=sel, out=out[0]);
16     Mux(a=a[1], b=b[1], sel=sel, out=out[1]);
17     Mux(a=a[2], b=b[2], sel=sel, out=out[2]);
18     Mux(a=a[3], b=b[3], sel=sel, out=out[3]);
19     Mux(a=a[4], b=b[4], sel=sel, out=out[4]);
20     Mux(a=a[5], b=b[5], sel=sel, out=out[5]);
21     Mux(a=a[6], b=b[6], sel=sel, out=out[6]);
22     Mux(a=a[7], b=b[7], sel=sel, out=out[7]);
23     Mux(a=a[8], b=b[8], sel=sel, out=out[8]);
24     Mux(a=a[9], b=b[9], sel=sel, out=out[9]);
25     Mux(a=a[10], b=b[10], sel=sel, out=out[10]);
26     Mux(a=a[11], b=b[11], sel=sel, out=out[11]);
27     Mux(a=a[12], b=b[12], sel=sel, out=out[12]);
28     Mux(a=a[13], b=b[13], sel=sel, out=out[13]);
29     Mux(a=a[14], b=b[14], sel=sel, out=out[14]);
30     Mux(a=a[15], b=b[15], sel=sel, out=out[15]);
31 }
32
```

Chip Mux16

Input pins

a 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 dec

b 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 dec

sel 1

Output pins

out 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 dec

Test

Test Script	Compare File	Output File	Diff Table
1	a	b	sel out
2	0000000000000000	0000000000000000	0 0000000000
3	0000000000000000	0000000000000000	1 0000000000
4	0000000000000000	0001001000110100	0 0000000000
5	0000000000000000	0001001000110100	1 0001001000
6	1001100001110110	0000000000000000	0 1001100001
7	1001100001110110	0000000000000000	1 0000000000
8	1010101010101010	0101010101010101	0 1010101010
9	1010101010101010	0101010101010101	1 0101010101

Simulation successful: The output file is identical to the compare file

2. Mux4Way16

NAND2Tetris / Hardware Simulator / Mux4Way16.hdl

HDL Built-in Project1 Mux4Way16

```
1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/1/Mux4Way16.hdl
5 /**
6  * 4-way 16-bit multiplexor:
7  * out = a if sel = 00
8  *      b if sel = 01
9  *      c if sel = 10
10 *      d if sel = 11
11 */
12
13 CHIP Mux4Way16 {
14     IN a[16], b[16], c[16], d[16], sel[2];
15     OUT out[16];
16
17     PARTS:
18     Mux16(a=a, b=b, sel=sel[0], out=abOut);
19     Mux16(a=c, b=d, sel=sel[0], out=cdOut);
20     Mux16(a=abOut, b=cdOut, sel=sel[1], out=out);
21 }
22
```

Chip Mux4Way16

Input pins

a 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 dec

b 1 0 0 1 1 0 0 0 0 1 1 1 0 1 1 0 dec

c 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 dec

d 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 dec

sel 1 1 dec

Output pins

out 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 dec

Internal pins

abOut 1 0 0 1 1 0 0 0 0 1 1 1 0 1 1 0 dec

cdOut 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 dec

Test

Test Script	Compare File	Output File	Diff Table
1	a	b	c
2	0000000000000000	0000000000000000	000000000000
3	0000000000000000	0000000000000000	000000000000
4	0000000000000000	0000000000000000	000000000000
5	0000000000000000	0000000000000000	000000000000
6	0001001000110100	1001100001110110	101010101010
7	0001001000110100	1001100001110110	101010101010
8	0001001000110100	1001100001110110	101010101010
9	0001001000110100	1001100001110110	101010101010

Simulation successful: The output file is identical to the compare file

3. Mux8Way16

NAND2Tetris / Hardware Simulator / Mux8Way16.hdl

HDL Builtin Project1 Mux8Way16 Chip Mux8Way16 Eval Reset Clock: 0 Test Test Script Compare File Output File Diff Table

```

1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/1/Mux8Way16.hdl
5 /**
6  * 8-way 16-bit multiplexor:
7  * out = a if sel = 000
8  *   b if sel = 001
9  *   c if sel = 010
10 *   d if sel = 011
11 *   e if sel = 100
12 *   f if sel = 101
13 *   g if sel = 110
14 *   h if sel = 111
15 */
16 CHIP Mux8Way16 {
17     IN a[16], b[16], c[16], d[16],
18         e[16], f[16], g[16], h[16],
19         sel[3];
20     OUT out[16];
21
22     PARTS:
23     Mux4Way16(a=a, b=b, c=c, d=d, sel[0]=sel[0], sel[1]=sel[1]);
24     Mux4Way16(a=e, b=f, c=g, d=h, sel[0]=sel[0], sel[1]=sel[1]);
25     Mux16(a=abcdOut, b=efghOut, sel=sel[2], out=out);
26 }

```

Input pins

a 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 dec

b 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 dec

c 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 dec

d 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 dec

e 0 1 0 1 0 1 1 0 0 1 1 1 1 0 0 0 dec

f 0 1 1 0 0 1 1 1 1 0 0 0 1 0 0 1 dec

g 0 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0 dec

h 1 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 dec

sel 1 1 1 dec

Output pins

out 1 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 dec

Internal pins

abcdOut 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 dec

efghOut 1 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 dec

Simulation successful: The output file is identical to the compare file

4. DMux4Way

NAND2Tetris / Hardware Simulator / DMux4Way.hdl

HDL Builtin Project1 DMux4Way Chip DMux4Way Eval Reset Clock: 0 Test Test Script Compare File Output File Diff Table

```

1 // This file is part of www.nand2tetris.org
2 // and the book "The Elements of Computing Systems"
3 // by Nisan and Schocken, MIT Press.
4 // File name: projects/1/DMux4Way.hdl
5 /**
6  * 4-way demultiplexor:
7  * [a, b, c, d] = [in, 0, 0, 0] if sel = 00
8  * [0, in, 0, 0] if sel = 01
9  * [0, 0, in, 0] if sel = 10
10 * [0, 0, 0, in] if sel = 11
11 */
12 CHIP DMux4Way {
13     IN in, sel[2];
14     OUT a, b, c, d;
15
16     PARTS:
17     DMux(in=in, sel=sel[1], a=a, b=c);
18     DMux(in=a, sel=sel[0], a=a, b=b);
19     DMux(in=c, sel=sel[0], a=c, b=d);
20 }

```

Input pins

in 1

sel 1 1 dec

Output pins

a 0

b 0

c 0

d 1

Internal pins

ab 0

cd 1

Simulation successful: The output file is identical to the compare file

15 /. DMux8Way

1.s file is part of www.nand2tetris.org

2.I the book "The Elements of Computing Systems"

3.Nisan and Schocken, MIT Press.

4.e name: projects/1/DMux8Way.hdl

5

6.way demultiplexor:

7 b, c, d, e, f, g, h] = [in, 0, 0, 0, 0, 0, 0, 0

8 [0, in, 0, 0, 0, 0, 0, 0

9 [0, 0, in, 0, 0, 0, 0, 0

10 [0, 0, 0, in, 0, 0, 0, 0

11 [0, 0, 0, 0, in, 0, 0, 0

12 [0, 0, 0, 0, 0, in, 0, 0

13 [0, 0, 0, 0, 0, 0, in, 0

14 [0, 0, 0, 0, 0, 0, 0, in

15

16.Mux8Way {

17 in, sel[3];

18 IT a, b, c, d, e, f, g, h;

19

20.RTS:

21 lux(in=in, sel=sel[2], a=abcd, b=efgh);

22 lux4Way(in=abcd, sel=sel[0..1], a=a, b=b, c=c, d=d);

23 lux4Way(in=efgh, sel=sel[0..1], a=e, b=f, c=g, d=h);

24

Input pins

in1

sel111dec

Output pins

a0

b0

c0

d0

e0

f0

g0

h1

Internal pins

abcd0

efgh1

Test

Test Script

Compare File

Output File

Diff Table

1	in	sel	a	b	c	d	e	f	g	h
2	0	000	0	0	0	0	0	0	0	0
3	0	001	0	0	0	0	0	0	0	0
4	0	010	0	0	0	0	0	0	0	0
5	0	011	0	0	0	0	0	0	0	0
6	0	100	0	0	0	0	0	0	0	0
7	0	101	0	0	0	0	0	0	0	0
8	0	110	0	0	0	0	0	0	0	0
9	0	111	0	0	0	0	0	0	0	0
10	1	000	1	0	0	0	0	0	0	0
11	1	001	0	1	0	0	0	0	0	0
12	1	010	0	0	1	0	0	0	0	0
13	1	011	0	0	0	1	0	0	0	0
14	1	100	0	0	0	0	1	0	0	0
15	1	101	0	0	0	0	0	1	0	0
16	1	110	0	0	0	0	0	0	1	0
17	1	111	0	0	0	0	0	0	0	1

Simulation successful: The output file is identical to the compare file