

**High Speed 5 Tuple Extraction Design for**

**IP Traffic Classification**

**School of Electrical and Electronic Engineering**

**And Computer Science**

**Final Year Report**

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**Abstract**

This project covers the background research required, system architecture design, verification and optimisation of a 10 Gigabits/second 5 Tuple extraction circuit for IP flow classification to be produced for a Field Programmable Gate Array (FPGA). The research that was carried out covers the OSI model, Physical layer and 10 Gigabits/second Media Independent Interface (XGMII), Ethernet frame format, Virtual Local Area Network (VLAN) tagging, Multi-Protocol Label Switching (MPLS), Internet Protocol (IP) header format, Internet Control Message Protocol (ICMP) header format, Transport Control Protocol (TCP) header format, User Defined Protocol (UDP), traffic classification, traffic normalisation, hardware design process, Ethernet header formats and Endianness. The 5 Tuple extraction module system architecture is thoroughly described and the design is extensively verified so to make sure of no possible hold states in the Finite State Machines (FSM) and that all data and errors are detected correctly. The optimisation done on the design was found to be affective by reducing the Lookup Table (LUT) and register count of the chosen FPGA. The project plan will also be addressed to comment on how the work load was completed in relation to the proposed strategy.

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