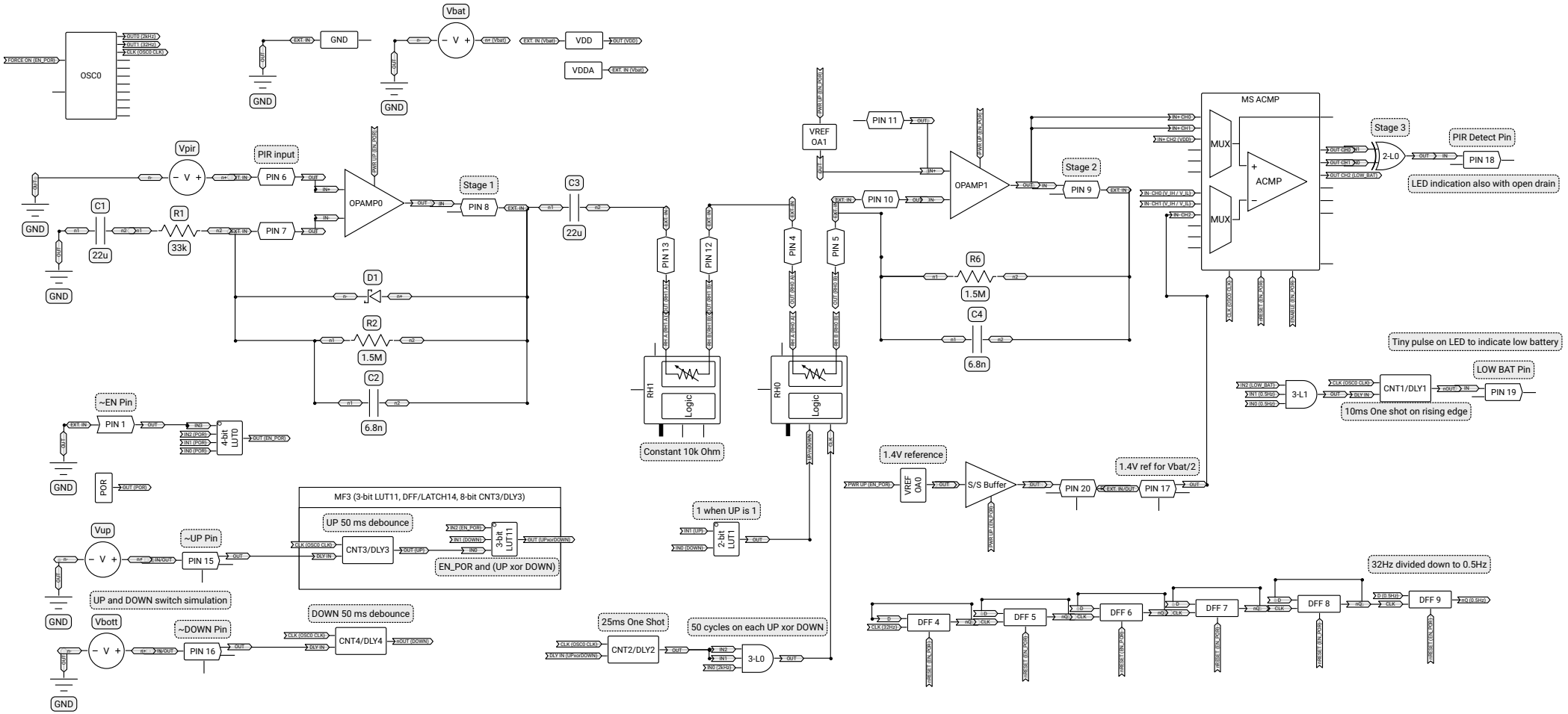
OSC0
FORCE ON (EN_POR)
OUT0 (3kHz)
OUT1 (32Hz)
CLK (OSC0 CLK)
GND
Vbat
VDD
VDDA
Vpir
PIR input
PIN 6
OPAMP0
Stage 1
PIN 8
C1
22u
R1
33k
PIN 7
C3
22u
D1
R2
1.5M
C2
6.8n
~EN Pin
PIN 1
4-bit LUT0
POR
Vup
~UP Pin
PIN 15
Vbott
~DOWN Pin
PIN 16
UP and DOWN switch simulation
MF3 (3-bit LUT11, DFF/LATCH14, 8-bit CNT3/DLY3)
UP 50 ms debounce
CNT3/DLY3
3-bit LUT11
EN_POR and (UP xor DOWN)
DOWN 50 ms debounce
CNT4/DLY4
PIN 13
PIN 12
PIN 4
PIN 5
RH1
RH0
Logic
Constant 10k Ohm
1 when UP is 1
2-bit LUT1
25ms One Shot
CNT2/DLY2
3-L0
50 cycles on each UP xor DOWN
VREF OA1
PIN 11
OPAMP1
Stage 2
PIN 9
PIN 10
R6
1.5M
C4
6.8n
MS ACMP
MUX
ACMP
Stage 3
2-L0
PIR Detect Pin
PIN 18
LED indication also with open drain
Tiny pulse on LED to indicate low battery
3-L1
CNT1/DLY1
LOW BAT Pin
PIN 19
10ms One shot on rising edge
1.4V reference
VREF OA0
S/S Buffer
PIN 20
PIN 17
1.4V ref for Vbat/2
32Hz divided down to 0.5Hz
DFF 4
DFF 5
DFF 6
DFF 7
DFF 8
DFF 9

PIN 1 (GPI0)
Label: "~EN Pin"

Property	*Value*
I/O selection	Digital input
In mode	Digital in with Schmitt trigger
Out mode	None
Resistor	Pull Up
Resistor value	1M

VDD (PIN 2)

Property	*Value*
Min. value (V)	2.40
Typ. value (V)	3.00
Max. value (V)	3.40

PIN 4 (RH0_A/GPI1)

Property	*Value*
I/O selection	Analog input/output
In mode	Analog input/output
Out mode	Analog input/output
Resistor	Floating

PIN 5 (RH0_B/GPI2)

Property	*Value*
I/O selection	Analog input/output
In mode	Analog input/output
Out mode	Analog input/output
Resistor	Floating

PIN 6 (OA0+)
Label: "PIR input"

Property	*Value*
I/O selection	Analog input/output
In mode	Analog input/output
Out mode	Analog input/output

PIN 7 (OA0-)

Property	*Value*
I/O selection	Analog input/output
In mode	Analog input/output
Out mode	Analog input/output

PIN 8 (OA0_OUT)
Label: "Stage 1"

Property	*Value*
I/O selection	Analog input/output
In mode	Analog input/output
Out mode	Analog input/output

PIN 9 (OA1_OUT)
Label: "Stage 2"

Property	*Value*
I/O selection	Analog input/output
In mode	Analog input/output
Out mode	Analog input/output

PIN 10 (OA1-)

Property	*Value*
I/O selection	Analog input/output
In mode	Analog input/output
Out mode	Analog input/output

PIN 11 (OA1+)

Property	*Value*
I/O selection	Analog input/output
In mode	Analog input/output
Out mode	Analog input/output

PIN 12 (RH1_B/GPI3)

Property	*Value*
I/O selection	Analog input/output
In mode	Analog input/output
Out mode	Analog input/output
Resistor	Pull Down
Resistor value	1M

PIN 13 (RH1_A/GPI4)

Property	*Value*
I/O selection	Analog input/output
In mode	Analog input/output
Out mode	Analog input/output
Resistor	Floating

VDDA (PIN 14)

Property	*Value*
Min. value (V)	N/D
Typ. value (V)	N/D
Max. value (V)	N/D

PIN 15 (GPIO0)
Label: "~UP Pin"

Property	*Value*
I/O selection	Digital input
In mode	Digital in with Schmitt trigger
Out mode	None
Resistor	Pull Up
Resistor value	1M

PIN 16 (GPIO1)
Label: "~DOWN Pin"

Property	*Value*
I/O selection	Digital input
In mode	Digital in with Schmitt trigger
Out mode	None
Resistor	Pull Up
Resistor value	1M

PIN 17 (GPIO2)
Label: "1.4V ref for Vbat/2"

Property	*Value*
I/O selection	Analog input/output
In mode	Analog input/output
Out mode	Analog input/output
Resistor	Floating

PIN 18 (SCL/GPIO4)
Label: "PIR Detect Pin"

Property	*Value*
I/O selection	Digital output
In mode	None
Out mode	3.2x open drain NMOS
Resistor	Pull Up
Resistor value	100K

PIN 19 (SDA/GPIO5)
Label: "LOW BAT Pin"

Property	*Value*
I/O selection	Digital output
In mode	None
Out mode	3.2x open drain NMOS
Resistor	Pull Up
Resistor value	100K

PIN 20 (GPIO3)

Property	*Value*
I/O selection	Analog input/output
In mode	Analog input/output
Out mode	Analog input/output
Resistor	Floating

Digital Rheostat0

Property	*Value*
Enable status	Enable
EPG data to Rheostat	Disable
Data mapping selection	MSB
Active level for UP/DOWN	Up when HIGH
Resistance (initial data)	500
Calculated resistance	~49.618 kOhm

Digital Rheostat1
Label: "Constant 10k Ohm"

Property	*Value*
Enable status	Enable
Mode	Rheostat
EPG data to Rheostat	Disable
Data mapping selection	MSB
Active level for UP/DOWN	Up when HIGH
Resistance (initial data)	101
Calculated resistance	~10.0228 kOhm

OPAMP0

Property	*Value*
Vref connection	Disconnected
Vref	1408 mV

OPAMP1

Property	*Value*
Vref connection	to IN+
Vref	VDD * (32 / 63)

VREF OPAMP0
Label: "1.4V reference"

Property	*Value*
Enable selection	From register
Register enable	Vref enable
Input voltage selection	2.016 V
Output selection	1408 mV
High side VREF selection	Disable
VREF LPF	Disable

VREF OPAMP1

Property	*Value*
Enable selection	From matrix
Register enable	Vref enable
Input voltage selection	VDD
Output selection	VDD * (32 / 63)
VREF LPF	Enable

MS ACMP

Property	*Value*
Mode selection	Sampling
Number of channels	3
Enable mode	High Level Activation
Output result appearance	One by one
Clock source	OSC0
Sampling clock	OSC0
Analog MUX input	Sampling engine (ACMP ON)
Analog MUX Out to GPIO2	Disable
Sync ready polarity	Non-inverted
Force bandgap on	Enable
Input voltage selection	VDD
Channel 0	
IN+ gain	Disable
IN+ source	OA1
IN- Low to High source	VDD * (48 / 63)
IN- High to Low source	VDD * (48 / 63)
Hysteresis	-
Output polarity	Q
Channel 1	
IN+ gain	Disable
IN+ source	OA1
IN- Low to High source	VDD * (16 / 63)
IN- High to Low source	VDD * (16 / 63)
Hysteresis	-
Output polarity	Q
Channel 2	
IN+ gain	x0.5
IN+ source	VDD
IN- Low to High source	Ext. Vref (PIN 17 (GPIO2))
IN- High to Low source	Ext. Vref (PIN 17 (GPIO2))
Hysteresis	-
Output polarity	nQ

2-bit LUT0/DFF/LATCH0
Label: "Stage 3"

IN1	IN0	OUT
0	0	0
0	1	1
1	0	1
1	1	0

Property	Value
Type	LUT
Standard gates	XOR

2-bit LUT1/DFF/LATCH1
Label: "1 when UP is 1"

IN1	IN0	OUT
0	0	0
0	1	0
1	0	1
1	1	1

Property	Value
Type	LUT
Standard gates	Defined by user

3-bit LUT0/DFF/LATCH2
Label: "50 cycles on each UP xor DOWN"

IN2	IN1	IN0	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Property	Value
Type	LUT
Standard gates	AND

3-bit LUT1/DFF/LATCH3

IN2	IN1	IN0	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Property	Value
Type	LUT
Standard gates	AND

3-bit LUT2/DFF/LATCH4

Property	Value
Type	DFF / LATCH
Mode	DFF
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Inverted (nQ)
Active level for RST/SET	Low level

3-bit LUT3/DFF/LATCH5

Property	Value
Type	DFF / LATCH
Mode	DFF
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Inverted (nQ)
Active level for RST/SET	Low level

3-bit LUT4/DFF/LATCH6/Shift Register 0

Property	Value
Type	DFF / LATCH
Mode	DFF
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Inverted (nQ)
Active level for RST/SET	Low level

3-bit LUT5/DFF/LATCH7/Shift Register 1

Property	Value
Type	DFF / LATCH
Mode	DFF
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Inverted (nQ)
Active level for RST/SET	Low level

3-bit LUT6/DFF/LATCH8/Shift Register 2

Property	Value
Type	DFF / LATCH
Mode	DFF
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Inverted (nQ)
Active level for RST/SET	Low level

3-bit LUT7/DFF/LATCH9/Shift Register 3
Label: "32Hz divided down to 0.5Hz"

Property	Value
Type	DFF / LATCH
Mode	DFF
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Inverted (nQ)
Active level for RST/SET	Low level

4-bit LUT0/DFF/LATCH10

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Property	Value
Type	LUT
Standard gates	Defined by user

MF1 (3-bit LUT9, DFF/LATCH12, 8-bit CNT1/DLY1)

8-bit CNT1/DLY1 (MF1)
Label: "10ms One shot on rising edge"

Property	Value
Mode	One shot
Counter data	20
Pulse width (typical)	10.2539 ms
Edge mode select	Rising
DLY IN init. value	Initial 0
Output polarity	Inverted (nOUT)
Mode signal SYNC	Bypass
Clock source	OSC0
Clock frequency	2.048 kHz

MF2 (3-bit LUT10, DFF/LATCH13, 8-bit CNT2/DLY2)

8-bit CNT2/DLY2 (MF2)
Label: "25ms One Shot"

Property	Value
Mode	One shot
Counter data	50
Pulse width (typical)	24.9023 ms
Edge mode select	Rising
DLY IN init. value	Initial 0
Output polarity	Non-inverted (OUT)
Mode signal SYNC	Bypass
Clock source	OSC0
Clock frequency	2.048 kHz

MF3 (3-bit LUT11, DFF/LATCH14, 8-bit CNT3/DLY3)

3-bit LUT11 (MF3)
Label: "EN_POR and (UP xor DOWN)"

IN2	IN1	IN0	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Property	Value
Standard gates	Defined by user

8-bit CNT3/DLY3 (MF3)
Label: "UP 50 ms debounce"

Property	Value
Mode	Delay
Counter data	101
Delay time (typical)	49.8047 ms
Edge mode select	Both
DLY IN init. value	Bypass the initial
Output polarity	Non-inverted (OUT)
Mode signal SYNC	Bypass
Clock source	OSC0
Clock frequency	2.048 kHz

MF4 (3-bit LUT12, DFF/LATCH15, 8-bit CNT4/DLY4)

8-bit CNT4/DLY4 (MF4)
Label: "DOWN 50 ms debounce"

Property	Value
Mode	Delay
Counter data	101
Delay time (typical)	49.8047 ms
Edge mode select	Both
DLY IN init. value	Bypass the initial
Output polarity	Inverted (nOUT)
Mode signal SYNC	Bypass
Clock source	OSC0
Clock frequency	2.048 kHz

OSC0

Property	Value
Control pin mode	Force on
OSC power mode	Force Power On
Clock selector	OSC
'OSC0' frequency	2.048 kHz
'CLK' predivider by	1
'OUT0' second divider by	1
'OUT1' second divider by	64

Sink/Source Buffer

Property	Value
Power up source	From register
Power up register	Enable
Input selection	OA0 VREF
Input selection from VREF	1408 mV

External Components

R1

Property	*Value*
Element	Resistor
Resistance	33kOhm

R2

Property	*Value*
Element	Resistor
Resistance	1.5MOhm

R6

Property	*Value*
Element	Resistor
Resistance	1.5MOhm

C1

Property	*Value*
Element	Capacitor
Capacitance	22uF
Series Resistance	1mOhm
Parallel Resistance	100GOhm

C2

Property	*Value*
Element	Capacitor
Capacitance	6.8nF
Series Resistance	1mOhm
Parallel Resistance	100GOhm

C3

Property	*Value*
Element	Capacitor
Capacitance	22uF
Series Resistance	1mOhm
Parallel Resistance	100GOhm

C4

Property	*Value*
Element	Capacitor
Capacitance	6.8nF
Series Resistance	1mOhm
Parallel Resistance	100GOhm

D1

Property	*Value*
Element	Diode
Diode type	Schottky

Vbat

Property	*Value*
Element	Voltage Source
Pre-start delay	0s
Internal capacitance	100nF
Internal resistance	1Ohm
Repeat state	One-shot
Pre-start state	Low
End state	Keep last state
Type	Trapeze
Mode	Invert
Umin	2.6V
Umax	3.3V
T low	1.7s
T rising	5ms
T high	5s
T falling	5ms

Vpir

Property	*Value*
Element	Voltage Source
Pre-start delay	0s
Repeat state	Cyclic
Pre-start state	Low
Type	Sine
Zero offset	0V
Amplitude	2mV
Frequency	5Hz
Damping factor	0Hz

Vup

Property	*Value*
Element	Voltage Source
Pre-start delay	0s
Repeat state	One-shot
Pre-start state	Low
End state	Keep last state
Type	Logic pattern
Mode	Normal
Umax	3V
Umin	0V
Levels adjustment	Standard
Rise time	1µs
Fall time	1µs

Vup Pattern Points

Duration	*Voltage*
100ms	3V
5ms	0V
5ms	3V
5ms	0V
100ms	3V
100ms	0V
100ms	3V
100ms	0V
100ms	3V
100ms	0V
500µs	3V

Vbott	
Property	*Value*
Element	Voltage Source
Pre-start delay	0s
Repeat state	One-shot
Pre-start state	Low
End state	Keep last state
Type	Logic pattern
Mode	Normal
Umax	3.3V
Umin	0V
Levels adjustment	Standard
Rise time	1µs
Fall time	1µs

Vbott Pattern Points	
Duration	*Voltage*
1000ms	3.3V
5ms	0V
5ms	3.3V
5ms	0V
5ms	3.3V
100ms	0V
100ms	3.3V
100ms	0V
100ms	3.3V
100ms	0V
100ms	3.3V

Project Specs			
	Min.	*Typ.*	*Max.*
VDD	2.40	3.00	3.40
Temperature (°C):	-20.00	25.00	50.00

General Settings	
Force bandgap on	Enable
GPIO quick charge	Disable
Lock status	Unlocked
Pattern ID	1

I2C Probing

Probe pins			
Pin	*Signal name*	*Register*	*In use*
GND (PIN 3) -> OUT		HEX: 0x3C`b0 DEC: 60`b0	+
2-bit LUT0/DFF/LATCH0 -> OUT	NET21	HEX: 0x3C`b1 DEC: 60`b1	+
2-bit LUT1/DFF/LATCH1 -> OUT	NET35	HEX: 0x3C`b2 DEC: 60`b2	+
3-bit LUT0/DFF/LATCH2 -> OUT	NET34	HEX: 0x3C`b3 DEC: 60`b3	+
3-bit LUT1/DFF/LATCH3 -> OUT	NET37	HEX: 0x3C`b4 DEC: 60`b4	+
3-bit LUT2/DFF/LATCH4 -> nQ	NET42	HEX: 0x3C`b5 DEC: 60`b5	+
3-bit LUT3/DFF/LATCH5 -> nQ	NET43	HEX: 0x3C`b6 DEC: 60`b6	+
3-bit LUT4/DFF/LATCH6/ Shift Register 0 -> nQ	NET44	HEX: 0x3C`b7 DEC: 60`b7	+
3-bit LUT5/DFF/LATCH7/ Shift Register 1 -> nQ	NET45	HEX: 0x3D`b0 DEC: 61`b0	+
3-bit LUT6/DFF/LATCH8/ Shift Register 2 -> nQ	NET39	HEX: 0x3D`b1 DEC: 61`b1	+
3-bit LUT7/DFF/LATCH9/ Shift Register 3 -> nQ	0.5Hz	HEX: 0x3D`b2 DEC: 61`b2	+
4-bit LUT0/DFF/LATCH10 -> OUT	EN_POR	HEX: 0x3D`b3 DEC: 61`b3	+
8-bit CNT0/DLY0/FSM0 (MF0) -> OUT		HEX: 0x3D`b4 DEC: 61`b4	-
3-bit LUT8 (MF0) -> OUT		HEX: 0x3D`b5 DEC: 61`b5	-
8-bit CNT1/DLY1 (MF1) -> nOUT	NET48	HEX: 0x3D`b6 DEC: 61`b6	+
3-bit LUT9 (MF1) -> OUT		HEX: 0x3D`b7 DEC: 61`b7	-
8-bit CNT2/DLY2 (MF2) -> OUT	NET32	HEX: 0x3E`b0 DEC: 62`b0	+
3-bit LUT10 (MF2) -> OUT		HEX: 0x3E`b1 DEC: 62`b1	-
8-bit CNT3/DLY3 (MF3) -> OUT	UP	HEX: 0x3E`b2 DEC: 62`b2	+

Probe pins			
3-bit LUT11 (MF3) -> OUT	UPxorDOWN	HEX: 0x3E`b3 DEC: 62`b3	+
8-bit CNT4/DLY4 (MF4) -> nOUT	DOWN	HEX: 0x3E`b4 DEC: 62`b4	+
3-bit LUT12 (MF4) -> OUT		HEX: 0x3E`b5 DEC: 62`b5	-
PIN 18 (SCL/GPIO4) -> OUT/I2C -> OUT8		HEX: 0x3E`b6 DEC: 62`b6	-
PIN 19 (SDA/GPIO5) -> OUT/I2C -> OUT9		HEX: 0x3E`b7 DEC: 62`b7	-
I2C -> OUT0		HEX: 0x3F`b0 DEC: 63`b0	-
I2C -> OUT1		HEX: 0x3F`b1 DEC: 63`b1	-
I2C -> OUT2/EPG -> OUT2		HEX: 0x3F`b2 DEC: 63`b2	-
I2C -> OUT3/EPG -> OUT3		HEX: 0x3F`b3 DEC: 63`b3	-
I2C -> OUT4/EPG -> OUT4		HEX: 0x3F`b4 DEC: 63`b4	-
I2C -> OUT5/EPG -> OUT5		HEX: 0x3F`b5 DEC: 63`b5	-
I2C -> OUT6/EPG -> OUT6		HEX: 0x3F`b6 DEC: 63`b6	-
I2C -> OUT7/EPG -> OUT7		HEX: 0x3F`b7 DEC: 63`b7	-
PIN 4 (RH0_A/GPI1) -> OUT	RH0 A	HEX: 0x40`b0 DEC: 64`b0	-
PIN 5 (RH0_B/GPI2) -> OUT	RH0 B	HEX: 0x40`b1 DEC: 64`b1	-
PIN 12 (RH1_B/GPI3) -> OUT	RH1 B	HEX: 0x40`b2 DEC: 64`b2	-
PIN 13 (RH1_A/GPI4) -> OUT	RH1 A	HEX: 0x40`b3 DEC: 64`b3	-
PIN 1 (GPI0) -> OUT	NET1	HEX: 0x40`b4 DEC: 64`b4	+
PIN 15 (GPIO0) -> OUT	NET49	HEX: 0x40`b5 DEC: 64`b5	+
PIN 16 (GPIO1) -> OUT	NET28	HEX: 0x40`b6	+

Probe pins			
		DEC: 64`b6	
PIN 17 (GPIO2) -> OUT	NET27	HEX: 0x40`b7 DEC: 64`b7	-
PIN 20 (GPIO3) -> OUT		HEX: 0x41`b0 DEC: 65`b0	-
P DLY -> OUT		HEX: 0x41`b5 DEC: 65`b5	-
OSC0 -> OUT0	2kHz	HEX: 0x41`b6 DEC: 65`b6	+
OSC0 -> OUT1	32Hz	HEX: 0x41`b7 DEC: 65`b7	+
OSC1 -> OUT		HEX: 0x42`b0 DEC: 66`b0	-
MS ACMP -> OUT CH0	NET23	HEX: 0x42`b1 DEC: 66`b1	+
MS ACMP -> OUT CH1	NET24	HEX: 0x42`b2 DEC: 66`b2	+
MS ACMP -> OUT CH2	LOW_BAT	HEX: 0x42`b3 DEC: 66`b3	+
MS ACMP -> OUT CH3		HEX: 0x42`b4 DEC: 66`b4	-
MS ACMP -> OUT CH4		HEX: 0x42`b5 DEC: 66`b5	-
MS ACMP -> OUT CH5		HEX: 0x42`b6 DEC: 66`b6	-
MS ACMP -> SYNC READY		HEX: 0x42`b7 DEC: 66`b7	-
OPAMP0 -> OUT	NET14	HEX: 0x43`b0 DEC: 67`b0	-
OPAMP1 -> OUT	NET26	HEX: 0x43`b1 DEC: 67`b1	-
POR -> OUT	POR	HEX: 0x43`b2 DEC: 67`b2	+
Digital Rheostat0 -> Overflow flag		HEX: 0x43`b3 DEC: 67`b3	-
Digital Rheostat1 -> Overflow flag		HEX: 0x43`b4 DEC: 67`b4	-
EPG -> OUT0		HEX: 0x43`b5 DEC: 67`b5	-

Probe pins			
EPG -> OUT1		HEX: 0x43`b6 DEC: 67`b6	-
VDD (PIN 2) -> OUT	VDD	HEX: 0x43`b7 DEC: 67`b7	-

Macrocells		
Macrocell	*Property*	*Register*
Digital Rheostat0	Resistance	HEX: 0x9A, 0x9B DEC: 154, 155
Digital Rheostat1	Resistance	HEX: 0x9C, 0x9D DEC: 156, 157