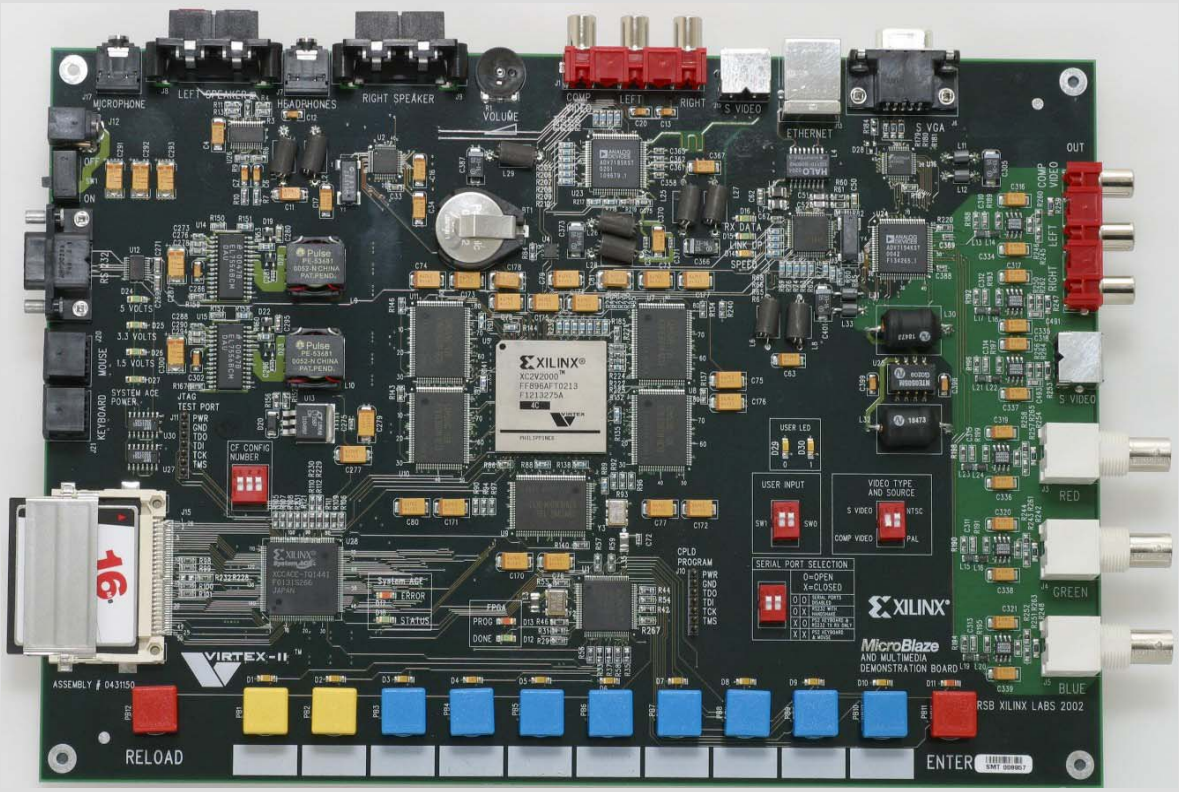
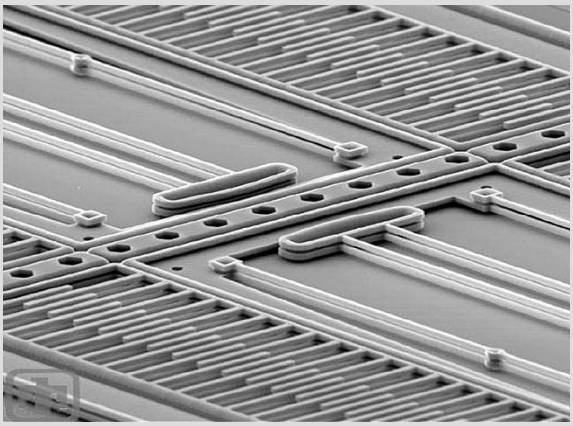
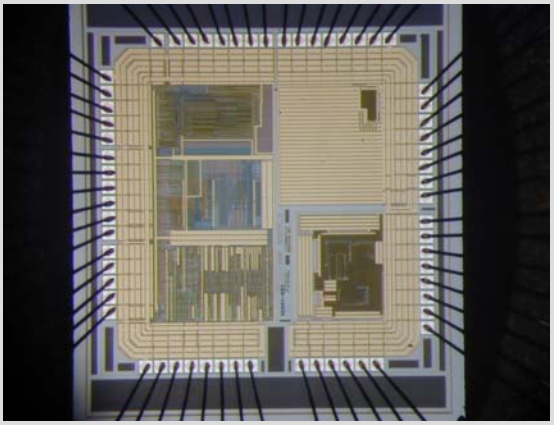
RESEARCH CENTRE FOR INTEGRATED MICROSYSTEMS (RCIM) REPORT

Jan. 01, 2006 - Mar. 30, 2007







Electrical & Computer Engineering
University of Windsor
Essex Hall, 401 Sunset Avenue
Windsor, Ontario, Canada N9B 3P4

RESEARCH CENTRE FOR INTEGRATED MICROSYSTEMS

DEPARTMENT OF ELECTRICL AND COMPUTER ENGINEERING

UNIVERSITY OF WINDSOR

Jan. 1, 2006 - Mar. 30, 2007

The Research Center for Integrated Microsystems within the Department of Electrical and Computer Engineering in the Faculty of Engineering at the University of Windsor is mandated to carry out leading edge research, developing collaborative partnerships and educating highly qualified graduate students in the following areas:

1. **MICROELECTRONIC,** including:

   - High Speed DSP System
   - Computer Arithmetic
   - Encryption
   - Testing of Mixed Signal Integrated Circuits
   - Field Programmable Chips and Systems
   - CMOS and nanoelectronic circuits design

2. **MICROELECTROMECHANICAL SYSTEMS (MEMS),** including:

   - Sensors and Filters
   - Capacitive Microphones and 3-D Acoustical Sensing
   - Electromagnetic Microactuators
   - Acousto_Magnetic Transducers
   - Optical Switching MEMS
   - Automotive Sensors
   - Customs MEMS Sockets
   - Micro power Generators
   - Atomic Force Microscopy
   - MEMS RADAR

3. **Digital Signal Processing and Communication,** including:

   - Algorithms
   - Massively Parallel Arrays and Special Architects
   - Computer Vision and Image Processing
   - Pattern Recognition and Document Analysis

- Network Security Management
- Network Management

The projects vary from fundamental pre-competitive research to mission oriented research and technology transfer. There is an emphasis on problems requiring signal processing systems implemented with advanced integrated Microsystems.

I. RCIM MEMBERS

(A) Faculty Members:

Eight professors in Electrical and Computer Engineering carry out research and supervise graduate students as members of the Research Centre for Integrated Microsystems. The day to day operation of the Center is administered by the Manager of the RCIM who provides training for the new graduate students on how to use the facilities as well as maintaining the hardware and CAD tools used by the RCIM members.

1 Dr. Majid Ahmadi, Professor (Director, RCIM)
2. Dr. Shervin Erfani, Professor
3. Dr. Chunhong Chen, Associate Professor
4. Dr. Esam Abdel-Raheem, Associate Professor
5. Dr. Sazzadur Chowdhury, Assistant Professor
6. Dr. Roberto Muscedere, Assistant Professor
7. Dr. Mohammed Khalid, Assistant Professor
8. Dr. Huapeng Wu, Assistant Professor
9. Mr. Rashid Rashidzadeh (Manager)

(B) Student Members:

RCIM has a track record of outstanding graduate outcomes. Our students have been very competitive in the job market and in admission to Ph.D. programs at major universities. Recent appointments to prominent positions include:

❖ RCIM Students Graduated in 2006 -2007

First name	Surname	Program	Supervisor	Date of Graduation	Career
Kevin	Biswas	M.A.Sc.	Dr. Ahmadi	Fall 2006	Ph.D. student in Carnegie Mellon University
Xiaoyin	Xu	M.A.Sc.	Dr. Ahmadi	Summer 2006	Mtekvision co Ltd, Ottawa
Thomas	Williams	Ph.D.	Dr. Ahmadi	Fall 2006	IT Center, St. Clair College
Amir	Yazdanshenas	M.A.Sc.	Dr. Khalid	Fall 2006	Associate IC Design Eng. Intellon, Toronto
Ian	Anderson	M.A.Sc.	Dr. Khalid	Winter 2007	
Jason	Tong	M.A.Sc.	Dr. Khalid	Winter 2007	Ph.D. student, McMaster University
Kevin	Banovic	M.A.Sc.	Dr. Khalid	Winter 2006	Ph.D. student in the University of Toronto
Andrew	TAM	M.A.Sc.	Dr. Chowdhury	October 2006	Ph.D. student the University of Ottawa
Matthew	Meloche	M.A.Sc.	Dr. Chowdhury	April 2007	CK-Energy in Chatham
Hu	Rongrong	M.A.Sc.	Dr. Chowdhury	June 2006	Private sector employment in China
Raymond	LEE	M.A.Sc.	Dr. Abdel-Raheem & Dr. Khalid	Winter 2007	
Harb	Abdulhamid	M.A.Sc.	Dr. Abdel-Raheem & Dr. Tepe.	Fall 2006	TapRoot Systems Inc.- North Carolina, USA
Mahzad	Azarmehr	M.A.Sc.	Dr. R. Muscedere	Fall 2006	Ph.D. student in the University of Windsor

❖ Current RCIM Students

First name	Surname	Program	Supervisor	Thesis Title
Carol Lynn	Deck	M.A.Sc.	Dr. M. Ahmadi(Co-supervise with Dr. Gaspar)	Signature Analysis of Engine Signals for Fault Detection Using ARMA Model
Bhaskar	Ray	M.A.Sc.	Dr. M. Ahmadi	Fault Detection of Engines Through Signature Analysis of Noise Vibration Using Wavelet Transforms
Peng	Chang	M.A.Sc.	Dr. M. Ahmadi	Low Power Digital Multiplier Design
Payman	Samadi	M.A.Sc.	Dr. M. Ahmadi	Application of Evolutionary Programming for Digital Filter Design
Songtao	Huang	Ph.D.	Dr. M. Ahmadi	Hidden Markov Model and Its Applications In Document Image Analysis
Mitra	Mirhassani	Ph.D.	Dr. M. Ahmadi (Co-Supervise with Dr. Jullien)	Low power area efficient current mode circuitry for continuous valued number system arithmetic
David	Li	Ph.D.	Dr. M. Ahmadi	Low power Efficient Design of H.264/AVC
Mohammed	Islam	Ph.D.	Dr. M. Ahmadi	Computer Vision for Quality Process Control Application
Jiuling	Tang	Ph.D.	Dr. M. Ahmadi	VLSI Implementation of Error Correcting Circuits for Communication
Elham	Shahinfard	Ph.D.	Dr. M. Ahmadi (Co-supervise with Dr. Sid-Ahmed)	Cost Efficient and Reliable HDTV
Ashkan	Hosseinzadeh Namin	Ph.D.	Dr. M.Ahmadi(Co-supervise with Dr. H.Wu)	VLSI implementation of an Elliptic Curve Processor
Yanjie	Mao	M.A.Sc.	Dr. C. Chen	Statistical model for single-electron threshold logic
Mohammed	Berhea	M.A.Sc.	Dr. C. Chen	Low power design for Radio-frequency identification
Bingxi	Li	M.A.Sc.	Dr. C. Chen	Memory design using single-electron devices
Karl	Leboeuf	M.A.Sc..	Dr. R. Muscedere	TBA
Neil	Scott	M.A.Sc..	Dr. R. Muscedere	Development of a low cost, high speed machine vision system for pill inspection
Anthony	Karloff	M.A.Sc.	Dr. R. Muscedere	Development of a low cost, high speed machine vision system for pill inspection

❖ Current RCIM Students

First name	Surname	Program	Supervisor	Thesis Title
Paresh	Bharkhada	M.A.Sc..	Dr. R. Muscedere	TBA
Sam	Farrokhi	Ph.D.	Dr. R. Muscedere	TBA
Farhad	Hajaliasghari	Ph.D.	Dr. J.Wu (Co-supervisor Dr. Ahmadi)	TBA
James	Wiebe	M.A.Sc.	Dr. S. Erfani	"Implementing the Five-Layer IPSec Framework using FPGAs"
Nima	Bayan	Ph.D.	Dr. S. Erfani	"On Frequency-Domain Analysis and Synthesis of Linear Time-Varying (LTV) Network Systems"
Fang	Chen	Ph.D.	Dr. S. Erfani	"Implementation and Stability of High-Order Continuous-Time Sigma-Delta Modulators"
Yonghong	Xu	M.A.Sc.	Dr. M. Khalid	Efficient Quadratic Placement for FPGAs
LIAO	Junsong (Jason)	M.A.Sc.	Dr. M. Khalid	FPGA implementation of a Wireless Sensor Network
Marvan	Kannan	M.A.Sc.	Dr. M. Khalid	Processor Based Emulation Using FPGAs
Omar	Al Rayahi	M.A.Sc.	Dr. M. Khalid	A CAD Tool for Synthesizing Variants of Altera NIOS II Softcore Processor
Aws	Ismail	M.A.Sc.	Dr. M. Khalid	Exploration of Networks-on-chip on FPGAs
Rashid	Rashidzadeh	Ph.D.	Dr. W. C. Miller	A PLL Tester Core for Mixed-Signal SoC Devices
Jose	Martinez Quijada	M.A.Sc.	Dr. S. Chowdhury	A MEMS Micropower Generator for Implantable Biomedical Devices
Ahmad	Sinjari	Ph.D.	Dr. S. Chowdhury	MEMS based High performance Sensor Design for Automotive Collision Avoidance System
Liton	Ghosh	M.A.Sc.	Dr. S. Chowdhury	Accurate Force Modeling of Micro Cantilevers used for Atomic Force Microcopy
Hongmei	Zong	M.A.Sc.	Dr.Abdel-Raheem	Low power FIR filter design

Graduate Student Summary

RCIM Faculty members are supervising 21 Masters and 12 Doctoral candidates. Over 90% of our graduate students were recipient of various scholarships from NSERC, OGS, and University of Windsor.

II. PROFESSIONAL ACTIVITIES of RCIM FACULTY MEMBERS

1. Dr. M. Ahmadi was the OCGS Consultant for the graduate programs in the Department of Electrical & Computer Engineering, Royal Military College of Canada, Sept.5-7, 2006.
2. Dr. M. Ahmadi was a PhD external examiner for Electrical and Computer Engineering Dept., University of Calgary, Oct 5, 2006 student name Hazem Kamel " Fuzzy Logic Particle Filter for High- Performance Target Tracking in Track-While-Scan Radar
3. Dr. M. Ahmadi is the Member of the NSERC Grant Selection Committee GSC-334, 2004-2007.
4. Dr. M. Ahmadi was a PhD External Examiner for Computer Science Department University of Guelph student name: Yasser Hamed Ebrahim "Shape Representation and Description Using the Dynamic Hilbert Curve" Nov. 2006.
5. Dr. M. Ahmadi is the Co-Chair of Tutorial sessions IEEE-ISCAS 2007
6. Dr. M. Ahmadi is the Co-Chair of Best Student Paper Award Committee 2007 IEEE Midwest Symposium on Circuits and Systems.
7. Dr. M. Ahmadi is the Co-Chair of Neural Network Track for 2006 IEEE International Conference on Electronics Circuits.
8. Dr. M. Ahmadi is a Member of the Technical Program Committee for the 2006 IEEE International Conference of Systems, Man and Cybernetics
9. Dr. M. Ahmadi is a Member of the Technical Program Committee of 2007 International
10. Conference on Document Analysis and Recognition.
11. Dr. M. Ahmadi is the Regional Editor for the Journal of Circuits, Systems and Computers.

12. Dr. M. Ahmadi is a Member of the Editorial Board Pattern Recognition Journal
13. Dr. M. Ahmadi is the Associate Editor for the Journal Computers in Electrical Engineering.
14. Dr. S. Chowdhury is the University of Windsor Member Representative (2006-2007) to the Canadian Microelectronics Corporation (CMC Microsystems), Nominated by the President of the University of Windsor.
15. Dr. S. Chowdhury was invited to participate in the CMC Microsystems, Canada's Technology Advisory Committee meeting (TAC97) to determine the future trend in Microsystem Technology and Canada's options in 2006.
16. Dr. S. Chowdhury represented University of Windsor in the Opening Ceremony of Advanced RF Testing Laboratory at the University of Manitoba, Winnipeg on September 7, 2006 as an invited guest
17. Dr. S. Chowdhury is the University of Windsor Investigator for the MICRONET, the Federal Network of Centres of Excellence on Microelectronics, Devices, Circuits and Systems
18. Dr. S. Chowdhury was a reviewer for journal of IEEE Transactions on Circuits and Systems I in 2006.
19. Dr. S. Chowdhury was a reviewer for IEEE Sensors Journal in 2006.
20. Dr. S. Chowdhury was a reviewer for Communications in Nonlinear Science and Numerical Simulations, Elsevier in 2006.
21. Dr. S. Chowdhury is a reviewer for Journal of Nanotechnology, Institute of Physics Publishing, Dirac House, Temple Back, Bristol, UK.
22. Dr. S. Chowdhury is a reviewer for Journal of Micromechanics and Microengineering, Institute of Physics Publishing, Dirac House, Temple Back, Bristol, UK.
23. Dr. S. Chowdhury is a reviewer for IEEE/ASME Journal of Microelectromechanical Systems

III. SCHOLARY ACTIVITIES AND PUBLICATIONS

(a) Refereed Journal Publications

1. Sazzadur Chowdhury, Majid Ahmadi, W. C. Miller, “Pull-In Voltage Study of Electrostatically Actuated Fixed-Fixed Beams Using a VLSI On-Chip Interconnect

Capacitance Model", IEEE/ASME Journal of Microelectromechanical Systems, vol. 15, no. 3, pp. 639-651, June 2006.

2. Raymond Lee, Esam Abdel-Raheem, and Mohammed A. S. Khalid, Improved NLMS-Based Adaptive Algorithms for Echo Cancellation Applications, Journal of Communications, Academy Publisher, vol. 1, No. 7, pp. 1-8, Nov./Dec. 2006.
3. Kevin Banovic, Mohammed A. S. Khalid, and Esam Abdel-Raheem, A Configurable Fractionally-Spaced Blind Adaptive Equalizer for QAM Demodulators, Digital Signal Processing, Elsevier, doi:10.1016/j.dsp.2006.10.009, 2006, In Press, Available online 27 Nov. 2006 via www.sciencedirect.com.
4. Kevin Banovic, Esam Abdel-Raheem, and Mohammed A. S. Khalid, A Novel Radius-Adjusted Approach for Blind Adaptive Equalization, IEEE Signal Processing Letters, pp. 37-40, vol. 13, Jan. 2006.
5. M. Mohajerin, E. Abdel-Raheem, C. Chen ,A Novel 12-b 40 MSamples/s, Low-Power, Low-Area Pipeline Analog-To-Digital Converter, Canadian Journal on Elec. Comp. Eng., pp. 25-29, vol. 31, No. 1, 2006.
6. C. Chen and Z. Li, "A Low-Power and Low-Noise CMOS Analog Multiplier", IEE Proc. Circuits, Devices & Systems, vol. 153, no. 3, June 2006, pp. 261-267.
7. C. Chen and Z. Li, "A Low Power CMOS Analog Multiplier," IEEE Transactions on Circuits and Systems II, vol. 53, no. 2, February 2006, pp. 100-104.
8. Mitra Mirhassani , M. Ahmadi, W.C. Miller " A Feed Forward Time- Multiplexed Neural Network with Mixed –Signal Neuron – Synapse Arrays" Microelectronic Engineering Journal " VLSI Design and Test" Elsevier Science Series. Vol.84, pp300-307, 2007
9. Idris El-Feghi, M.A. Sid-Ahmed, M.Ahmadi " Automatic Localization of Craniofacial Landmarks using Multi Layer Perceptron as a Function Approximator" Pattern Recognition Letters 27, 2006, pp544-550
10. P. Mokrian, G.A. Jullien, M.Ahmadi " On the Reduction of Interconnect Effects in Deep Submicron Implementation of Digital Multiplication Architectures" Journal of Circuits,Systems and Computers, Vol. 15, No.1, Feb. 2006 ,pp83-106.
11. F.Farshadjam ,M.Dehghan, M.Fathi, M.Ahmadi, " A New Compression Based Approach for Reconfiguration Overhead Reduction in Virtex Based RTR Systems " International Journal of Computers and Electrical Engineering, Vol.32, 2006, pp322-347

12. S. Alirezaee, H. Aghania, K. Faez, M.Ahmadi " Off-Line Recognition of Handwritten Middle Age Persian Characters Using Moment" Journal of Pattern Recognition and Image Analysis, Vol. 16, No.4 ,Dec. 2006, pp 622-631
13. Rashid Rashidzadeh, M.Ahmadi, W.C. Miller " On-Chip Measurement of Waveforms in Mixed Signal Circuits Using a Segmented Subsampling Technique" Journal of Analog Integrated Circuits and Signal Processing" Vol. 50,No.2, pp105-113, Feb. 2007

(b) Refereed Journal Papers Accepted for Publication

1. T. Williams, M. Ahmadi, W.C. Miller " Design of 2-D FIR and IIR Filters with Canonic Signed Digit Coefficients using Singular Value Decomposition and Genetic Algorithms" to appear in the Journal of Circuits, Systems and Signal Processing. Date of acceptance Aug. 14,2006, 18 manuscript pages.
2. R. Rashidzadeh, M.Ahmadi, W.C. Miller" Test and Measurement of Analog and RF Cores in Mixed-Signal SoC Environment" accepted for publication in IEEE Transactions on CAD. Date of acceptance 12/25/2006.
3. Harb Abdulhamid, Esam Abdel-Raheem, and Kemal Tepe, 5.9 GHz DSRC Receiver for Wireless Access Vehicular Environments, accepted with minor revision at IET Communications (formerly IEE Proc. on Comm.), Nov. 2006(7-page, 2-column format manuscript). Feb. 1st, 2007.
4. R. Lee, E. Abdel-Raheem, and M.A.S. Khalid, Computationally-Efficient DNLMS-Based Adaptive Algorithms for Echo Cancellation Application, Journal of Communication, Academy Publisher, November, 2006.
5. Kevin Banovic, Esam Abdel-Raheem, and Mohammed A. S. Khalid, Computationally-Efficient Methods for Blind Decision Feedback Equalization for QAM Signals, submitted to Int. Journal. of Electronics & Communications (AEU), Elsevier, July 2006 (11-page, 2-column format manuscript).
6. Banovic, Kevin; Khalid, Mohammed; Abdel-Raheem, Essam, A configurable Fractionally-Spaced Blind Equalizer for QAM Signals, Digital Signal Processing, Elesvier, 2006.

7. A. H. Namin, H. Wu, and M. Ahmadi "Comb Architectures for Finite Field Multiplication in F2m" IEEE transaction on Computers, regular paper, Accepted Jan. 2007.
8. Harb Abdulhamid, Kemal Tepe, and Esam Abdel-Raheem, Performance of DSRC Systems using Conventional Channel Estimation at High Velocities, Int. Journal. of Electronics & Communications (AEU), Elsevier, doi:10.1016/j.aeue.2006.10.005, 2006, In Press, available online 6 Dec. 2006 via www.sciencedirect.com.
9. S. Talakoub, L. Sabeti, B. Shahrrava, M. Ahmadi "An Improved Max-Log-MAP Algorithm for Turbo Decoding and Turbo Equalization" Accepted for publication in IEEE Transactions on Instrumentation and Measurement. Date of acceptance July 20, 2006, 13 manuscript pages

(c) Papers Submitted to Journals

I. Tong, Jason, G; Khalid, Mohammed, A.S., A Comparison of Profiling Tools for FPGA-Based Embedded Systems, Journal of Computers, Academy Publisher, 2006.

II. Raymond Lee, Mohammed A. S. Khalid, and Esam Abdel-Raheem, Configurable Hardware Implementation of a Pipelined DNLMS Adaptive Filter, submitted to Journal of Circuits, Systems and Computer, World Scientific, Feb. 11, 2007.

III. Banovic, Kevin; Abdel; Abdel-Raheem, Esam; Khalid, Mohammed A.S., Computationally Efficient Methods for Blind Decision Feedback Equalization of QAM Signals, AEU International Journal of Electronics and Communication, 2006.

IV. Muscedere, R., A Hardware Efficient Single-Digit 2-Dimensional Logarithmic Number System Addition and Subtraction Circuit, IEEE Transactions on Circuits and Systems I, 12, 2007.

V. A. H. Namin, H. Wu, and M. Ahmadi "A New Finite Field Multiplier Using Redundant Representation", IEEE transaction on Computers. Second round of review, Minor changes, 2006.

VI. A. H. Namin, H. Wu, and M. Ahmadi “A Word Level finite Field Multiplier Using Normal Basis”, IEEE Transaction on Circuits and Systems, 2006.

VII. M. Mirhassani, M. Ahmadi and G. A. Jullien, "Fault Tolerant Arithmetic of Continuous Valued Number System ", Submitted to IEEE Transaction on Computers, 2006.

VIII. M. Mirhassani, M. Ahmadi and G. A. Jullien, "Continuous Valued Digit Adders for Two Operand Binary Addition", Submitted to IEEE Transaction on Computers, 2006.

(d) Refereed Conference papers

1. Chen, Fang; Kuendiger, Till; Erfani, Shervin, “Improved Direct Stability Analysis of High-Order Continuous-Time Sigma-Delta Modulators,” *Proceedings of the 4th International IEEE - NEWCAS Conference*, pp. 73 - 76, Gatineau, Quebec, Canada, June, June 18 – 21, 2006.
2. Adibi, Sasan; Ho, Pin-Han; Lin, Bin; Agnew, G.B.; Erfani, S., “Authentication Authorization and Accounting (AAA) Schemes in WiMAX,” *Proc. 2006 IEEE International Conf. on Electro/Information Technology*, pp. 210 - 215, East Lansing, Michigan, USA, May 7-10, 2006.
3. Adibi, Sasan; Erfani, Shervin; Harbi, Hani, “Security Routing in MANETs - A Comparative Study,” *Proc. 2006 IEEE International Conf. Electro/Information Technology*, pp. 625 - 630, East Lansing, Michigan, USA, IEEE, May 7-10, 2006.
4. Bayan, Nima; Erfani, Shervin, “Frequency Analysis of Time-Varying Systems,” *Proc. 2006 International Conf. Electro/Information Technology*, pp. 33 – 36, East Lansing, Michigan, USA, IEEE, May 7 - 10, 2006.
5. Chen, Fang; Kuendiger,T.; Erfani, Shervin, “Compensation of Finite GBW Induced Performance Loss on a Fifth-order Continuous-time Sigma-Delta Modulator,” *Proceedings Canadian Conference Electrical & Computer Engineering*, pp. 1093 - 1096, Ottawa, Quebec, Canada, IEEE Canada, May 7-10, 2006.
6. Adibi, Sasan; Erfani, Shervin, “A Multipath Routing Survey for Mobile Ad-Hoc Networks,” *The IEEE CCNC 2006 Proceedings*, pp. 984 - 988, Las Vegas, Nevada, USA, January 2006.

7. Adibi, Sasan; Erfani, Shervin, "Mobile Ad-Hoc Networks with QoS and RSVP Provisioning," *Proceedings of 18th Annual Canadian Conference on Electrical and Computer Engineering (IEEE CCECE 2005)*, pp. 2015 - 2018, Saskatoon, Saskatchewan, Canada, May 2005.
8. H. Rastgar, M.A. Sid-Ahmed, M. Ahmadi " 3D Position Sensing Using Hopfield Neural Network Stereo Matching Algorithm" Proc. of IEEE International Conference on Circuits and Systems, May 21-24 ,2006, Island of Kos,Greece.pp3638-3641
9. S. Huang, M.A. Sid-Ahmed, M.Ahmadi, I. El-Feghi " A Binarization Method for Scanned Documents Based on Hidden Markov Model" Proc. of IEEE International Conference on Circuits and Systems, May 21-24 ,2006, Island of Kos,Greece.pp4309-4312
10. S. Huang, M. Ahmadi, M.A. Sid-Ahmed " An Edge Based Thresholding Method" Proceedings of 2006 IEEE International Conference on Systems, Man, and Cybernetics, October 8-11, Taipei ,Taiwan, pp1603-1606
11. X. Xu, M. Ahmadi, W.C. Miller " A Human Face Recognition System Using Neural Classifiers"International Technical Conference on Circuits,Systems, Computers and Communications, July 10-13 2006, Chiang Mai ,Thailand.ppI-109-112
12. M. Mirhassani, X. Chen, A. Tahmasebi, M.Ahmadi " On Control of HCCI Combustion-Neural Network Approch " To appear in the proceedings of 2006 CCA/CACSD/ISIC (IEEE Int. Conf. on Control Appl., IEEE Int. Symp. On Computer- Aided Control Systems Design and IEEE Int. Symp. On Intelligent Control) October 4-6 ,2006, Munich ,Germany
13. M. Mirhassani, M. Ahmadi, G.A. Jullien " 16-Bit Radix-4 Continuous Valued Digit Adder" to appear in the proceedings of 2006 SPIE conference on Advanced Signal Processing Algorithms,Architectures, and Implementations. August 13-17, 2006, San Diego Convention Center ,San Diego, California
14. M. Mirhassani , M. Ahmadi, G. A. Jullien, " 16- bit Binary Multiplication Using High Radix Analog Digits " To appear in the Proceedings of 40th

Asilomar Conference on Signals, Systems and Computers, Oct.29 – Nov.1, 2006, Pacific Grove, California

15. K. Biswas, H. Wu, M. Ahmadi " Fixed – Width Multi-Level Recursive Multipliers" To appear in the Proceedings of 40th Asilomar Conference on Signals, Systems and Computers, Oct.29 – Nov.1, 2006, Pacific Grove, California
16. A. Hosseinzadeh Namin , H. Wu, M. Ahmadi " A Serial- In Parallel-Out Multiplier Using Redundant Representation for a Class of Finite Fields" To appear in the Proceedings of 40th Asilomar Conference on Signals, Systems and Computers, Oct.29 – Nov.1, 2006, Pacific Grove, California
17. A. Hosseinzadeh Namin , H. Wu, M. Ahmadi " A Parallel-In Serial-Out Multiplier Using Redundant Representation for a Class of Finite Fields" To appear in the Proceedings of 2006 IEEE International Conference on Electronics Circuits and Systems, Dec.10-13 ,2006, Nice, France.
18. Andrew Tam, Sazzadur Chowdhury, "A MEMS Ultra-Stable Short Duration Current Pulse Generator", IEEE Computer Society Annual Symposium on VLSI 2007 (ISVLSI2007), May 9-11, 2007, Porto Alegre, Brazil. (Accepted paper).
19. Matthew Meloche, Sazzadur Chowdhury, "An Integrated Active Vehicle Safety System (IAVSS) to Improve Vehicle Dynamic Safety", XVII Canadian Multidisciplinary Road Safety Conference (CMRSC2007), Montreal, June 3-6, 2007. (Accepted paper).
20. Jose Martinez-Quijada, Sazzadur Chowdhury, "Body-Motion Driven MEMS Generator for Implantable Biomedical Devices", in Proceedings of 20th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE2007), April 22-26, 2007, (Accepted paper).
21. Matthew Meloche, Sazzadur Chowdhury, "A MEMS Non-Planar Constant Beamwidth Ultrasonic Sensor Microarray", in Proceedings of the 4th International IEEE-NEWCAS Conference, Gatineau, Canada, June 18-21, 2006. vol. 1, pp. 273-276, 2006.
22. Andrew Tam, Sazzadur Chowdhury, "A MEMS Sonoluminescent Ultrasonic Sensor", in Proceedings of 2006 IEEE International Conference on Electro/Information Technology, Lansing, Michigan, May 7-10, 2006. vol. 1, pp. 508-511.

23. Harb Abdulhamid, Esam Abdel-Raheem, and Kemal Tepe, Channel Tracking Techniques for OFDM Systems in Wireless Access Vehicular Environment, Proc. of Int. Symp. On Signal processing and its Applications (ISSPA), Sharjah, UAE, Feb. 2007 (no page numbers)
24. E. Abdel-Raheem, Blind Adaptive Equalization with Variable Step Size, Proc. ITI - Int. Conf. on Information & Communication Technologies, Cairo, Egypt, pp. 91-100, Dec. 2006.
25. Harb Abdulhamid, Raymond Lee, and Esam Abdel-Raheem, FPGA Implementations of FIR Nyquist Filters, Proc. ITI - Int. Conf. on Information & Communication Technologies, Cairo, Egypt, pp. 123-133, Dec. 2006.
26. Anderson, Ian; Khalid, Mohammed, Design Space Exploration Using Parameterized Cores: A Case Study, Proceedings of Canadian Conference on Electrical and computer Engineering, 2006.
27. Khalid, Mohammed, A. S.; Salitrennik, Viktor, Scalability Evaluation of a Hybrid Routing Architecture for Multi FPGA systems, Proc. of International Conference on Microelectronics, 2006.
28. Tong, Jason, G; Anderson, Ian, D.L., Khalid, Mohammed, A.S., Soft-core Processors for Embedded Systems, Proc. of International Conference on Microelectronics, 2006.
29. Muscedere, Roberto, A Hardware Efficient Very Large Bit Word Binary to Double Base Number System Converter for Encryption Applications, 4, 2007, In Press, May, IEEE International Symposium on Circuits and Systems.
30. J. Mi and C. Chen, “Power-Oriented Delay Budgeting for Combinational Circuits,” in Proc. of the 2006 IEEE International Symposium on Circuits and Systems (ISCAS’06), Island of Kos, Greece, pp. 3033-3036, May 2006.
31. J. Mi and C. Chen, “Finite State Machine Implementation with Single-Electron Tunneling Technology,” in Proc. of the 2006 IEEE Computer Society Annual Symposium on VLSI (ISVLSI’06), Karlsruhe, Germany, pp. 237-241, March 2006.
32. Yanjie Mao and C. Chen, “Performance Evaluation and Optimization of Full Adders with Single-Electron Technology,” IEEE Canadian Conference on Electrical and Computer Engineering (CCECE’06), Ottawa, Canada, pp. 2105-2108, May 2006.

33. C. Chen and J. Mi, “Parameter Selection for Single-Electron Threshold Logic with Reliability Analysis,” in Proc. of the 2006 6th IEEE International Conference on Nanotechnology (IEEE-Nano’06), Cincinnati, Ohio, USA, vol. 1, pp. 371-374, July 2006.
34. Shun Li, Feng Zhou, C. Chen, Hua Chen, and Yipin Wu, “Quasi-Static Energy Recovery Logic with Single Power-Clock Supply,” accepted by the 2007 IEEE International Symposium on Circuits and Systems (ISCAS’07), New Orleans, USA, May 2007.

(e) Papers Submitted to Refereed Conferences

1. M. Azarmehr and R. Muscedere, "A Simple Central Processing Unit with Multi-Dimensional Logarithmic Number System Extensions", IEEE 18th International Conference on Application-specific Systems, Architectures and Processors . Submitted 2007/03/05.
2. Kevin Banovic, Mohammed A. S. Khalid, and Esam Abdel-Raheem, FPGA Implementation of Fractionally-Spaced Complex Blind Adaptive Equalizer, submitted to IEEE Int. Symp. On Signal processing and Information Tech. (ISSPIT), Cairo, Egypt, 15-18 Dec. 2007.
3. P. Samadi, M. Ahmadi, "Genetic Algorithm and Its Application for the Design of QMF Banks with Canonical Signed Digit Coefficients: A Comparative Study and New Results", submitted to IEEE MWSCAS-NEWCAS 2007, Montreal, QC.
4. M. Mirhassani, M. Ahmadi, Function Evaluation in Continuous Valued Number System with application to Analog Neural Networks, submitted to IEEE 18th International Conference on Application-specific Systems, Architectures and Processors, 2006.
5. A. H. Namin, H. Wu, and M. Ahmadi “A Word Level finite Field Multiplier Using Reordered Normal Basis”, IEEE 18th International Conference on Application-specific Systems, Architectures and Processors, Jul. 2007.

(f) Papers Presented at Special Workshops and Symposia

1. Martinez-Quijada, Jose, Chowdhury, Sazzadur, “A MEMS Micropower Generator for Implantable Medical Devices, CMC Microsystems 2006 Annual Symposium, Ottawa, October 23-24, 2006. (Poster presentation).

2. M. Mirhassani, M. Ahmadi, IEEE Asilomar Conference on Signals, Systems and Computers, Asilomar, 2006
3. M. Mirhassani, M. Ahmadi, Conference on Advanced Signal Processing, Algorithms, Architectures, and Implementations XVI, SPIE Symposium, 2006
4. A. H. Namin, H. Wu, and M. Ahmadi "A Word Level finite Field Multiplier Using Reordered Normal Basis", IEEE 18th International Conference on Application-specific Systems, Architectures and Processors, Jul. 2007.

IV. LIST OF SEMINARS HELD IN 2006

- **A Multi A Multi-Dimensional Logarithmic Number Dimensional Logarithmic Number System based CPU**
  Dec. 01, 2006.
  Presenter: Mahzad Azarmehr

- **High-level language synthesis overview**
  Jun. 30, 2006.
  Presenter: Junsong Liao

- **Fixed-Width Digital Multipliers Based on Multi-Level Recursive Architectures**
  Jun. 16, 2006.
  Presenter: Kevin Biswas

- **Compensation of Finite GBW Induced Performance Loss in a Fourth-order Continuous-Time Sigma-Delta ADC**
  May 08, 2006.
  Presenter: Fang Chen

- **IPSec Implementation and Management Methods**
  May 05, 2006.
  Presenter: James Wiebe

- **Issues Motivating Research in Linear Time-Varying Systems Analysis Area**
  Apr. 28, 2006.
  Presenter: Nima Bayan

- **Architecture and CAD tools for Processor-based Logic Emulation Systems**
  Apr. 7, 2006.
  Presenter: **Amir Ali Yazdanshenas**

- **Design Space Exploration Using Parameterized Cores**
  Mar. 31, 2006.
  Presenter: Ian Anderson

- **Immune Programming**
  Mar. 24, 2006.
  Presenter: Payman Samadi

- **Three Dimensional Interpolation of Video Signals**
  Mar. 10, 2006.
  Presenter: Elham Shahinfard

- **Hybrid Finite Field multiplier using Optimal Normal Basis**
  Feb. 24, 2006.
  Presenter: Ashkan Hosseinzadeh

- **Computer Arithmatic Based on Analog-Digit Number System**
  Feb. 17, 2006.
  Presenter: Mitra Mirhassani

- **A PLL Based Tester Core for System_on_Chip Environment**
  Feb. 10, 2006.
  Presenter: Rashid Rashidzadeh

- **Profiling Techniques for FPGA-Based Hardware-Software CoDesign**
  Feb. 3, 2006.
  Presenter: Jason Tong

- **Fixed-Width Recursive Multipliers**
  Jan. 26, 2006.
  Presenter: Kevin Biswas

V. AWARDS AND HONOURS

1. Dr. M. Ahmadi and Dr. S. Erfani were recipient of "The tribute to Iranian-Canadian Academia" Award by the Persian Circle in a Gala dinner in Westin Prince Hotel in Toronto with the Presence of Mr. Mike Miller Mayor of Toronto on May 11, 2006.
2. The Vancouver based Persian Magazine Goonagoon has carried two feature articles on successful Iranians in Canada for Dr. Shervin Erfani and Dr. Majid Ahmadi in their 9th issue of 2006 and 17th issue of 2007 respectively.
3. Dr. Sazzadur Chowdhury was featured in the University of Windsor Pinnacle Magazine 2006
4. Dr. Sazzadur Chowdhury was featured in the Faculty Recognition article of the University of Windsor Alumni magazine VIEW, November 2006 issue.

VI. GRANTS AND CONTRACTS RECEIVED BY THE RCIM MEMBERS

1. Dr. G.A. Jullien, Dr. M.Ahmadi, Dr. R. Muscedere and 2 others "Integrated Systems for High Performance Signal Processing. NSERC-CRD with industrial support from Gennum" ($97590 per year) Jan. 2007- Jan 2010
2. Dr. M.Ahmadi NSERC Discovery Grant ($52500 per year) 2006-2007
3. Dr. M.Ahmadi, Dr. R. Muscedere, Dr. W. Abdul-Kadir"A Computer Vision-Based Quality Process Controller for Pharmaceutical Products" OCE-MMO with Pharmaphil of Windsor, Ontario Jan 2007- Dec. 2008 ($ 169695)
4. Dr. S. Erfani, NSERC Discovery Grant $18000 (2006-2007)
5. Dr. S. Erfani, U. of Windsor Start Up $50000.00 (2002-2007)
6. Dr. C. Chen, NSERC Discovery Grant - $20,000 (2006 – 2007)
7. Dr. E. Abdel-Raheem, NSERC Discovery Grant $12000 (2006-2007),
8. Dr. M. Khalid, NSERC Discovery Grant $20,000 (2006 – 2007)
9. Dr. Sazzadur Chowdhury, NSERC Discovery Grant $ 38,500 (2006-2007)
10. Dr. R. Muscedere, NSERC Discovery Grant $18,000 (2006-2007)
11. Dr. Huapeng Wu, NSERC Discovery Grant $20,000(2006-2007)

12. Dr. M.Ahmadi , University of Windsor support for RCIM $65000 (2006-2007)

Total Grants received by RCIM members for 2006-2007 totals $581,285.

VII. Graduate COURSES TAUGHT BY RCIM MEMBERS DURING 2006

1.	Dr. S. Erfani	06-88-557: Network Security
2.	Dr. S. Erfani	06-88-523: System Theory
3.	Dr. M. Ahmadi	06-88-521 Digital Signal Processing
4.	Dr. M. Ahmadi	06-88-590 Motion Estimation
5.	Dr. E. Abdel-Raheem	06-88-562: VLSI Implementation of DSP Systems
6.	Dr. M. Khalid	06-88-560: Reconfigurable Computing
7.	Dr. M. Khalid	06-88-590: Physical Design Automation for VLSI and FPGAs
8.	Dr. R. Muscedere	06-88-531: VLSI Design
9.	Dr. C. Chen	06-88-541: Low Power CMOS Design
10.	Dr. H. Wu	0688-555 Computer Arithmetic
11.	Dr. H. Wu	0688-529 Discrete Transforms & Number Theoretical
12.	Dr. S. Chowdhury	88-552: Advanced Topics in MEMS

VIII. COLLABORATIVE RESEARCH WITH THE PRIVATE SECTOR

Gennum Corporation , 970 Fraser Drive, Burlington, Ontario L7L 5P5

***Principal Investigator*:** Dr. M. Ahmadi

Project: Integrated Systems for High Performance Signal Processing. NSERC-CRD with industrial support from Gennum

Pharmaphil , 3190 Devon Rd , Windsor, Ontario N8X 4L2

Principal Investigator: Dr. M. Ahmadi

Project: A Computer Vision-Based Quality Process Controller for Pharmaceutical Products OCE project with support from MMO, NSERC and Pharmaphil of Windsor, Ontario

Canadian Bank Note Company, 145 Richmond Rd Ottawa, ON , K1Z 1A1

Principal Investigator: Dr. M. Ahmadi

Project: FD- Document Authentication. Contract Research

IntellliSense Software Inc. 600 West Cummings Park, Suite 2000, Woburn, MA,

Project: Collaborative research partnership. Worth $210030 CAD per annum

Principal Investigator: Dr. S. Chowdhury

Canadian Microsystems Corporation, 210A Carruthers Hall, Kingston, Ontario, Canada K7L 3N6

Principal Investigators: M.Ahmadi, C. Chen, W.C. Miller, .S.Chowdhury, . R. Muscedere

Project: System-on-Chip (SoC) Design Methodology, Authoring IP Cores

IX. ACKNOWLEDGEMENT

On behalf of the RCIM faculty and student members I would like to express our sincere thanks for the continued support we have been receiving from Dr. Ross Paul, the President, Professor Neil Gold the Provost and Vice President Academic and Dr. Graham Reader the Dean of Engineering, at the University of Windsor. The support and encouragement received from Dr. Sid-Ahmed the Head of Electrical and Computer Engineering department is very much appreciated. Finally we are thankful to CMC for providing us with a multi-million dollar the state-of-the-art facilities allowing us to conduct research in the area of Integrated Microsystems and subsidizing our chip fabrication costs.

Majid Ahmadi, Ph.D., C.Eng., FIET, FIEEE

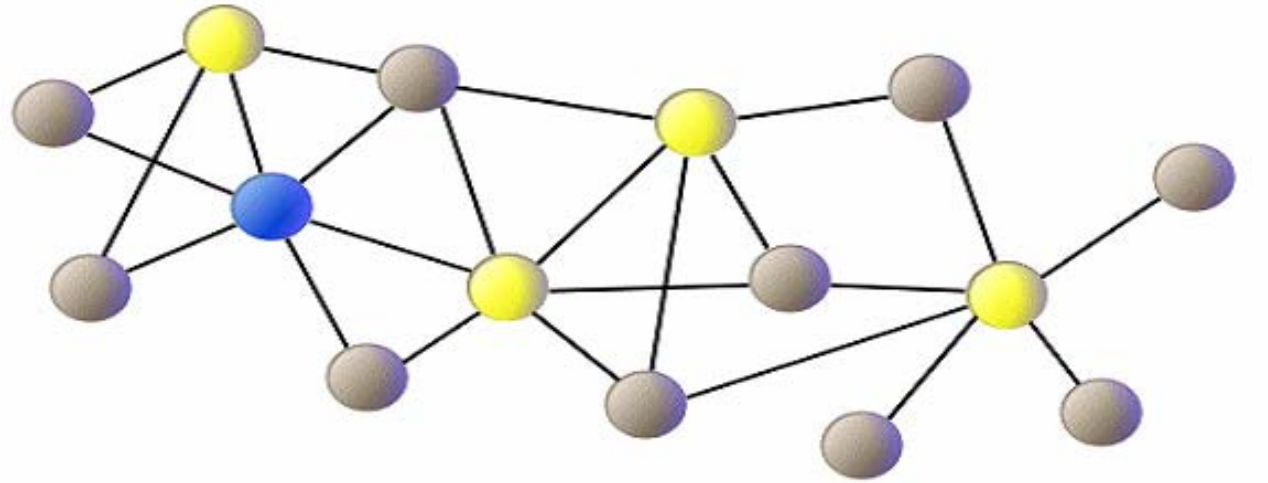
University Professor, Director

Research Center for Integrated Microsystems

April 18, 2007

FPGA implementation of a Wireless Sensor Network

Junsong Liao, M.A.Sc. Student
Supervisor: Dr. Mohammed A. S. Khalid



Meshed Network Topology

Zigbee is a new specification for sensor networks. The network nodes that are compliant with Zigbee require low-power operation. Therefore, it would be useful to implement high-level protocol in hardware. The goal of this research is to implement Zigbee protocol in FPGA, explore potential benefits of implementing high-level protocol in hardware, and build a flexible sensor-networking platform.

A Passport Authentication System

Songtao Huang, Ph.D. Student
Supervisor: Dr. Ahmadi

Sample of passport

The objective of this research work is to develop an advanced image processing method to authenticate passports. It includes: verifying passport numbers, names, photos, signatures on the passport, issue and expiration dates, matching the MRZ to the VIZ, and verifying the issuer country.

An Embedded Tester Core for Mixed-Signal System-on-Chip (SoC) Circuits

Rashid Rashidzadeh, Ph.D. Student
Supervisor: Dr. William C. Miller

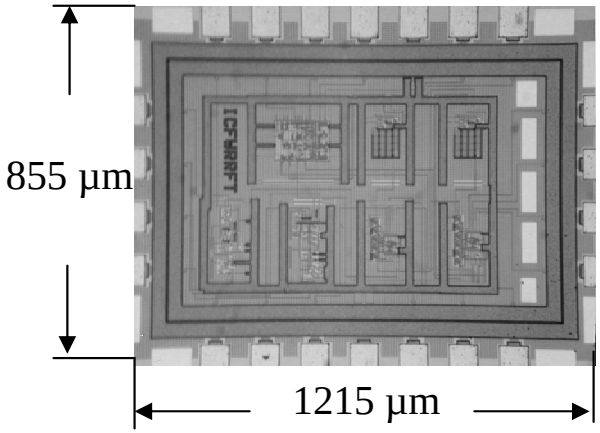


Photo of the Proposed Embedded Tester Core Implemented in CMOS 0.18 µmTechnology

The proliferation of mixed-signal SoC devices has lead to significant cost, size and power reduction in electronic systems. However, testing such complex devices presents a new set of formidable challenges. A new test method using an embedded tester has been proposed to eliminates the I/O bandwidth limitations and also negate the need for a high frequency interface with an external device. A prototype of the embedded tester with a chip area of 1 mm^2 has been fabricated in CMOS 0.18 µm process. The measurement results show that the proposed test methodology can successfully be employed to measure performance metrics of fast analog/RF circuits via a low speed external controller.

Interframe and intraframe interpolation of video signals for compatibility with HDTV standard

Elham Shahinfard, M.A.Sc. Student
Supervisor: Dr. M. Ahmadi and Dr. M. Sid-Ahmed

Original Video Sequence

Reconstructed Video Sequence

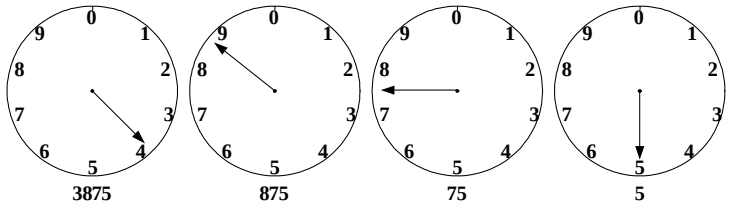
HDTV video format is different than conventional NTSC format in several aspects, including aspect ration, transmission format (progressive format instead of interlace format), frame rate. In this project we are investigating efficient methods for conversion between these formats which could be useful in converting old movies to new standards or converting interlaced cameras signal to progressive format.

High-Density Fault-Tolerant Memory System Based on Continuous Values Number System

Mitra Mirhassani, Ph.D. Candidate
Supervisors: Dr. M. Ahmadi and Dr. G. A. Jullien

It has been estimated that more than 10^{32} CMOS transistors are fabricated each year worldwide and 50% of these transistors are utilized in some type of memory structure. More than half of the transistors in today's high-performance microprocessor ICs are devoted to cache memories. Therefore, high performance and dense memory circuits are of primary concern to today's semiconductor design engineers and researchers. In response to today's research needs, ***University of Windsor's Research Centre for Integrated Microsystems (RCIM)*** developed a novel number system called *Continuous Values Number System (CVNS)* which has interesting features and its main idea is from utility meter reading.

CVNS is analog in nature, which results in compact, low-noise and low-power systems. Moreover, it is fault-tolerant and is able to detect and correct multiple errors. The fault tolerant nature of this number system, makes it a perfect candidate for developing dense, multiple-valued memory systems, where traditionally a lot of area is devoted to the error checking bits.

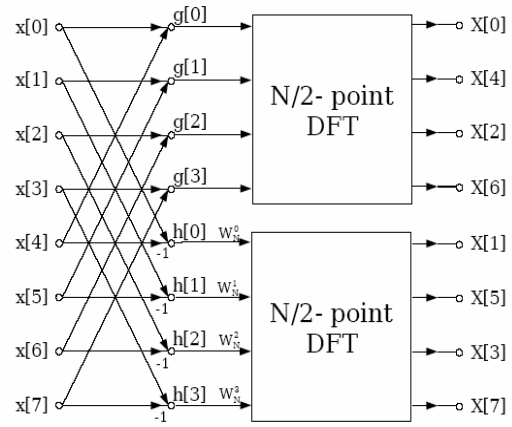


CVNS Example: 3875

Efficient VLSI Architectures and Implementation for DSP Using Residue Number Representations

Ashkan Namin, Ph.D Candidate
Supervisor(s): Majid Ahmadi and Huapeng Wu

Applications of residue number systems (RNS) to DSP have been paid much attention recently due to its characteristic parallel structures for arithmetic operations such as addition and multiplication. Our proposed research work has several aspects. Firstly, most research work on the RNS chooses the base elements as Fermat or Mesenne numbers. We propose a study on efficient algorithms and VLSI architectures for RNS computation for a more general class of numbers as the base elements.

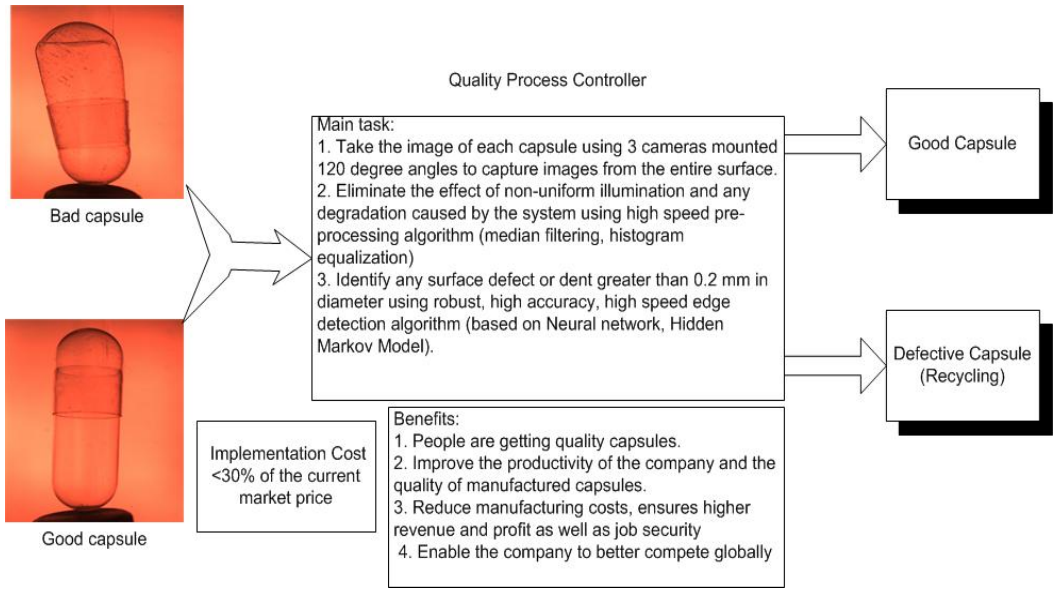


Simplified DFT Computation

Secondly, it is known that computation of DFT can be greatly simplified when DFT is defined in a properly chosen finite field where the order of 2 is a factor of the block size n. Thirdly, low-power considerations for DSP-related hardware have been one of major concerns for wireless applications. Efficient algorithms and architectures for the above two aspects (RNS and DFT) with low-power features are also under our intense study

Image Processing Techniques for Quality Process Control and Inspection

Mohammed Jahirul Islam , Ph.D. Student
Supervisor: Dr. M. Ahmadi



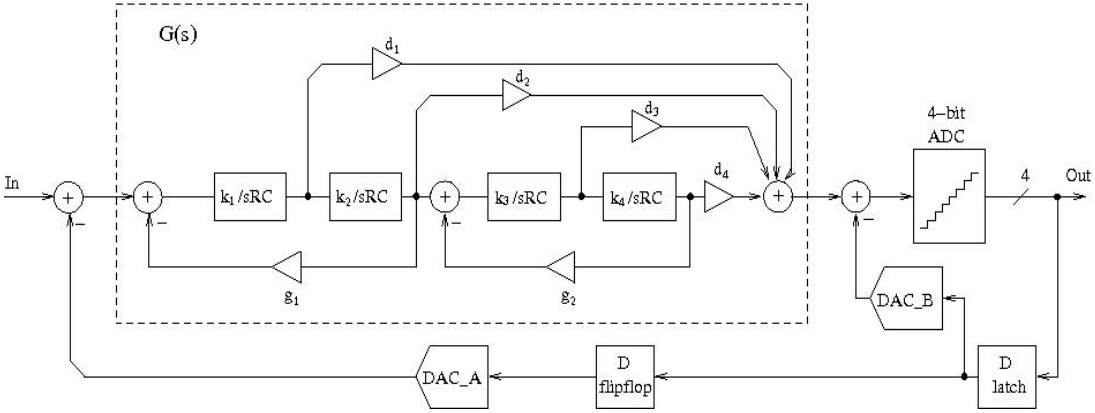
Proposed Solution for Quality Process Control of Pharmaceutical Products

The aim of this research work is to develop image processing techniques for implementation on a low-cost, robust, high accuracy and high speed computer vision system for use in a manufacturing setting for quality process control of pharmaceutical products. Currently human inspectors evaluate the quality of the capsules manufactured in most pharmaceutical companies.

Design of an Enhanced Wideband Continuous-Time Sigma-Delta Analog-to-Digital Converter on 90nm CMOS

Fang Chen, Ph.D. Student
Supervisor: Dr. S. Erfani

For four decades the evolution of integrated circuits has followed Moore's law. At the same time, this scaling towards deep sub-micron CMOS technologies provides faster transistors. Therefore, the processing power of digital circuits increases every generation. For analog circuits, this evolution of technology scaling is not as beneficial.

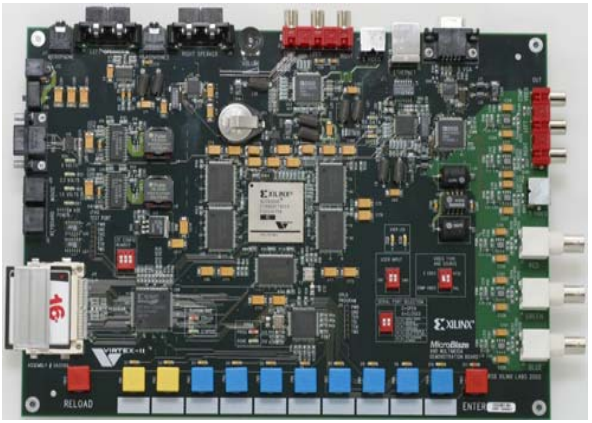


System Diagram of the Proposed Wideband ADC

This research is focused on the design of an enhanced wideband continuous-time sigma-delta analog-to-digital converter on deep sub-micron 90nm CMOS technology which can be used in communication, high-end test instruments and medical imaging applications.

Architecture and CAD for Processor Based Logic Emulation Systems

Amir Yazdanshenas, M.A.Sc. Student
Supervisor: Dr. Mohammed A. S. Khalid



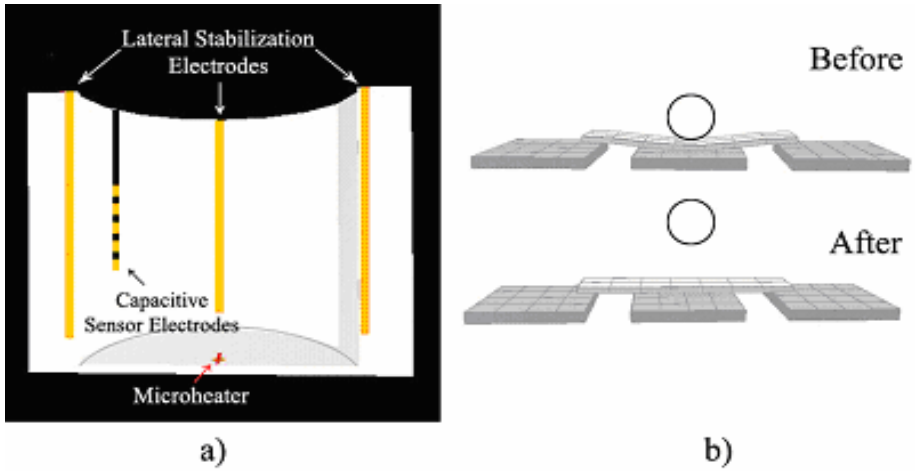
Xilinx Virtex-II Platform FPGA Used to Implement the Proposed Emulation System

The objectives of this research are to explore efficient architectures and CAD tools for processor-based logic emulation systems. A research infrastructure is being developed that allows for exploration of architectures and associated mapping CAD tools. So far, a design flow has been implemented that enables mapping of MCNC benchmark circuits to models processor-based logic emulation architectures. Different scheduling algorithms have been implemented and compared.

A MEMS Sonoluminescent Ultrasonic Sensor

Andrew Tam, M.A.Sc. Student
Supervisor: Dr. Sazzadur Chowdhury

A recently discovered physical phenomenon known as the Single Bubble Sonoluminescence (SBSL) offers the possibility of realizing a new type of MEMS based ultrasonic sensor that can overcome the limitations of capacitive type ultrasonic sensors. SBSL generates highly stable and precise short duration light pulses when a bubble suspended in a liquid collapses due to an applied ultrasonic pressure field. Contrary to conventional transducers, where no energy amplification occurs during the transduction process itself, a higher sensitivity ultrasonic sensor can be realized if these emitted light pulses can be detected with a suitable photodetector.



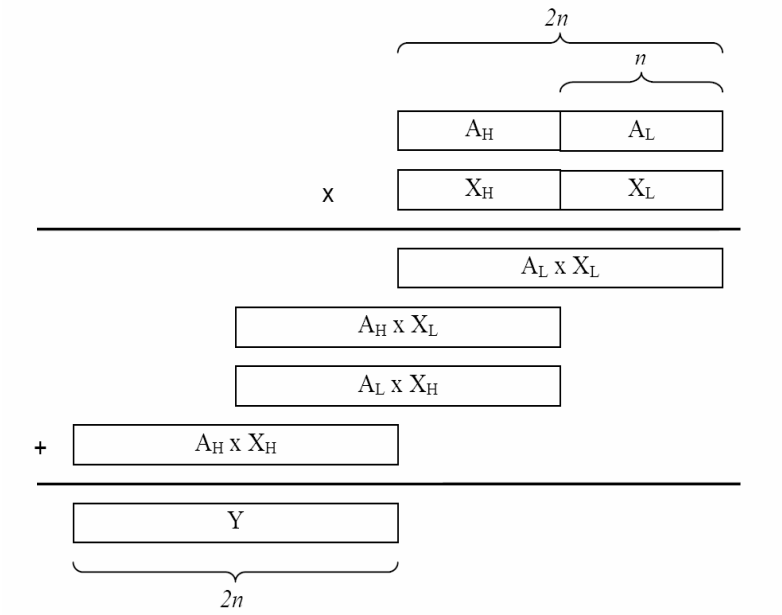
(a) A vertical cross-section of the MEMS micro-chamber. (b) The microbubble is released by an electrical pull-and-release mechanism employing a short duration electrical pulse.

Without any vibrating diaphragm as used in capacitive sensing, the sensor will be able to withstand very high acoustical pressure (larger dynamic range) compared to conventional MEMS-based ultrasonic sensors and will be free of any pull-in effects.

Fixed-width Digital Multipliers and their VLSI Implementation

Kevin Biswas, M.A.Sc. Candidate
Supervisors: Dr. Majid Ahmadi and Dr. Huapeng Wu

Almost all computational tasks can be broken down into arithmetic operations such as shift/extension, addition/subtraction, multiplication and others. The multiplier is the most important arithmetic hardware component in many applications, esp. DSP, because multiplication is the most critical operation. A novel fixed-width multiplier has been developed based on the recursive multiplier architecture. The recursive multiplier works on principles of "divide and conquer" multiplication, where the product of two long integers is computed by executing multiplications and additions on their divided parts.



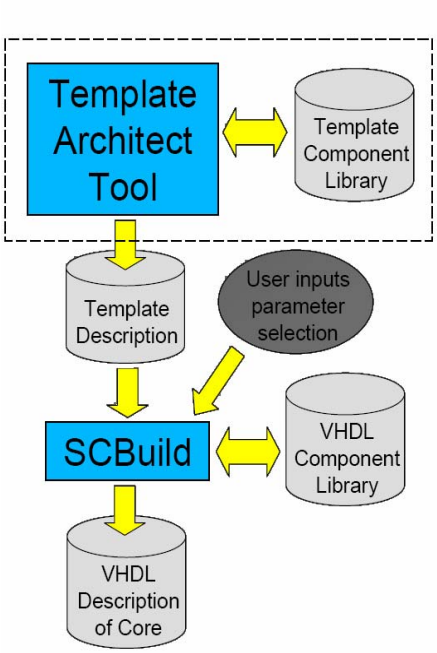
Proposed Fixed-width *2n*-bit Recursive Multiplier

The resultant fixed-width multipliers have minimal error and offer hardware complexity savings of up to 25%. Performance of these multipliers have compared favorably to those found in literature.

A CAD Tool for Synthesizing Variants of Altera NIOS II Soft Core Processor

Omar Al Rayahi, M.A.Sc. Student
Supervisor: Dr. Mohammed A. S. Khalid

As the complexity of embedded system designs has increased, it is becoming impossible to design each system from scratch within reasonable cost and time. The objectives of this research are to explore design and evaluation of embedded CPU cores targeted for FPGAs. In the first phase of the research a library of **soft processor building** blocks will be created. In the second phase, a processor builder CAD tool will be developed that can be used to generate variants of a CPU core from high level parameter specifications. In the third and final phase, different CPU variants will be tested using real world application benchmarks.



Soft Core (SC) Build System Environment

A Multi-Dimensional Logarithmic Number System (MDLNS) based Central Processing Unit

Mahzad Azarmehr, Master Student
Supervisor: Dr. Roberto Muscedere

The major challenges in Digital Signal Processing field are the design complexity to achieve high-speed performance, area efficiency, low power dissipation and reliability. DSP systems manipulate signals as a sequence of numbers and require massive arithmetic computations to perform algorithmic processing. Many DSP algorithms, such as digital demodulation, filtering and equalization make use of multiplier accumulators. The implementation of a MAC in either HW or SW needs intensive computation and consumes much resources..

MDLNS as an alternative number system has been developed in order to reduce hardware complexity particularly in multiplication as well as providing a larger dynamic range. A 2DLNS based CPU is developed which will be able to perform conversion between MDLNS and Binary representations, arithmetic and logic computations as well as dedicated MAC operations. As an application we will design and implement a filterbank architecture as a microcode running on this CPU. Since the size and contents of lookup tables are dependent on optimal second base, the settings program of this CPU should be dynamic which will allow runtime loading of the parameters.

Processor Based Emulation Using FPGAs

Marwan Kanaan, M.A.Sc. Student
Supervisor: Dr. Mohammed A. S. Khalid

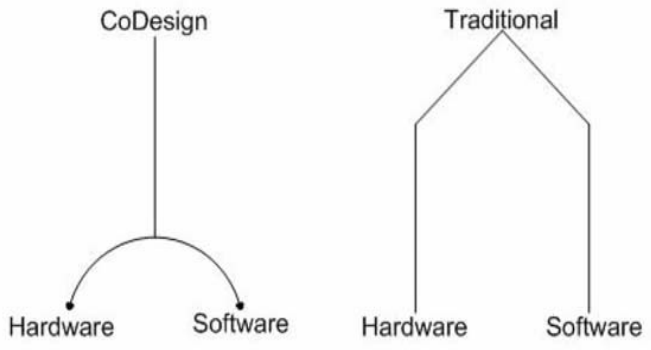
In the past three decades design verification has become a crucial part of the design cycle. With the increase in chip size and the need to reduce time-to-market, more efficient design verification tools became required. Logic Emulation is a design verification tool where a reprogrammable system, known as the emulator, imitates the functional behavior of a logic design. The system would be able to act exactly as the desired chip and thus giving the user the ability to check the logic design in real time circuit conditions before manufacturing.

One type of Logic Emulation is Processor Based Emulation where multiple processors are packaged together in an emulation engine capable of emulating a logic design of significant size and complexity. While PBE systems are considered to be an efficient verification tool, they are implemented on custom made chips and therefore are very expensive. The aim of this research is to explore the implementation of the PBE system on a FPGA. By doing so we would be combining the advantages of the processor based emulator with the cheap cost of FPGA implementation.

Profiling Tools for FPGA-Based Embedded System Design

Jason Tong, M.A.Sc. Student
Supervisor: Dr. Mohammed A. S. Khalid

Profiling tools are CAD tools that measure the performance of a software system. Embedded systems consist of hardware and software components that execute concurrently and efficiently to execute a specific task or application. In order to determine such a heterogeneous hardware-software configuration, profiling tools are indispensable. They measure the performance of a system and provide information that helps designers decide whether to implement a given function in hardware or software domain.



CoDesign and Traditional Methods

The objectives of this research are to explore different profiling techniques and to develop an efficient profiling tool targeting the Altera Stratix FPGA. The tool can be used by designers of FPGA-based embedded systems to codesign complex systems and obtain an effective hardware-software partition.