Complexity reduction for HW implementation of H.264/AVC

Jianjun Li

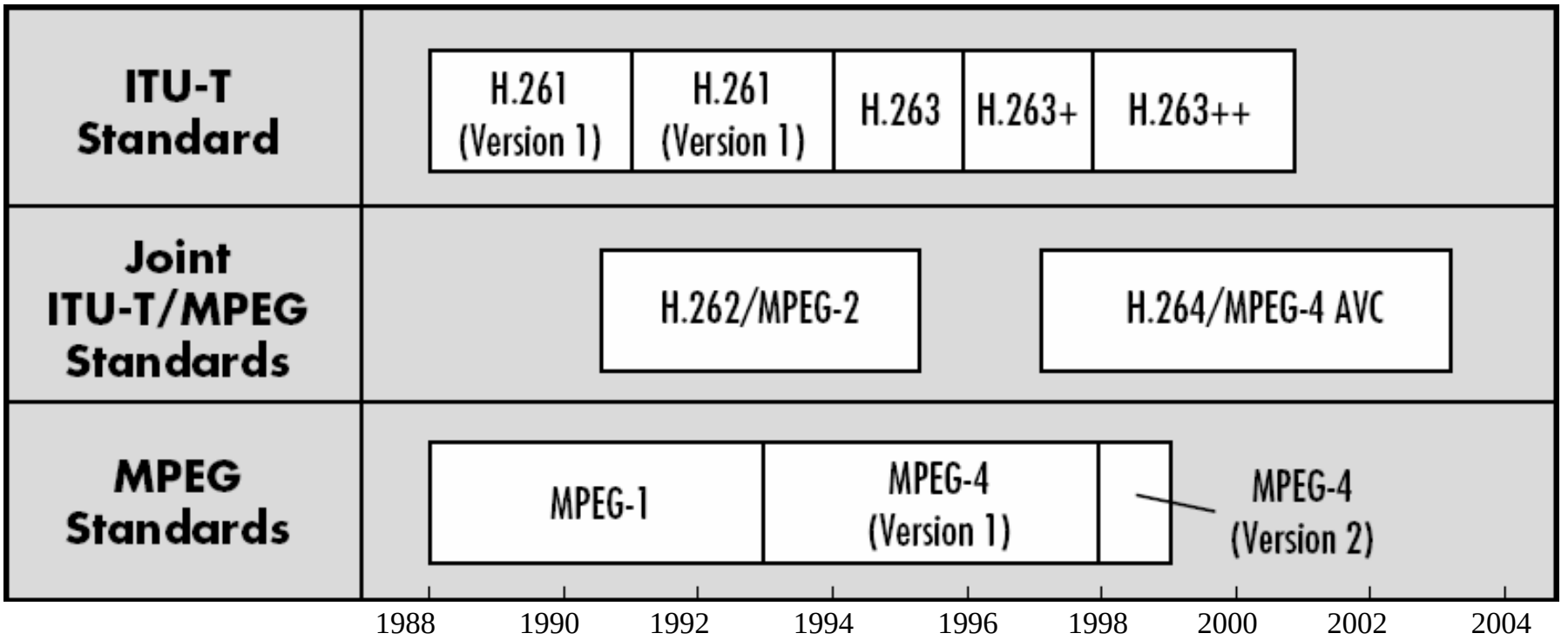
Research **C**entre for **I**ntegrated **M**icrosystems
Electrical and **C**omputer **E**ngineering
University of **W**indsor

Supervisor: Dr. M.Ahmadi
Feb 23, 2007

Outline

- H.264/AVC codec overview
  - H.264/AVC development roadmap
  - H.264/AVC features
  - Applications
- H.264 Intra-frame prediction
  - Intra prediction features
  - Intra prediction method
- Intra prediction complexity reduction algorithms
  - Instruction level complexity analysis
  - Mode decision criteria
  - Complexity reduction algorithms searching
- Research considerations
  - Design methodology
  - Test & verification
  - Design challenges
- Conclusions

H.264/AVC roadmap



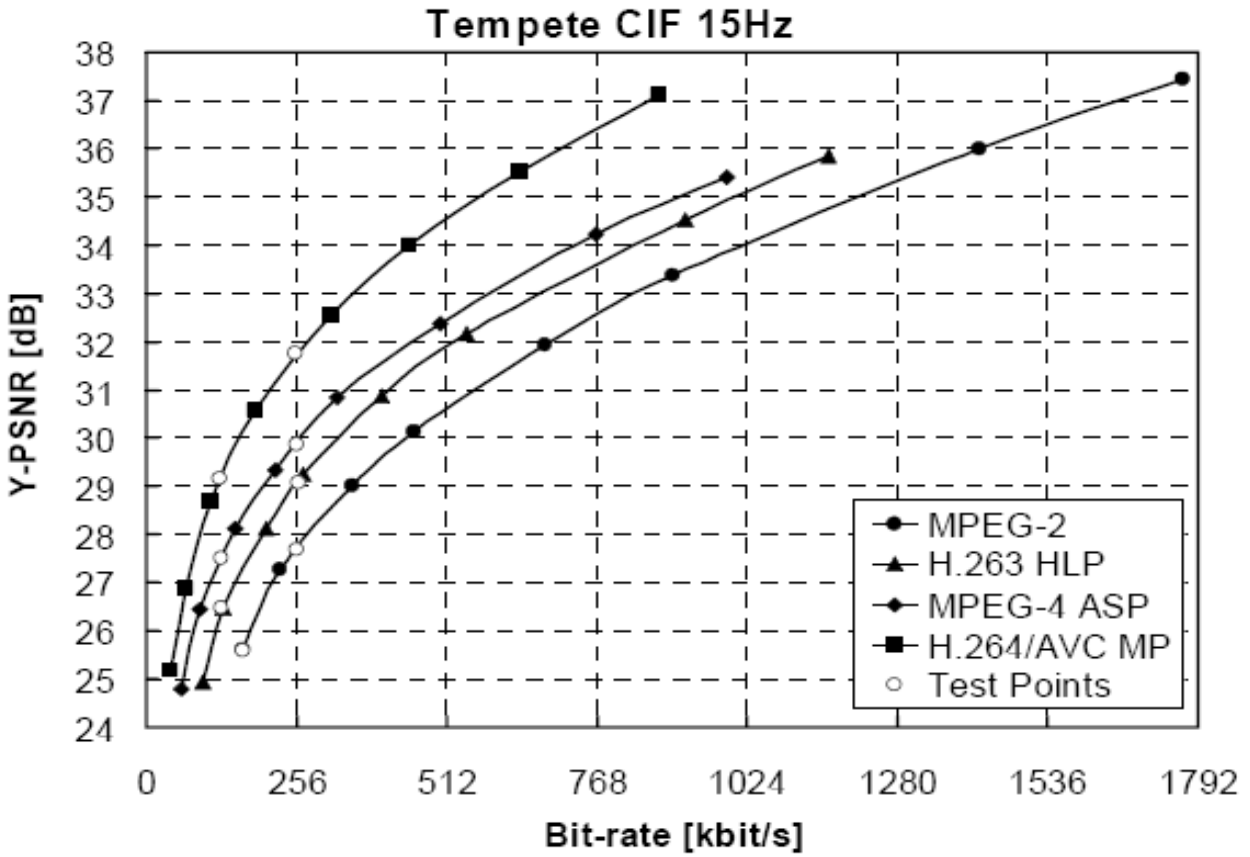
H.264/AVC features

- Hybrid video compression standard
  - Temporal correlation: inter prediction to reduce redundancy between frames.
  - Spatial correlation: Intra prediction to reduce spatial redundancy between adjacent blocks.
  - Frequency correlation: integer DCT transform to reduce frequency redundancy.

- H.264/AVC defines three different profiles:
  - Baseline : provides the least compression efficiency and complexity, better for real-time communication.
  - Extended : superset of Baseline, better for video streaming.
  - Main : provides the highest compression efficiency and highest complexity, better for huge storage.

- New techniques (tools) used in H.264/AVC.
  - Multiple reference frames;
  - Variable block size;
  - ¼ and 1/8 pixel accuracy motion estimation;
  - Multiple Intra prediction modes;
  - De-blocking to reduce artifact;
  - Variable length coding (CAVLC) and arithmetic coding (CABAC);

H.264/AVC higher compression



[T. Wiegand and G. J. Sullivan: The H.264/MPEG-4 AVC Video Coding Standard]

Bit-rate savings

	Average bit-rate savings relative to:		
Coder	MPEG-4 ASP	H.263 HLP	MPEG-2
H.264/AVC MP	37.44%	47.58%	63.57%
MPEG-4 ASP	-	16.65%	42.95%
H.263 HLP	-	-	30.61%

[T. Wiegand and G. J. Sullivan: The H.264/MPEG-4 AVC Video Coding Standard]

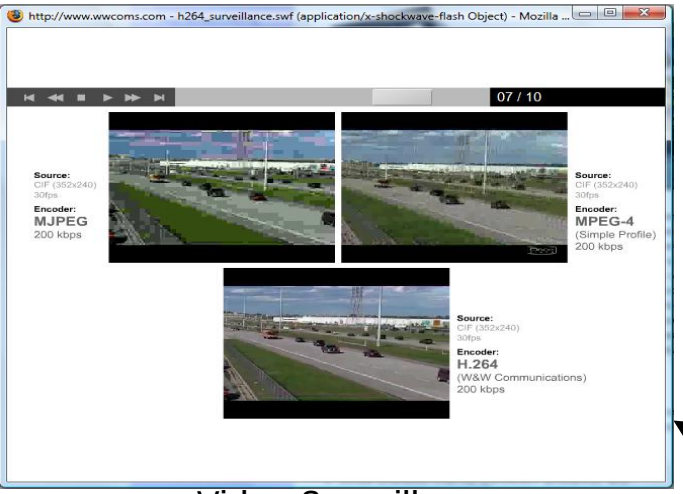
Comparison visually

MPEG-4
D1 30Hz 1Mbps

H.264
D1 30Hz 1Mbps

[DSP/IC Lab, ECE of National Tanwai University]

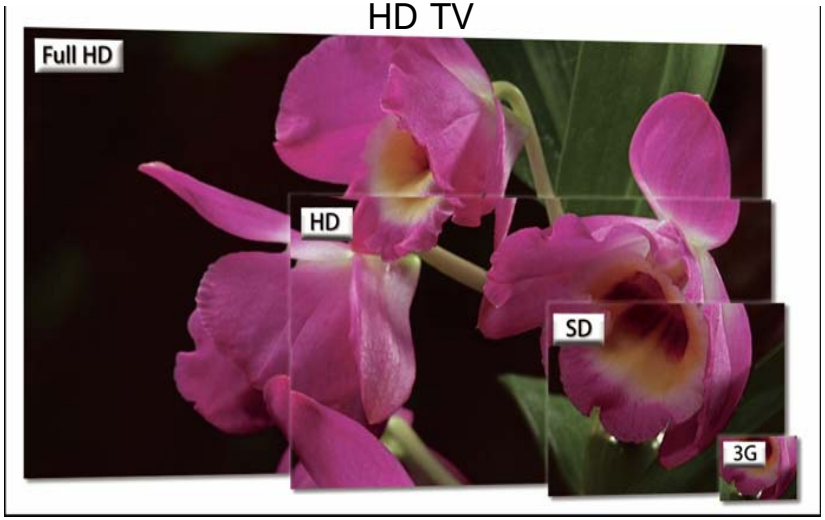
H.264/AVC applications



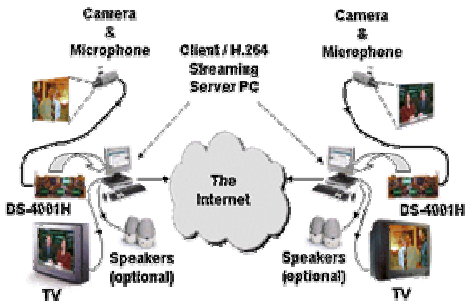
Video Surveillance
(W&W communications)

Apple ipod

HD TV



H.264/AVC



Video conference over IP

HD DVD player

Toshiba
announced
at Jan 9, 2007

3-layer 51GB HD-DVD Disc with H.264

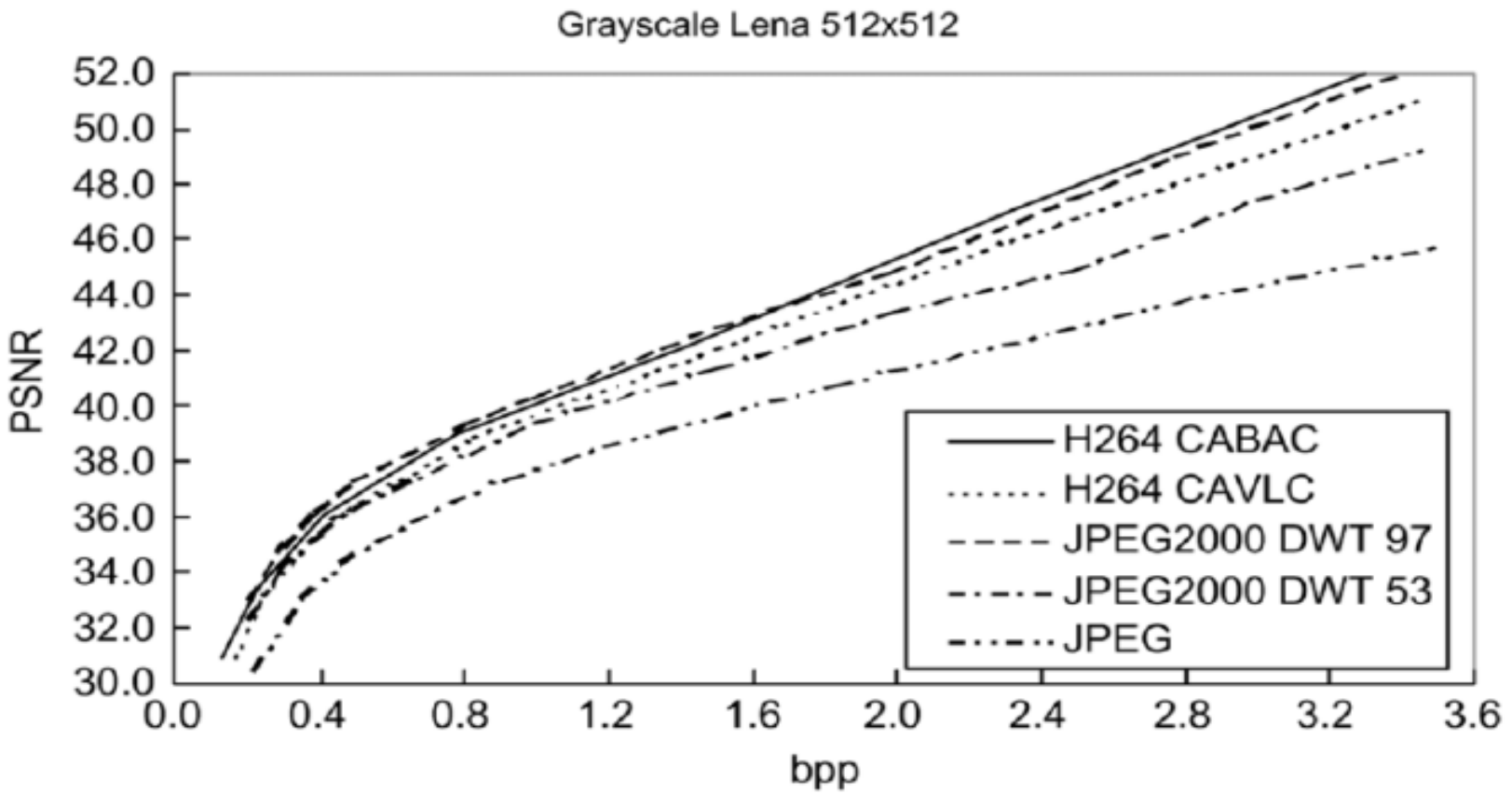
Outline

- H.264/AVC codec overview
  - H.264/AVC development roadmap
  - H.264/AVC features
  - Applications
- ☞ H.264 Intra-frame prediction
  - Intra prediction features
  - Intra prediction method
- Intra prediction complexity reduction algorithms
  - Instruction level complexity analysis
  - Mode decision criteria
  - Complexity reduction algorithms searching
- Research considerations
  - Design methodology
  - Test & verification
  - Design challenges
- Conclusions

H.264/AVC Intra prediction advantage

- A new feature of H.264/AVC.
- Utilize spatial correlation.
- Its performance can beat with still image compression standard JPEG2000.

Compression efficiency



[DSP/IC lab, ECE, National TaiWan University]

Comparison visually

JPEG (Left)

JPEG2000(Middle)

H.264, I frame (Right)

[DSP/IC lab, ECE, National TaiWan University]

Complexity comparison

COMPARISON OF COMPUTATIONAL COMPLEXITY

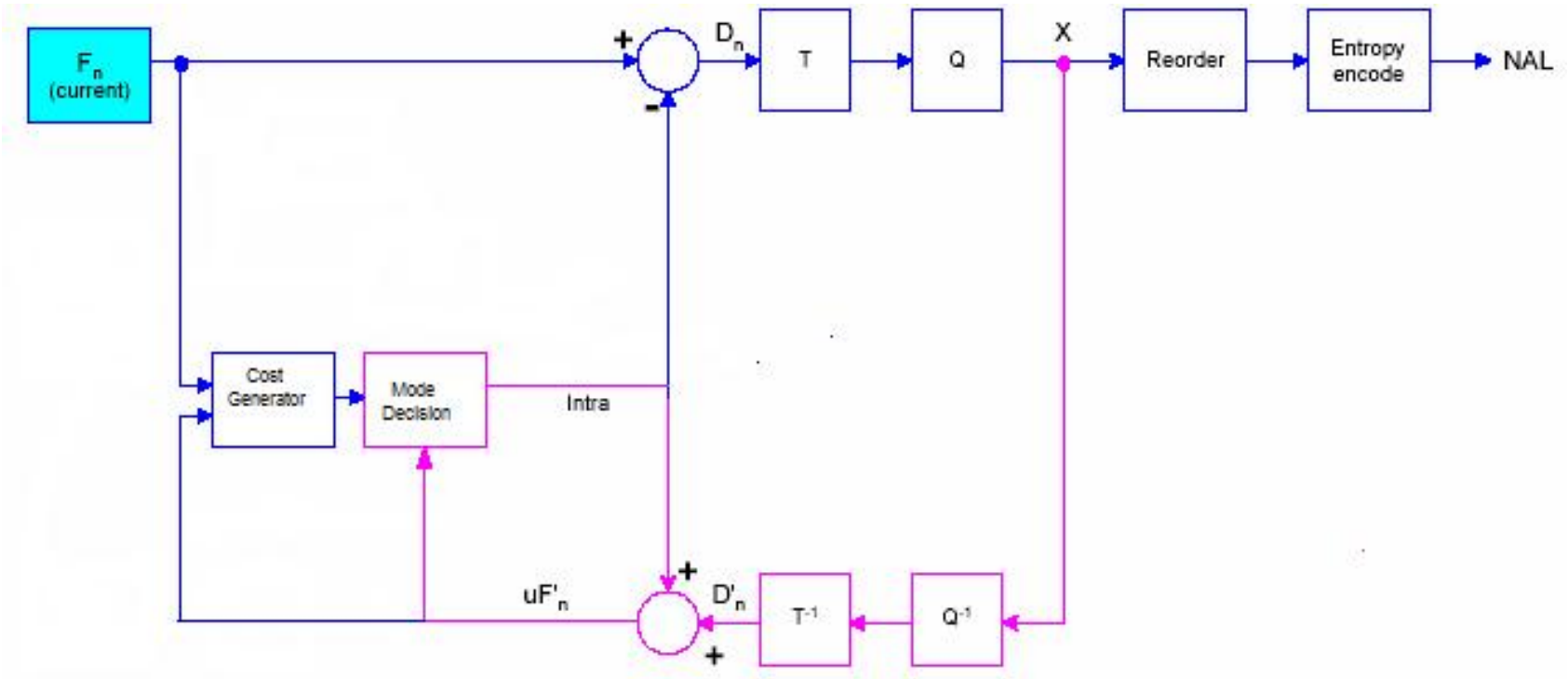
Standard	Encode	Decode
JPEG	544	298
JPEG2000	3430	3180
H.264/AVC	3648	584

Units in million instructions

Test image: Bike, 2048×2560×8b

[DSP/IC lab, ECE, National TaiWan University]

Intra prediction diagram



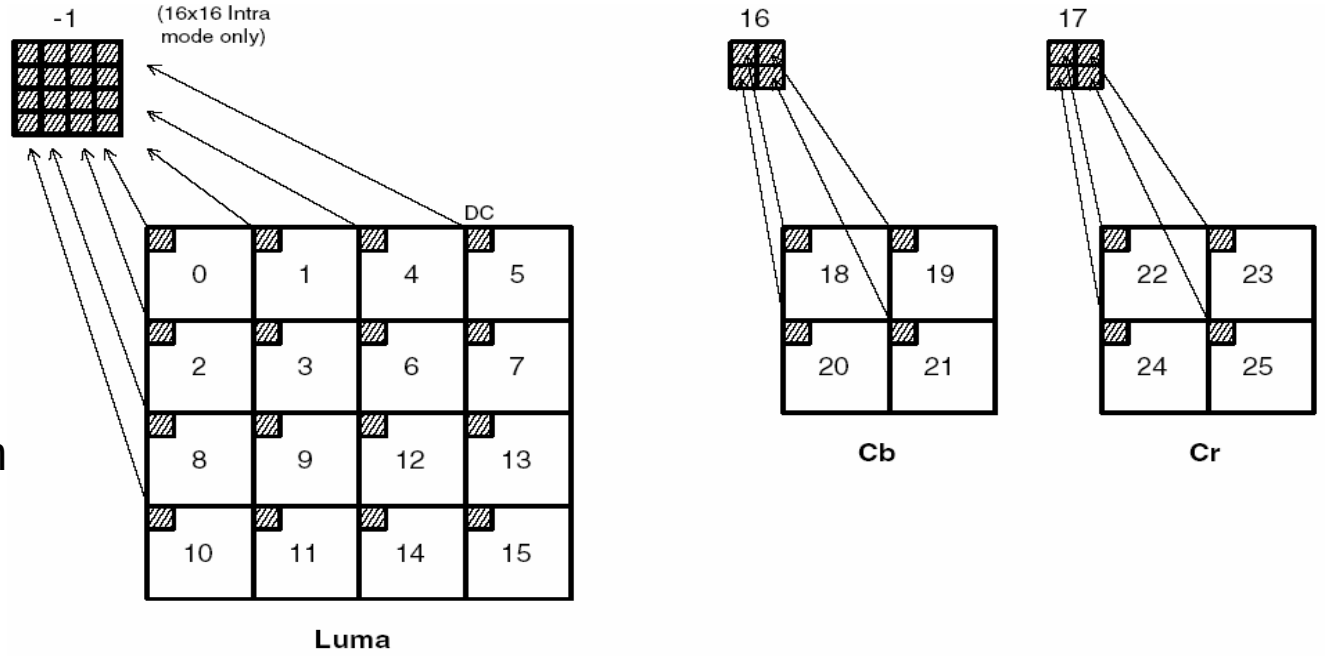
[T. Wiegand "Overview of the H.264/AVC Video Coding Standard,"]

H.264/AVC Transforms

- Transform and Quantization
  - 4×4 integer transform

Hadamard transform

DCT-based integer transform



[T. Wiegand "Overview of the H.264/AVC Video Coding Standard,"]

H.264/AVC transforms (Cont's)

- DCT

  a = 1/2

  b = $\sqrt{\frac{1}{2}}\cos(\frac{\pi}{8})$

  c = $\sqrt{\frac{1}{2}}\cos(\frac{3\pi}{8})$

$$\begin{pmatrix} a & a & a & a \\ b & c & -c & -b \\ a & -a & -a & a \\ c & -b & b & -c \end{pmatrix} \begin{pmatrix} r_{00} & r_{01} & r_{02} & r_{03} \\ r_{10} & r_{11} & r_{12} & r_{13} \\ r_{20} & r_{21} & r_{22} & r_{23} \\ r_{30} & r_{31} & r_{32} & r_{33} \end{pmatrix} \begin{pmatrix} a & b & a & c \\ a & c & -a & -b \\ a & -c & -a & b \\ a & -b & a & -c \end{pmatrix}$$

- Integer DCT

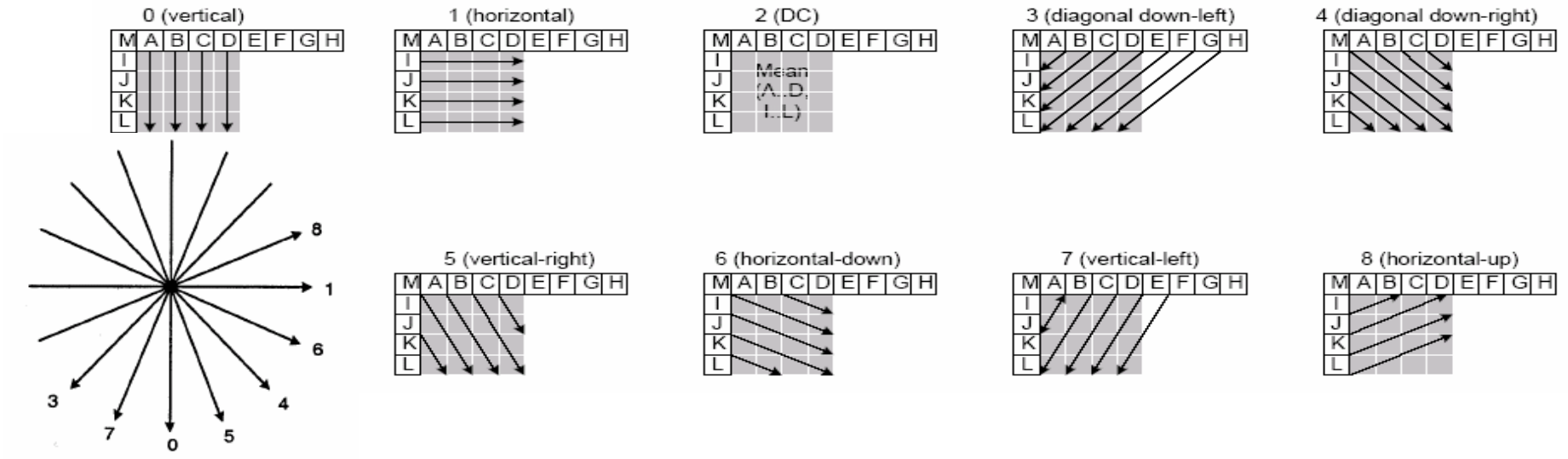
$$\begin{pmatrix} 1 & 1 & 1 & 1 \\ 2 & 1 & -1 & -2 \\ 1 & -1 & -1 & 1 \\ 1 & -2 & 2 & -1 \end{pmatrix} \begin{pmatrix} r_{00} & r_{01} & r_{02} & r_{03} \\ r_{10} & r_{11} & r_{12} & r_{13} \\ r_{20} & r_{21} & r_{22} & r_{23} \\ r_{30} & r_{31} & r_{32} & r_{33} \end{pmatrix} \begin{pmatrix} 1 & 2 & 1 & 1 \\ 1 & 1 & -1 & -2 \\ 1 & -1 & -1 & 2 \\ 1 & -2 & 1 & -1 \end{pmatrix}$$

- Hadamard

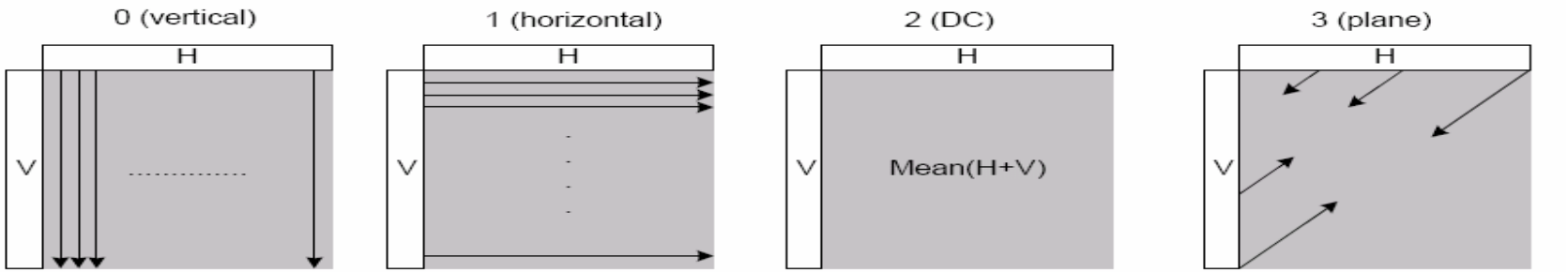
$$\begin{pmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \\ 1 & -1 & 1 & -1 \end{pmatrix} \begin{pmatrix} r_{00} & r_{01} & r_{02} & r_{03} \\ r_{10} & r_{11} & r_{12} & r_{13} \\ r_{20} & r_{21} & r_{22} & r_{23} \\ r_{30} & r_{31} & r_{32} & r_{33} \end{pmatrix} \begin{pmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \\ 1 & -1 & 1 & -1 \end{pmatrix}$$

Intra prediction modes

1. Intra 4x4 prediction modes:



2. Intra 16x16 prediction modes:



[T. Wiegand "Overview of the H.264/AVC Video Coding Standard,"]

Intra prediction complexity

- H.264/AVC reference module recommends Rate-Distortion Optimization (RDO) technique for mode decision procedure. It has higher compression efficiency, but it is computational complexity.
- For each macroblock(16x16 pixels), we have:
  - 16 4x4 blocks, each 4x4 block has 9 Intra 4x4 modes;
  - 4 Intra16x16 modes;
  - 4 Intra 8x8 modes for chroma, which can be different with luma intra prediction modes)
- we have to make cost computation and comparison:

  (16*9+4)*4 = 596 times/MB
- So, even though we only make Intra prediction, it is still complex and not feasible for real-time implementation.

Outline

- H.264/AVC codec overview
  - H.264/AVC development roadmap
  - H.264/AVC features
  - Applications
- H.264 Intra-frame prediction
  - Intra prediction features
  - Intra prediction method
- ☞ Intra prediction complexity reduction algorithms
  - Instruction level complexity analysis
  - Mode decision criteria
  - Complexity reduction algorithms searching
- Research considerations
  - Design methodology
  - Test & verification
  - Design challenges
- Conclusions

Instruction level complexity analysis

- Codec complexity in CIF format

CIF 352x288 @ 30Hz	**MPEG-4**	**H.264/AVC**	**JPEG2000**
Encoder Side	12,000 MIPS	80,000 MIPS	5,737 MIPS
Decoder Side	200 MIPS	450 MIPS	5,401 MIPS

- Codec complexity in SDTV format

SDTV 720x480 @ 30Hz	**MPEG-4**	**H.264/AVC**	**JPEG2000**
Encoder Side	40,800 MIPS	272,000 MIPS	19,584 MIPS
Decoder Side	680 MIPS	1,500 MIPS	18,438 MIPS

Intra prediction complexity

– Intra prediction complexity in SDTV format

Instruction Type	**MIPS**	**%**	**Category (%)**
Arithmetic	1,785	16.5	Computing (19.85%)
Logic	83	0.77	
Shift	279	2.58	
Jump,Test,and Comp	1,558	14.4	Controlling (14.4%)
Stack instruction	3,154	29.15	Memory accessing (65.75%)
Data Instruction	3,961	36.6	
Total	10,820	100	(100%)

Mode decision criteria

- Rate-Distortion Optimized (RDO) method;

$$J_{SSD} = SSD_{Luma} + SSD_{Cr} + SSD_{Cb} + \lambda * Rate$$

$$SSD = \sum_i |B_i - \mathrm{Re}_i|^2$$

$$\lambda = 0.85 * 2^{(QP-12)/6}$$

- Sum Absolute Transform Difference (SATD) method;

$$J_{SATD} = SATD_{Luma} + SATD_{Cr} + SATD_{Cb} + \lambda * Rate_{est}$$

$$SATD = \sum_i \left| T_H \{ B_i - P_i \} \right|$$

Complexity reduction algorithms searching

- H.264/AVC only specifies decoding semantics, and interpret the syntax elements in the bitstream, therefore it leaves much more flexibility to encoder side. That means we can have more choices in selecting encoding algorithms to meet our design.
  - 4x4 DCT-based mode decision algorithm
  - SDS complexity reduction algorithm
  - Candidate reduced algorithm
  - HHR complexity reduction algorithm

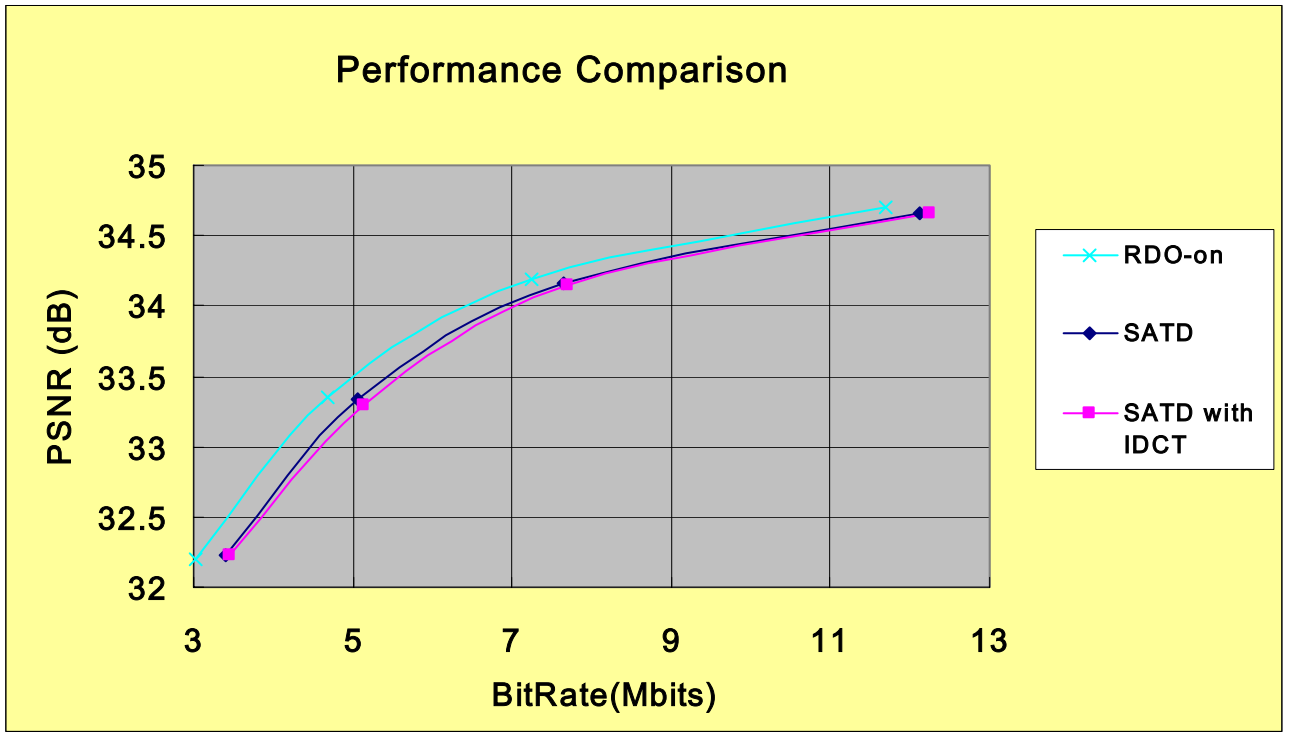
4x4 DCT-based mode decision

- In the H.264/AVC reference software, Hadamard transform is adopted to generate cost for mode decision, which has less computation, but it increases memory access, which is not smart in hardware design.
- We compute Integer DCT instead of Hadamard, the result can be saved in memory so that it can be used directly for the next step.

$$J_{DCT} = SATD_{Luma} + SATD_{Cr} + SATD_{Cb} + \lambda * Rate_{est}$$

$$SATD = \sum_{i} \left| T_{DCT}\{B_i - P_i\} \right|$$

Performance of IDCT-based MD

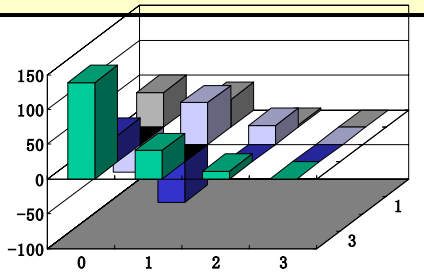


SDS complexity reduction algorithm

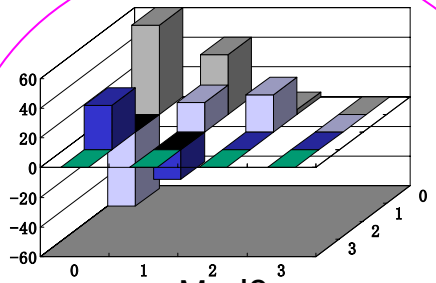
- Assumptions:
  - Non-zero coefficients of 4x4 residual block are less when RDO cost of a mode is low;
  - They are centre at zero;
- Difference & Sum:
  - Diff = |Bmax-Bmin|, when Bmax is the biggest coefficient, and Bmin is the smallest coefficient; It corresponds to “range”;
  - Sum = |Bmax+Bmin|; It corresponds to “symmetry”;
- New criteria:

  SDS=Diff + Sum>>1; we give “Diff” more weight than “Sum”;
- Oberservation:
  - Mode has a minimal SDS value is almost at the same time when it has a minimal SATD value.

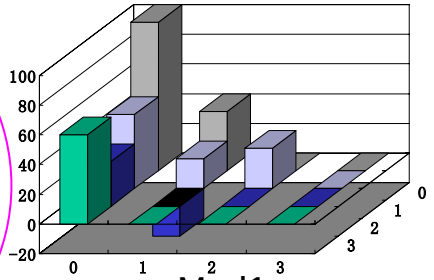
SATD vs. SDS



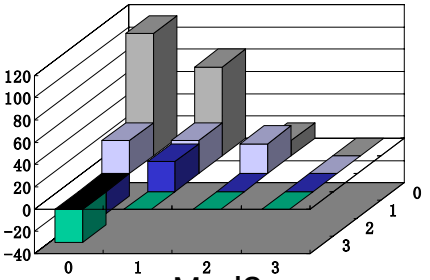
Mod8,
SATD=1206,SDS=307



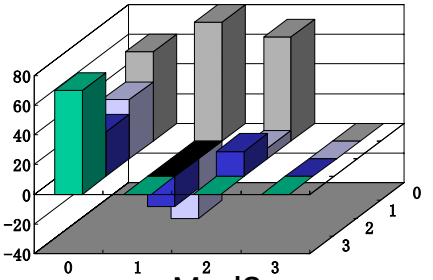
Mod0,
SATD=868,SDS=108;



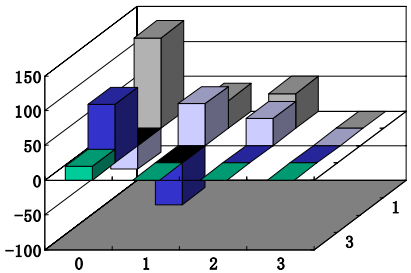
Mod1,
SATD=1178,SDS=287;



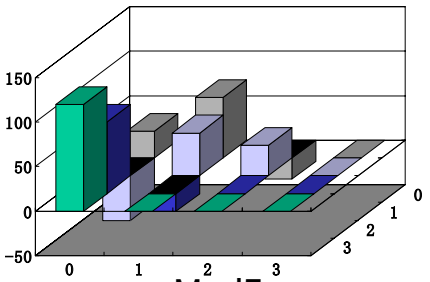
Mod2,
SATD=1102,SDS=268;



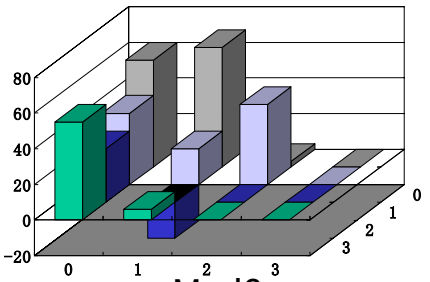
Mod3,
SATD=1436,SDS=314



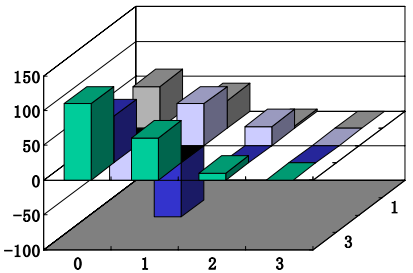
Mod4,
SATD=1268,SDS=329



Mod5,
SATD=1130,SDS=286

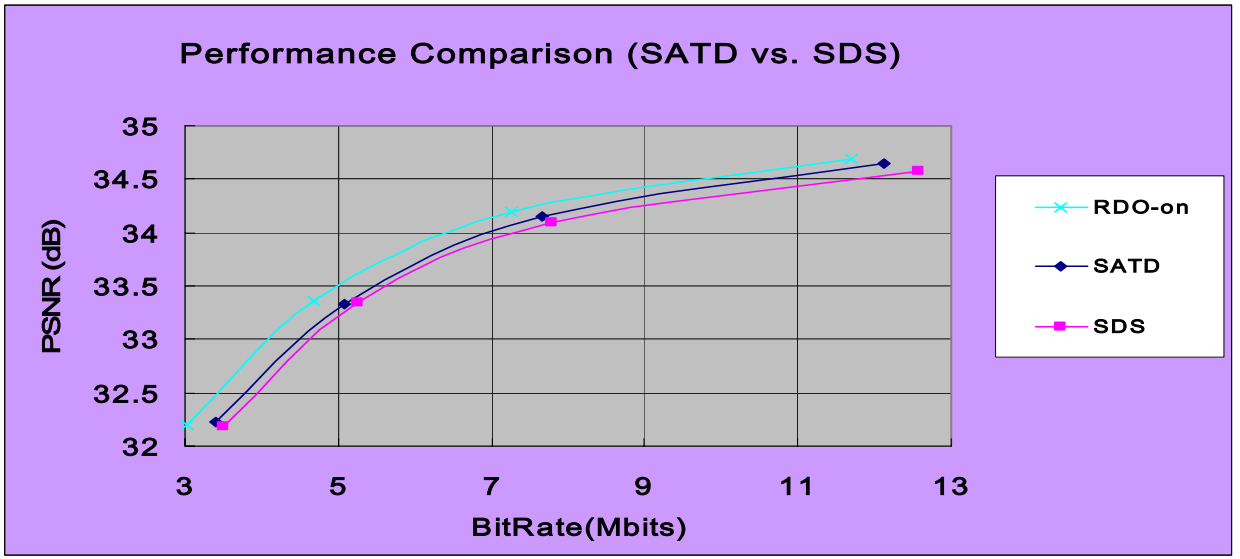


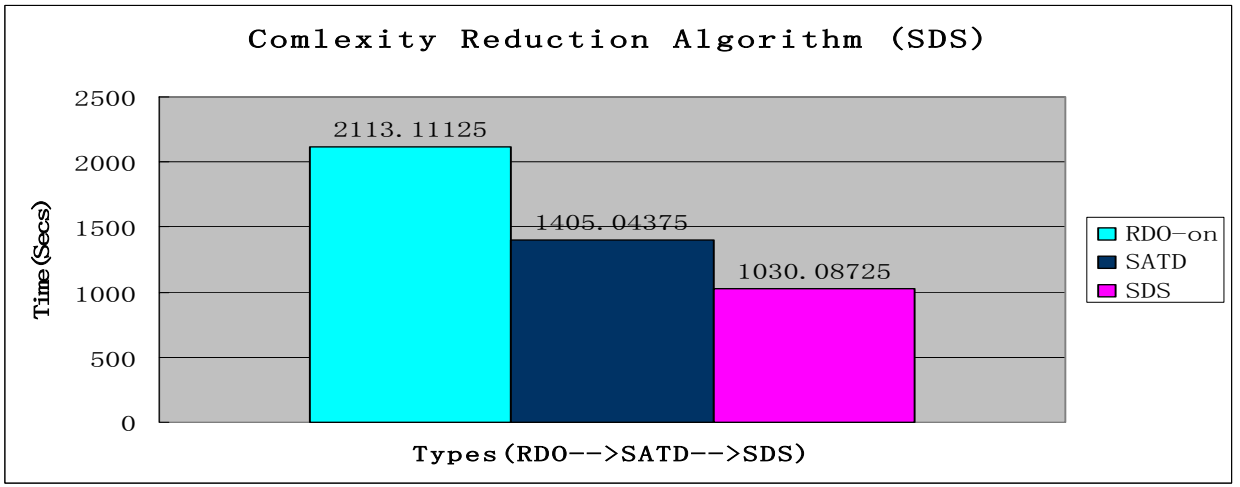
Mod6,
SATD=1134,SDS=306



Mod7,
SATD=1173,SDS=306

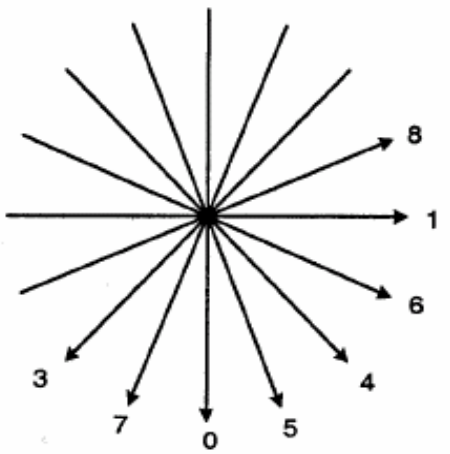
Performance & Complexity of SDS





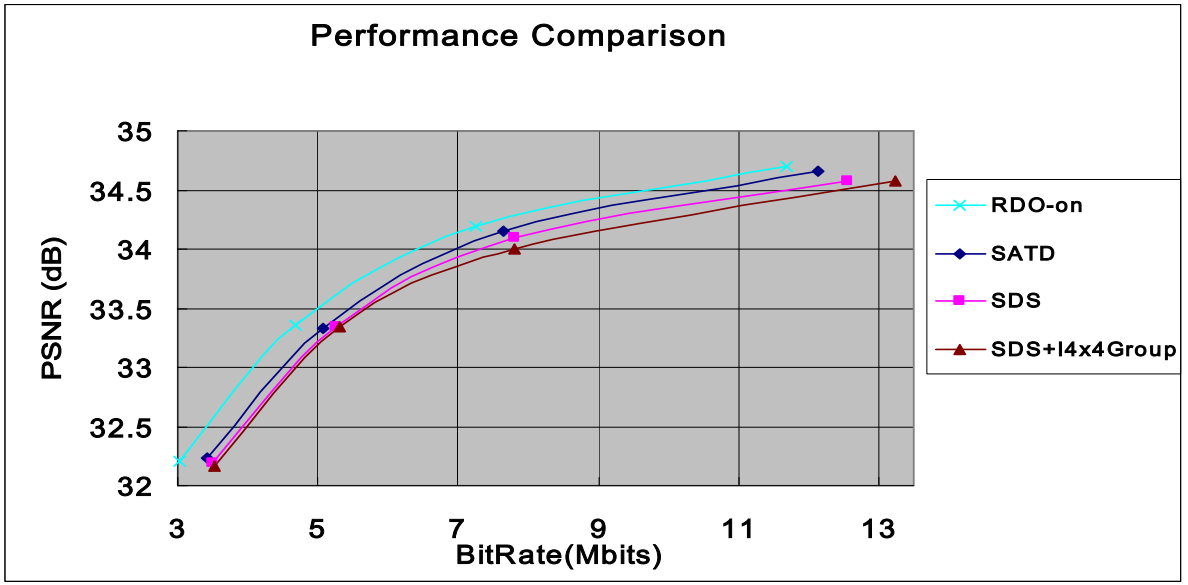
Candidates reduced algorithm

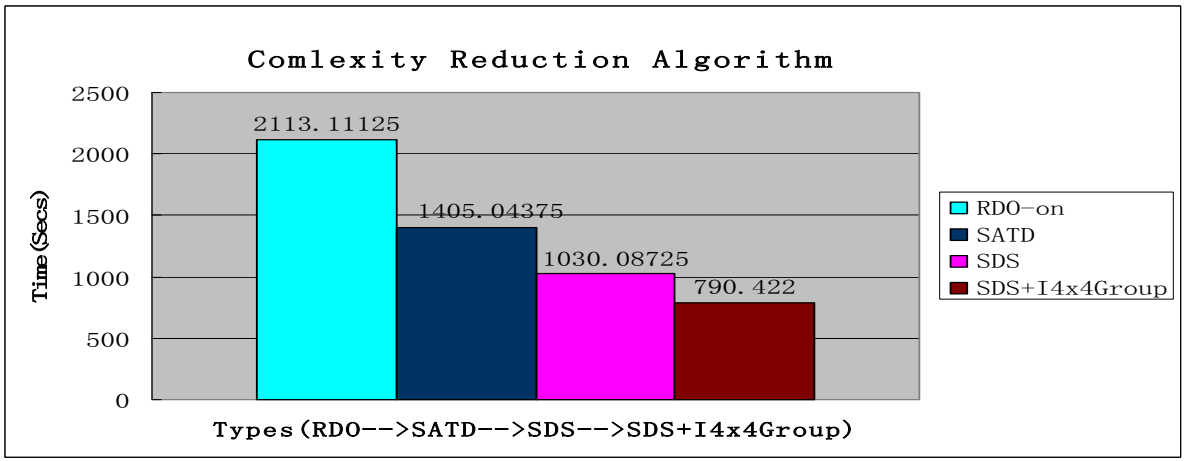
- Step1:We divide Intra 4x4 modes(9 modes) into 5 groups:
  - Group1: DC intra prediction;
  - Group2: mode1,6,8;
  - Group3: mode0,5,7;
  - Group4: mode3;
  - Group5: mode4;



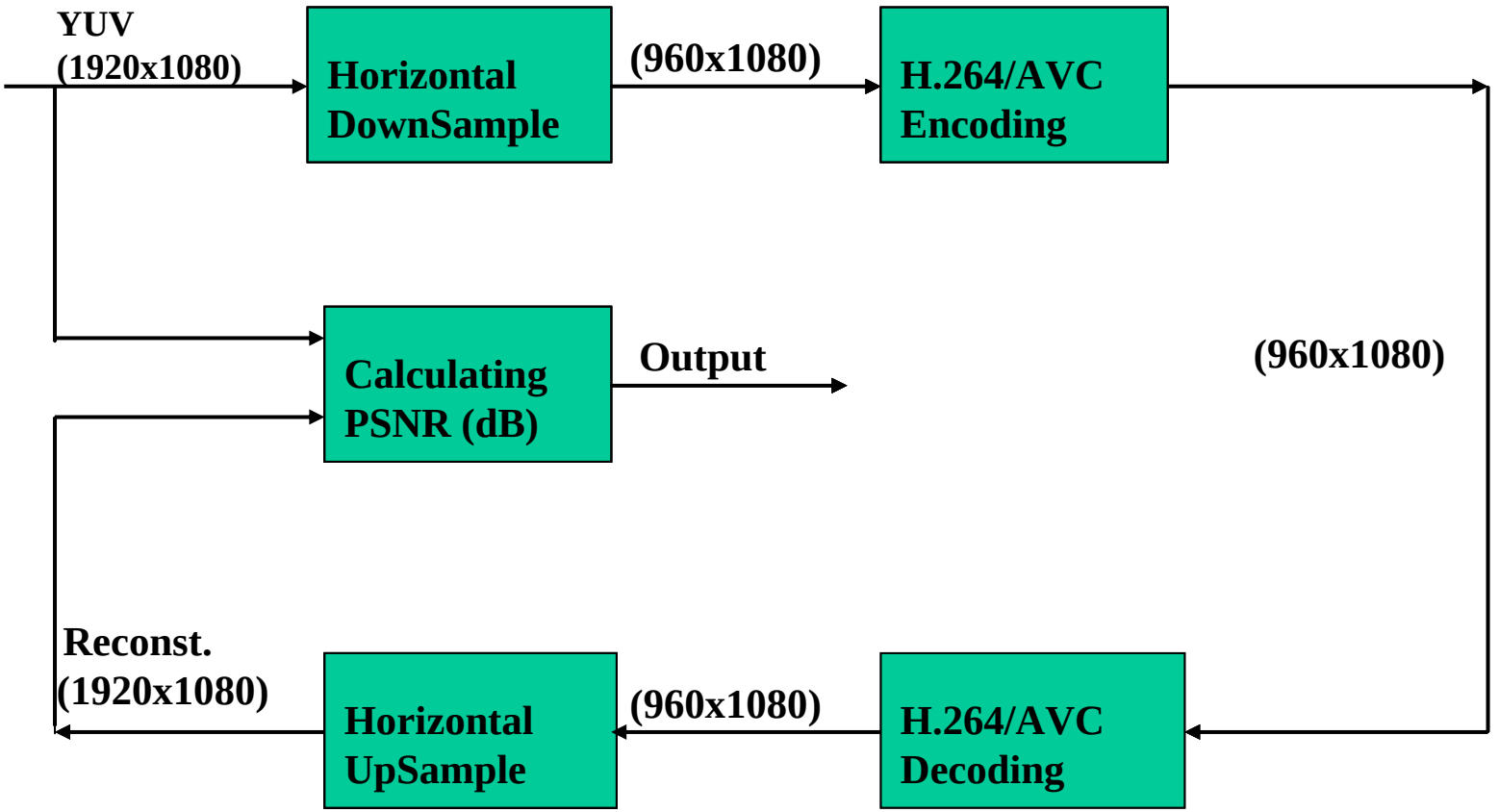
- Step2:Calculate and compare costs of DC,mode1,mode0, mode3 and mode4;
- Step3: Calculate costs of the rest modes inside the group if one group has minimal cost.
- Average complexity saving: 9-((1/9)*5*3+(1/9)*7*6)=2.7 times/MB (30%).

Performance & complexity

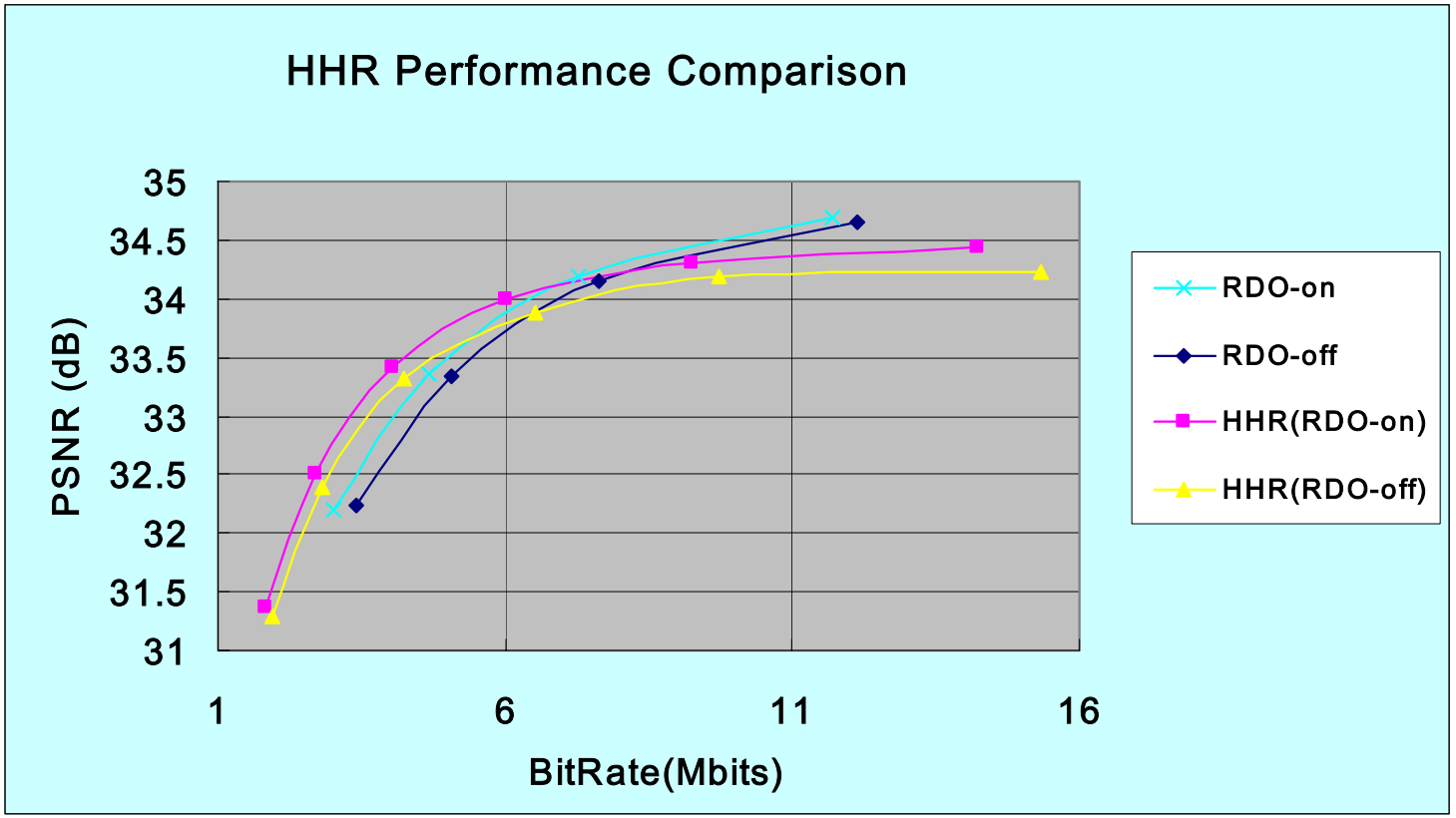




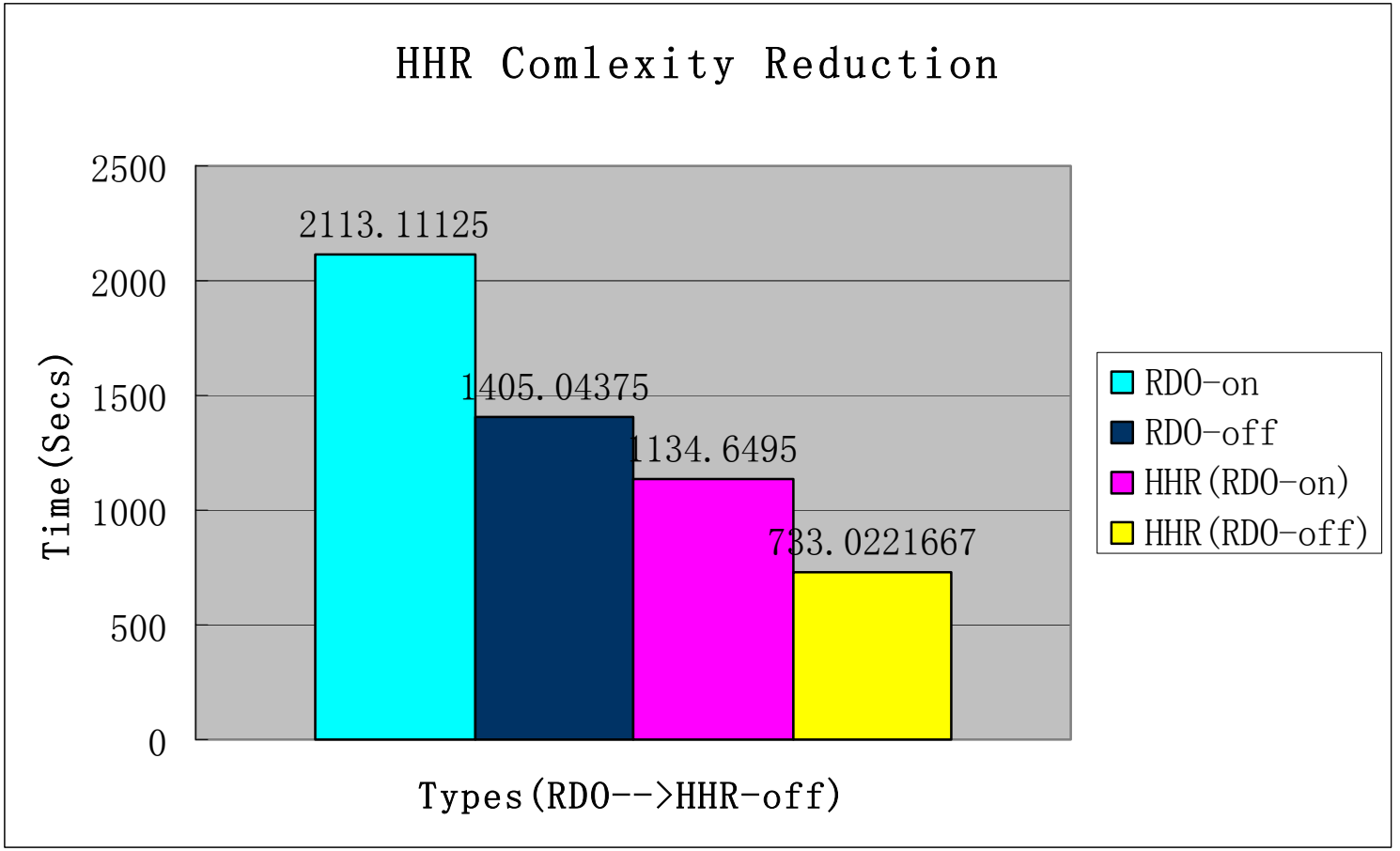
HHR complexity reduction



HHR Performance



HHR Complexity Reduction



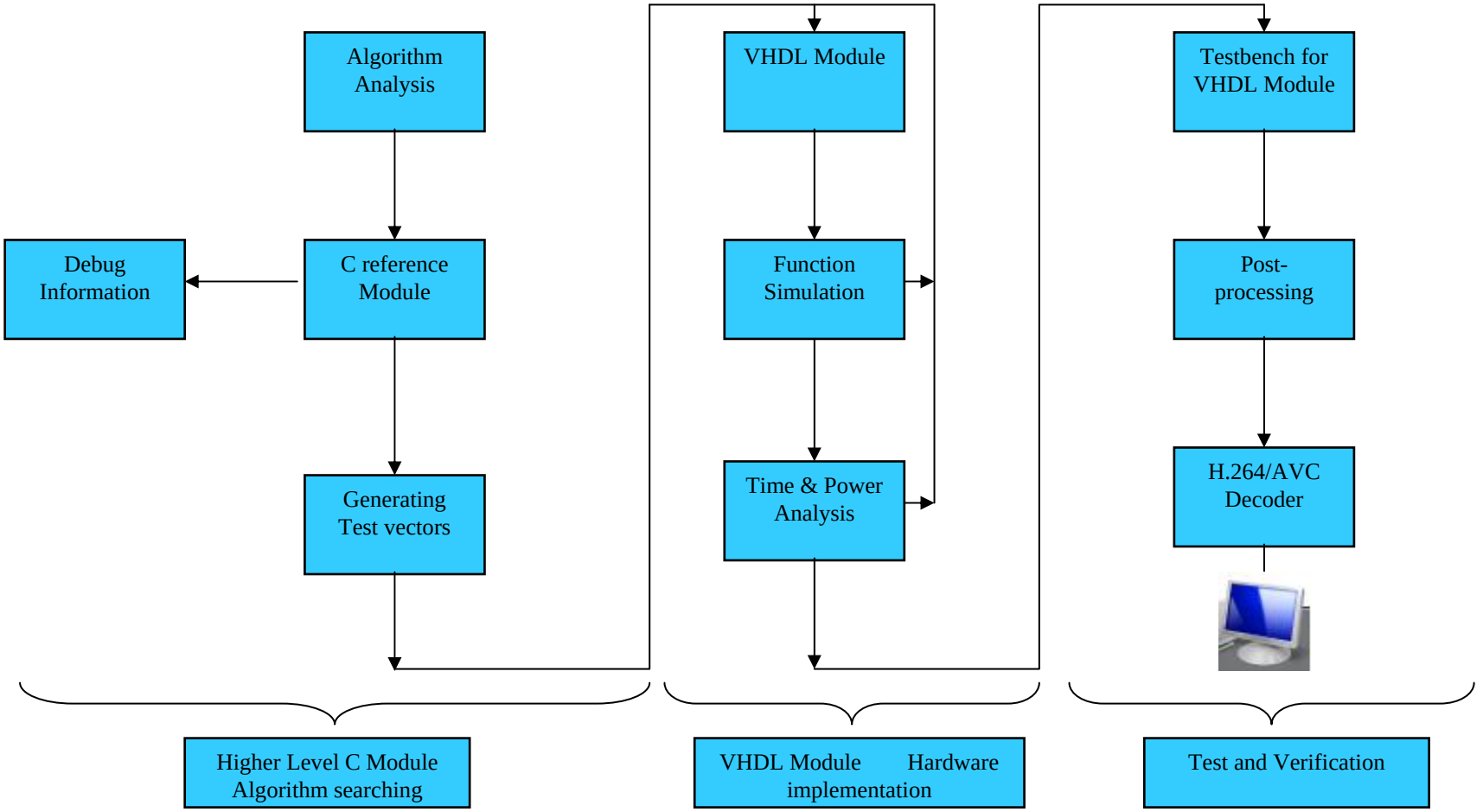
Outline

- H.264/AVC codec overview
  - H.264/AVC development roadmap
  - H.264/AVC features
  - Applications
- H.264 Intra-frame prediction
  - Intra prediction features
  - Intra prediction method
- Intra prediction complexity reduction algorithms
  - Instruction level complexity analysis
  - Mode decision criteria
  - Complexity reduction algorithms searching
- ☞ Research considerations
  - Design methodology
  - Test & verification
  - Design challenges
- Conclusions

Design methodology

- Review SPEC. (ISO 14496 Part 10) of H.264/AVC and related papers.
- Search valuable algorithms aiming to complexity reduction design.
- Test and verify them in reference JM software C module.
- Build HW architecture.
- Write RTL code and go through all the VLSI design procedures.
- Build test and debug platform for validation.

Design flow


Algorithm Analysis
Debug Information
C reference Module
Generating Test vectors
VHDL Module
Function Simulation
Time & Power Analysis
Testbench for VHDL Module
Post-processing
H.264/AVC Decoder
Higher Level C Module Algorithm searching
VHDL Module Hardware implementation
Test and Verification

Design challenges

- Tradeoff among three elements:
  - **Complexity reduction**: We hope that mode decision process does not involve too many computations so that it can be easily applied to real-time applications (normally less than 1024 cycles for a MB).
  - **Compression bitrate**: The less bitrate, the better compression efficiency. We need high quality algorithms to reduce bitrate.
  - **Quality**: High fidelity or low distortion is preferred. Normally, we use PSNR as objective evaluation standard and visually observation as subjective evaluation standard.

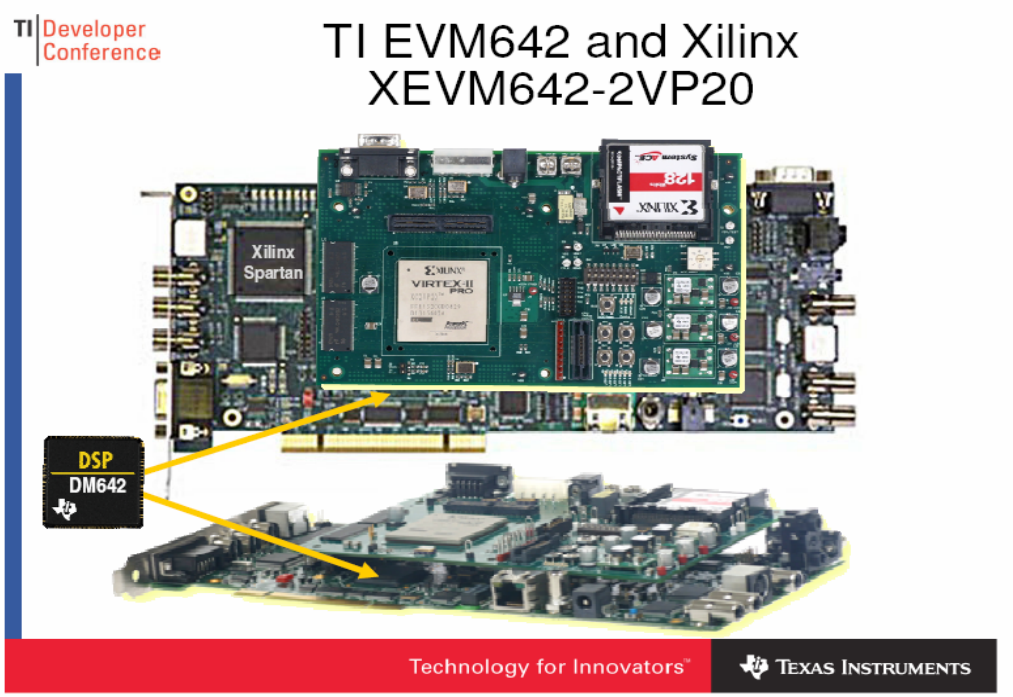
- Low power considerations
  - Decrease memory accessing;
  - Parallel architecture design to decrease frequency;

Industrial H.264/AVC codec

- Several companies are producing custom chips capable of decoding H.264/AVC video. Chips capable of real-time decoding at HDTV picture resolutions include these:
  - Broadcom BCM7411
  - Conexant CX2418X
  - Sigma Designs SMP8630, EM8622L, and EM8624L
- Many other hardware implementations are deployed in various markets, ranging from inexpensive consumer electronics to real-time FPGA-based encoders for broadcast.
  - ATI Technologies' newest graphics processing unit (GPU), the Radeon X1000-series, features hardware acceleration of H.264 decorder.
  - NVIDIA GeForce 7 Series graphic card.
  - Apple's 5th Generation iPod.
  - The Sony Portable playstation3.

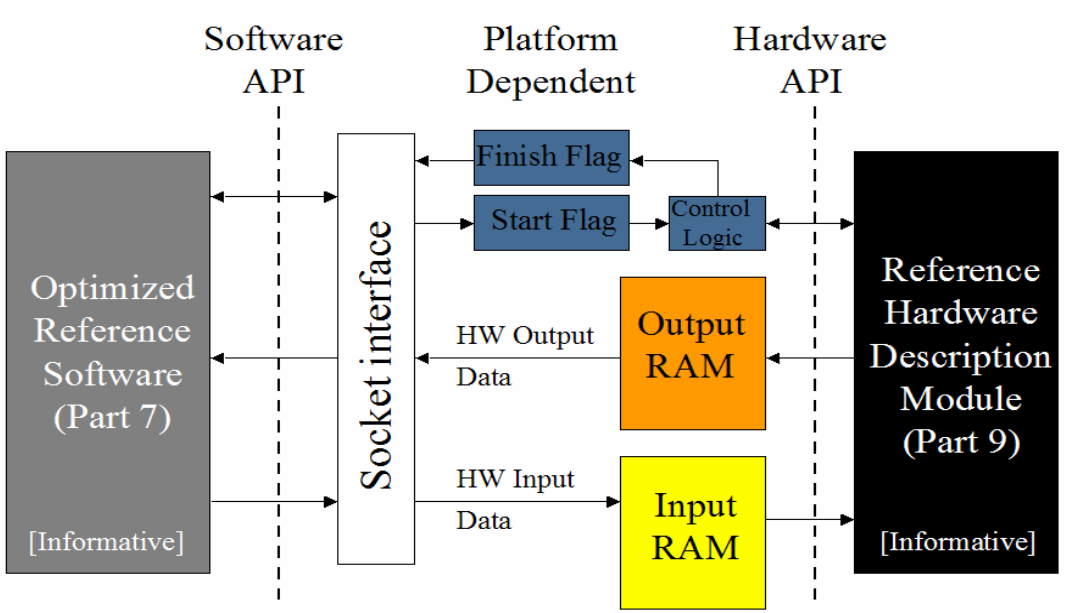
Overview of available H.264 encoder design platform

- Texes Instrument:
  - DSP+FPGA-based solution



PC-based SW/HW co-design platform

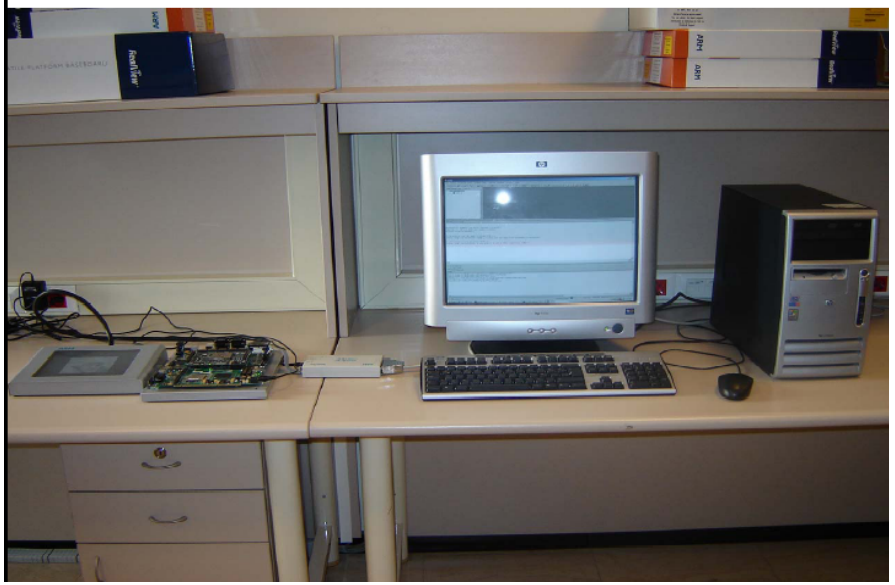
- University of Calgary.
  - Virtual Socket Co-design Platform



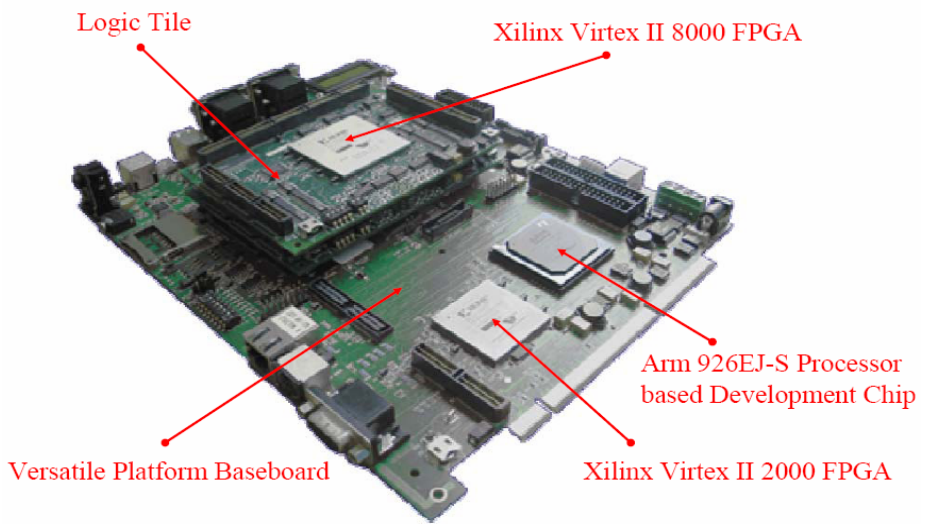
ARM+FPGA-based H.264 encoder

- Sabanci University of Turkey

Arm Versatile Development Platform



Arm Versatile Development Platform



[Sabanci University of Turkey]

Conclusions

- Introduce the latest video compression standard H.264/AVC.
- Intra prediction and its computational complexity is analyzed.
- Algorithms search of complexity reduction and software simulation results are presents.

- Future works:
  - Mode decision part complexity reduction algorithms has been analyzed, transform, quantization and CAVLC part also need complexity reduction algorithms, especially for HW implementation
  - Low power design will be further considered in the next step.

References

[1]. Anthony Vetro, Jianjun Li, Shun-ichi Sekiguchi, “Motion Mapping for MPEG-2 to H.264/AVC Transcoding”, submitted to ISCAS 2007.

[2]. T. Wiegand, G.J. Sullivan, G. Bjøntegaard and A. Luthra, “Overview of the H.264/AVC Video Coding Standard,” *IEEE Transaction on Circuits and Systems for Video Technology*, Vol. 13, no. 7, Jul. 2003.

[3]. “N. Ozbek and T. Tunali, “A Survey on the H.264/AVC Standard,” Turk J. Elec. Engin., vol. 13, no. 3, pp. 287-302, 2005.

[4]. I.E.G. Richardson, “H.264/MPEG4 Part 10: Intra Prediction,” available at http://www.vcodex.com

[5]. Y.W. Huang, B.Y. Hsieh, T. Chen, L.G. Chen et al., “Analysis, Fast Algorithm, and VLSI Architecture Design for H.264 Intra Frame Core”, *IEEE Transactions on Circuit And Systems for Video Technology*, Vol. 15, No. 3, MARCH 2005.

[6]. S. Park, Y. Lee, H. Shin et al., “Quality-Adaptive Requantization for Low-Energy MPEG-4 Video Decoding in Mobile Devices”, *IEEE Transactions on Consumer Electronics*, Vol. 54, No. 3, AUGUST 2005.

[7]. Y.W. Moon, G.Y. Kim, J.H. Kim al., “An Efficient Decoding of CAVLC in H.264/AVC Video Coding Standard”, *IEEE Transactions on Consumer Electronics*, Vol. 51, No. 3, AUGUST 2005.

[8]. ITU-T Rec. H.264 / ISO/IEC 11496-10, “Advanced Video Coding”, Final Committee Draft, Document JVT-E022, September 2002.

[9]. H.264/AVC Reference Software JM10.2, available online at http://bs.hhi.de/~suehring/tml/download/.

Thanks!
&
Questions?