DSD Final Project Scores MIPS

組別：M3

Baseline

(1) Area: (um^2)

```
Number of ports:                         2387
Number of nets:                         23077
Number of cells:                        20928
Number of combinational cells:          16527
Number of sequential cells:              4387
Number of macros/black boxes:               0
Number of buf/inv:                       5941
Number of references:                      19

Combinational area:             175429.683867
Buf/Inv area:                    44035.648060
Noncombinational area:          125444.651712
Macro/Black Box area:                0.000000
Net Interconnect area:         2739627.321136

Total cell area:                 300874.335580
Total area:                     3040501.656716
```

(2) Total Simulation Time of given hasHazard testbench: (ns)

Timing violations before reset & glitches

T = 6616.5 ns

Test bench cycle time = 3ns

```
------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 6616500 PS + 0
./tb/Final_tb.v:158           #(`CYCLE) $finish;
ncsim> exit
```

(3) Area*Total Simulation Time: (um^2 * ns)

A * T = 1990735041 (um^2 * ns)

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

clock cycle = 3 (ns)

BrPred

(1) Total execution cycles of 'I_mem_BrPred'

Timing violations before reset & glitches

cycle time = 6ns

cycles = 1053ns/6ns = 175 cycles

```
Branch Part C is complete.

------------------------- Simulation FINISH !!-------------------------
==============================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

==============================================================================
Simulation complete via $finish(1) at time 1053 NS + 0
./tb/Final_tb.v:158            #(`CYCLE) $finish;
ncsim> exit
[b06014@cad30 ~/DSD_final_project]$
```

(2) Total execution cycles of 'I_mem_hasHazard'

10251ns/6ns = 1708 cycles

```
------------------------- Simulation FINISH !!-------------------------
==============================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

==============================================================================
Simulation complete via $finish(1) at time 10251 NS + 0
./tb/Final_tb.v:158            #(`CYCLE) $finish;
ncsim> exit
[b06014@cad30 ~/DSD_final_project]$
```

(3) Synthesis area of BPU (um^2)

Total area of BrPred minus baseline design, two designs' clock cycle need to be the same when synthesize
6809.968332 (um^2)

(4) Clock cycle of post synthesis simulation

```
1  // this is a test bench feeds initial instruction and data
2  // the processor output is not verified
3
4  `timescale 1 ns/10 ps
5
6  `define CYCLE 6 // You can modify your clock frequency
7
8  `define DMEM_INIT "./pattern/D_mem"
9  `define SDFFILE   "./src_extension/CHIP_syn.sdf"    // Modify your SDF file name
10
```

L2Cache

(1) Average memory access time : 0.8ns (D_mem)

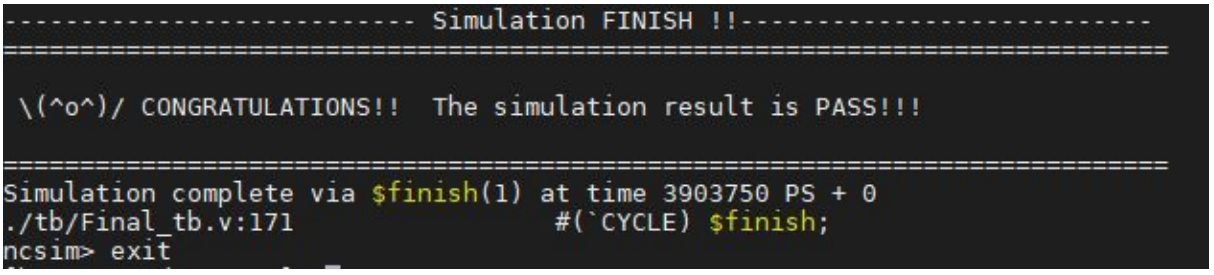
(2) Total execution time of given I_mem_L2Cache : 296,250.5

```
================================================================================
---------------------------- Simulation FINISH !!----------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 296250500 PS + 0
./tb/Final_tb.v:171                #(`CYCLE) $finish;
ncsim> exit
```

MultDiv

(1) Area of MultDiv : 117,365 (um^2)

(2) Total execution time of test program : 3,903.75 (ns)



(3) Minimum clock period : 7 (ns)