TFT LCD Specification

Model Name: TD028TTEC1

Customer Signature
Date

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Record of Reversion

Rev	Issued Date	Description
1.00	July 11 , 2007	New create.
1.10	Aug. 22,2007	Page 18 : Add Response Time Max. value Page 20 : Add Note 10-2
1.20	Oct.3,2007	Page 27 : Modify Mechanical Drawing

1 FEATURES

The 2.8 inch (real 2.83 inch) LCD module is the Transmissive active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used and COG design are built on the panel. Highly integrated LCD module includes backlight and TFT LCD panel with minimal external circuits and components required.

2 GENERAL SPECIFICATION

Item		Description	Unit
Display Size (Diagonal)		2.8 inch (real 2.83 inch)	-
Display Type		Transmissive	-
Active Area (HxV)		43.2 X 57.6	mm
Number of Dots (HxV)		480 x RGB x 640	dot
Dot Pitch (HxV)		0.03 X 0.09	mm
Color Arrangement		RGB Stripe	-
Color Numbers		262,144 (18 bits)	-
Outline Dimension (HxVxT)		52.9x73.7x3.21 (max 3.5 ; FPC excluded)	mm
Shipment Type		COG	
Brightness		200	nits
NTSC		70	%
White Chromaticity (x,y) (Light On)		(0.31,0.33)	
Response Time		20	msec
Viewing Angle (Light On) (R/U/L/D)		55/55/55/50 @CR>10	
Gray Scale Inversion Direction		12 o'clock	
Contrast Ratio (Light On)		300:1	
Operation Temperature		-20~60	℃
Storage Temperature		-30~70	℃
Interface		Parallel RGB	
Weight		25+/-3	g
Power consumption	LCD Panel + System	50 (typ. Color Bar)	mW
	Backlight	305.9 (Typ, I_F= 23mA)	

3 INPUT/OUTPUT TERMINALS

3.1 TFT LCD Module

Recommend connector:

Compatible with Hirose FH23-39S-0.3SHW(05)

PIN No.	P/I/O	Symbol	Descriptions	Remark
1	P	LED+	B/L LED Anode	
2	P	LED-	B/L LED Cathode	
3	P	VDDIO	Power supply for I/O logic	
4	P	VDC	Power supply for analog	
5	P	VSS	GND	
6	O	YU	T/P terminal (Y-Upper)	
7	O	XL	T/P terminal (X-Left)	
8	O	YL	T/P terminal (Y-Lower)	
9	O	XR	T/P terminal (X-Right)	
10	I	XCS	Serial interface chip select	
11	I/O	DIN	Serial interface data input/output	
12	P	VSS	GND	
13	I	SCL	Serial interface clock input	
14		NC	NC pin	
15	I	XRES	Reset (low active)	
16	I	B0	BLUE signal 0(LSB) (ID2)	Pull Down-10K ohm
17	I	B1	BLUE signal 1	
18	I	B2	BLUE signal 2	
19	I	B3	BLUE signal 3	
20	I	B4	BLUE signal 4	
21	I	B5	BLUE signal 5 (MSB)	
22	I	G0	GREEN signal 0(LSB) (ID1)	Pull Down-10K ohm
23	I	G1	GREEN signal 1	
24	I	G2	GREEN signal 2	
25	I	G3	GREEN signal 3	
26	I	G4	GREEN signal 4	
27	I	G5	GREEN signal 5 (MSB)	
28	I	R0	RED signal 0 (LSB) (ID0)	Pull Down-10K ohm
29	I	R1	RED signal 1	
30	I	R2	RED signal 2	
31	I	R3	RED signal 3	

32	I	R4	RED signal 4	
33	I	R5	RED signal 5 (MSB)	
34	P	VSS	GND	
35	I	PCLK	Clock signal for Display Data	
36	P	VSS	GND	
37	I	VSYNC	Vertical synchronous for Display DATA	
38	I	HSYNC	Horizontal synchronous for Display DATA	
39	I	DE	Enable signal for Display	

3.2 Touch Panel Pin

Touch Panel Pin	Module Pin	Symbol	Description	Remark
1	9	XR	Touch Panel Right Side	
2	8	YL	Touch Panel Lower Side	
3	7	XL	Touch Panel Left Side	
4	6	YU	Touch Panel Upper Side	

4 ABSOLUTE MAXIMUM RATINGS

GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	VDDIO	-0.3	+6.5	V	
Analog Supply Voltage	VDC	-0.3	+6.5	V	
Maximum supply voltage	V_{IN}	-0.3	VDDIO+0.3	V	
	V_{OUT}	-0.3	VDDIO+0.3	V	
Touch Panel Operation Voltage	V_{Touch}	-	5.0	V	
Backlight LED forward Voltage	V_F	-	4	V	
Backlight LED reverse Voltage	V_R	-	5	V	
Backlight LED forward current (Ta=25℃)	I_F	-	30	mA	Note 2
Operating Temperature	Topr	-10	60	℃	
Storage Temperature	Tstg	-20	70	℃	

Note 1. Reference voltages must satisfy the following relationship: VDC ≧ VDDIO.

Note 2. Relation between maximum LED forward current and ambient temperature is showed as bellow.

5 ELECTRICAL CHARACTERISTICS

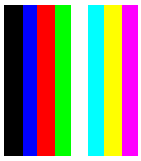
5.1 Driving TFT LCD Panel

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage	VDDIO	+1.7	+3.0	+3.3	V	
	VDC	+2.8	+3.0	+3.3	V	
Input Voltage	VIL	VSS	—	0.3VDDIO	V	Note 1
	VIH	0.7VDDIO	—	VDDIO	V	
Output Voltage	VOL	VSS	—	0.2VDDIO	V	DIN/DOUT
	VOH	0.8VDDIO	—	VDDIO	V	
Input Current	I_{IL}	-10	—	—	uA	Note 2
	I_{IH}	—	—	10	uA	
Supply Current	I_{DDIO}	—	40	50	uA	Note 3
	I_{DC}	—	15	20	mA	
Power consumption	Power	—	50	60	mW	Note 3,4

Note 1: Related pins: VSYNC, HSYNC, DE, PCLK, XRES, XCS, SCL, DIN, and PD0-17

Note 2: The supply current specification is measured at the line inversion test pattern (Color bar vertical as the diagram shown below).



Note 3: Base on VDDIO=3.0V, VDC=3.0V

Note 4: LCD Panel + Driver IC

5.2 Driving Backlight

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	23		mA	LED/Part
LED Life Time	-	-	10000	-	Hr	I_F: 20mA
Forward Current Voltage	V_F	-	13.3	16	V	I_F: 23mA ,LED/Part

Note: Backtlight driving circuit is recommend as the fix current circuit.

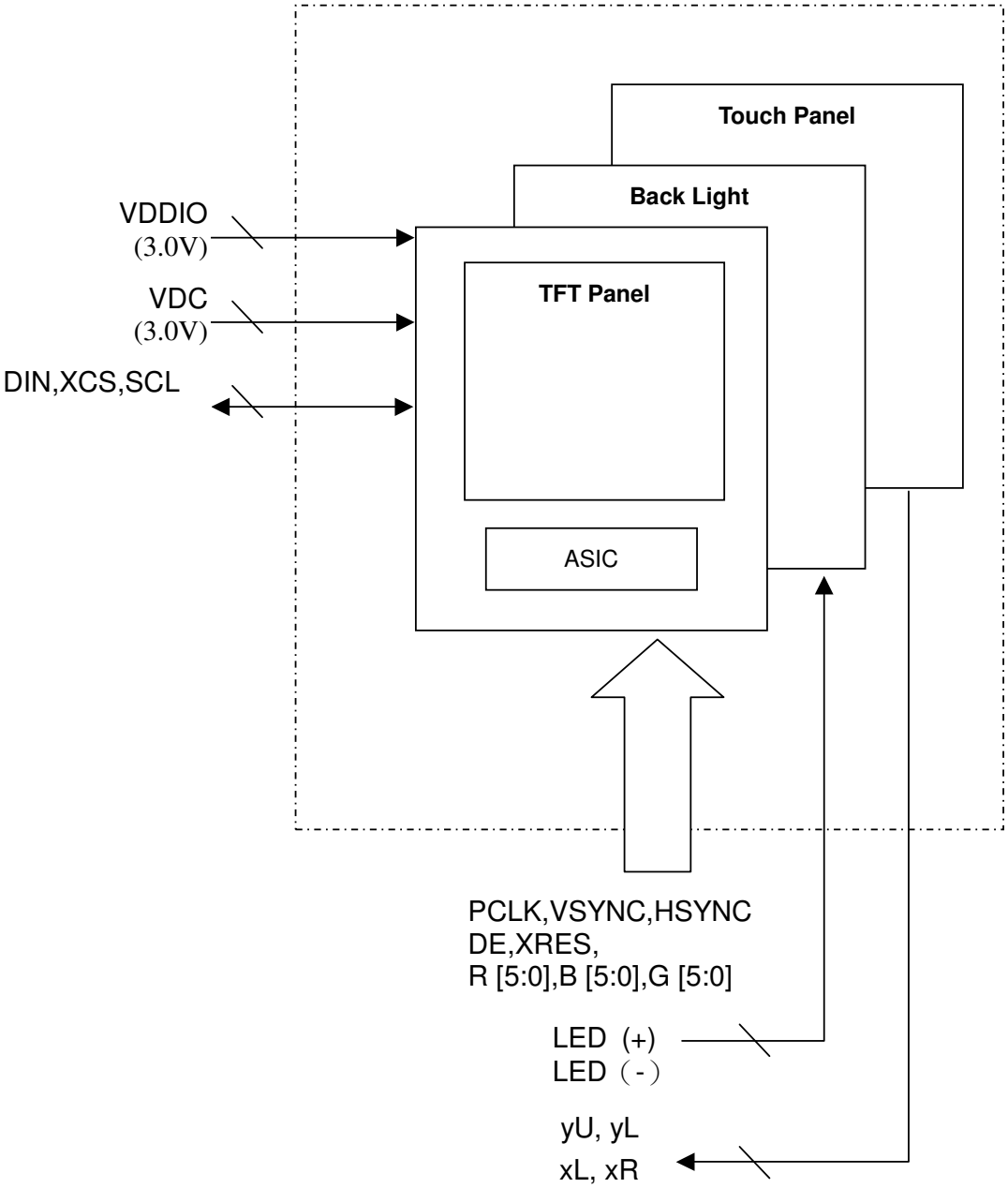
5.3 Driving Touch Panel (Analog Resistance Type)

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Resistor between terminals (XR-XL)	Rx	250	-	950	Ω	
Resistor between terminals (YU-YL)	Ry	250	-	950	Ω	
Operation Voltage	V_{Touch}	-	2.5	-	V	DC
Line Linearity (X direction)	-	-1.5	-	+1.5	%	Note
Line Linearity (Y direction)	-	-1.5	-	+1.5	%	
Chattering	-	-	10	-	ms	
Surface Hardness	-	3	-	-	H	JIS K 5600
Minimum tension for detecting	-	-	-	80	g	
Insulation Resistance	Ri	20	-	-	MΩ	At DC 25V

Note: The minimum test force is 80 g.

6 BLOCK DIAGRAM



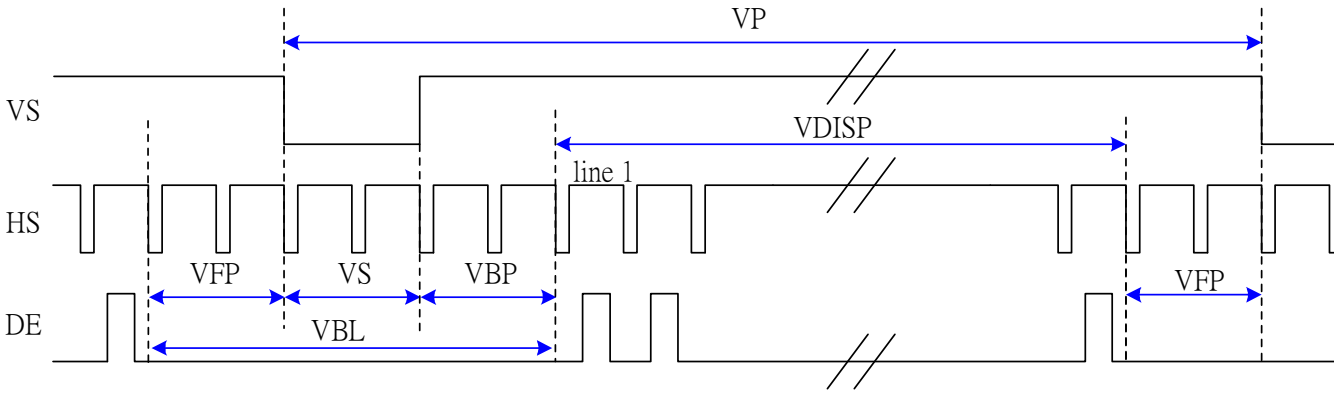
7 TIMING CHART

7.1 Display Timing

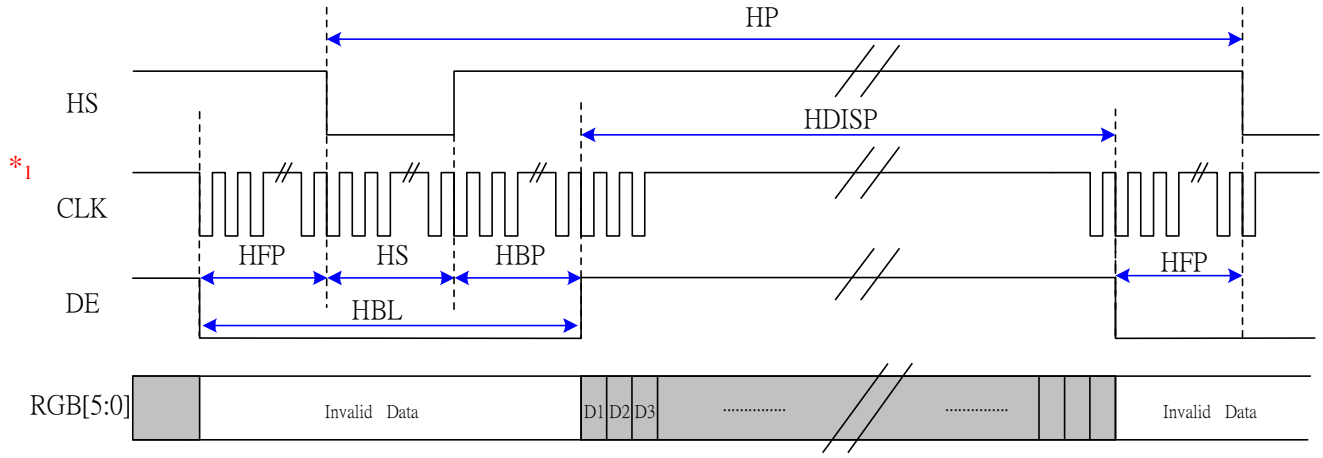
Display Mode	Parameter	Symbol	Conditions	Ratings			Unit
				MIN	TYP	MAX	
Normal	Vertical cycle	VP		648	—	—	Line
	Vertical data start	VDS	VS+VBP	4	—	—	Line
	Vertical Sync Pulse width	VS		2	—	—	Line
	Vertical front porch	VFP		4	—	—	Line
	Vertical Back porch	VBP		2	—	—	Line
	Vertical blanking period	VBL	VS+VBP+VFP	8	—	—	Line
	Vertical active area	VDISP		640	—	—	Line
	Horizontal cycle	HP		520	—	—	dot
	Horizontal front porch	HFP		24	—	—	dot
	Horizontal Sync Pulse width	HS		8	—	—	dot
	Horizontal Back porch	HBP		8	—	—	dot
	Horizontal Data start	HDS	HS+HBP	16	—	—	dot
	Horizontal active area	HDISP		480	—	—	dot
	Clock frequency	fclk		22	—	—	MHz
		tclk		45	—	—	nS

7.2 Input Timing Chart

＜Vertical Timing chart＞

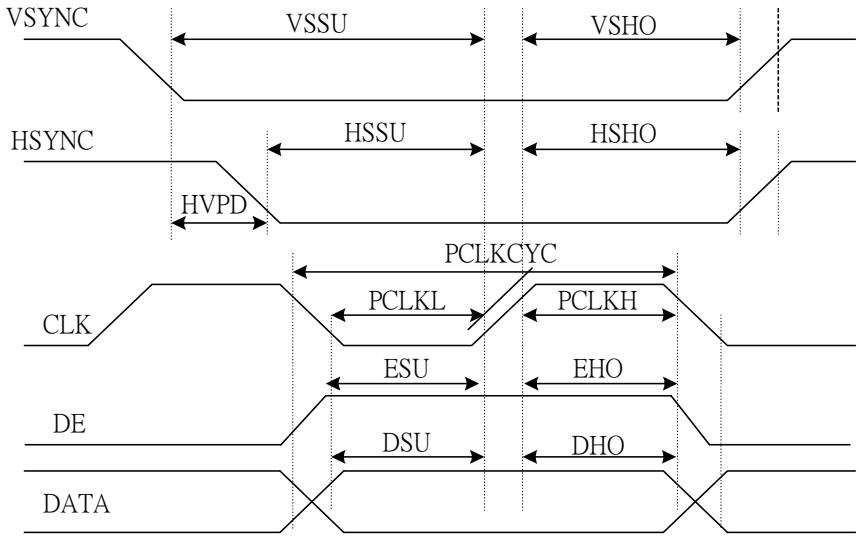


＜Horizontal Timing chart＞



Note: The frequency of CLK should be continued whether in display or blank region to ensure IC operating normally.

7.3 Setup / Hold Timing Chart



7.4 AC Characteristics:

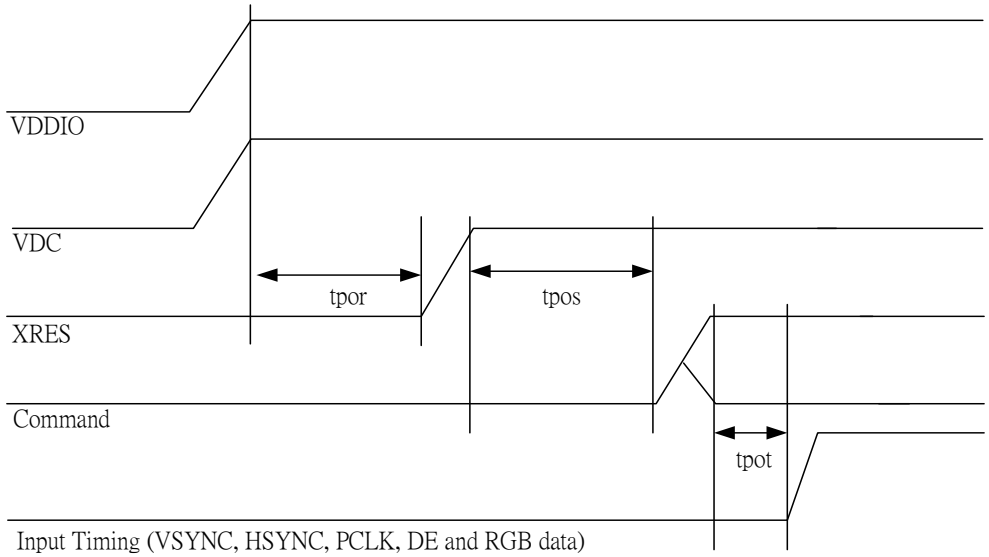
Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
VSYNC Setup time	VSSU		15	—	—	ns
VSYNC Hold time	VSHO		15	—	—	ns
HSYNC Setup time	HSSU		15	—	—	ns
HSYNC Hold time	HSHO		15	—	—	ns
VSYNC-HSYNC Falling edge	HVPD		0	—	—	ns
PCLK cycle time	PCLKCYC		40	—	—	ns
Clock “L” pulse width	PCLKL		15	—	—	ns
Clock “H” pulse width	PCLKH		15	—	—	ns
DE setup time	ESU		15	—	—	ns
DE Hold time	EHO		15	—	—	ns
Data setup time	DSU		15	—	—	ns
Data Hold time	DHO		15	—	—	ns

Note 1：Input signal rise/fall time：tr, tf ≦5 ns

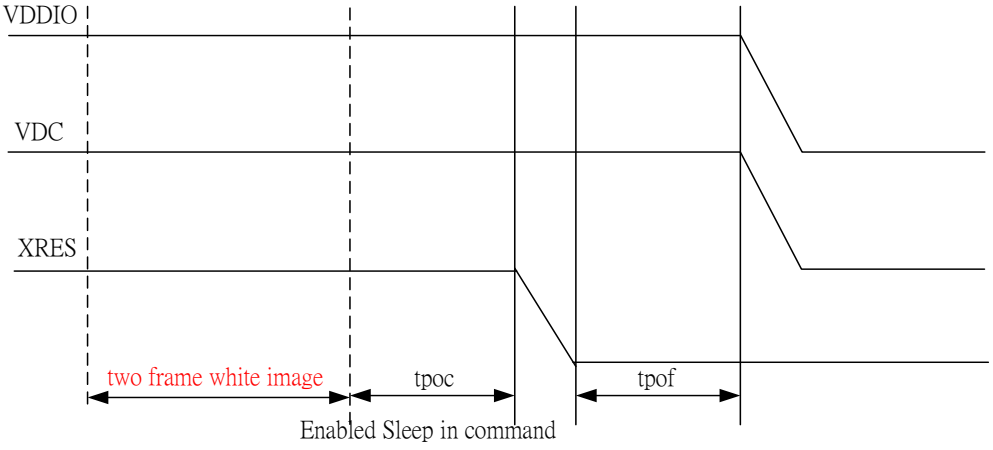
Note 2：The threshold voltage of input signal：VIH = 0.7xVDDIO, VIL = 0.3xVDDIO

8 POWER ON/OFF SEQUENCE

Power on sequence



Power off sequence



Characteristics	Symbol	Conditions	Min	Typ.	Max	Unit
Power on reset time	tpor	–	1	–	–	ms
Reset release time (Reset H - CMD)	tpos	–	20	–	–	ms
CMD – Input timing time	tpot	–	10	–	–	ms
Sleep mode release time	tpoc	–	250	–	–	ms
XRES – VDC power off time	tpof	–	1	–	–	ms

Note 1 To avoid image retention , please input white image for two frame before power off.

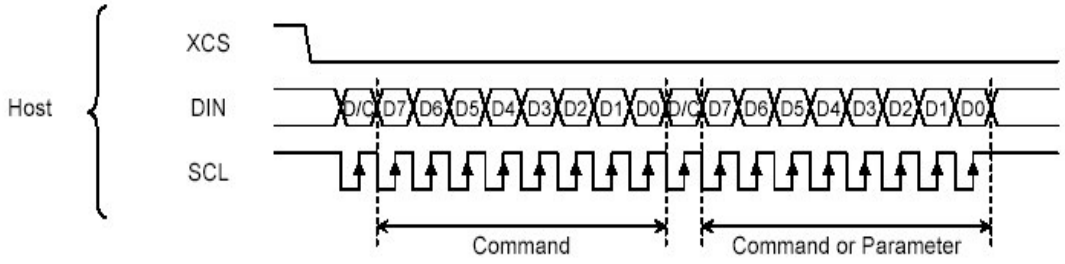
9 SERIAL INTERFACE

The LCM support the 3-Wire serial interface to set internal register. Read/Write bit D/C, Serial address D7 to D0 (DIN) and serial data D7 to D0 (DOUT) are read at the rising edge of the serial clock, via the serial input pin. This data is synchronized on the rising edge of eighth serial clock and is then converted to parallel data. The serial interface signal timing chart is shown below.

9.1 Serial Interface Signal Timing Chart

a) Command write instruction

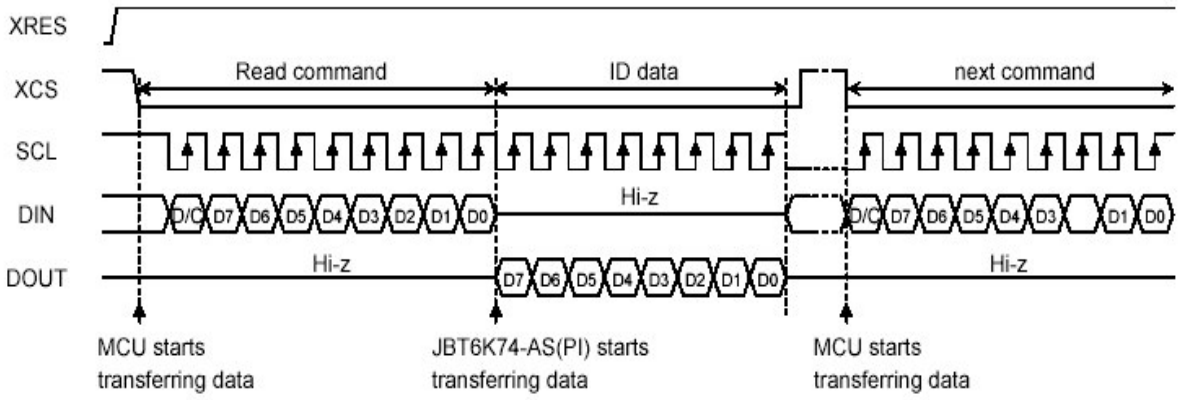
While the XCS signal is low, a zero detected in the DIN signal causes the serial interface controller to recognize the next SCL rising edge as D7 of a command and start fetching data. In the input data, MSB = D7 and LSB = D0. Once the LSB of the command has been input, the serial interface controller expects either a command or parameter data according to the rising edge. If D/C = high, it recognizes the data the host transmits next as a parameter. If D/C = low, it recognizes the next data as a command.



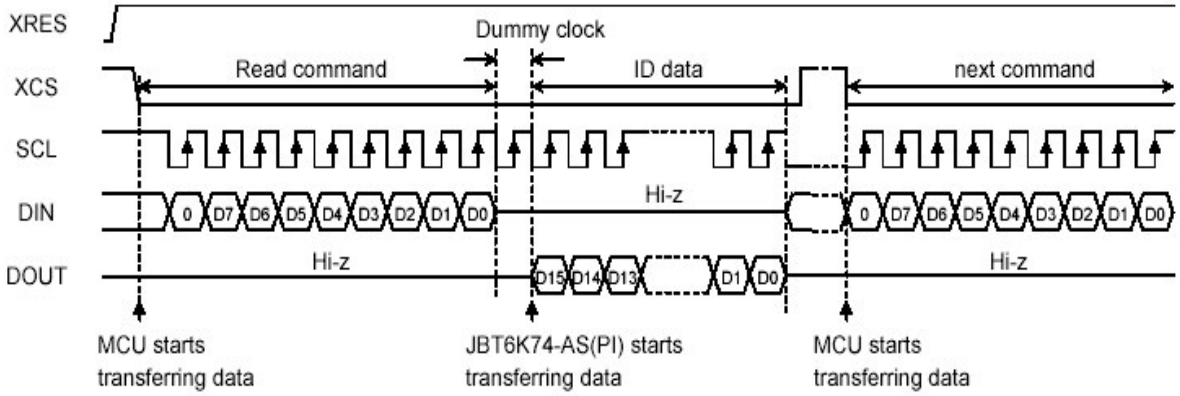
b) Status read

The JBT6K78-AS(PI) allows the host to issue a request (status read instruction) to retrieve the internal chip status and ID information. Status data and ID information are output on the rising edge of SCL. After reading status data and ID information, the host can enable the next command transfer by driving XCS high temporarily and then back low. Note that the status read protocol varies with the operation command type.

■ For the 8 bits long operation command (06, 07, 08h, and 0Ah to 0Eh)

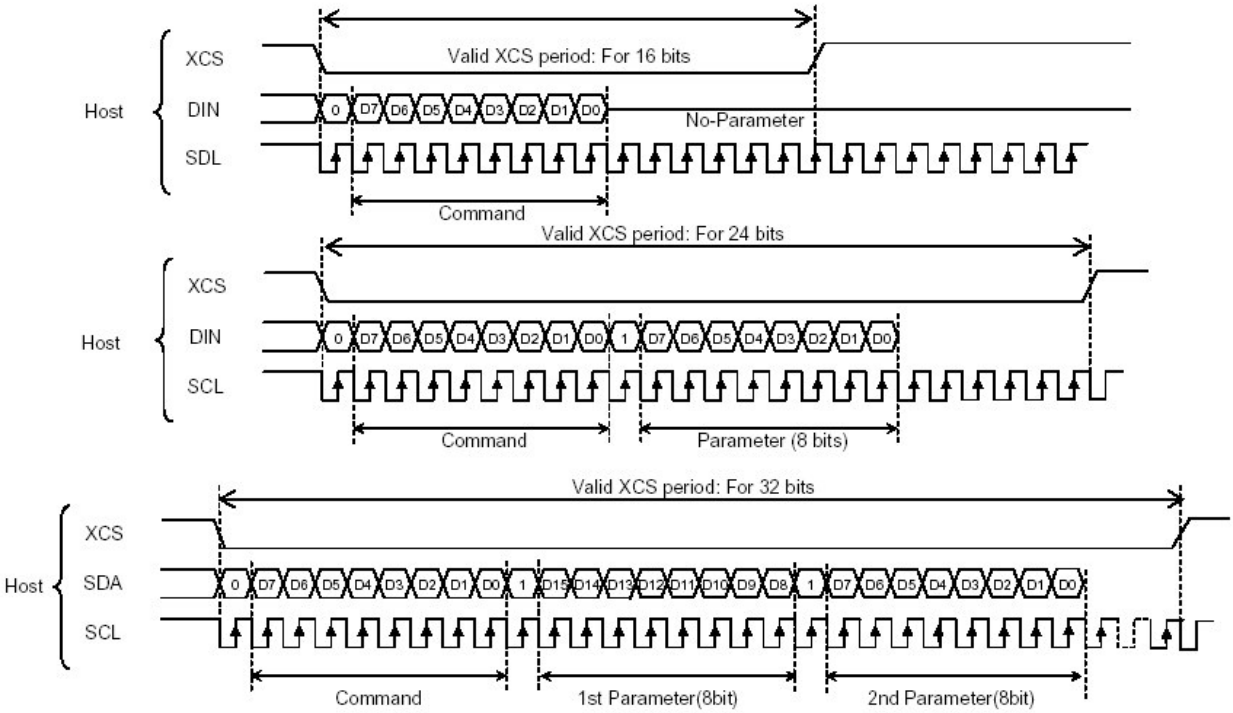


■ For the 16 or more bits long operation command (04,09h, and EBh)



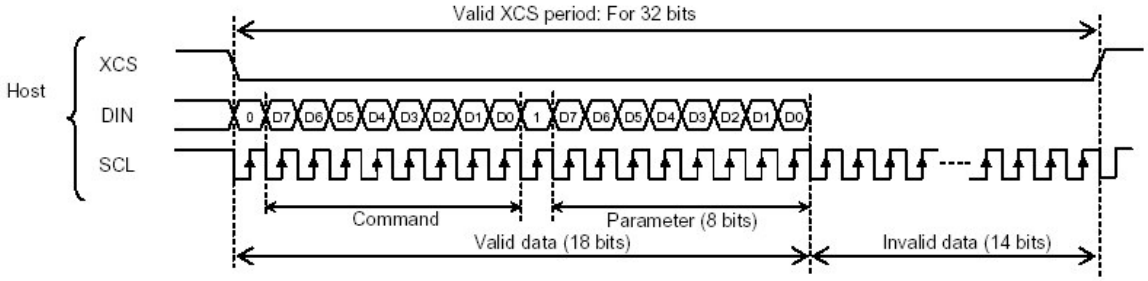
■ Transfer out of rule

Example of introducing conventions for transferring the XCS signal in units of 8 bits



In the above example of transfer for the JBT6K74-21AS, an operation code is specified in the command area configured when D/C = 0. In this case, the internal command register accepts only the data of the parameter assigned by the operation code, with excess data invalidated in the valid XCS period. If the valid XCS period is fixed, however, the following status is set up.

Example) When XCS = 32 bits, and DIN = 9 bits (command) + (1 bit (D/C) + 8 bits (parameter))



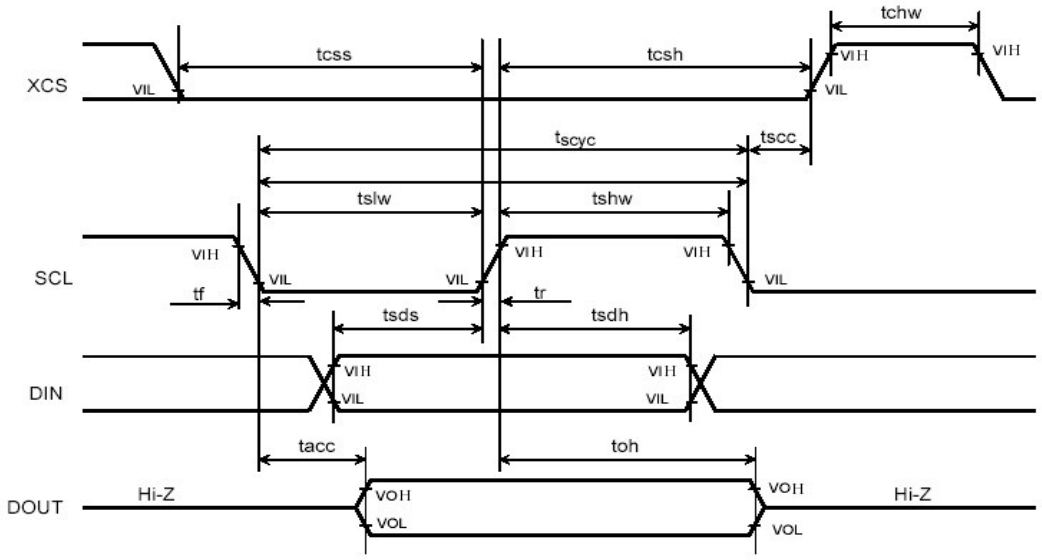
Note : In the above example, the 32-bit XCS signal is valid and fixed. This also applies to 16- or 24-bit applications.

You should note the following points.

- For consecutive command transfer, if data is transferred in the invalid-data period in the above example and the transfer doesn't finish in the valid XCS period, the data transfer is interrupted by the break or pause function. In this case, you resend data according to rules covered in paragraph c), "Data recovery after transfer interruption or suspension."
- With transfer restrictions (for example, a XCS signal format is set) or with other restrictions, you should prevent trouble by driving the XCS signal high for each command.

9.2 Serial Interface and Reset Waveform

Serial Interface



Serial interface and Reset							
Parameter		**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Write mode	Clock cycle	tscyc	—	100	—	—	ns
	SCL “H” Period	tshw	—	35	—	—	ns
	SCL “L” Period	tslw	—	35	—	—	ns
	Data Set-up Time	tsds	—	20	—	—	ns
	Data Hold Time	tsdh	—	20	—	—	ns
Read mode	Clock cycle	tscyc	—	150	—	—	us
	SCL “H” Period	tshw	—	60	—	—	ns
	SCL “L” Period	tslw	—	60	—	—	ns
	Output Data Delay Time	tacc	—	—	—	120	ns
	Output Data Hold Time	toh	—	15	—	50	ns
XCS “L” cancel time		tscc	—	20	—	—	ns
XCS “H” pulse width		tchw	—	40	—	—	ns
XCS signal setup time		tcss	—	30	—	—	ns
XCS signal hold time		tcsh	—	35	—	—	ns

Note 1：Input signal rise/fall time：tr, tf ≦15 ns

Note 2：The threshold voltage of input signal：VIH = 0.8xVDDIO, VIL = 0.2xVDDIO

10 OPTICAL CHARACTERISTIC

10.1 Optical Specification

10.1.1 Backlight On

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ11(R)		CR ≥ 10	50	55	-	Degree	Note 10-1
	Θ12(L)			50	55	-		
	Θ21(U)			50	55	-		
	Θ22(D)			45	50	-		
Response Time	Tr+Tf		Θ=0°	-	20	30	ms	Note 10-3
Contrast Ratio	CR		Θ=0°	250	300	-	-	Note 10-4
Luminance	L		Θ=0° I_F =TBD	165	200	-	nits	Note 10-5
NTSC	-		-	60	65	-	%	Note 10-2
Uniformity	-		-	75	80	-	%	Note 10-6
Chromaticity	Red	x	Θ=0°	0.577	0.627	0.677	-	Note 10-7
		y		0.305	0.355	0.405		
	Green	x		0.253	0.303	0.353		
		y		0.562	0.612	0.662		
	Blue	x		0.093	0.143	0.193		
		y		0.013	0.063	0.113		
	White	x		0.250	0.300	0.350		
		y		0.263	0.313	0.363		

10.2 Basic Measure Condition

(1) Driving voltage

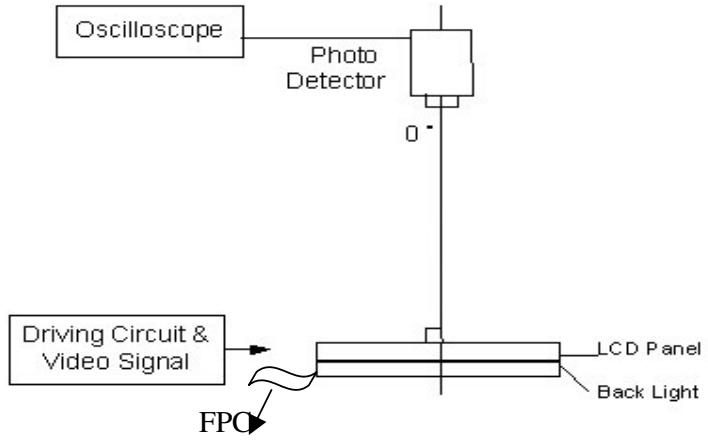
VDD= 12.0V, VEE=-6.5V

(2) Ambient temperature: Ta=25℃

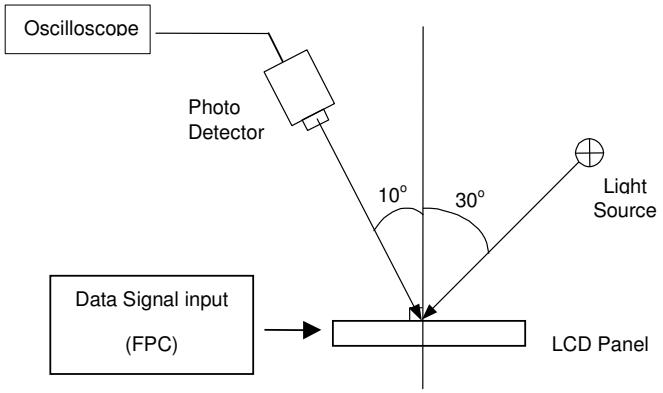
(3) Testing point: measure in the display center point and the test angle Θ=0°

(4) Testing Facility: Environmental illumination: ≦1 Lux

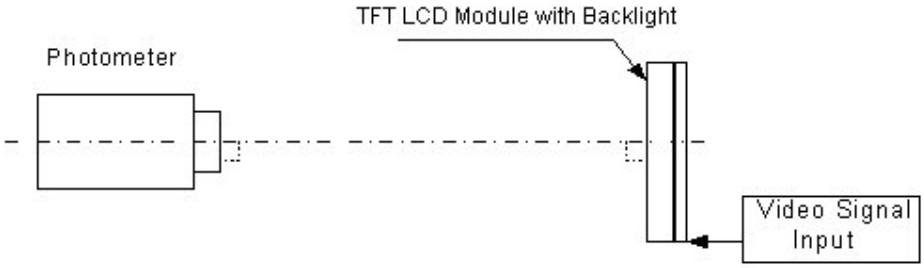
A. System A (DMS 900 series)



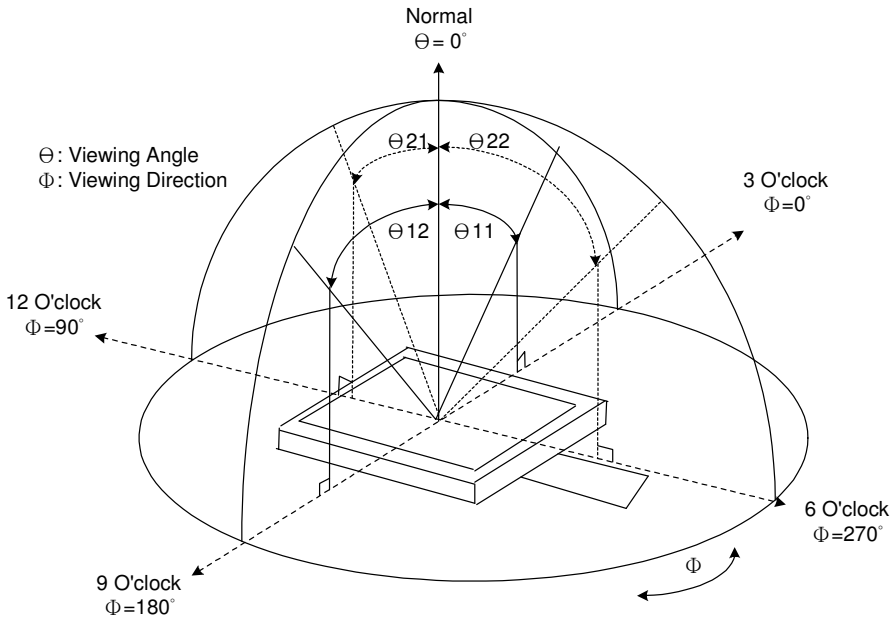
B. System B (DMS 900 series)



C. System C (BM5A)



Note 10-1: Viewing angle diagrams (Measure System A)

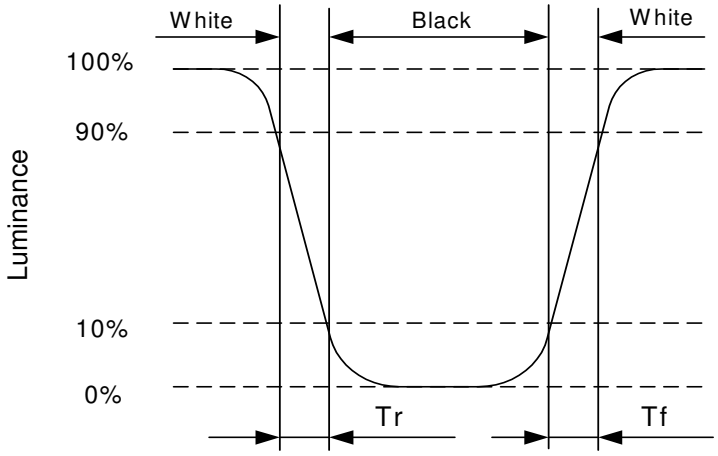


Note 10-2: NTSC (Measure System A_ Spectrum meter)

$$NTSC = 100 \times \frac{\left| R_x G_y + G_x B_y + B_x R_y - G_x R_y - B_x G_y - R_x B_y \right|}{2 \times 0.1582} \%$$

$R(R_x, R_y)$ $G(G_x, G_y)$ $B(B_x, B_y)$

Note 10-3: Definition of response time: (Measure System C)



Note 10-4: Contrast Ratio in back light on (Measure System A)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

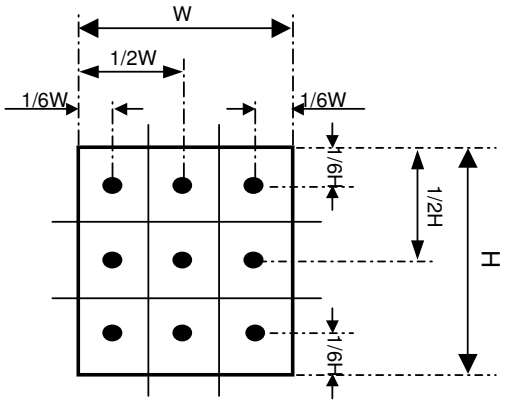
Note 10-5: Luminance : (Measure System A_ Spectrum meter)

Test Point: Display Center

Note 10-6: Uniformity (Measure System C)

The luminance of 9 points as the black dot in the figure shown below are measured and the uniformity is defined as the formula:

$$\text{Uniformity} = \frac{\text{The minimum luminance among 9 points}}{\text{The maximum luminance among 9 points}}$$



Active Area (W x H)

Note 10-7: White chromaticity as back light on and NTSC (Measure System A_Spectrum)

11 RELIABILITY

No	Test Item	Condition
1	High Temperature Operation	Ta=+60℃, 240hrs
2	High Temperature & High Humidity Operation	Ta=+40℃, 95% RH, 240hrs
3	Low Temperature Operation	Ta=-20℃, 240hrs
4	High Temperature Storage (non-operation)	Ta=+70℃, 240hrs
5	Low Temperature Storage (non-operation)	Ta=-30℃, 240hrs
6	Thermal Shock (non-operation)	-20℃(30min) ← → +70℃(30min), 50 cycles
7	Surface Discharge (non-operation)	C=150pF, R=330 Ω; Discharge: Air: ±15kV; Contact: ±8kV 5 times / Point; 5 Points / Panel
8	Vibration (non-operation)	Frequency: 10~55Hz; Amplitude: 1.5mm Sweep Time: 11min Test Time: 2 hrs for each direction of X, Y, Z
9	Shock (non-operation)	Acceleration: 100G; Period: 6ms Directions: ±X, ±Y, ±Z; Cycles: Three times
10	Pin Activation Test (Touch Panel)	Hit 1,000,000 times with a silicon rubber of R8 HS 60. Hitting Force: 250g Hitting Speed: 3 time/sec
11	Writing Friction Resistance Test (Touch Panel)	Hit 100,000 times Pen: 0.8R Polyacetal stylus Load: 250g Speed: 3 Strokes/sec Stroke: 35mm

12 HANDLING CAUTIONS

12.1 ESD (Electrical Static Discharge) Strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy. In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connects wrist to the earth and the conducting shoes to the earth necessary is:

(1) The machine and working table for the panel should have ESD protection strategy.
(2) In handling the panel, ionized airflow decreases the charge in the environment is necessary.
(3) In the process of assemble the module, shield case should connect to the ground.

12.2 Environment

(1) Working environment of the panel should be in the clean room.
(2) Because touch panel has protective film on the surface, please remove the protection film slowly with ionized air to prevent the electrostatic discharge.

12.3 Touch Panel

(1) The front touch panel is vulnerable to heavy weight, so any input must be done by special stylus or by finger. Do not put any heavy stuff on it.
(2) When any dust or stain is observed on a film surface, clean it using a glass lens cleaner for something similar.

12.4 Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.
(2) Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.
(3) Water drop on the surface or condensation as panel power on will corrode panel electrode.
(4) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.
(5) In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and soap as soon as possible.

12.5 Design Notes on Touch Panel

(1) Explanation of each boundary of touch panel
Boundary of Double-sided adhesive: Electrically detectable within this zone. When holding the touch panel by housing, it needs to be held at outside of this zone. Film is supported by double-sided adhesive tape.
(2) Viewing area
Cosmetic inspection to be done for this area. This area is set as inside of boundary of double-sided

adhesive with tolerance.

(3) Boundary of transparent insulation

a. Purpose is to〝Help〞to secure insulation.

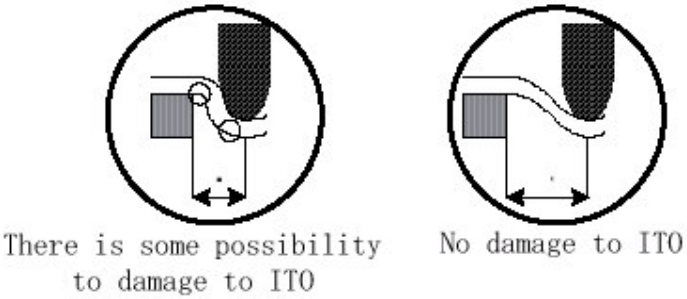
b. Electrical insulation on this area is not guaranteed.

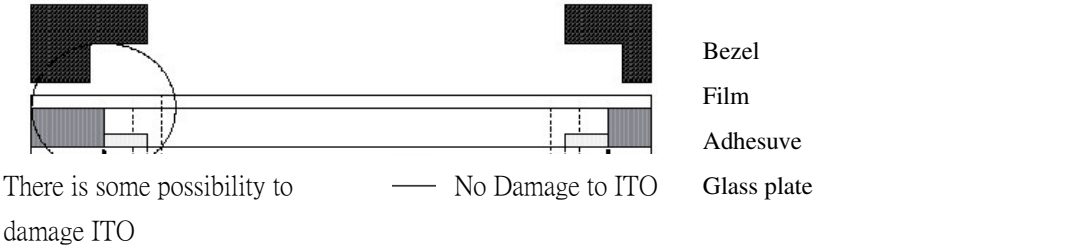
c. We do recommend not to hold this area by something like housing or gasket.

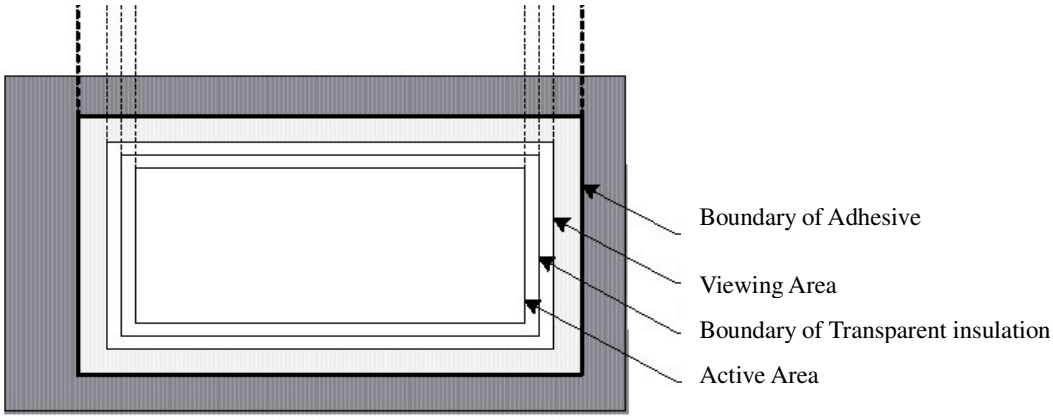
(4) Active area

a. This area is where the performance is guaranteed.

b. This area set as 2.3mm inside from the boundary area of double-sided adhesive tape since its neighboring area is less durable to writing friction.



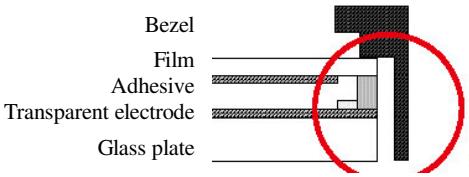




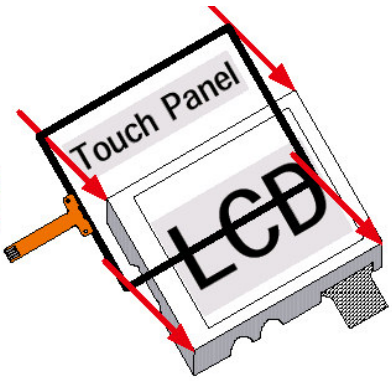
(5) Housing and Touch Panel

a. Please have clearance between the side of touch panel and any conductive material such as metal frame (Drawing.1). Transparent electrode exists on glass of touch panel from end to end.

b. It is recommended to fix a touch panel on the LCD module chassis rather than the touch panel housing. Clinging at conductive material and side of touch panel might cause the malfunction.

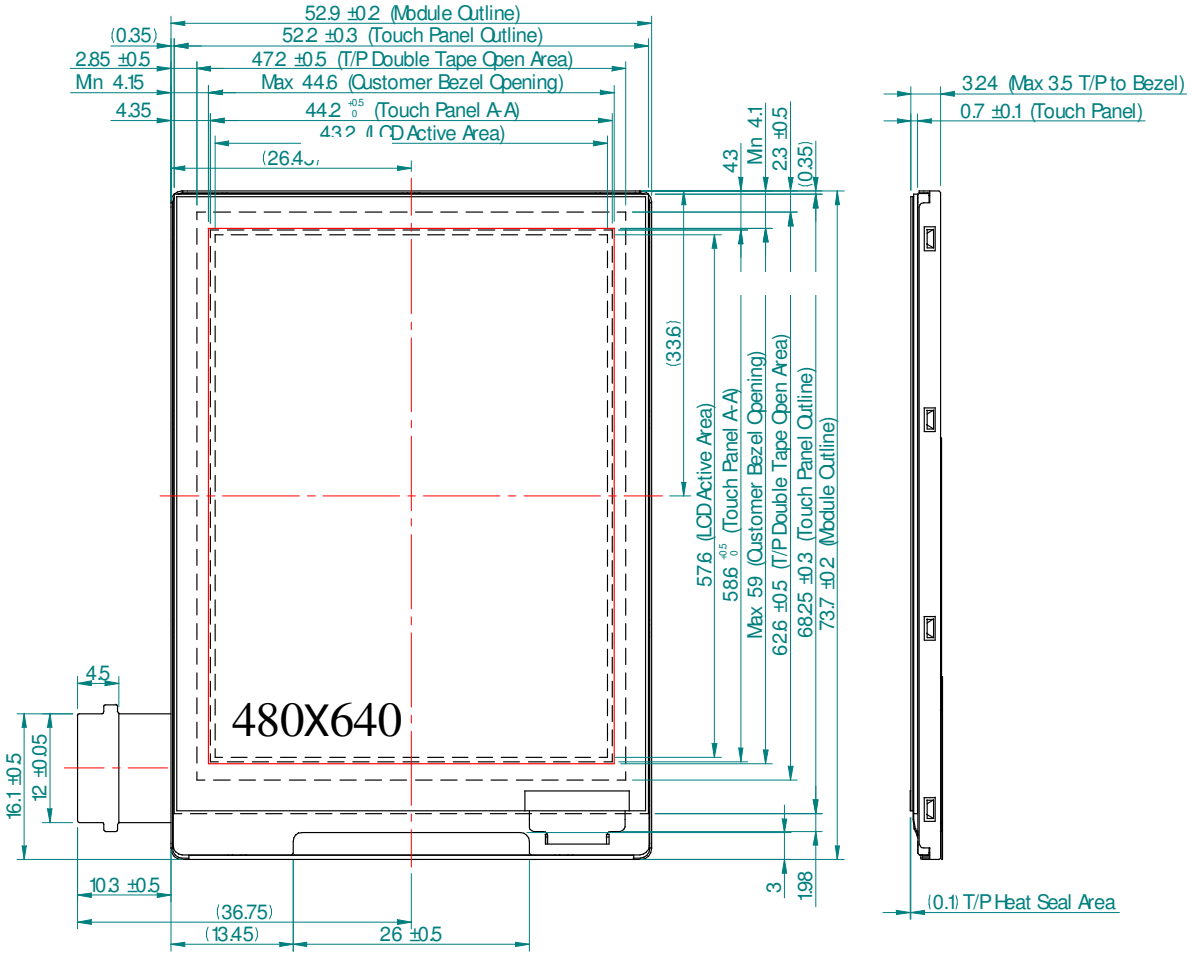


Drawing 1



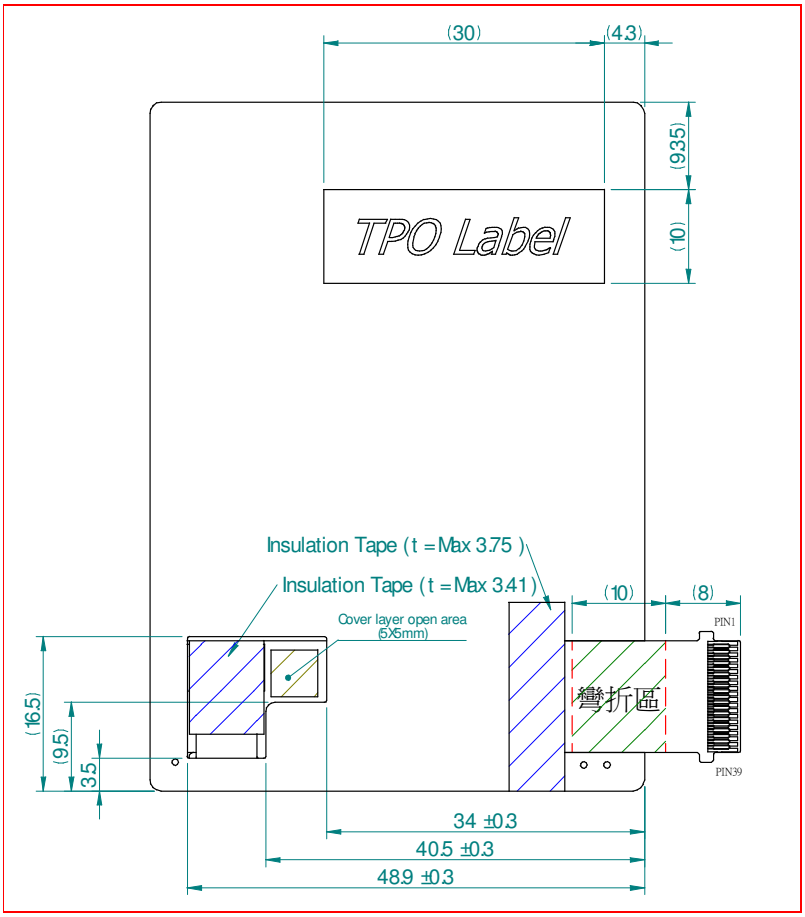
Drawing 2

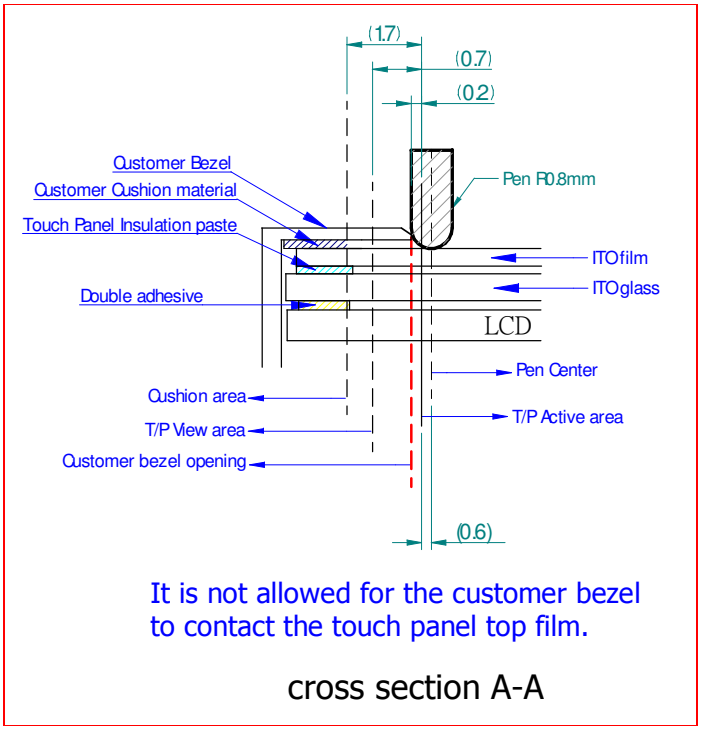
13 MECHANICAL DRAWING



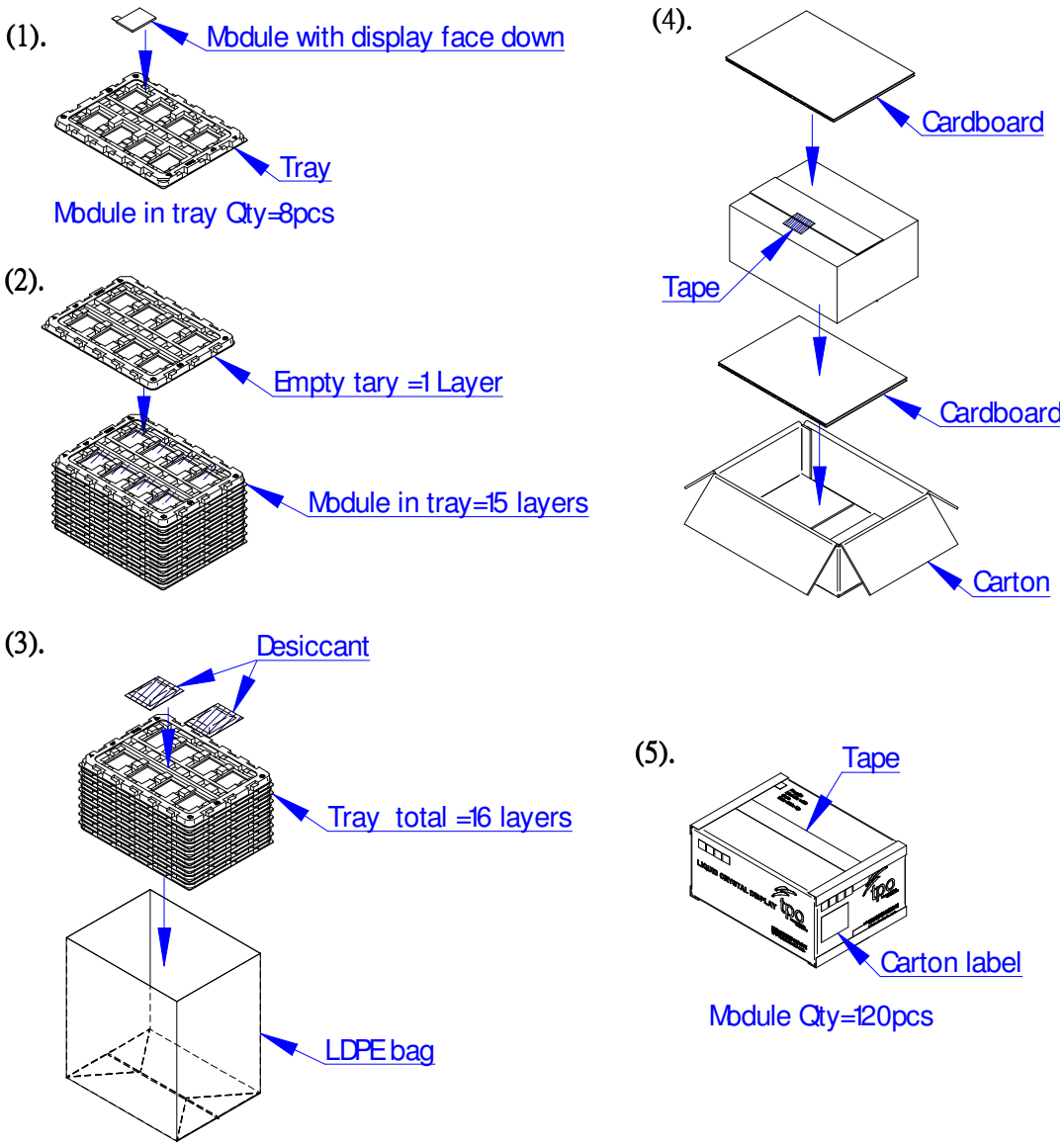
Note:

1. Please design the bezel not to contact with the T/P upper electrode film. Otherwise, T/P may input incorrectly by giving the force to the bezel, and we recommend using the bezel material which is hard to bend.
2. The tolerance of module height is excluded warp of the shield case and the FPC.
3. Please design the bezel cushion within the T/P double tape area.
4. The dimension without tolerance is for reference only.
5. Recommend connector: FH23-39S-0.3SHW(05), HIROSE





14 PACKING DRAWING



2.8" module (TD028TTEC1) delivery packing method

(1). Module packed into tray cavity (with Module display face down).

(2). Tray stacking with 15 layers and with 1 empty tray above the stacking tray unit.
2pcs desiccant put above the empty tray

(3). Stacking tray unit put into the LDPE bag and fix by adhesive tape.

(4). Put 1pc cardboard inside the carton bottom, and then pack the package unit into the carton. Put 1pc cardboard above the package unit.

(5). Carton tapping with adhesive tape.