Freescale Semiconductor
Application Note

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i.MX23 Layout and Industrial Design Guidelines

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This application note describes proper design, placement, and routing techniques for the i.MX23 applications processor.

Contents

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1 Planes

The PCB should use four or six layers, minimum.

1.1 Layer Stack-Up

The recommended four-layer PCB stack-up is as follows:

Layer 1 (top—i.MX23 location)—signal + ground plane fill
Layer 2 (inner)—complete ground plane, no signal traces
Layer 3 (inner)—power planes + few signal traces if necessary
Layer 4 (bottom)—signal + ground plane fill

The recommended six-layer PCB stack-up is as follows:

Layer 1 (top—i.MX23 location)—signal + ground plane fill
Layer 2 (inner)—complete ground plane, no signal traces
Layer 3 (inner)—power plane + few signal traces if necessary
Layer 4 (inner)—signal
Layer 5 (inner)—complete ground plane, no signal traces
Layer 6 (bottom)—signal + ground plane fill

1.2 Ground Plane

Use at least one internal ground plane. Do not split the ground plane into analog and digital sections.

1.3 Power Plane

Split the power plane layer into separate VDDD (digital core), VDDA (analog supply), and VDDIO (digital I/O supply) planes.

1.4 Chassis Ground Ring

Create a chassis ground ring around the entire perimeter of the PCB. The chassis ground ring should be a minimum of 1.27 mm (50 mils) thick, if possible, and be routed on all layers. On top and bottom layers, the solder mask should be cleared from the ground ring.

Figure 1 shows a chassis ground ring example.

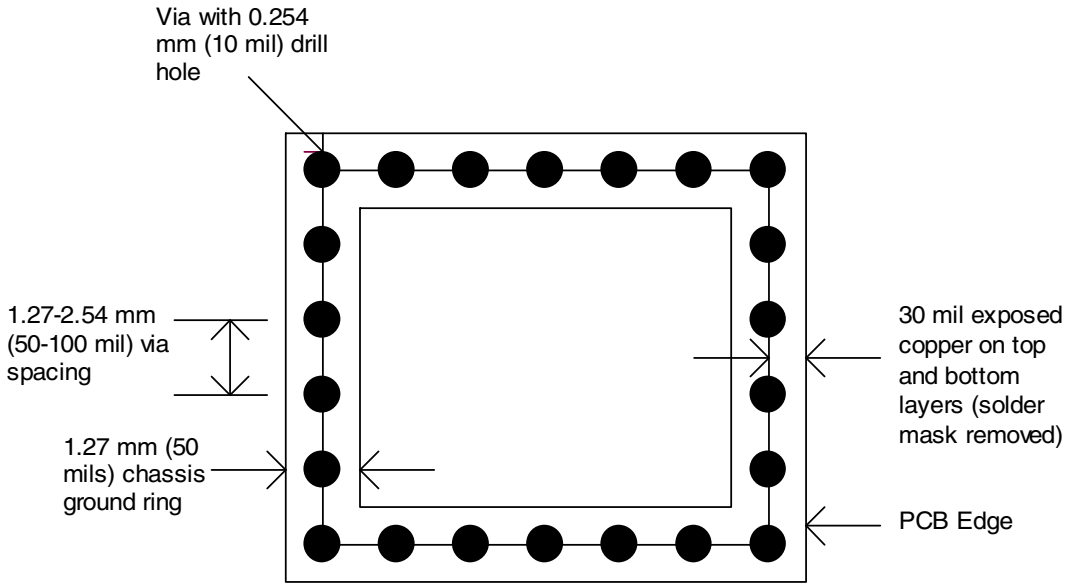

Figure 1. Chassis Ground Ring Example

2 DC-DC Converter

2.1 Vias

- Use at least two ground vias immediately next to the DCDC_GND ball. The DCDC_GND pin switches a large current at a high frequency; decreasing the impedance to the ground plane reduces DCDC converter noise and increases stability.
- Make sure the DCDC_GND pin has a good low impedance connection to the other i.MX23 ground pins. If a voltage difference is created between the DCDC_GND pin and the other i.MX23 VSSS pins, the system may be more susceptible to ESD failure.
- The power inductor traces should be 15-20 mils thick and should not use vias. If, for some reason, the power inductor cannot be placed on the same side of the PCB as the i.MX23, then multiple vias should be used to connect the inductor to the i.MX23 DC-DC converter pins.

2.2 Minimize Switching Current Loops

The DCDC converter switching current loops should be kept as small as possible to reduce the radiated emissions.

This can be accomplished by making sure the following layout rules are followed:

- Place the DCDC_BATT pin input capacitors as close as possible to the DCDC_BATT pin (less than 5 mm away).
- Place the DCDC inductor as close as possible to the DCDC_LP and DCDC_LN1 pins.
- Route the inductor traces close together.

- Place the DCDC output capacitors as close as possible to their respective DCDC output pins (less than 5 mm away): DCDC_VDDIO, DCDC_VDDA, DCDC_VDDD.
- Place the ground connections of the DCDC_BATT input capacitors as close as possible to both the DCDC_GND pin and the ground connections of the DCDC output capacitors.
- Place the ground connections of the DCDC output capacitors as close as possible to both the DCDC_GND pin and the ground connections of the DCDC_BATT pin input capacitors.

Figure 2 illustrates the current loop during inductor charging and discharging.

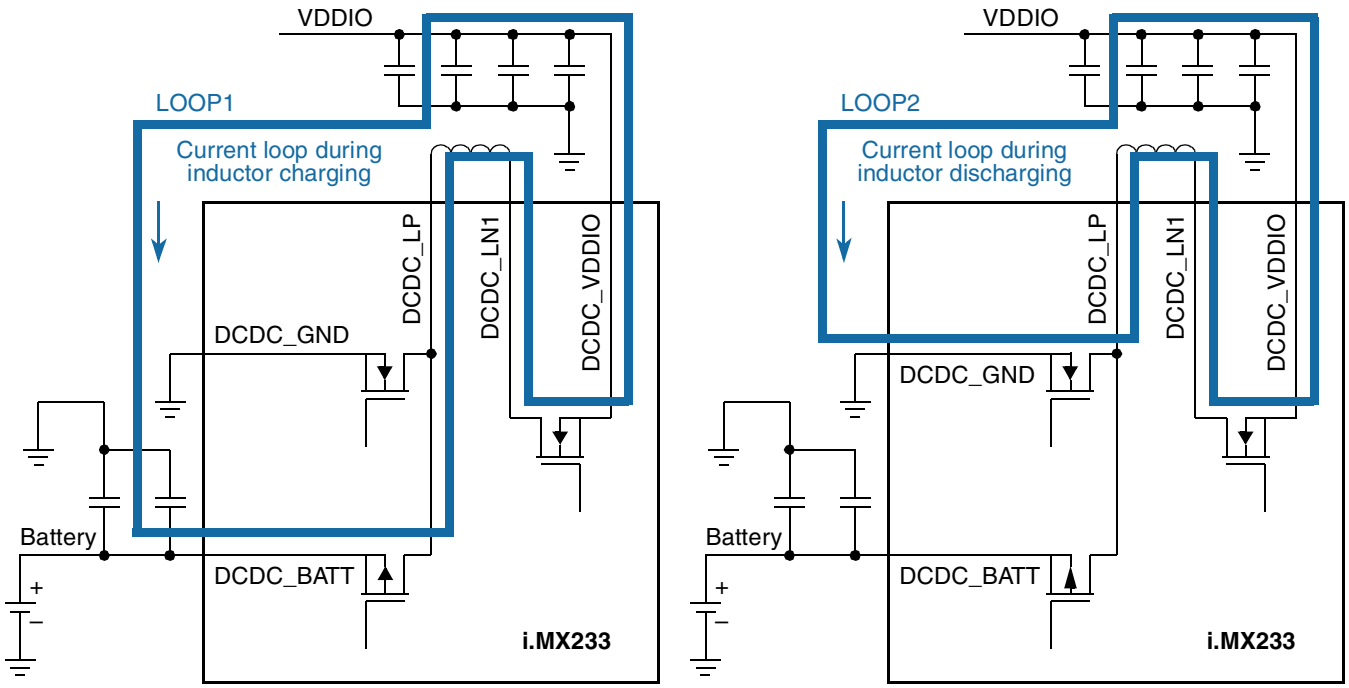

Figure 2. Current Loop During Inductor Charging and Discharging

2.3 Battery Connection

- Route the positive battery terminal on the power plane layer using a minimum trace width of 30 mils (0.762 mm). A thicker trace may be required for longer battery trace runs.
- Connect the negative battery terminal directly to the ground plane(s) using multiple thermal reliefs (three or more). Use multiple vias (three or more) near the thermal reliefs to connect the negative battery terminal to the ground plane layer and ground fill on the opposite side of the PCB.
- Try placing the negative battery terminal close to the DCDC_GND pin if possible. This reduces the length of the DCDC switching current ground return path and reduces overall PCB noise.

3 DRAM

3.1 DRAM Supply Decoupling

Each i.MX DRAM supply ball or pin must have its own via. The via must connect to a broad power plane which has (if possible) capacitors for each via—the more capacitors the better.

The most critical issue is NOT the timing. It is GND bounce or noise due to badly supplied i.MX DRAM supply pins. Something as simple as the layout engineer using too few vias to connect the i.MX DRAM supply pins may cause the DRAM memory interface to fail.

3.2 Routing

The DRAM traces should be routed as short as possible to reduce trace capacitance.

Route the DRAM DATA, DQMs and STROBE traces as equally as possible in terms of number of vias and used layers. In other words, use the same number of vias and route the traces on the same layers.

Matching the numbers of vias and layers used is more important than matching the trace length.

3.3 Minimizing Reflections

Keep the DRAM DATA, DQM, STROBE, and CLOCK traces short enough so that a maximum of 30% of the edge appears on the trace. Thus, in equation form,

$$\text{Trace Length} \leq (0.3 \times \text{Rise/Fall Time} \times 15\ \text{cm/ns}).$$

The speed of a signal edge traveling from sender to receiver on widely used FR4 material is about 1/5 the speed of light (or 15 cm/ns).

The full reflection occurs if the time for an edge travelling from sender (i.MX) to receiver (DRAM) is ≥ the rise/fall time of the signal. Example:

> If the rise/fall time = 0.5 ns and trace length = 7.5 cm, the receiver still sees “0 V” even though the sender is now driving at the maximum DRAM supply voltage. Because the full edge is now on the line, full reflection occurs.
>
> So for this example, the signal traces should not exceed 2.25 cm (30% of 7.5 cm). This is valid for the distance between one sender and one receiver.

Note that this example calculation is for a point-to-point connection. If more than one memory device is connected to the bus, the rise/fall time is slower, and the trace length may be longer.

Control signals like CS, ADDRESS, RAS, CAS, and WE are not critical and can be routed without these constraints.

3.4 Routing to Multiple DRAM Devices

In terminated systems, “daisy chain” routing is recommended because the impedance can be matched along the whole trace. In nonterminated systems, “Y” routing is much better because it makes the trace lengths shorter, which reduces the capacitive loading.

For a design with 4 DRAM devices attached to the clock, the first two DRAMs should be routed as a “Y” and the other two as “daisy chain.”

4 Analog and Audio

Place analog components (line-in, headphone, LRADC, video DAC) in a section of the PCB that is isolated from digital components and traces.

4.1 Headphone

- For best audio quality, route the audio signals (HPR, HPL, and VGND) at least 8 mm away from any high-speed or noisy signals (for example, NAND Flash data and control signal lines, LCD signals, the DRAM bus, the crystal oscillator circuit, the DC-DC converter).
- Headphone jack components should be placed and routed as close as possible to the headphone jack.
- Place the i.MX23 VAG pin capacitor as close as possible to the pin. Improper routing of this capacitor can decrease the THD and SNR performance.
- The VSSA1, VSSA2, and VSSA5 pins should be connected to the ground plane with a via right next to the pin.

4.2 Speaker Amplifier (169-BGA Package Only)

- The i.MX23 speaker amp pins (SPEAKERP / SPEAKERN) should connect directly to a 8-Ω or 4-Ω speaker. No external components are required. Optionally, ferrite beads can be connected in series with the speaker signal lines to suppress ESD events and radiated emissions. If used, they should be placed as close as possible to the speaker connector.
- The speaker connector and speaker amp traces should be placed and routed in the analog section of the PCB. Avoid routing the speaker amp traces close to digital components and traces.
- Care should be taken to ensure the speaker amp traces are routed thick enough to minimize power loss. The peak speaker amp current can reach 1 A. For example, a PCB trace resistance of 200 mΩ can cause a 5% power loss when driving a 4-Ω speaker. The copper weight, temperature, and routing distance all have an effect on the PCB trace resistance. The following formula can be used to calculate the resistance of a copper PCB trace:

  Trace Resistance = Copper Resistivity × (Length / (Thickness × Width)) × (1+ (Copper Temp_Co × (Temp – 25)))

  Copper Resistivity = 1.7E-6 Ω-cm

  Copper Temp_Co = 0.00393 (per °C)

4.3 Video DAC

- The only external component required for the i.MX23 video DAC circuit is a 50-pF capacitor between the VDAC trace and ground.
- The video DAC signal trace should be routed with 75-Ω impedance with respect to the video DAC ground.

- The video DAC ground trace/plane should be routed as a star connection to the capacitor attached to the VAG pin.
- The two layout requirements above can be accomplished by routing the VDAC trace above a video DAC ground plane/trace (to achieve 75-Ω impedance) connected between the RCA jack ground and VAG capacitor ground.

4.4 Crystal

- Place the crystal and load capacitors as close as possible to the XTALI and XTALO pins.
- Place the VDD_XTAL capacitor close to its pin, and ground the capacitor away from digital traces.

5 USB

- USB signal lines should be routed on top or bottom layers to meet the 90-Ω differential impedance requirement.
- Using the recommended 6-layer stack-up allows the power planes and signal traces to all be adjacent to a ground plane. This improves the signal integrity of high speed signals and reduces radiated emissions.
- Maintain parallelism between USB differential signals for the trace routing needed to achieve 90-Ω differential impedance between D+ and D-. Slight deviations normally occur due to package and USB jack footprints, as well as routing to connector pins. The number and length of the deviations are kept to a minimum.
- Use an impedance calculator to determine the trace width and spacing required for the specific board stack up and material being used.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines, to minimize crosstalk. High speed and periodic signals should be kept at least 50 mils away from USB D+/D-.
- All other signals should be kept at least 20 mils away from the high-speed USB signal pairs to help prevent crosstalk.

5.1 Common USB Routing Mistakes

- Stubs—Avoid creating unnecessary stubs by placing any component footprints over the path of the data traces. If a stub is unavoidable in the design, no stub should be greater than 200 mils in length.
- Crossing a plane split—The USB data lines should never cross a power or ground plane split. This causes unpredictable return path currents, which can cause signal quality failures as well as EMI problems.
- Failure to maintain parallelism—Failing to maintain parallelism causes impedance discontinuities that directly affect signal quality. It also contributes to the trace-length mismatch and causes an increase in signal skew.

6 ESD and Radiated Emissions

- Ideally, the PCB design should use six or more layers, with solid power and ground planes. With four layers, ESD immunity may be compromised.
- All components with ground chassis shields (HP jack, USB jack, buttons, and so on) should connect the shield to the PCB chassis ground ring.
- Ferrite beads should be placed on each signal line connecting to an external cable (for example, USB or headphones). These ferrite beads must be placed as close to the jack as possible.
- Ferrite beads should NOT be placed on the USB D+/D- signal lines, because this can cause USB signal integrity problems. For radiated emissions problems due to USB, a common mode choke may be placed on the D+/D- signal lines. However, in most cases, it should not be required if the PCB layout is satisfactory. Ideally, the common mode choke should be approved for high speed USB use or tested thoroughly to verify there are no signal integrity issues created.
- Ferrite beads should have a minimum impedance of 500 Ω at 100 MHz with the exception of the ferrite on USB_5V.
- For the headphone ferrites, DCR should be 0.4 Ω or less. For USB_5V ferrite, DCR should be less than 0.1 Ω.

7 Industrial Design

- Buttons or switches on the player case should be non-conductive.
- The USB jack should be covered by a non-conductive case or rubber plug.
- If metal or conductive player cases are used, they should be designed to allow equal charge distribution on all sides of the PCB.
- Air gaps between buttons and the player case should be kept as small as possible.
- Avoid using a headphone jack with a metal ring connected to the industrial design metal casing. When using direct drive headphone mode, this can short out the common mode amplifier.

8 Revision History

Table 1 provides a revision history for this application note.

Table 1. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	11/04/2009	Initial release.

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