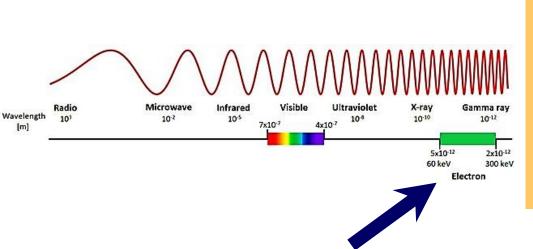
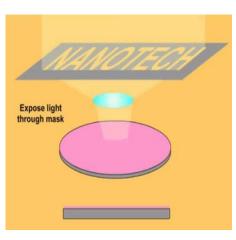
# Marker-Free Direct-Write Patterning of Transmon Chip

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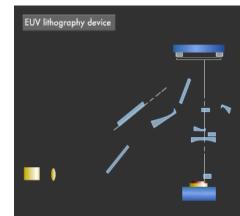
#### Background

- Conventional optical lithography = ultraviolet photon exposure.
- Electron beam lithography = electron beam exposure.
- Ultimately, the wavelength of the energy being applied to a resist coating determines the feature size.
- It's possible to obtain 3-5 nm resolution with electron-beam lithography
  - Depends on your <u>skill level</u> (abstract).

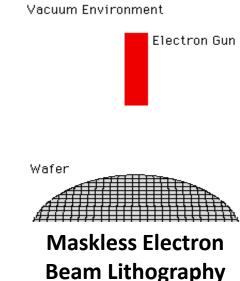




Maskless Ultraviolet Lithography



Maskless Extreme
Ultraviolet
Lithography



- 1. Venturi, PhD Thesis (2017)
- 2. Taken from: thumbs.gfy.com
- 3. Taken from: Wikimedia Commons

#### Equipment Advantages & Disadvantages

#### Advantages:

- Relatively high-resolution lithography.
- Maskless procedure allows for indirectly importing AutoCAD drawings.
- Fast design modification.
- Vacuum environment leads to better control of contamination.
- Markers can be avoided

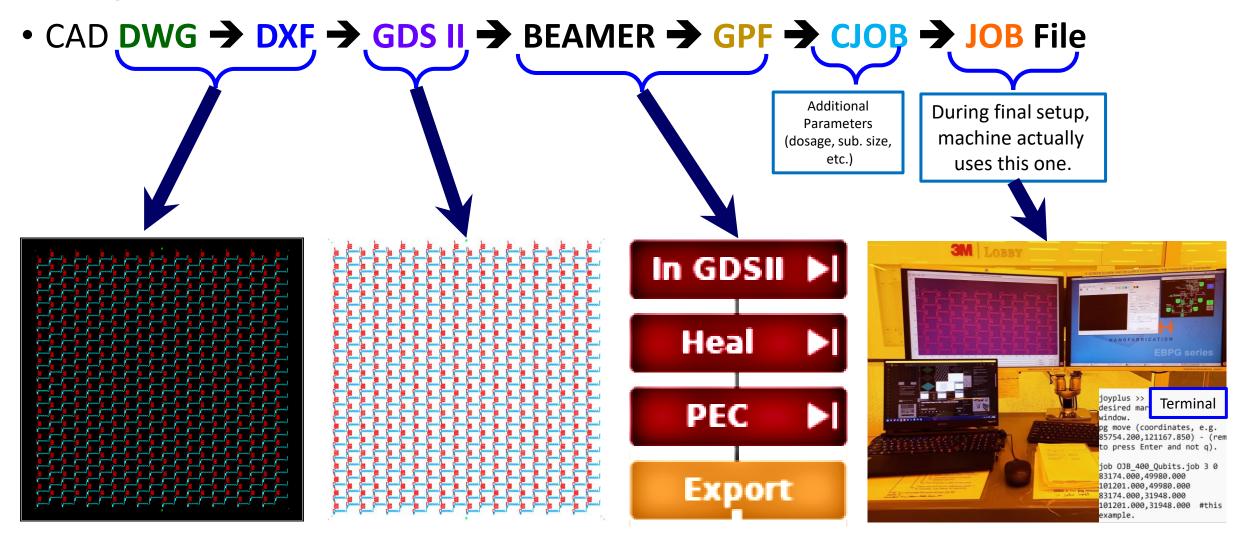
#### Disadvantages:

- Vacuum environment required.
- Charge build-up, even during SEM inspection.
- Low throughput.
- Proximity effects.



#### Design Process Flow to Test Pattern Quality

• Design file conversion is a bit extensive.



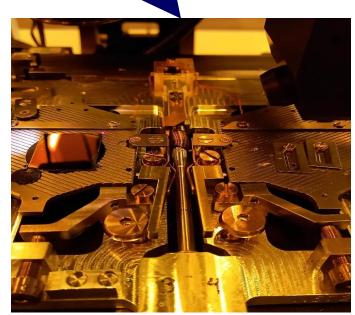
### Maskless Direct Writing Using "Joyplus"

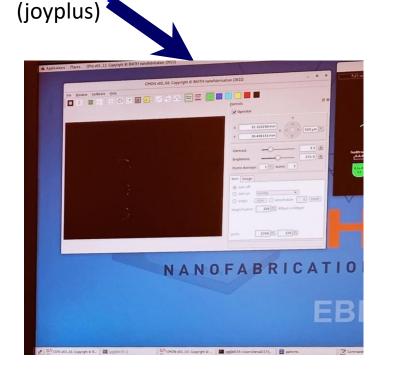
- Doses:
  - For relatively larger features (pads & stripes):  $450 \mu C/cm^2$ .
  - For smaller features (pillars): 825-875 μC/cm<sup>2</sup>.
- Basically:

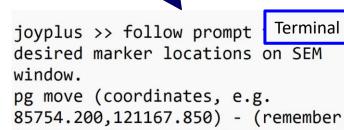
• Locate 4 Points - SEM-Aided 'Marker' Location - Record Final Marker Position - &











to press Enter and not q).

job OJB\_400\_Qubits.job 3 0 83174.000,49980.000 101201.000,49980.000 83174.000,31948.000 #this is an example.



### Basic Flow Summary of "Joyplus" for E-Beam

- Enter relative coordinates >> locate desired marker reference points >> record real coordinates found >> enter (pg move position) of real coordinates >> type (joyplus) >> confirm real coordinates of marker locations by inspecting SEM scan >> press Enter.
- You may now continue with job file locations and other parameters for stage selection >> copy-paste job command into teminal >> press Enter >> watch 1st few steps of exposure >> Done!

### **Stack Composition**

E-Beam Resist

Hardmask (15 nm)

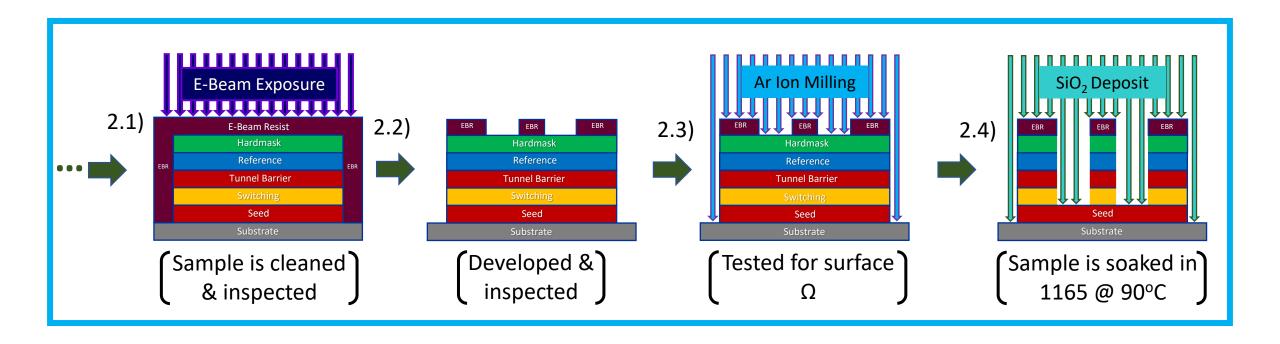
Metal Stack (X nm)

Substrate

# Sample can contain any stack (deposited on substrate) for hardmask testing purposes

Hardmask layer will help us reduce or increase the density of device drive lines & other fine features as needed.

#### Generic E-Beam Patterning Flow for Tunnel Junction

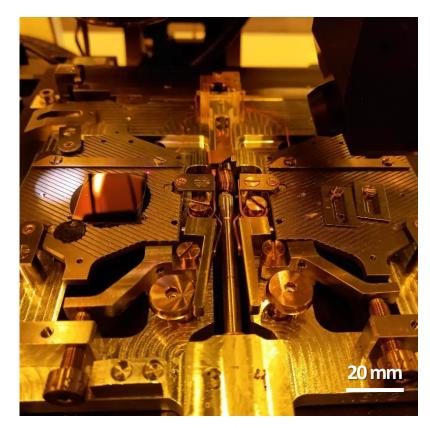


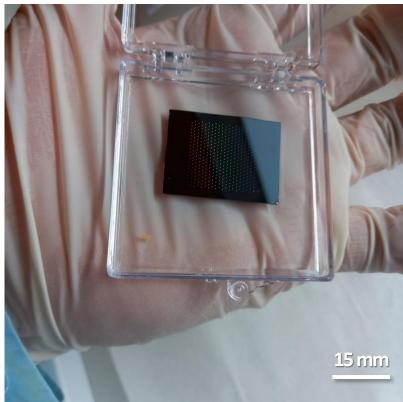
Seed layer doubles as an adhesion layer

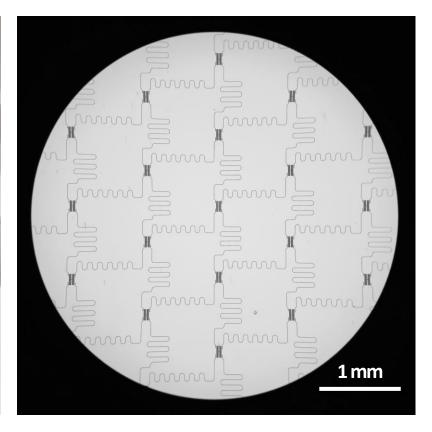
PR: Photoresist  $\Omega$ : Resistance

EBR: Electron-Beam Resist 1165: Strong Solvent

#### Results







On the sample stage, carbon tape is being used to prevent charge build-up

## Results (Continued)

