Marker-Free Direct-Write Patterning of Transmon Chip

Onri Jay Benally
University of Minnesota
Department of Electrical & Computer Engineering
Principal Investigator: Prof. Jian-Ping Wang

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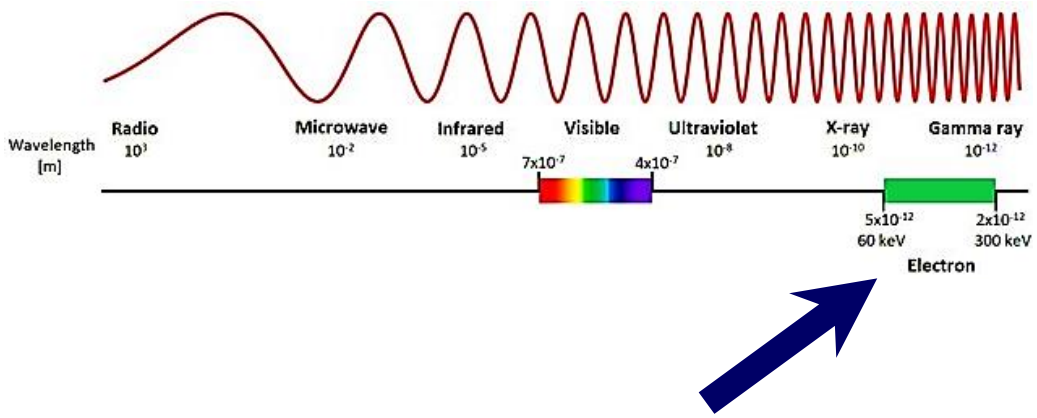
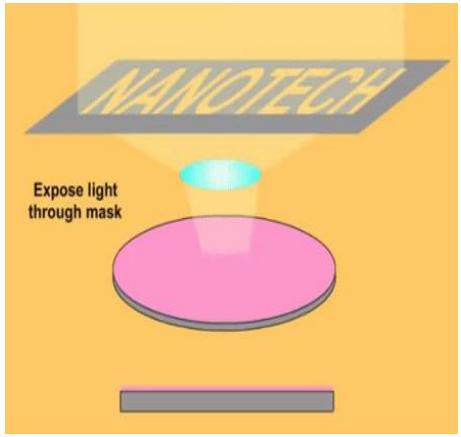
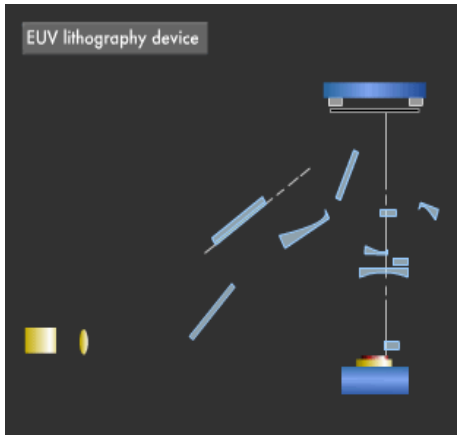
Background

- Conventional optical lithography = ultraviolet **photon** exposure.
- Electron beam lithography = **electron** beam exposure.
- Ultimately, the *wavelength* of the energy being applied to a resist coating determines the feature size.
- It's possible to obtain 3-5 nm resolution with electron-beam lithography
  - Depends on your skill level (abstract).

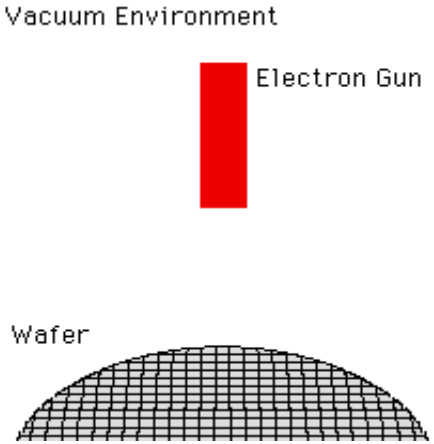




Maskless Ultraviolet Lithography



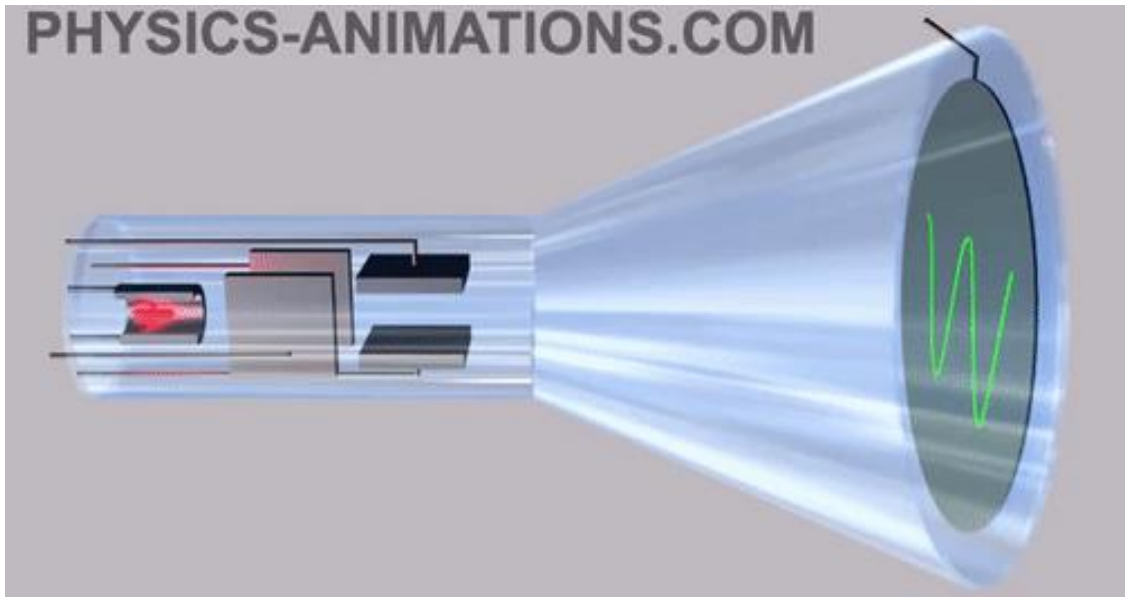
Maskless Extreme Ultraviolet Lithography

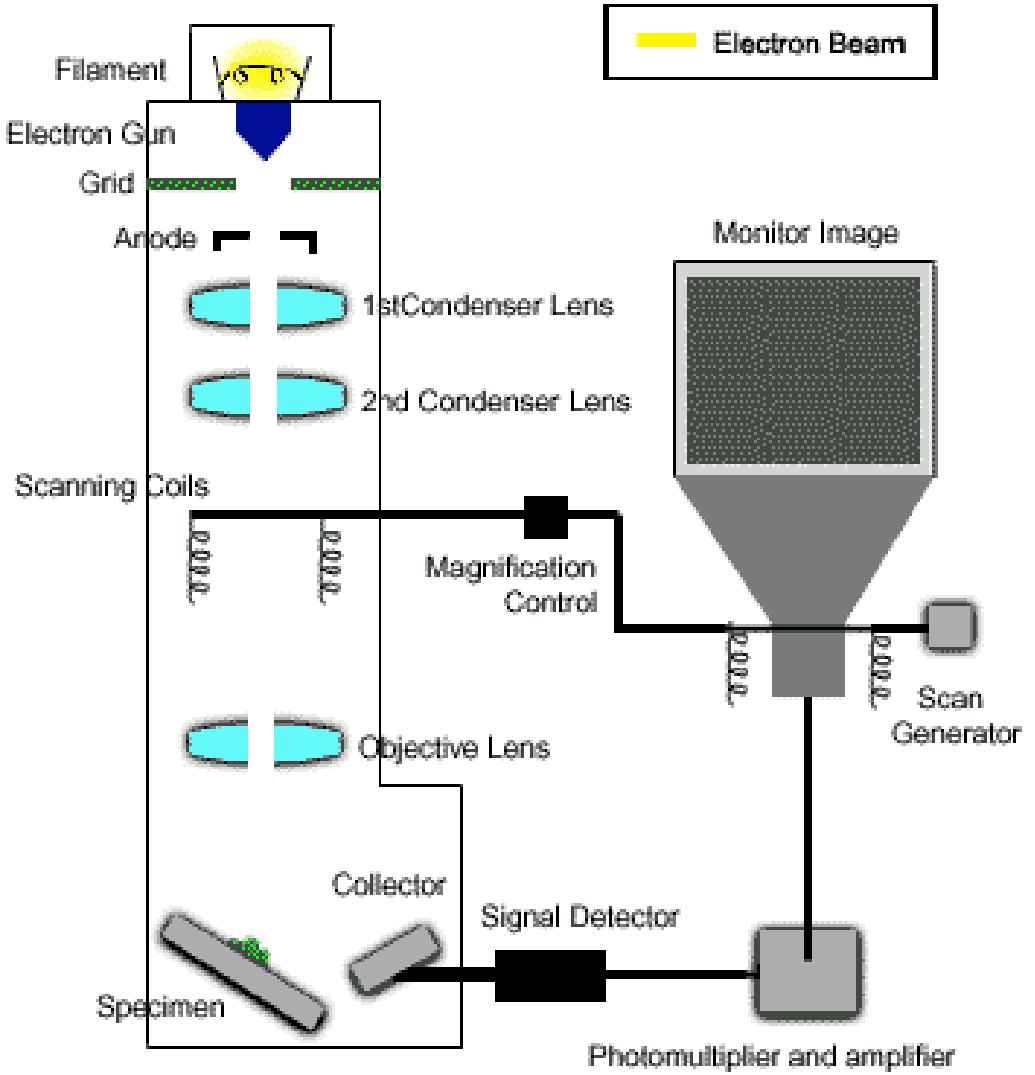


Maskless Electron Beam Lithography

1. Venturi, *PhD Thesis* (2017)
2. Taken from: thumbs.gfy.com
3. Taken from: *Wikimedia Commons*

Bonus: Basic Operating Principle of Electron-Beam-Based Technology





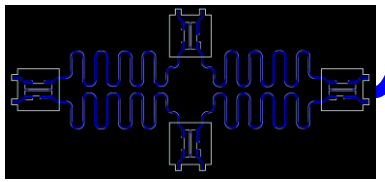
1. Taken from: *Wikimedia Commons*
2. Taken from: makeagif.com

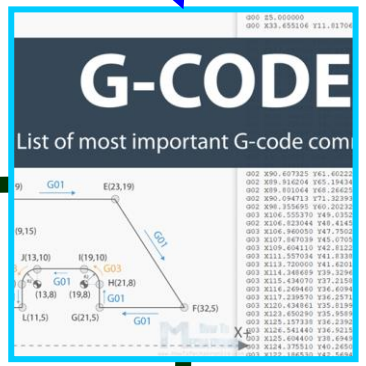
Equipment Advantages & Disadvantages

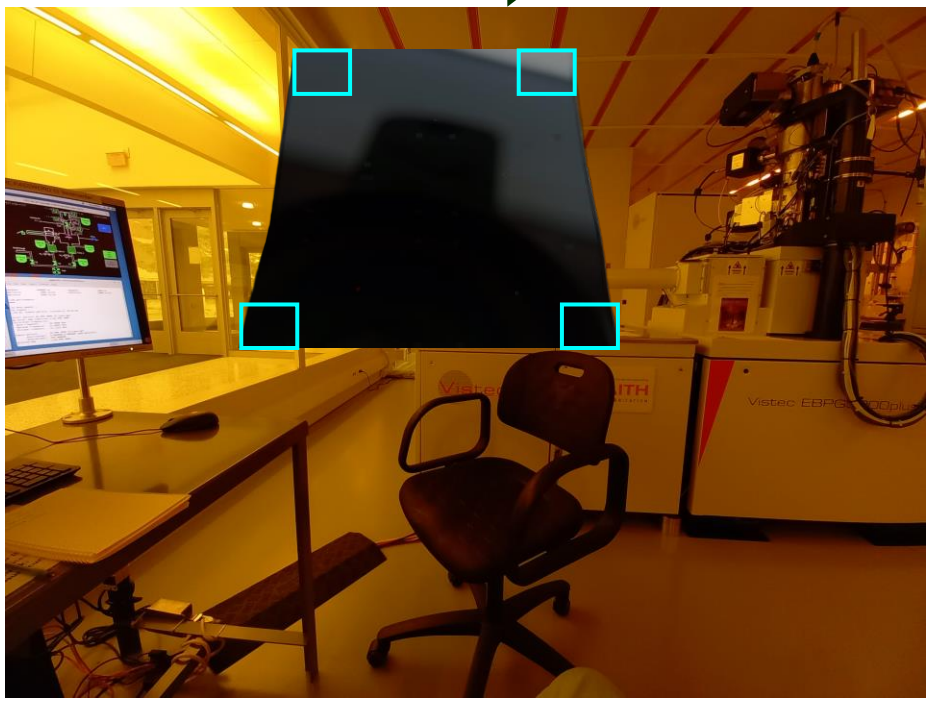
- Advantages:
  - Relatively high-resolution lithography.
  - Maskless procedure allows for indirectly importing AutoCAD drawings.
  - Fast design modification.
  - Vacuum environment leads to better control of contamination.
  - Markers can be avoided.
- Disadvantages:
  - Vacuum environment required.
  - Charge build-up, even during SEM inspection.
  - Low throughput.
  - Proximity effects.

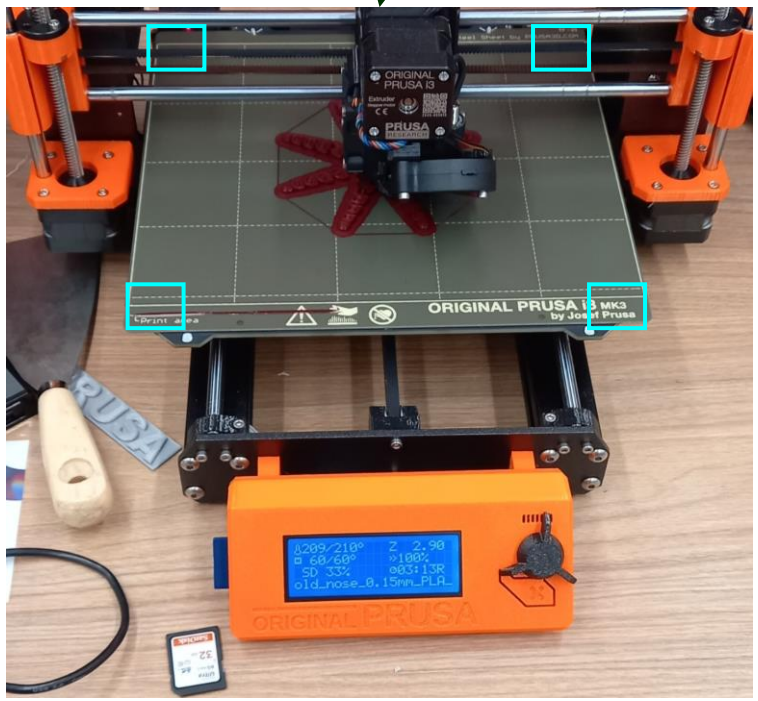
E-Beam vs. 3D Printing vs. CNC Machining

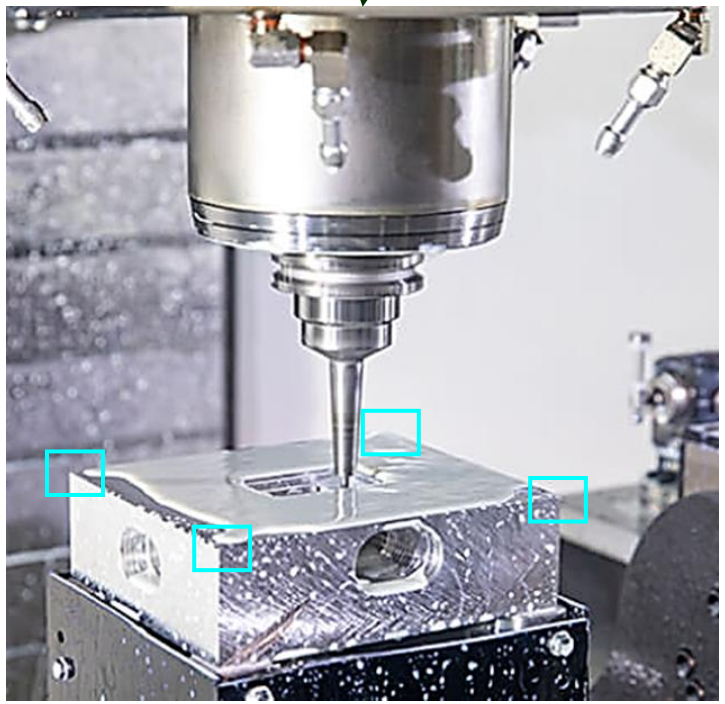
- Similarities:
  - Uses of a type of **G-CODE** or coordinate system.
  - Initial preparation procedure (pick reference points).
  - CAD **DWG** → **DXF** → "the **G-CODE**".











*E-Beam = Electron-Beam
**CNC = Computer Numerical Control
*3D = 3 Dimensional

1. Taken from: howtomechatronics.com
2. Taken from: protolabs.co.uk

Design Process Flow to Test Pattern Quality

- Design file conversion is a bit extensive.
- **GDS II** ➔ CAD **DXF** ➔ **GDS II** ➔ **BEAMER** ➔ **GPF** ➔ **CJOB** ➔ **JOB** File

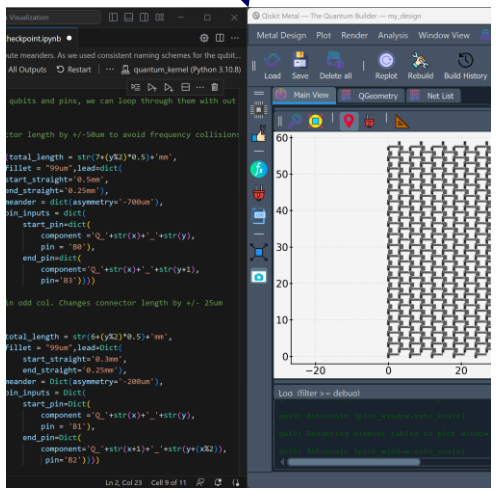
Export GDS file from Qiskit Metal.

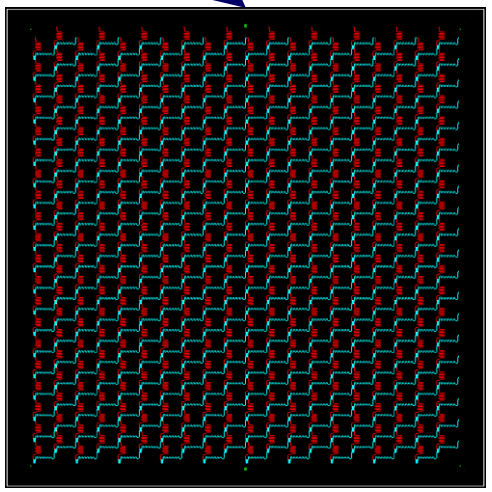
For modifiable polygons & layer separation. (Pattern editors allow GDS-to-DXF conversion & some degree of layer separation).

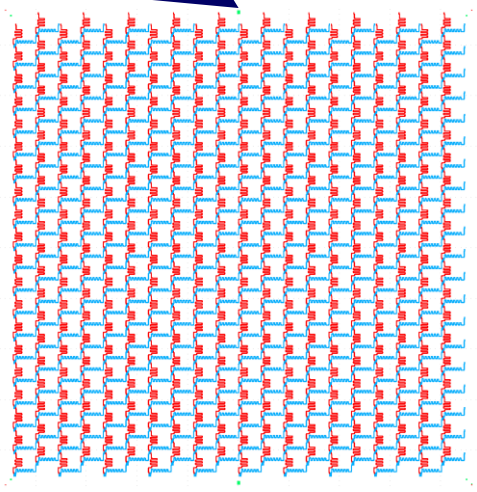
At this point, each layer should be labeled based on their feature sizes, ready for lithography software.

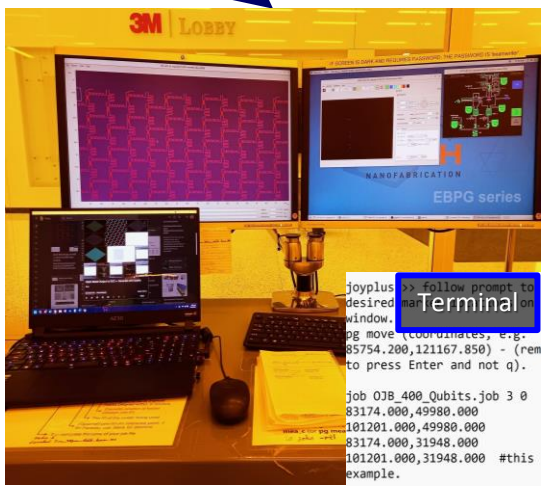
Additional Parameters (dosage, sub. size, etc.)

During final setup, machine actually uses this one.







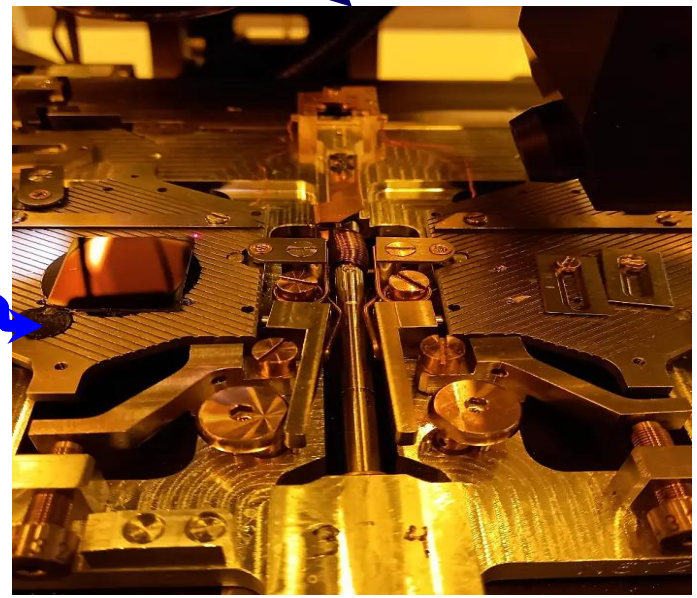


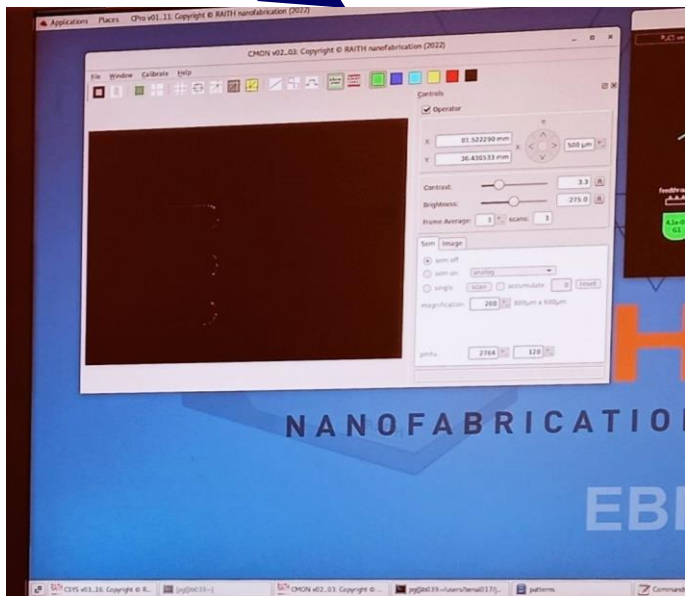
Maskless Direct Writing Using “Joyplus”

- Doses:
  - For relatively larger features (**pads** & **stripes**): 450 µC/cm^2.
  - For smaller features (**pillars** & **junctions**): 825-875 µC/cm^2.
- Basically:
  - Locate 4 Points ➔ SEM-Aided ‘Marker’ Location ➔ Record Final Marker Position ➔ **Confirm & Write!**

(joyplus)

Conductive carbon tape





Terminal

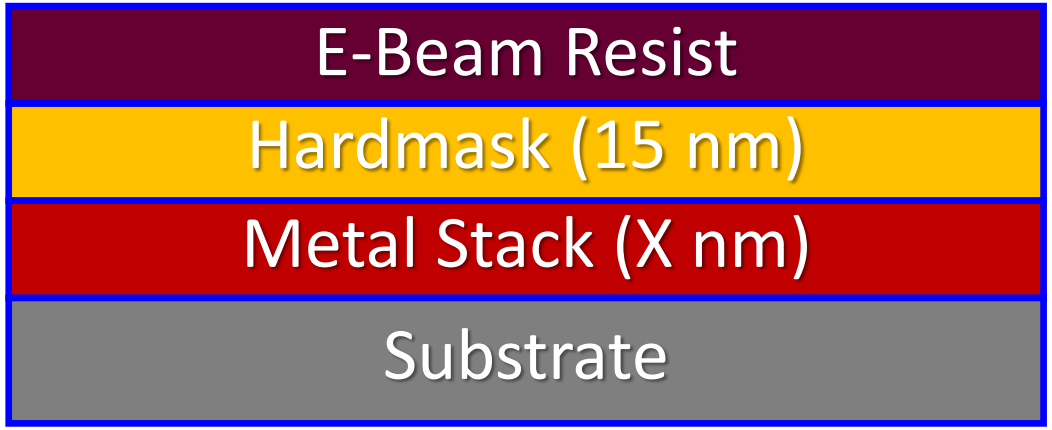
```
joyplus >> follow prompt to center
desired marker locations on SEM
window.
pg move (coordinates, e.g.
85754.200,121167.850) - (remember
to press Enter and not q).

job OJB_400_Qubits.job 3 0
83174.000,49980.000
101201.000,49980.000
83174.000,31948.000
101201.000,31948.000  #this is an
example.
```

Basic Flow Summary of “Joyplus” for E-Beam

- Enter relative coordinates >> locate desired marker reference points >> record real coordinates found >> enter (pg move position) of real coordinates >> type (joyplus) >> confirm real coordinates of marker locations by inspecting SEM scan >> press Enter.
- You may now continue with job file locations and other parameters for stage selection >> copy-paste job command into teminal >> press Enter >> watch 1st few steps of exposure >> Done!

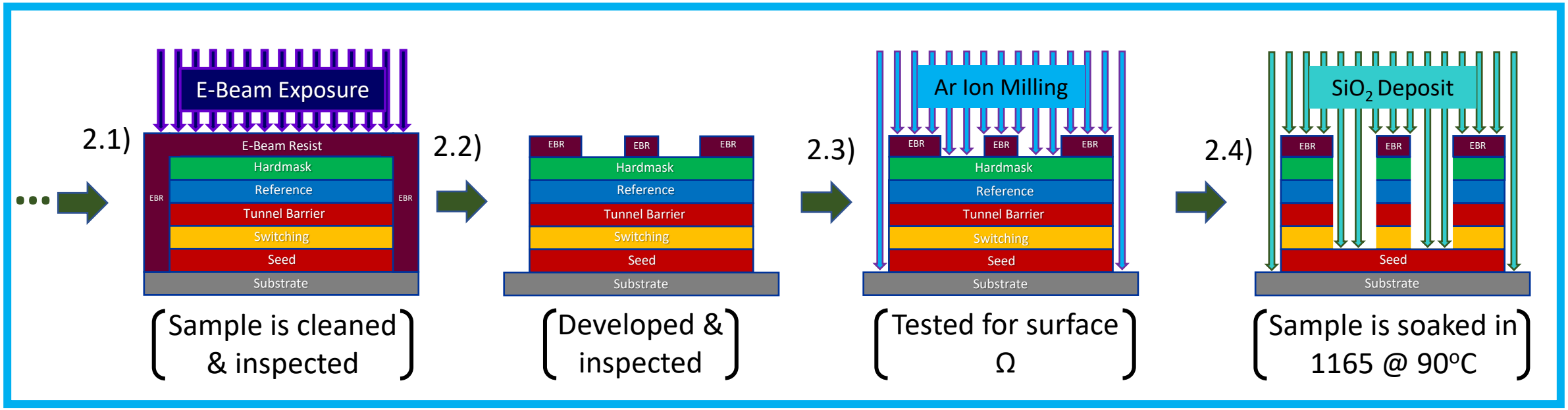
Stack Composition



Sample can contain any stack (deposited on substrate) for hardmask testing purposes

Hardmask layer can help reduce dimension size or increase the density of device drive lines & other fine features as needed.

Generic E-Beam Patterning Flow for Tunnel Junction



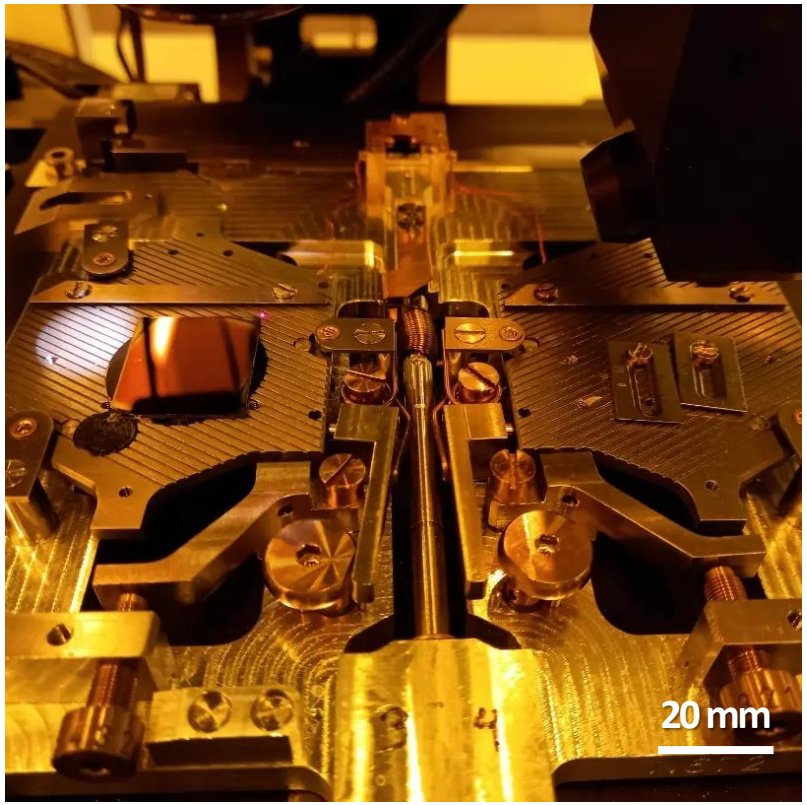
Here, the seed layer doubles as an adhesion layer

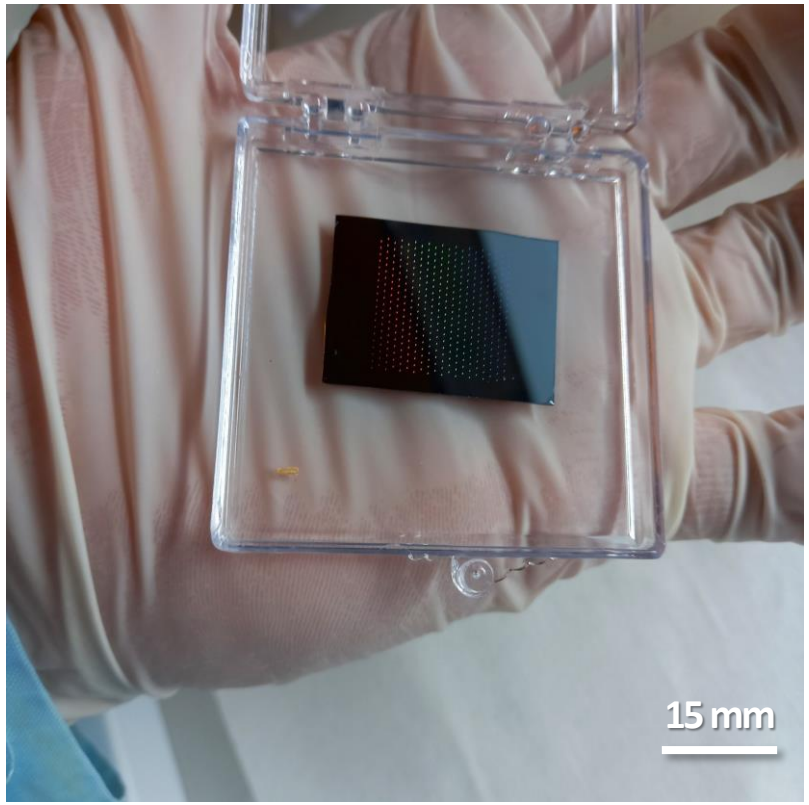
PR: Photoresist
Ω: Resistance

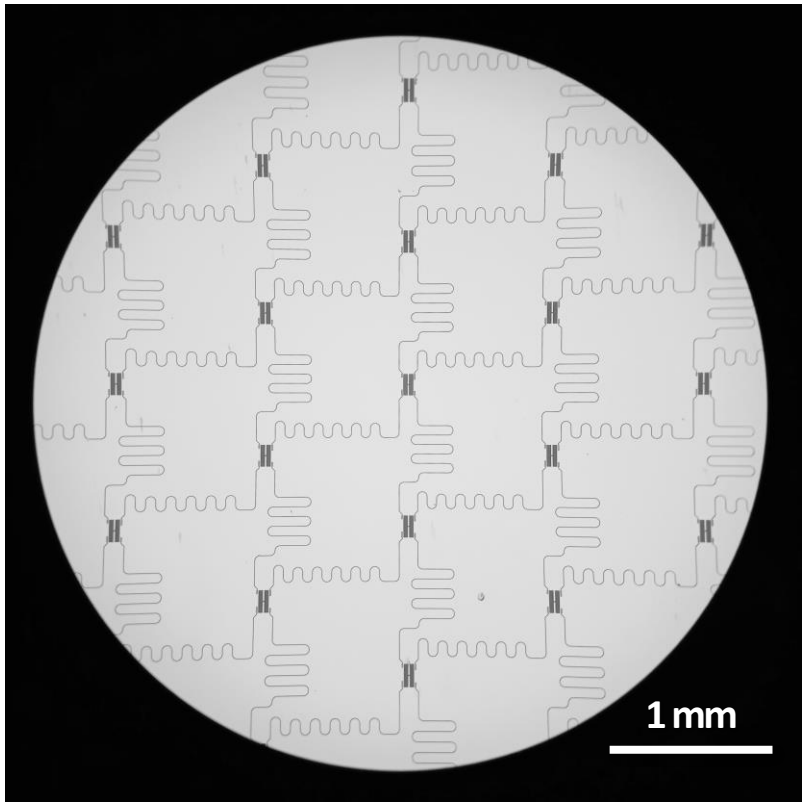
EBR: Electron-Beam Resist
1165: Strong Solvent

* For more details on basics of thin films for quantum chips, see "Onri's_Quantum_Hardware_Tutorial_Part_2_of_5" on GitHub.

Results







On the sample holder, conductive carbon tape is used to stick sample to grounded metal to prevent charge build-up. Charge build-up deflects the electron-beam & causes undesired patterns on the chip.

Results (Continued)