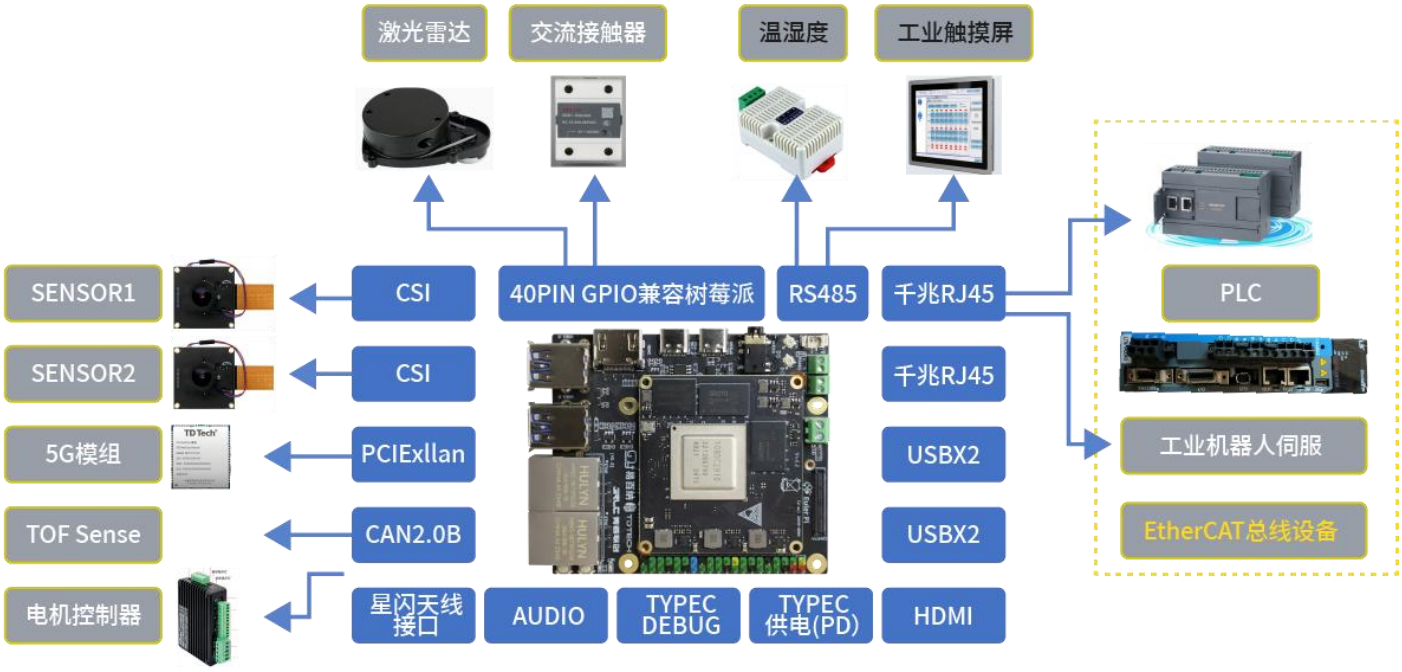
1. Product overview

1.1 Product Introduction

The main control chip of Seagull Pai development board SS928V100 has built-in quad-core A55, which provides efficient, rich and flexible CPU resources to meet customers' computing and control needs. Integrated single-core RISCV to meet some low delay scenarios.

The mainboard integrates common video hardware interface, and all peripheral interface circuits pass strict anti-interference test to make the product have good performance in EMC and stability; use the system software (Linux system) with stability test and depth optimization, support the industry mainstream deep learning framework, and provide comprehensive platform development and compilation tools. The hardware block diagram is shown below:



Seagull School development board adopts the composition mode of core board and bottom plate, and connects with PC through serial port and network port line to form a basic development system. To achieve a more complete development system or demonstration environment.

1.2 Product Configuration

- RAM: onboard 4GB LPDDR4X (optional 8GB)
- ROM: Onboard 32GB EMMC5.1 (optional 64GB / 128GB)
- Support 2-road gigabit network ports

- The MIPI-CSI interface with multiple combinations of 2x4-Lane or 4x2-Lane (requiring expansion) supports up to 4 sensor parallel input
- Support for 1-channel HDMI 2.0 output
- Support single audio input / stereo output 1 each
- Support for a 4-way USB 3.0
- Support 1 PCIE interface, connected to 4G / 5G / NVME hard disk module
- Support 1 Debug debugging (Type_C),
- Power supply: 12V-2A, Type_C interface (PD power supply)
- Others: 1 FAN interface, 1 CAN interface, 1 RS485, reserved I2C / DTSI / GPIO / I2S and other interfaces

1.3 Application field

Seagull School development board is suitable for industrial automation, intelligent monitoring, robot control, intelligent home system, intelligent medical system, transportation system, embedded control system and other intelligent video processing terminals, which can fully meet the design requirements of new ultra-high definition visual perception and recognition system.

2. SS928 chip introduction

2.1 Chip function framework

Seagull Pai development board is SS928, which is a professional ultra HD intelligent network video recorder SoC launched for the market. The chip supports up to four-way sensor input, ISP image processing capability of up to 4K60, and supports 3 FWDR, multi-stage noise reduction, six-axis anti-shake, and hardware stitching.

Integrated with efficient image analysis tool reasoning unit, the highest 10.4Tops INT8 computing power, and support the industry mainstream image analysis tool framework. Built-in dual-core Vision DSP to meet some differentiated CV computing needs.

In addition, the bottom plate can be customized design, combined with SS928 core board, to meet the functional needs of users in different application scenarios, which can fully improve the development efficiency and support customers to rapid mass production of products.

2.2 Chip characteristic parameters

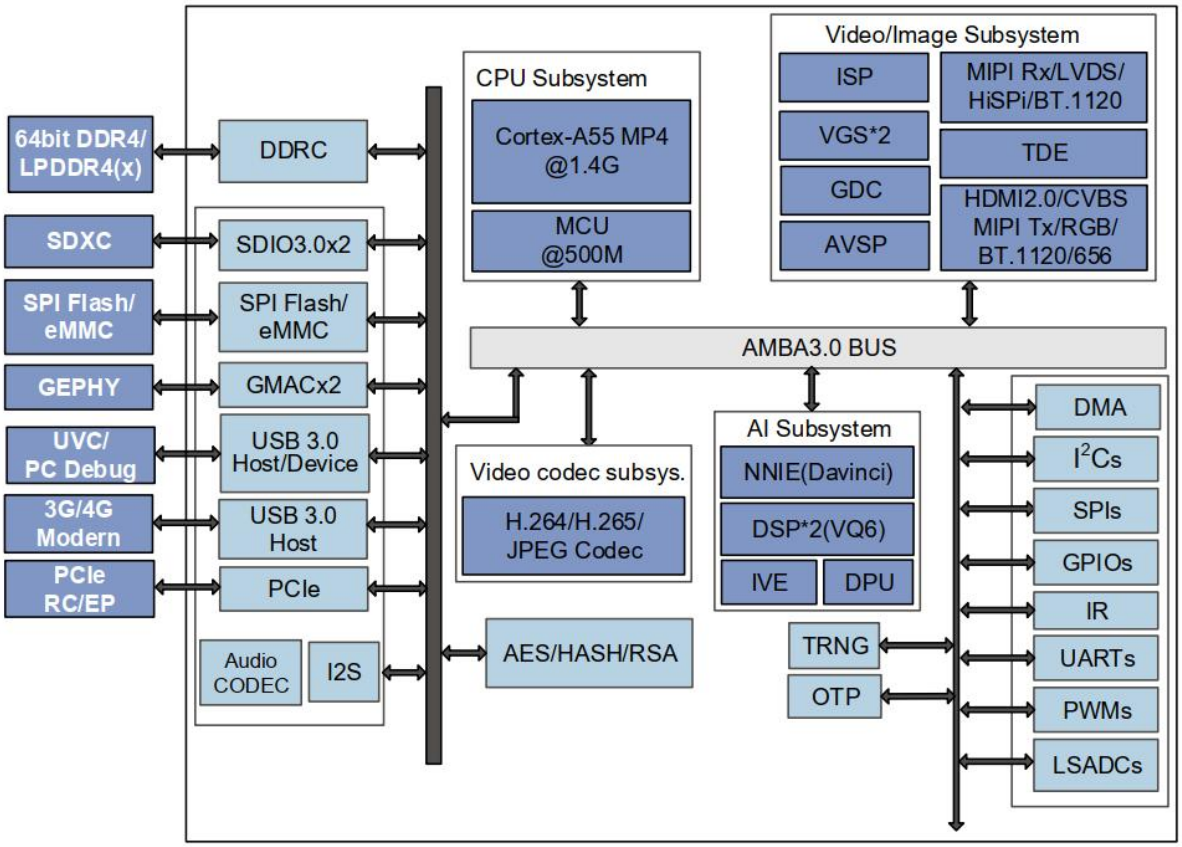
SS928 main features	Specific parameters
CPU	● Tetrinuclear ARM Cortex A55@1.4GHz ● – 32KB I-Cache, 32KB D-Cache /512KB L3 cache ● Support for Neon acceleration, integrated FPU processing unit ● Built-in at 32 bit MCU @ 500 MHz ● – 32KB I-Cache, 32KB D-Cache /64KB TCM
Intelligent video analysis	● Image analysis tool acceleration engine, up to 10.4Tops INT8 computing power Support for INT 4 / FP16 Support full API and tool chain, easy to customer development ● Dual-core Vision Q6 DSP – 32K I-Cache /32K D-Cache /32K IRAM/320K DRAM ● Built-in intelligent computing acceleration engine ● Built-in binocular depth acceleration unit

	● The built-in matrix calculates the acceleration cells
Video codec	● H.264 BP/MP/HP ● H.265 Main Profile ● H.264/H.265 The maximum codec resolution is 8192 x8192 ● H.264/H.265 Cocoding supports I / P frames ● H.264/H.265 Multicode stream encoding ability: – 3840 x 2160@60fps + 1280x720@30fps – 7680 x 4320@15fps ● H.264/H.265 / MPEG-4 Multi-decoding stream decoding capability: – 3840 x 2160@60fps + 1920x1080@60fps ● Support for precoding OSD stacking for up to 8 regions ● Support multiple bit rate control modes such as CBR / VBR / AVBR / FIX QP / QPMAP ● The maximum output bit rate is 100Mbps ● The 8 regions of interest (ROI) codes are supported ● Support for JPEG Baseline codec ● JPEG codec maximum resolution of 16384x16384 ● JPEG, the maximum performance Code: 3840 x 2160 @ 60 fps (YUV420) Decode: 3840 x 2160 @ 75 fps (YUV420)
Video input interface	● Support 8-Lane image sensor serial input, and support MIPI / LVDS / Sub-LVDS / HiSPi multiple interfaces ● Support multiple combinations of 2x4-Lane or 4x2-Lane, up to 4-channel sensor serial input ● Maximum resolution of 8192 x 8192 ● Support 8 / 10 / 12 / 14 Bit RGB Bayer DC timing video input, clock frequency 150 MHz ● support BT.601、BT.656、BT.1120 Video input interface ● Support for the mainstream CMOS level thermal imaging sensor
Digital Image Processing (ISP)	● ISP supports time-sharing multiplexing for multiple sensor input videos ● Support 3A (AE / AWB / AF) function, 3A control is adjustable by the user ● Support for de-fixed mode noise (FPN) ● Support for bad point correction, lens shadow correction; ● Up to three frames of WDR and Advanced Local Tone Mapping support ● Support multi-stage 3D denoising, image edge enhancement, defogging, dynamic contrast enhancement and other processing functions ● Support for 3D-LUT color adjustment ● Support lens distortion correction, support fisheye correction ● Support 6-DoF, digital stabilization and Rolling-Shutter correction ● Support image Mirror, Flip, 90 degree / 270 degree rotation ● Provide the PC-terminal ISP adjustment tool
Video and graphics handle	● Support graphics and image 1 / 15.5~16x zoom function ● Support for up to 4-road video panoramic splicing Enter 2 route 3840x2160 and output 4320x3840 Enter 4 routes 2688x1520 and output 6080x2688

	● Support for video layer, graphics layer superposition ● Support for color space conversion
Video output interface	● Support for HDMI 2.0 interface output ● Support 4-Lane Mipi DSI / CSI interface output, up to 2.5 Gbps / lane ● Built-in analog standard definition CVBS output ● Support for 8 / 16 / 24 bit RGB, BT.656、BT.1120 and other digital interfaces ● Also supports 2 independent HD video output Supports the non-homologous output of any two interfaces One way can support PIP (Piture In Piture) ● Maximum output capacity is 3840 x 2160 @ 60 fps + 1920 x 1080 @ 60 fps
Audio interface and processing	● Built-in Audio codec, supports 16bit voice input and output ● Support for the I2S interface Support multichannel TM transmission mode (TDM) ● Support for HDMI Audio output ● Multi-protocol voice codec is implemented through the software ● Supports audio 3A (AEC / ANR / ALC) processing ● support G.711/G.726 / AAC / other audio coding format
Security isolation with the engine	● Support safe start ● Support for the TrustZone-based REE / TEE hardware isolation scheme ● Hardware implements the AES symmetric encryption algorithm ● The hardware implements the RSA2048 / 3072 / 4096 signature verification algorithm ● The hardware implementation is based on SHA / 256 / 384 / 512 and HMAC _ SHA256 / 384 / 512 algorithms ● Hardware implementation of a random number generator ● Integrated 30Kbit OTP of storage space for customer use
network interface	● 2 gigabit Ethernet interfaces Supports both RGMII and RMII interface modes Support for TSO, UFO, COE and other acceleration units Support for Jumbo Frame
peripheral interface	● Support the upper power reset (POR) and external input reset ● Integrated 4-channel LSADC ● Multiple UART, I 2C, SPI, and GPIO interfaces ● 2 SDIO3.0 interfaces SDIO 0 supports SDXC card with a maximum capacity of 2TB SDIO 1 supports the docking of the wifi modules ● 2 USB3.0/USB2.0 interfaces The USB0 is the Host port only The USB1 Host / Device is switchable ● The 2-Lane PCIe2.0 high-speed interface The RC / EP mode is supported Be configurable as 2-Lane PCIe2.0 Configurable as 1-Lane PCIe2.0 + USB3.0
external memory interface	● The DDR 4 / LPDDR4 / LPDDR4x interface Support for 4 x 16bit DDR4

	Support for 2 x 32bit LPDDR4 / LPDDR4x The highest rate of DDR 4 was 3200Mbps The highest LPDDR4 / LPDDR4x rate was 3,733 Mbps Maximum capacity of 8GB ● The SPI Nor / SPI Nand Flash interface Support 1,2,4 line mode SPI Nor Flash Supports 3 Byte and 4 Byte address mode ● NAND Flash Interface Support for SLC and MLC asynchronous interface devices Supports 2 / 4 / 8 / 16 KB page size Support 8 / 16 / 24 / 28 / 40 / 64bit ECC (in 1 KB) ● The eMMC 5.1, interface, a maximum capacity of 2TB ● Opselect from eMMC, SPI Nor / SPI Nand Flash, ● NAND Flash, or PCIe, starting from the slices
SDK	● Arm CPU Support for Linux SMP ● The DSP / MCU supports the LiteOS
Chip physical specifications	● power dissipation – (TBD) W Typical power consumption (4K60 + 4 Tops) ● working voltage The core voltage was 0.8V The IO voltage is set at 1.8/3.3V The DDR 4 / LPDDR4 / LPDDR4x interface voltage is 1.2/1.1/0.6V, respectively ● Packaging form RoHS, and the FC-BGA 23mm x 23mm package Pipe pin spacing: 0.65mm

2.3 Chip hardware block diagram



3. size of product

3.1 Performance parameters

Main frequency parameters of the main console system

name	parameter	specifications				explain
		minimum	typical case	maximum	unit	
Quadtranuclear ARM Cortex-A55	System main frequency	—	1.4	—	GHz	—

* This table configuration is the optimal system configuration, it is not recommended to modify.

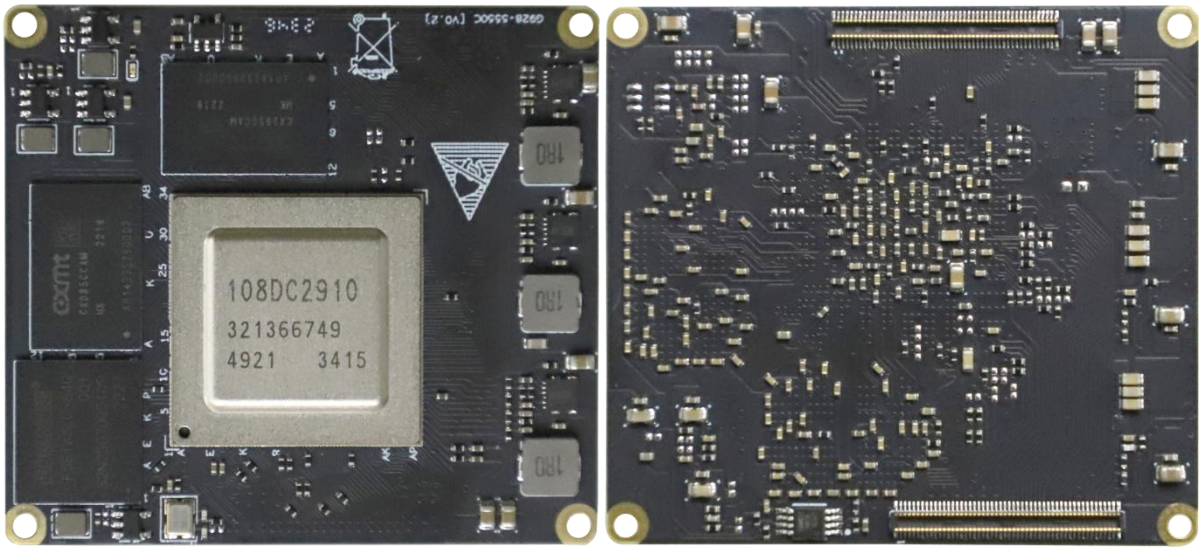
Working environment parameters

Eulerpi Development board	parameter	specifications				explain
		lowest	typical case	highest	unit	
work environment	operating ambient temperature	-30	25	85	℃	—
	Humidity of working environment	5	—	95	%RH	Without condensation

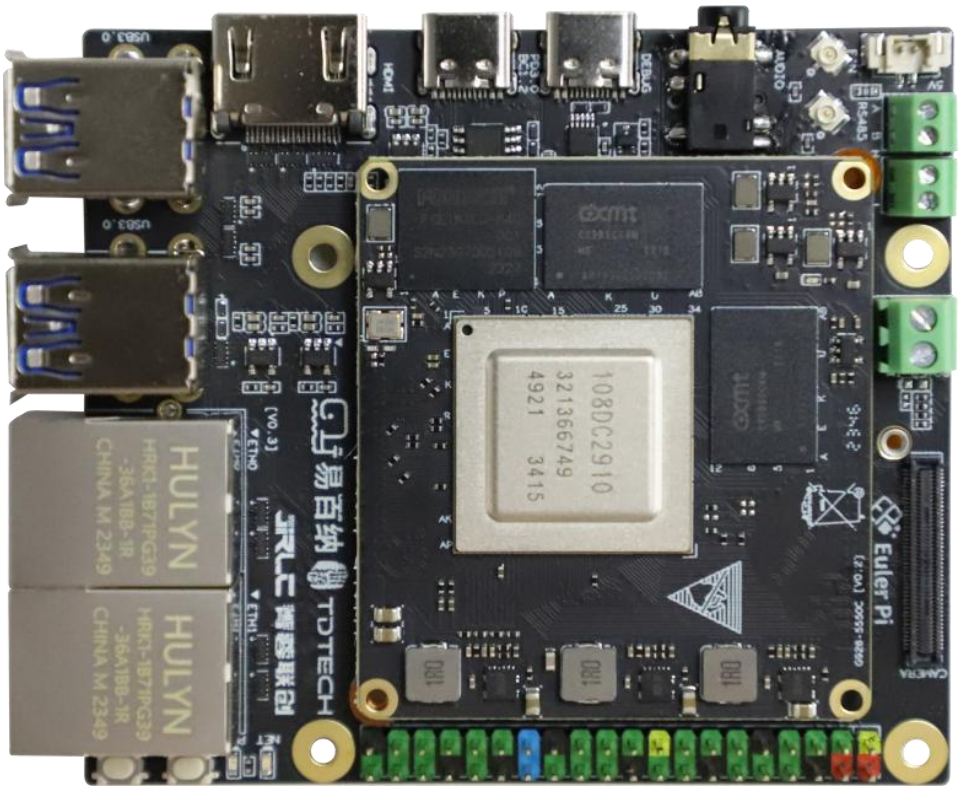
* The working environment in this table is seagull development board, and the temperature of industrial master control board is not indicated in this table.

3.2 Physical drawing of the development board

The physical map of the Seagull School core board is shown in the following figure:



The physical map of the seagull school core board + bottom plate is shown in the figure below:



Whole plate front diagram

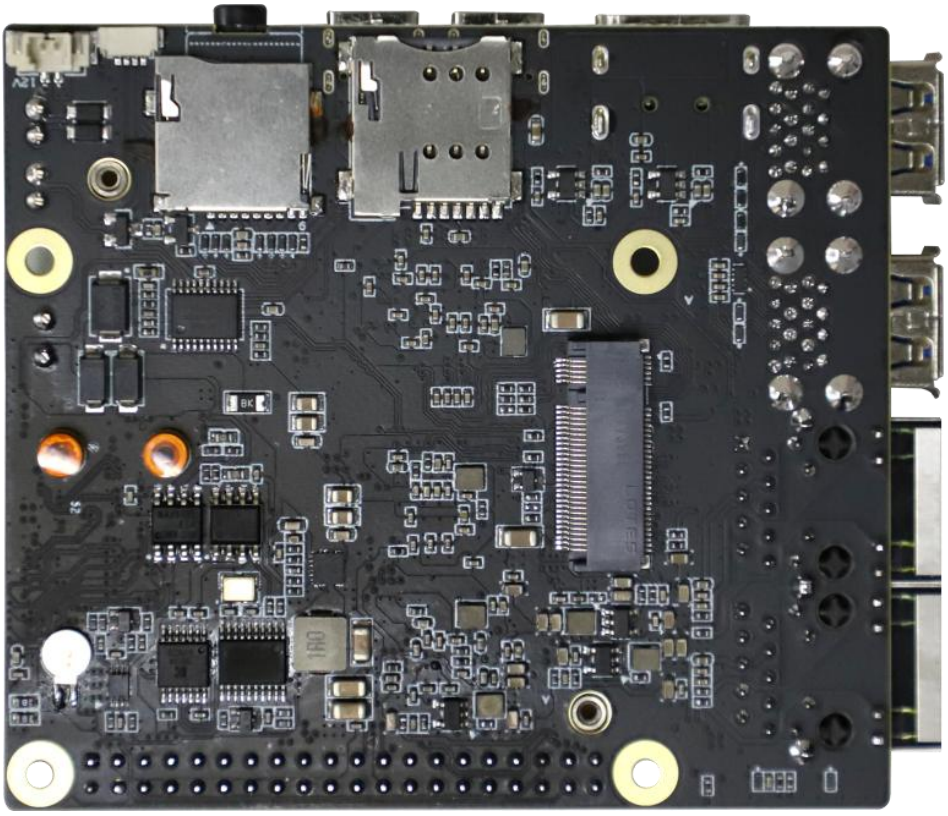


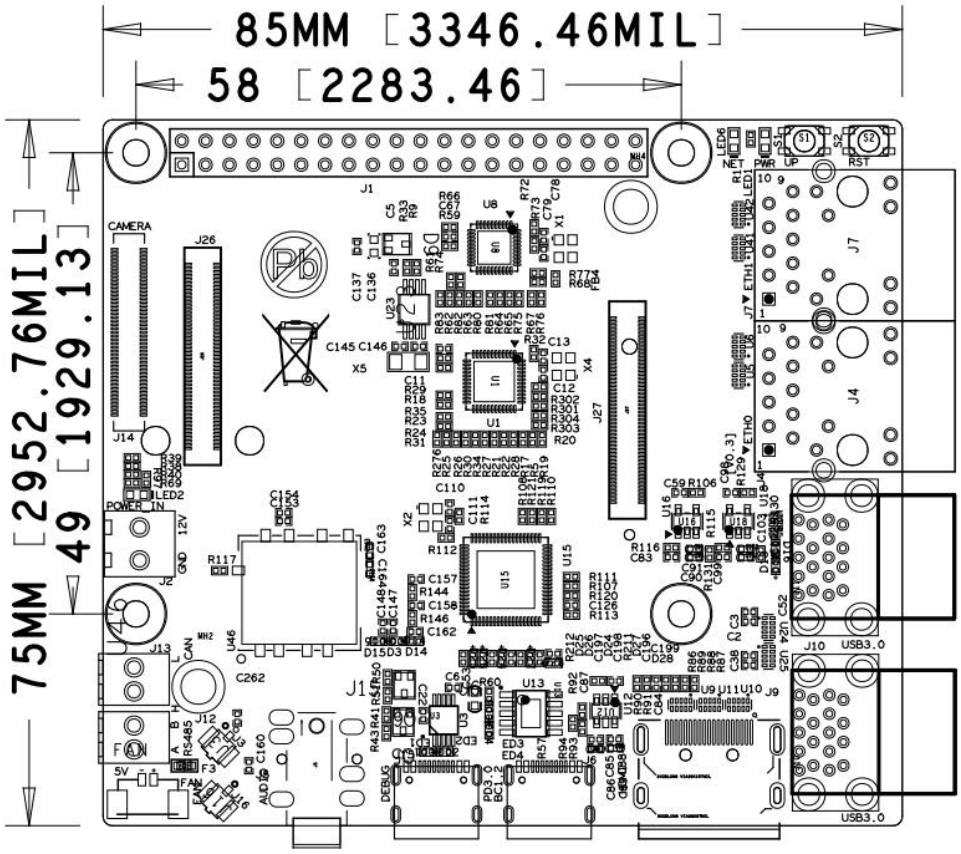
Figure on the back of the whole board

3.3 Mechanical dimensions of the development plates

Core plate: 50 * 55 (unit: mm) as shown in the figure below, and the inner hole diameter of the 4 positioning holes is 2.2 mm.

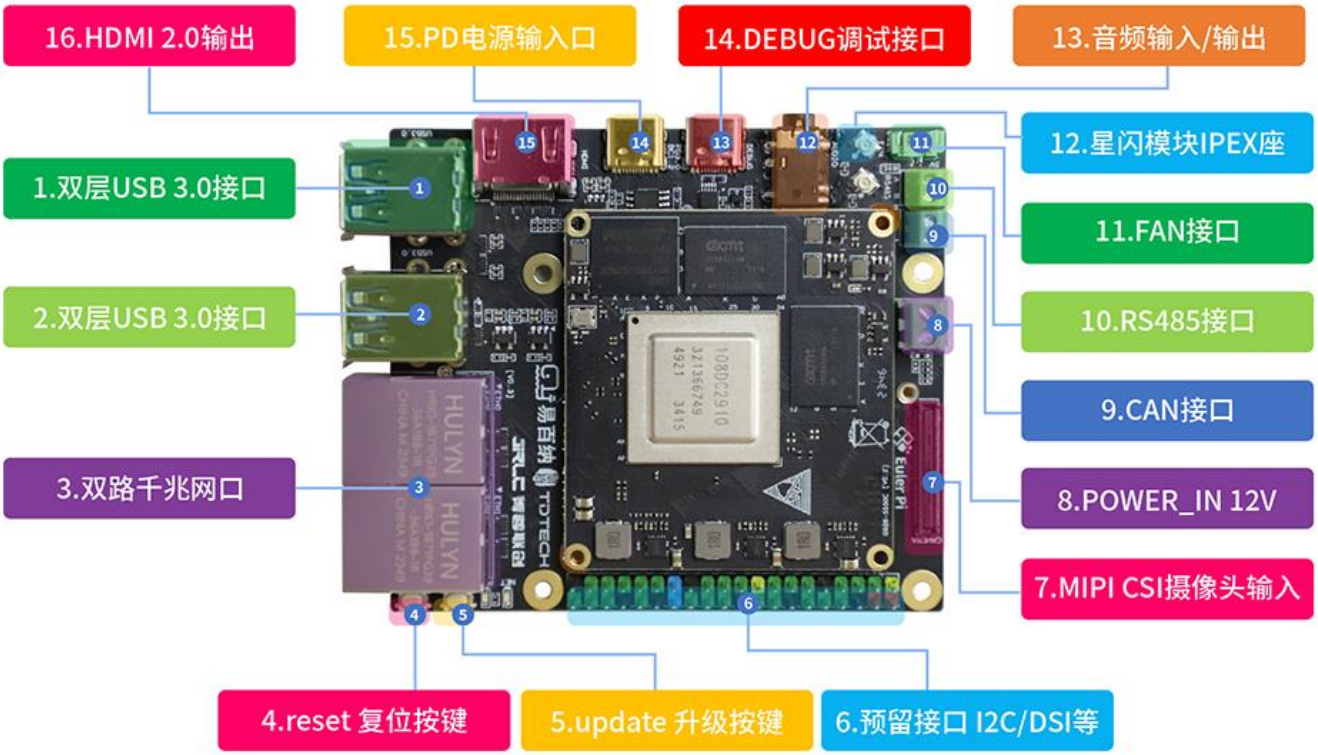
Base plate: 75 * 85 (unit: mm) as shown in the figure below, and the inner hole diameter of the 4 positioning holes is 2.7 mm.

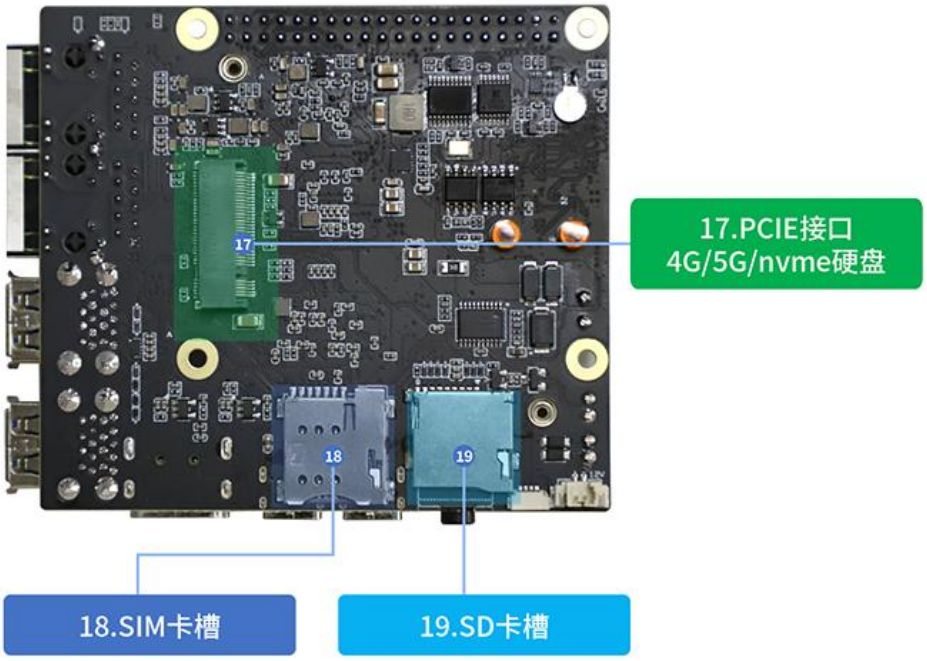
For a more detailed mechanical size map, consult the Seagull School Development Board mechanical size drawing.DXF》。



3.4 External resources of the main control board

Seagull pie development board contains a large number of interface resources, and reliable peripheral circuits must be designed to cooperate with it. This manual gives the reference design method for some of the peripheral circuits, all circuits are strict functional verified. The card peripheral interface annotation diagram is shown in the figure below:





3.5 Schematic diagram of the core board connector

The core board of Seagull development board is connected with the bottom board in the form of board to board connector. The model of the core board connector is DF40C-100DP, and the model of the bottom board connector is DF40HC (3.0) -100DS. The specific pin definition of the core board connector is shown in the following figure:

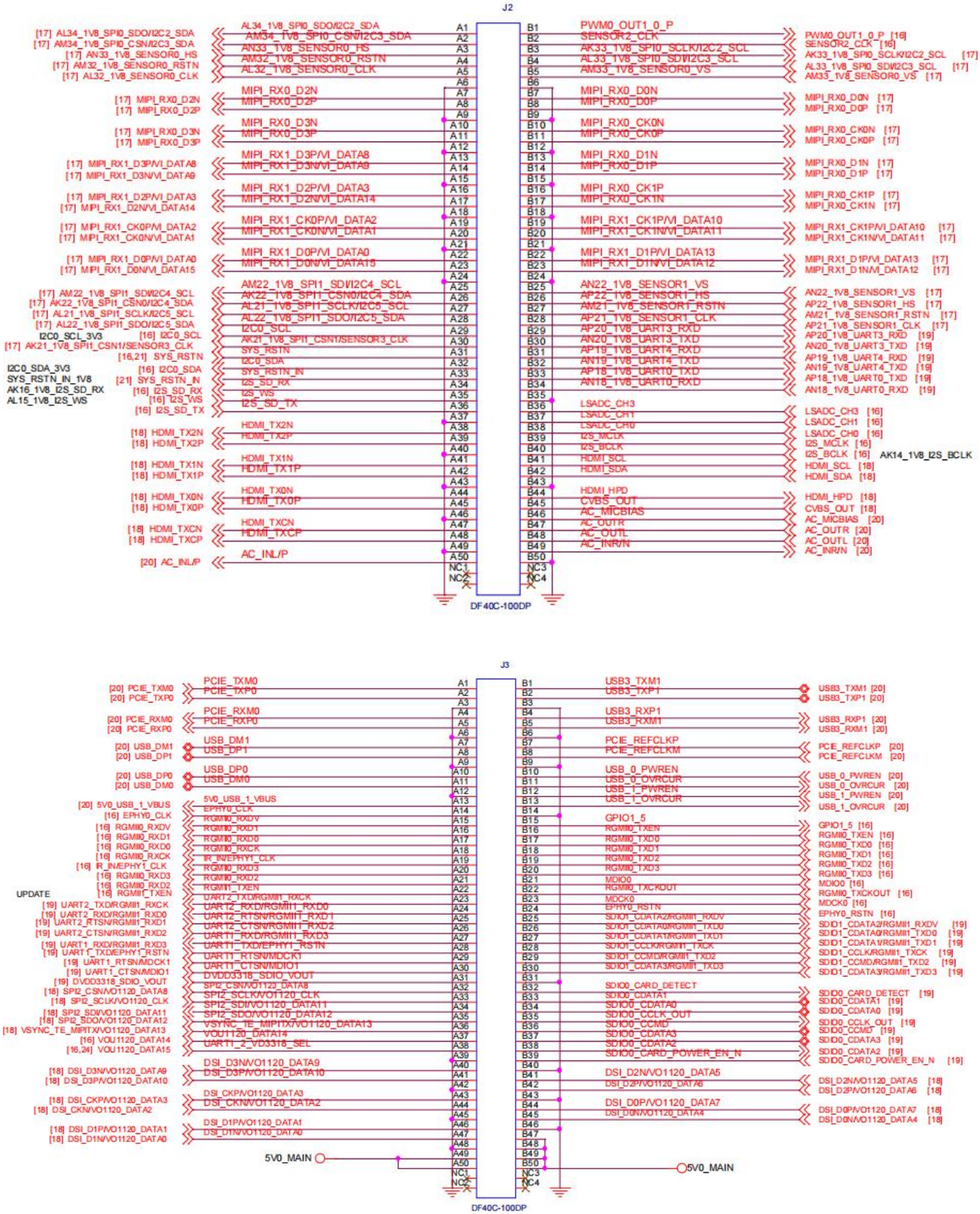


Table 3.1 Definition of the left pin of the core board connector J2

Pipe foot number	name	functional description	reference level (V)	Input / output	The processor corresponds to the pin
A1	AL34_1V8_SPI0_SDO/I2C2_SDA	SPI 0 data output / I2C2 bus data / address, OD output	1.8	O	AL34
A2	AM34_1V8_SPI0_CSN/I2C3_SDA	SPI 0 chip signal / I2C2 bus data / address, OD output	1.8	O	AM34
A3	AN33_1V8_SENSOR0_HS	Line reference signal for from mode Sensor0 the input signal, for the main mode Sensor0 the output signal, optional in the main mode	1.8	O	AN33
A4	AM32_1V8_SENSOR0_RSTN	Sensor0 Reset position of the signal	1.8	O	AM32
A5	AL32_1V8_SENSOR0_CLK	Sensor0 Working clock signal	1.8	O	AL32
A6	GND	GND	—	—	—
A7	MIPI_RX0_D2N	MIPI RX0 Interface difference data 2 negative pole	1.8	I	AK30
A8	MIPI_RX0_D2P	MIPI RX0 Interface difference data 2 positive pole	1.8	I	AL30
A9	GND	GND	—	—	—
A10	MIPI_RX0_D3N	MIPI RX0 Interface difference data 3 negative pole	1.8	I	AK28
A11	MIPI_RX0_D3P	MIPI RX0 Interface difference data 3 positive pole	1.8	I	AL28
A12	GND	GND	—	—	—
A13	MIPI_RX1_D3P/VI_DATA8	MIPI RX1 Interface difference data 3 negative pole / VI input data 8	1.8	I	AK26
A14	MIPI_RX1_D3N/VI_DATA9	MIPI RX1 Interface difference data 3 negative pole / VI input data 9	1.8	I	AL26
A15	GND	GND	—	—	—
A16	MIPI_RX1_D2P/VI_DATA3	MIPI RX1 Interface difference data 2 negative pole / VI input data 3	1.8	I	AK24
A17	MIPI_RX1_D2N/VI_DATA14	MIPI RX1 Interface difference data 2 negative pole / VI input data 14	1.8	I	AL24
A18	GND	GND	—	—	—
A19	MIPI_RX1_CK0P/VI_DATA2	MIPI RX1 Interface differential clock positive pole / VI input data 2	1.8	I	AN25
A20	MIPI_RX1_CK0N/VI_DATA1	MIPI RX1 Interface differential clock negative electrode / VI input data 1	1.8	I	AP25

A21	GND	GND	—	—	—
A22	MIPI_RX1_D0P/VI_DATA0	MIPI RX1 Interface difference data 0 positive pole / VI input data 0	1.8	I	AN24
A23	MIPI_RX1_D0N/VI_DATA15	MIPI RX1 Interface difference data 0 negative pole / VI input data 15	1.8	I	AP24
A24	GND	GND	—	—	—
A25	AM22_1V8_SPI1_SDI/I2C4_SCL	SPI 1 data input / I2C4 bus clock, OD output	1.8	O	AM22
A26	AK22_1V8_SPI1_CSN0/I2C4_SDA	SPI 1 chip signal 0 / I2C4 bus data / address, OD output	1.8	O	AK22
A27	AL21_1V8_SPI1_SCLK/I2C5_SCL	SPI 1 data clock / I2C5 bus clock, OD output	1.8	O	AL21
A28	AL22_1V8_SPI1_SDO/I2C5_SDA	SPI 1 data output / I2C5 bus data / address, OD output	1.8	O	AL22
A29	I2C0_SCL	I2C0 bus clock, OD output	3.3	O	AM19
A30	AK21_1V8_SPI1_CSN1/SENSOR3_CLK	SPI 1 chip signal 1 / Sensor3 working clock signal	1.8	I	AK21
A31	SYS_RSTN	System reset output, low level effective	1.8	I	AL17
A32	I2C0_SDA	I2C0 bus data / address, OD output	3.3	I/O	AM20
A33	SYS_RSTN_IN	—	—	—	—
A34	I2S_SD_RX	I2S or PCM interface data input	1.8	I	AK16
A35	I2S_WS	I2S left and right sound channel selection signal, or PCM 0 frame synchronization signal	1.8	O	AL15
A36	I2S_SD_TX	I2S or PCM interface data output	1.8	O	AL14
A37	GND	GND	—	—	—
A38	HDMI_TX2N	HDMI TX Channel 2 serial differential signal negative electrode	1.8	O	AP14
A39	HDMI_TX2P	HDMI TX Channel 2 serial differential signal positive pole	1.8	O	AN14
A40	GND	GND	—	—	—
A41	HDMI_TX1N	HDMI TX Negative electrode of the serial differential signal in channel 1	1.8	O	AP13
A42	HDMI_TX1P	HDMI TX Channel 1 serial differential signal positive pole	1.8	O	AN13
A43	GND	GND	—	—	—
A44	HDMI_TX0N	HDMI TX Negative electrode of the serial differential signal for channel 0	1.8	O	AP12
A45	HDMI_TX0P	HDMI TX Channel 0 serial differential signal positive pole	1.8	O	AN12
A46	GND	GND	—	—	—

A47	HDMI_TXCN	HDMI TX Differential pixel clock negative electrode	1.8	O	AP11
A48	HDMI_TXCP	HDMI TX Differential pixel clock positive pole	1.8	O	AN11
A49	GND	GND	—	—	—
A50	AC_INL/P	Audio input to the left sound channel	1.8	I	AP3

Table 3.2 Definition of the right pin of the core board connector J2

Pipe foot number	name	functional description	reference level (V)	Input / output	The processor corresponds to the pin
B1	PWM0_OUT1_0_P	PWM signal output	1.8	O	AJ34
B2	SENSOR2_CLK	Sensor2 Working clock signal	1.8	I	AJ33
B3	AK33_1V8_SPI0_SCLK/I2C2_SCL	SPI 0 data clock / I2C2 bus clock, OD output	1.8	O	AK33
B4	AL33_1V8_SPI0_SDI/I2C3_SCL	SPI 0 data input / I2C3 bus clock, OD output	1.8	I	AL33
B5	AM33_1V8_SENSOR0_VS	Field synchronization signal, for the slave mode Sensor0 is the input signal, for the main mode Sensor0 is the output signal, optional in the main mode.	1.8	O	AM33
B6	GND	GND	—	—	—
B7	MIPI_RX0_D0N	MIPI RX0 Interface difference data 0 negative pole	1.8	I	AN31
B8	MIPI_RX0_D0P	MIPI RX0 Interface difference data 0 positive pole	1.8	I	AP31
B9	GND	GND	—	—	—
B10	MIPI_RX0_CK0N	MIPI RX0 Interface difference clock 0 negative pole	1.8	I	AN30
B11	MIPI_RX0_CK0P	MIPI RX0 Interface difference clock 0 positive pole	1.8	I	AP30
B12	GND	GND	—	—	—
B13	MIPI_RX0_D1N	MIPI RX0 Interface difference data 1 negative pole	1.8	I	AN29
B14	MIPI_RX0_D1P	MIPI RX0 Interface difference data 1 positive pole	1.8	I	AP29
B15	GND	GND	—	—	—
B16	MIPI_RX0_CK1P	MIPI RX0 Interface difference clock 1 positive	1.8	I	AN28

		pole			
B17	MIPI_RX0_CK1N	MIPI RX0 Interface difference clock 1 negative pole	1.8	I	AP28
B18	GND	GND	—	—	—
B19	MIPI_RX1_CK1P/VI_DATA10	MIPI RX1 Interface differential clock 1 positive pole / VI input data 10	1.8	I	AN27
B20	MIPI_RX1_CK1N/VI_DATA11	MIPI RX1 Interface difference clock 1 negative pole / VI input data 11	1.8	I	AP27
B21	GND	GND	—	—	—
B22	MIPI_RX1_D1P/VI_DATA13	MIPI RX1 Interface difference data 1 positive pole / VI input data 13	1.8	I	AN26
B23	MIPI_RX1_D1N/VI_DATA12	MIPI RX1 Interface difference data 1 negative pole / VI input data 12	1.8	I	AP26
B24	GND	GND	—	—	—
B25	AN22_1V8_SENSOR1_VS	Field synchronization signal, for the slave mode Sensor1 is the input signal, for the main mode Sensor1 is the output signal, optional in the main mode.	1.8	O	AN22
B26	AP22_1V8_SENSOR1_HS	Line reference signal for from mode Sensor1 the input signal, for the main mode Sensor1 the output signal, optional in the main mode.	1.8	O	AP22
B27	AM21_1V8_SENSOR1_RSTN	Sensor1 Reset of the signal	1.8	O	AM21
B28	AP21_1V8_SENSOR1_CLK	Sensor1 Working clock signal	1.8	O	AP21
B29	AP20_1V8_UART3_RXD	The UART 3 data reception	1.8	O	AP20
B30	AN20_1V8_UART3_TXD	The UART 3 data is sent	1.8	O	AN20
B31	AP19_1V8_UART4_RXD	The UART 4 data reception	1.8	O	AP19
B32	AN19_1V8_UART4_TXD	The UART 4 data is sent	1.8	O	AN19
B33	AP18_1V8_UART0_TXD	The UART 0 data is sent	1.8	O	AP18
B34	AN18_1V8_UART0_RXD	The UART 0 data reception	1.8	I	AN18
B35	GND	GND	—	—	—
B36	LSADC_CH3	Register Sampling Channel 3	1.8	I	AP17
B37	LSADC_CH1	Register sampling channel 1	1.8	I	AP16
B38	LSADC_CH0	Register sampling channel 0	1.8	I	AN16
B39	I2S_MCLK	The I2S or PCM interface main clock, which can serve as a working clock for the audio CODEC	1.8	O	AK15
B40	I2S_BCLK	The I2S or the PCM clock	1.8	O	AK14
B41	HDMI_SCL	HDMI I2C Bus clock, OD output	1.8	O	AL12
B42	HDMI_SDA	HDMI I2C Bus data / address, OD output	1.8	O	AL11
B43	GND	GND	—	—	—
B44	HDMI_HPD	The HDMI hot-swap signal	1.8	O	AK11
B45	CVBS_OUT	The CVBS channel output	1.8	O	AP9
B46	AC_MICBIAS	Audio-based microphone input	1.8	O	AP7

B47	AC_OUTR	Audio output right audio channel	1.8	O	AN6
B48	AC_OUTL	Audio output left sound channel	1.8	O	AP5
B49	AC_INR/N	Audio input to the right audio channel	1.8	I	AN4
B50	GND	GND	—	—	—

Table 3.3 Definition of the left pin of the core board connector J3

Pipe foot number	name	functional description	reference level (V)	Input / output	The processor corresponds to the pin
A1	PCIE_TXM0	Negative signal of PCIE Lane0 port	1.8	O	H5
A2	PCIE_TXP0	Send the differential signal positive pole of the PCIE Lane0 port	1.8	O	H4
A3	GND	GND	—	—	—
A4	PCIE_RXM0	Receiving differential signal negative electrode of the PCIE Lane0 port	1.8	I	H1
A5	PCIE_RXP0	Receiving the differential signal positive pole of the PCIE Lane0 port	1.8	I	H2
A6	GND	GND	—	—	—
A7	USB_DM1	Data signal for USB2.0 port 1 (negative pole)	1.8	I/O	D2
A8	USB_DP1	Data signal for USB2.0 port 1 (positive electrode)	1.8	I/O	D1
A9	GND	GND	—	—	—
A10	USB_DP0	Data signal for USB2.0 of port 0 (positive electrode)	1.8	I/O	M2
A11	USB_DM0	Data signal for USB2.0 port 0 (negative pole)	1.8	I/O	M1
A12	GND	GND	—	—	—
A13	5V0_USB_1_VBUS	A 5V power supply for the USB2.0 port 1	—	—	—
A14	EPHY0_CLK	Net port PHY 0 working clock	3.3	O	T6
A15	RGMII0_RXDV	RGMII0 Mode: receive data valid signal; RM II0 mode: receive data validity and carrier detection signal.	3.3	I	T3
A16	RGMII0_RXD1	RGMII0 Mode: receive data 1	3.3	I	U3
A17	RGMII0_RXD0	RGMII0 Mode: received data 0	3.3	I	V3
A18	RGMII0_RXCK	RGMII0 Mode: To receive the clock	3.3	O	V5
A19	IR_IN/EPHY1_CLK	Net port PHY 1 working clock	3.3	O	Y6
A20	RGMII0_RXD3	RGMII0 Mode: receive data 3	3.3	I	W5
A21	RGMII0_RXD2	RGMII0 Mode: receiving data 2	3.3	I	W4

A22	RGMII1_TXEN	RGMII1 / RMII 1 mode: send data valid signal	3.3	O	Y4
A23	UART2_TXD/RGMII1_RXCK	UART 2 data sending / RGMII1 mode: receiving the clock	3.3	I/O	AB5
A24	UART2_RXD/RGMII1_RXD0	UART 2 data receiving / RGMII1 mode: Receive data 0	3.3	I/O	AB4
A25	UART2_RTSN/RGMII1_RXD1	UART 2 sends request signal / RGMII1 mode: receive data 1	3.3	I/O	AC3
A26	UART2_CTSN/RGMII1_RXD2	UART 2 sends clear signal / RGMII1 mode: receive data 2	3.3	I/O	AC4
A27	UART1_RXD/RGMII1_RXD3	UART 1 Data receiving / RGMII1 mode: Receive data 3	3.3	I/O	AD4
A28	UART1_TXD/EPHY1_RSTN	UART 1 data transmission / network port PHY 1 reset signal, low effective	3.3	I/O	AE4
A29	UART1_RTSN/MDCK1	The UART 1 sends the request signal / MDIO 1 interface clock output	3.3	I/O	AF5
A30	UART1_CTSN/MDIO1	The UART 1 sends the input / output signal of the clear signal / MDIO 1 interface	3.3	I/O	AF4
A31	DVDD3318_SDIO_VOUT	SDIO 0 power supply output	3.3	O	AF6
A32	SPI2_CSN/VO1120_DATA8	SPI 2 chip selection signal / VOBT.1120 for output data 8	1.8	O	AH5
A33	SPI2_SCLK/VO1120_CLK	SPI 2 Data Clock / VOBT.1120 Interface clock	1.8	O	AH4
A34	SPI2_SDI/VO1120_DATA11	SPI 2 Data Entry / VOBT.1120 Output data 11	1.8	O	AJ4
A35	SPI2_SDO/VO1120_DATA12	SPI 2 Data Output / VOBT.1120 Output data 12	1.8	O	AJ5
A36	VSYNC_TE_MIPITX/VO1120_DATA13	MIPI interface frame synchronization signal / VOBT.1120 Output data 13	1.8	O	AL4
A37	VOU1120_DATA14	VO BT.1120 Output data 14	1.8	O	AL5
A38	VOU1120_DATA15	VO BT.1120 Output data 15	1.8	O	AL6
A39	GND	GND	—	—	—
A40	DSI_D3N/VO1120_DATA9	DSI interface difference data 3 negative pole / VOBT.1120 for the output data 9	1.8	O	AH1
A41	DSI_D3P/VO1120_DATA10	DSI interface Differential data 3 positive electrode / VOBT.1120 Output data 10	1.8	O	AH2
A42	GND	GND	—	—	—
A43	DSI_CKP/VO1120_DATA3	DSI interface differential clock negative electrode / VOBT.1120 for the output data 3	1.8	O	AK2
A44	DSI_CKN/VO1120_DATA2	DSI interface differential clock negative electrode / VOBT.1120 The output data is available for 2	1.8	O	AK1
A45	GND	GND	—	—	—
A46	DSI_D1P/VO1120_DATA1	DSI interface difference data 1 positive electrode / VOBT.1120 The output data is 1	1.8	O	AL2
A47	DSI_D1N/VO1120_DATA0	DSI interface difference data 1 negative pole / VOBT.1120 The output data is 0	1.8	O	AL1

A48	GND	GND	—	—	—
A49	5V0_MAIN	5V power supply	—	—	—
A50	5V0_MAIN	5V power supply	—	—	—

Table 3.4 Definition of the right pin of the core board connector J3

Pipe foot number	name	functional description	reference level (V)	Input / output	The processor corresponds to the pin
B1	USB3_TXM1	Negative negative difference signal of the USB3 port	1.8	O	F5
B2	USB3_TXP1	Send differential signal positive electrode of the USB3 port	1.8	O	F4
B3	GND	GND	—	—	—
B4	USB3_RXP1	Send differential signal positive electrode of the USB3 port	1.8	I	F2
B5	USB3_RXM1	Negative negative difference signal of the USB3 port	1.8	I	F1
B6	GND	GND	—	—	—
B7	PCIE_REFCLKP	PCIE refers to the positive clock tube pin	1.8	O	K2
B8	PCIE_REFCLKM	The PCIE refers to the clock tube foot anode	1.8	O	K1
B9	GND	GND	—	—	—
B10	USB_0_PWREN	USB port 0 power control output pin, high and low level can be matched, the default is low level effective	1.8	O	L4
B11	USB_0_OVRCUR	USB port 0 overcurrent indication signal, the default is high validity	1.8	O	L3
B12	USB_1_PWREN	USB port 1 power control output pin, high and low level is available, the default is low level effective	1.8	O	C4
B13	USB_1_OVRCUR	USB port 1 overcurrent indication signal, the default is high validity	1.8	O	D4
B14	GND	GND	—	—	—
B15	GPIO1_5	General input and output	1.8	O	B2
B16	RGMII0_TXEN	RGMII0 / RM II0 mode: send data valid signal	3.3	O	T4
B17	RGMII0_TXD0	RGMII0 Mode: Send data to 0	3.3	O	T1
B18	RGMII0_TXD1	RGMII0 Mode: Send data to 1	3.3	O	T2
B19	RGMII0_TXD2	RGMII0 Mode: Send data to 2	3.3	O	U1

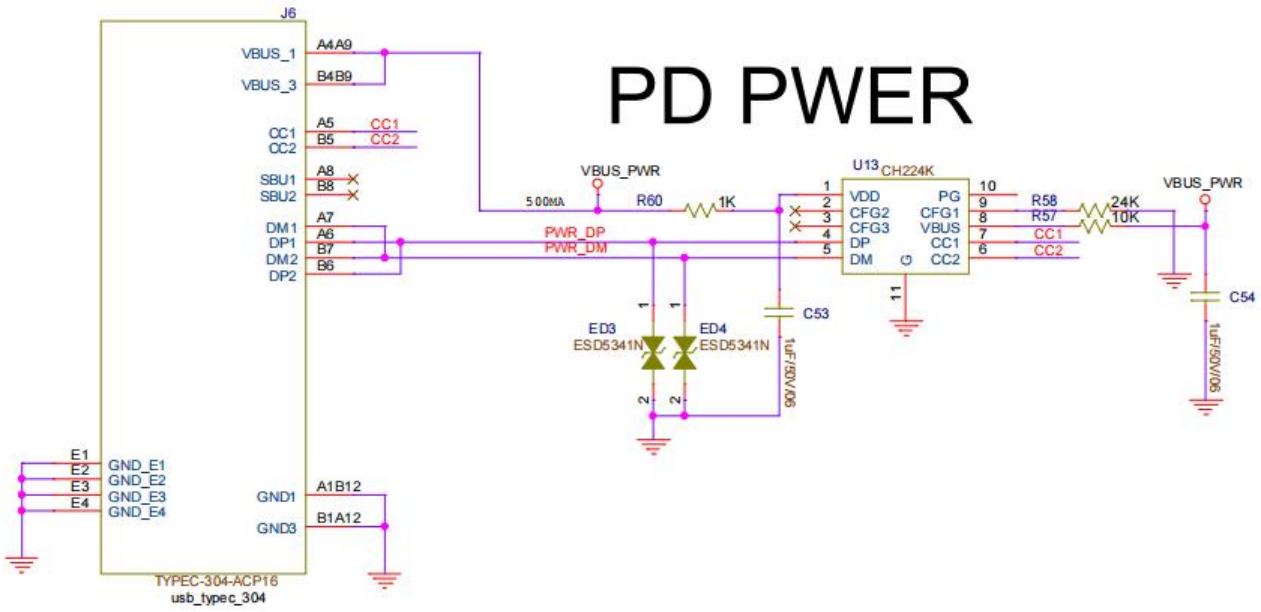
B20	RGMII0_TXD3	RGMII0 Mode: Send data to 3	3.3	O	U2
B21	MDIO0	Input / output signal of the MDIO 0 interface	3.3	O	V1
B22	RGMII0_TXCKOUT	RGMII0 Gigabit mode: send the clock	3.3	O	V2
B23	MDCK0	The MDIO 0 interface clock is in output	3.3	O	W1
B24	EPHY0_RSTN	Net port PHY 0 working clock	3.3	O	Y2
B25	SDIO1_CDATA2/RGMII1_RXDV	SDIO 1 data transmission 2 / RGMII1 mode: receiving the data valid signal; RMII 1 mode: received data validity and carrier detection signal.	3.3	I/O	AA2
B26	SDIO1_CDATA0/RGMII1_TXD0	SDIO 1 data transfer 0 / RGMII1 mode: Send data 0	3.3	I/O	AA1
B27	SDIO1_CDATA1/RGMII1_TXD1	SDIO 1 Data transfer 1 / RGMII1 mode: Send data 1	3.3	I/O	AB3
B28	SDIO1_CCLK/RGMII1_TXCK	SDIO 1 interface clock output / RGMII1 Gigabit mode: Send clock	3.3	O	AB1
B29	SDIO1_CCMD/RGMII1_TXD2	SDIO 1 interface command signal transmission / RGMII1 mode: send data 2	3.3	O	AC2
B30	SDIO1_CDATA3/RGMII1_TXD3	SDIO 1 Data transfer 3 / RGMII1 mode: send data 3	3.3	I/O	AC1
B31	GND	GND	—	—	—
B32	SDIO0_CARD_DETECT	SDIO 0 interface access detection	3.3	I	AD2
B33	SDIO0_CDATA1	SDIO 0 data transfer 1	3.3	I/O	AD1
B34	SDIO0_CDATA0	SDIO 0 data transfer 0	3.3	I/O	AD3
B35	SDIO0_CCLK_OUT	SDIO 0 interface clock output	3.3	O	AE2
B36	SDIO0_CCMD	SDIO 0 interface command signal transmission	3.3	O	AF3
B37	SDIO0_CDATA3	SDIO 0 Data Transfer 3	3.3	I/O	AF2
B38	SDIO0_CDATA2	SDIO 0 Data Transfer 2	3.3	I/O	AF1
B39	SDIO0_CARD_POWER_EN_N	SDIO 0 interface power supply to enable control	3.3	O	AG3
B40	GND	GND	—	—	—
B41	DSI_D2N/VO1120_DATA5	DSI interface difference data 2 negative pole / VOBT.1120 to output data 5	1.8	O	AJ1
B42	DSI_D2P/VO1120_DATA6	DSI interface difference data 2 positive electrode / VOBT.1120 for the output data 6	1.8	O	AJ2
B43	GND	GND	—	—	—
B44	DSI_D0P/VO1120_DATA7	DSI interface difference data 0 positive electrode / VOBT.1120 for the output data 7	1.8	O	AM2
B45	DSI_D0N/VO1120_DATA4	DSI interface difference data 0 negative electrode / VOBT.1120 to output data 4	1.8	O	AM1
B46	GND	GND	—	—	—
B47	5V0_MAIN	5V power supply	—	—	—
B48	5V0_MAIN	5V power supply	—	—	—
B49	5V0_MAIN	5V power supply	—	—	—

B50	5V0_MAIN	5V power supply	—	—	—

3.6 Description of the interface parameters

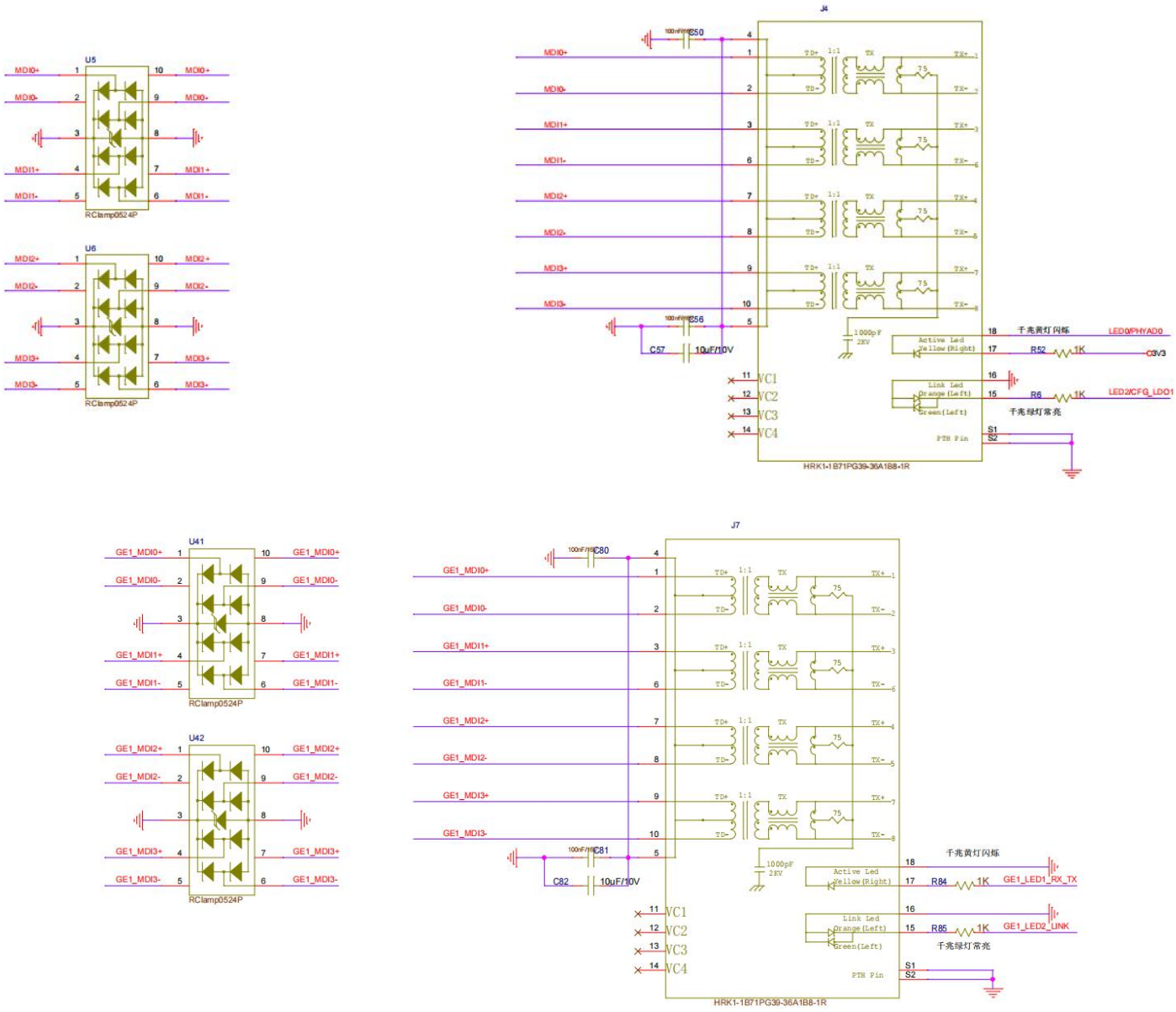
3.6.1 PD charging interface

The Seagull Pai development board is equipped with PD power charging interface (interface marking diagram number 15), the interface corresponding PCB screen position number is J6, and the seat specification is TYPEC-304-ACP 16. The reference circuit for this section is shown in the figure below:



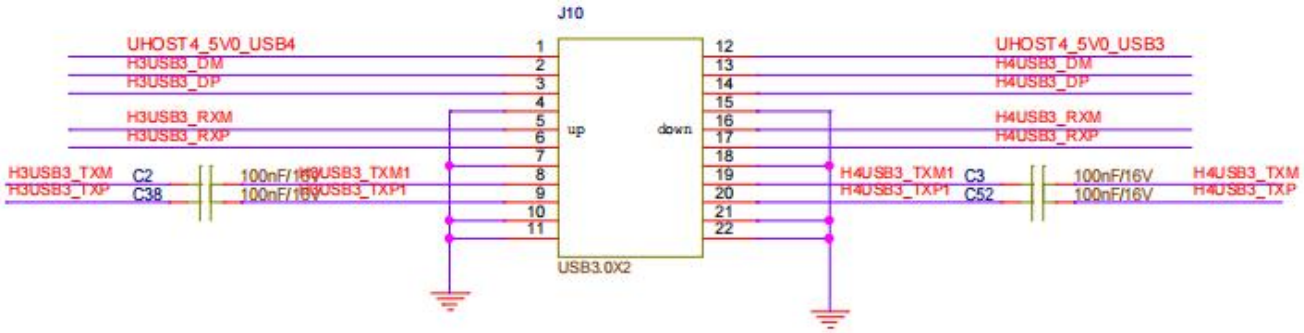
3.6.2 Network Interface

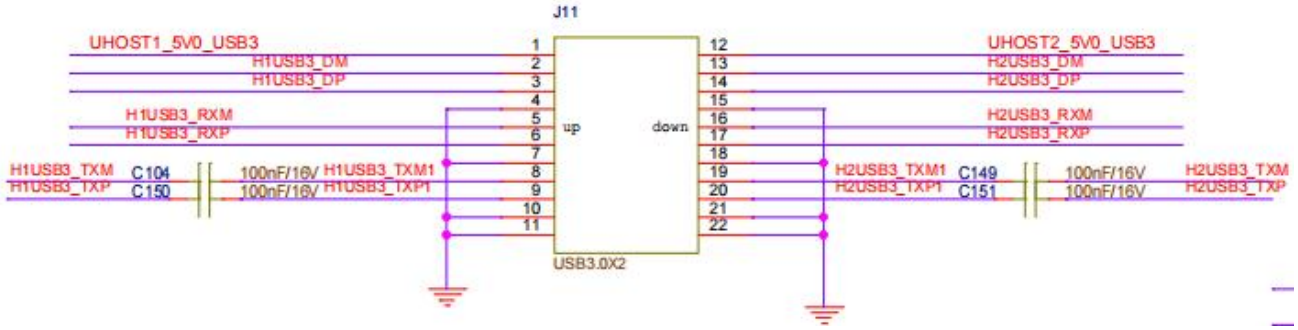
There are two Gigabit network ports on the development board (interface annotation diagram number 3), the corresponding PCB screen printing number is J4 and J7, and the seat size is HRK 1-1B71PG39-36A1B8-1R network port partial reference circuit is shown in the figure below:



3.6.3 USB interface

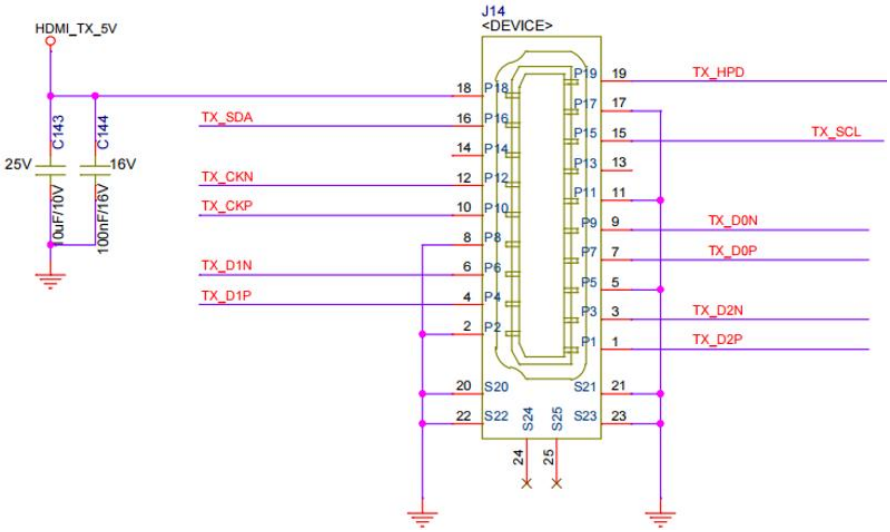
There are four USB 3.0 interfaces (the interface diagram number 1 and 2), the maximum flow limit of each port is 1.5A, and the corresponding PCB screen number is J10 and J11. There are two standard double-layer USB 3.0 interface bases (with rolling edges). The reference circuit for this part is shown in the figure below:





3.6.4 HDMI interface

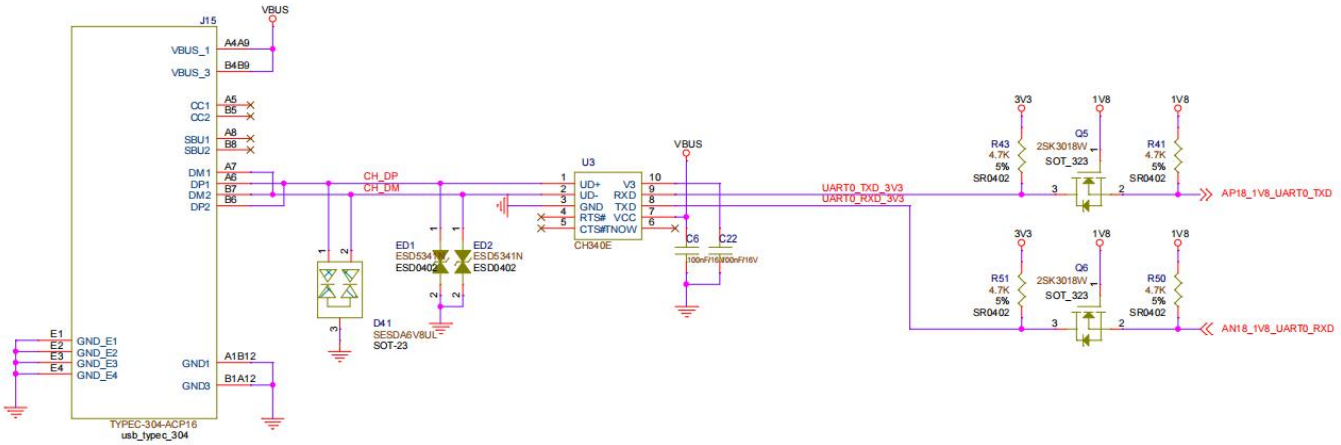
There is one HDMI 2.0 output interface on the board with resolution up to 4 K @ 60 fps (interface annotation diagram number 16). The PCB screen number is J14, which is a standard horizontal HDMI 19P mother seat. The reference circuit for this part is shown in the figure below:



3.6.5 Debug Debug interface

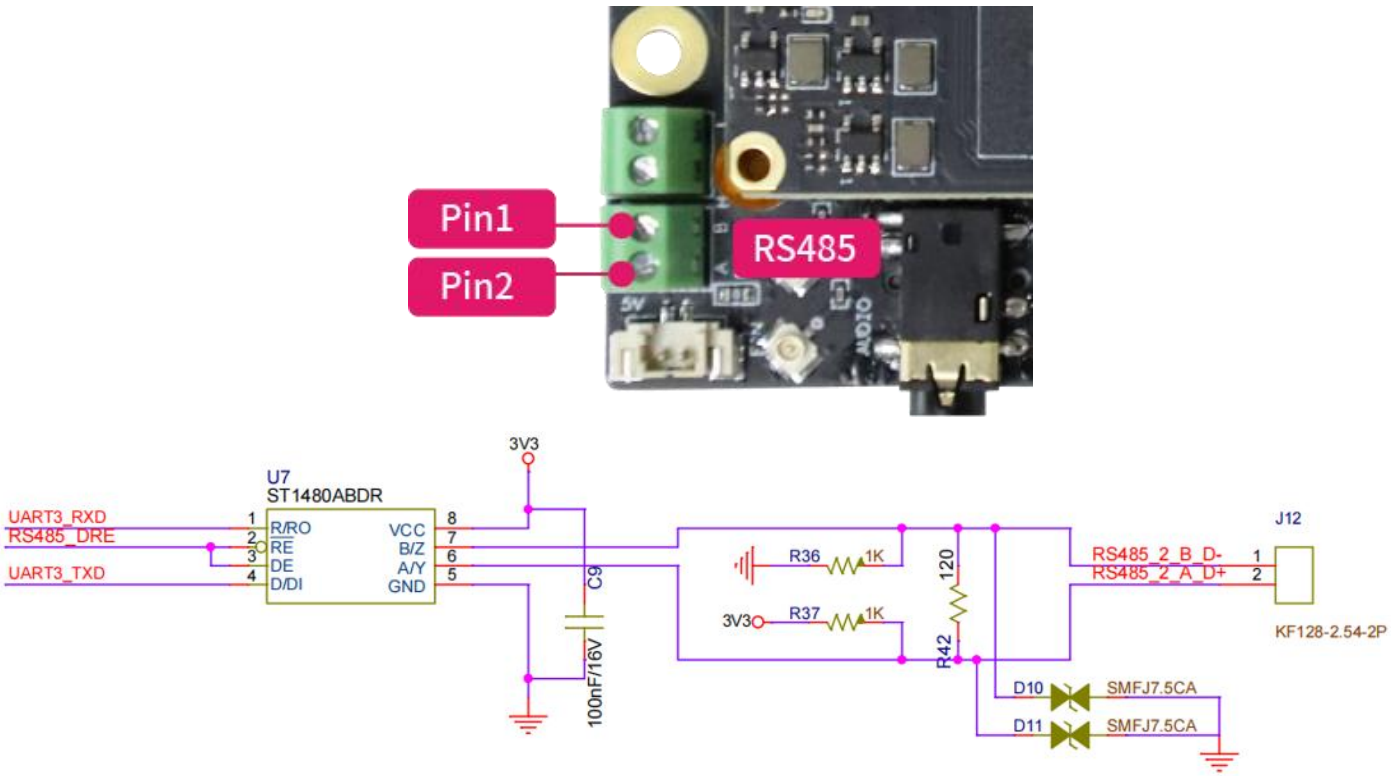
The Debug debugging serial port of Seagull Pai development board is UART 0 (interface annotation diagram no. 14), the corresponding PCB screen mark number is J15, and the seat specification is TYPEC-304-ACP 16. The reference circuit for this part is shown in the figure below:

DEBUG



3.6.6 RS485 interface

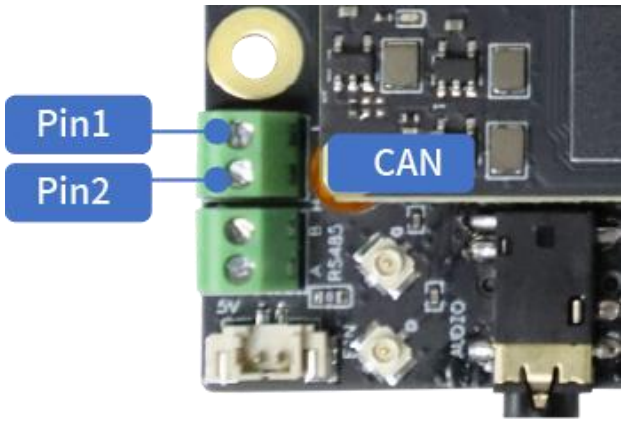
The RS485 interface of the seagull development board is changed from UART 3 (No.10 of the interface annotation diagram), the corresponding PCB screen number is J12, and the seat size is KF128-2.54-2P. The pin arrangement and reference circuit of this part are shown in the figure below:

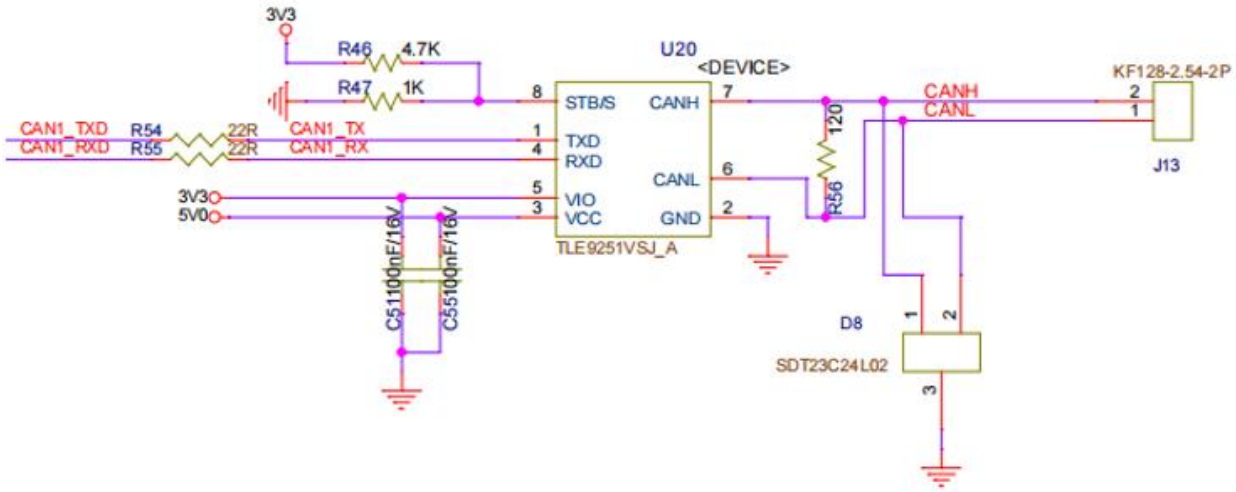


The pin number	Signal description	function
PIN1	RS485_2_B_D-	The RS485 signal, B
PIN2	RS485_2_A_D+	The RS485 signal, A

3.6.7 CAN Interface

There is 1 CAN interface (interface annotation diagram serial number 9). The interface corresponding PCB screen mark number is J13, and the seat size is KF128-2.54-2P. The pin arrangement and reference circuit of this part are shown in the figure below:

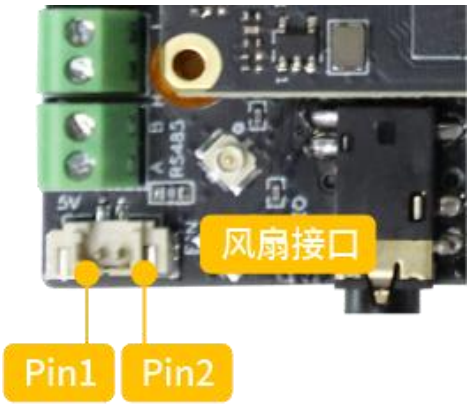


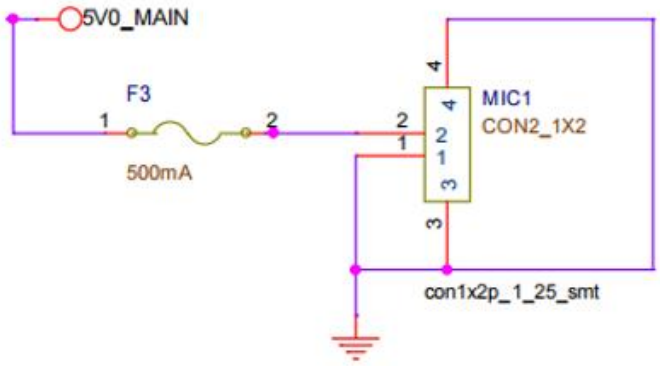


The pin number	Signal description	function
PIN1	CANL	CAN_L signal wire
PIN2	CANH	CAN_H signal wire

3.6.8 Fan interface

There is 1 fan interface on the development board, 5V power supply (interface annotation diagram no. 11), the PCB screen position number of the interface is MIC 1, and the seat specification is con1x2p _ 1 _ 25 _ smt. The pin arrangement and reference circuit of this part are shown in the figure below:

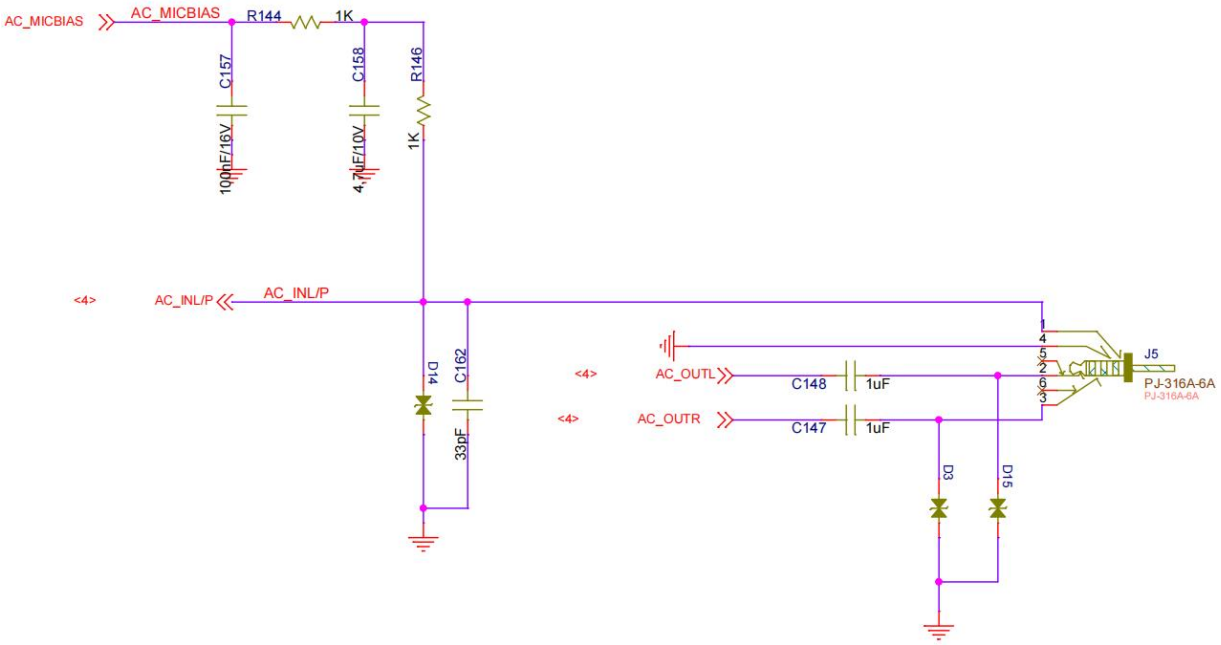




The pin number	Signal description	function
PIN1	GND	GND
PIN2	5V0_MAIN	Fan 5V power supply port

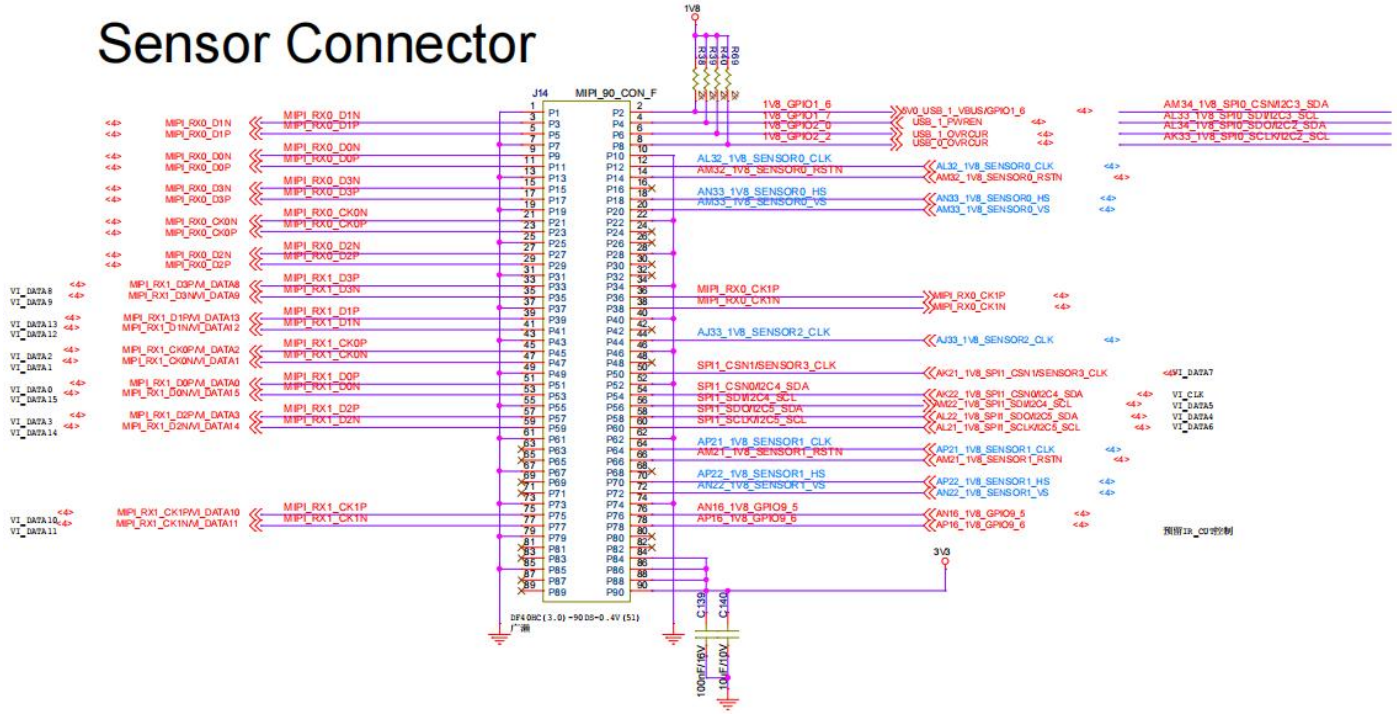
3.6.9 Audio interface

The Seagull School development board has one audio input and output circuit (interface annotation diagram No.13). The audio signal is directly connected to the interface by the MCU, if the audio output needs to be used with external power amplifier. The corresponding PCB screen position number is J5, the seat size model is PJ-316A-6A, and the reference circuit for this part is shown in the figure below:



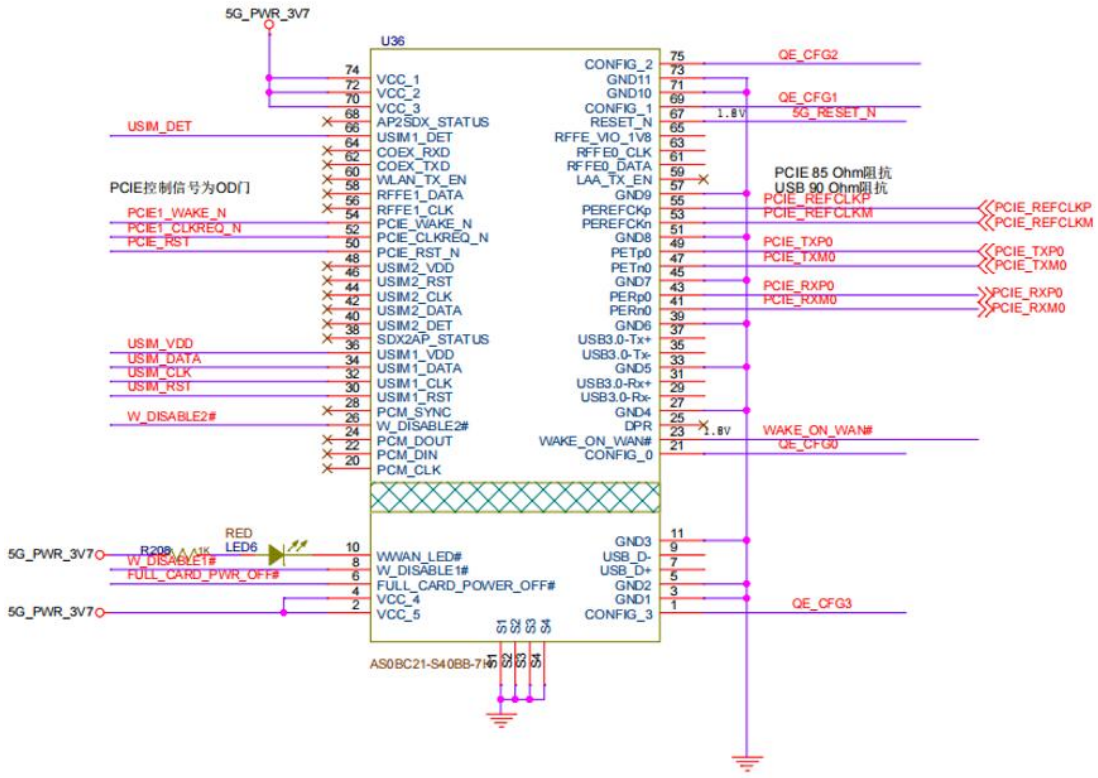
3.6.10 MIPI CSI interface

There are 24Lane MIPI_CSI camera input interface (interface annotation diagram No.7), which requires the expansion board to be used by external Sensor. Currently, Sensor has IMX347, GC2053, OS08A20, etc.. The corresponding PCB screen position number is J14, and the seat size is Hirose DF40HC(3.0)-90DS-0.4V (51). The pins involved in this interface can retrieve the corresponding definitions, levels and MCU pins in 4 tables in Section 3.5. The reference circuit for this section is shown in the figure below:



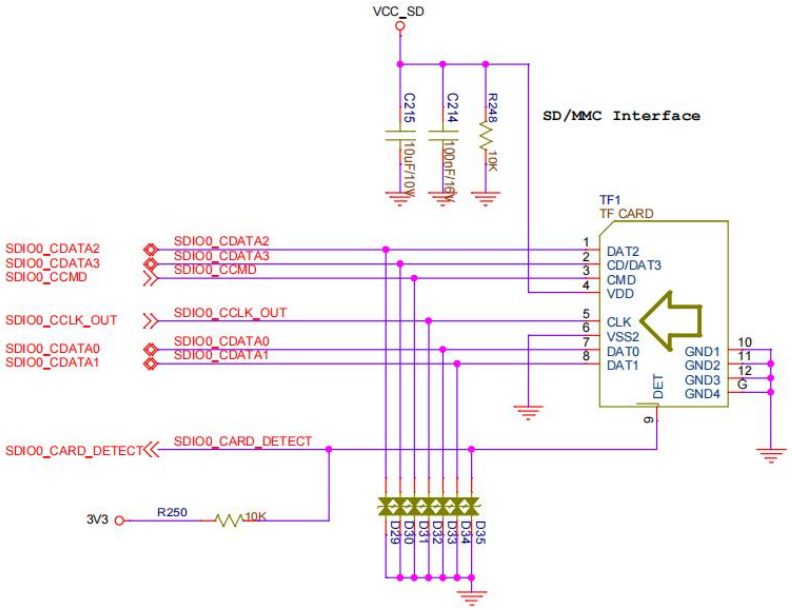
3.6.11 PCIE interface

There is 1 PCIE interface and 1 SIM card slot, which can be connected to 4G / 5G / nvme hard disk (interface annotation diagram No.17). The interface corresponds to the PCB gold finger connector with U36 and seat size of 52 Pin _ miniPCIE _ height 5.6mm. The reference circuit for this part is shown in the figure below:



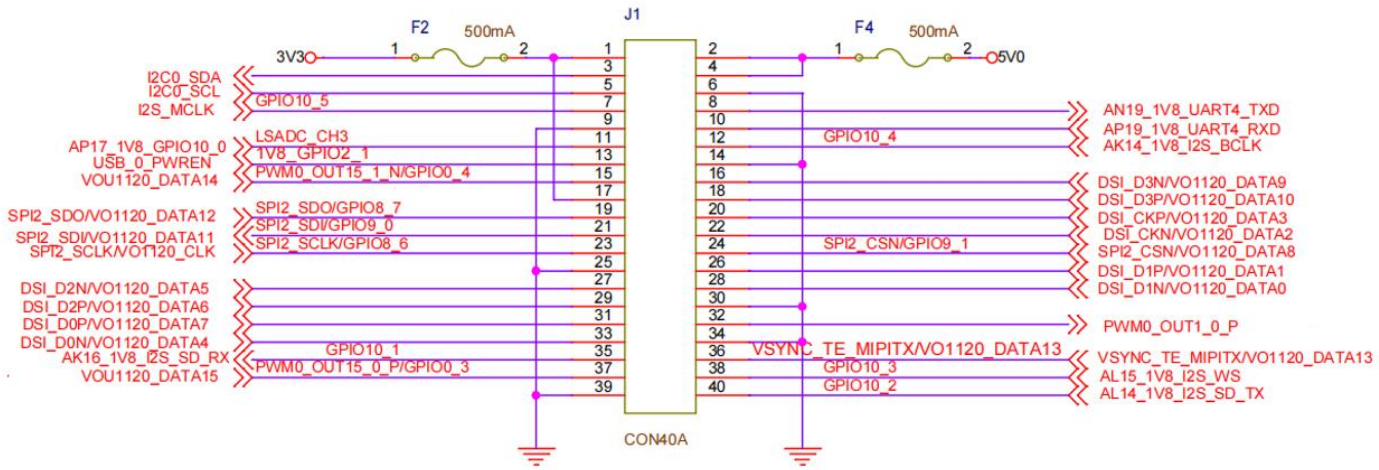
3.6.12 SD card interface

There is 1 Micro_SD card interface (No.19). PCB screen mark number is TF 1 and seat size is TF-01A. The reference circuit for this part is shown in the figure below:



3.6.13, other reserved interfaces

Many interfaces are reserved on the Seagull School development board, such as I2C, DSI, UART, I2S, etc. (interface annotation diagram number 6). The interface corresponds to PCB screen mark number of J1, and the seat size is 2.54mm spacing 2 * 20pin. The pins involved in this interface can retrieve the corresponding definitions, levels and MCU pins in 4 tables in Section 3.5. The pin arrangement and reference circuits for this section are shown in the figure below:



The pin number	Signal description	functional description	reference level (V)	processor Corresponding to the pin
PIN1	3V3	Reserve 3.3V	—	—
PIN3	I2C0_SDA	I2C0 bus data / address, OD output	3.3	AM20
PIN5	I2C0_SCL	I2C0 bus clock, OD output	3.3	AM19
PIN7	I2S_MCLK	The I2S or PCM interface main clock, which can serve as a working clock for the audio CODEC	1.8	AK15
PIN9	GND	GND	—	—
PIN11	AP17_1V8_GPIO10_0	General input and output	1.8	AP17
PIN13	USB_0_PWREN	USB port 0 power control output pin, high and low level can be matched, the default is low level effective	1.8	L4
PIN15	VOU1120_DATA14	VO BT.1120 Output data 14	1.8	AL5
PIN17	3V3	Reserve 5V	—	—
PIN19	SPI2_SDO/VO1120_DATA12	SPI 2 Data Output / VOBT.1120 Output	1.8	AJ5
PIN21	SPI2_SDI/VO1120_DATA11	SPI 2 Data Entry / VOBT.1120 Output	1.8	AJ4
PIN23	SPI2_SCLK/VO1120_CLK	SPI 2 Data Clock / VOBT.1120 Interface	1.8	AH4
PIN25	GND	GND	—	—
PIN27	DSI_D2N/VO1120_DATA5	DSI interface difference data 2 negative pole / VOBT.1120 to output data 5	1.8	AJ1
PIN29	DSI_D2P/VO1120_DATA6	DSI interface difference data 2 positive electrode / VOBT.1120 for the output data 6	1.8	AJ2
PIN31	DSI_D0P/VO1120_DATA7	DSI interface difference data 0 positive electrode / VOBT.1120 for the output data 7	1.8	AM2

PIN33	DSI_D0N/VO1120_DATA4	DSI interface difference data 0 negative electrode / VOBT.1120 to output data 4	1.8	AM1
PIN35	AK16_1V8_I2S_SD_RX	I2S or PCM interface data input	1.8	AK16
PIN37	VOU1120_DATA15	VO BT.1120 Output data 15	1.8	AL6
PIN39	GND	GND	—	—
PIN2	5V0	Reserve 5V	—	—
PIN4	5V0	Reserve 5V	—	—
PIN6	GND	GND	—	—
PIN8	AN19_1V8_UART4_TXD	The UART 4 data is sent	1.8	AN19
PIN10	AP19_1V8_UART4_RXD	The UART 4 data reception	1.8	AP19
PIN12	AK14_1V8_I2S_BCLK	The I2S or the PCM clock	1.8	AK14
PIN14	GND	GND	—	—
PIN16	DSI_D3N/VO1120_DATA9	DSI interface difference data 3 negative pole / VOBT.1120 for the output data 9	1.8	AH1
PIN18	DSI_D3P/VO1120_DATA10	DSI interface Differential data 3 positive electrode / VOBT.1120 Output data 10	1.8	AH2
PIN20	DSI_CKP/VO1120_DATA3	DSI interface differential clock negative electrode / VOBT.1120 for the output data 3	1.8	AK2
PIN22	DSI_CKN/VO1120_DATA2	DSI interface differential clock negative electrode / VOBT.1120 The output data is available for 2	1.8	AK1
PIN24	SPI2_CSN/VO1120_DATA8	SPI 2 chip selection signal / VOBT.1120	1.8	AH5
PIN26	DSI_D1P/VO1120_DATA1	DSI interface difference data 1 positive electrode / VOBT.1120 The output data is 1	1.8	AL2
PIN28	DSI_D1N/VO1120_DATA0	DSI interface difference data 1 negative pole / VOBT.1120 The output data is 0	1.8	AL1
PIN30	GND	GND	—	—
PIN32	PWM0_OUT1_0_P	PWM signal output	1.8	AJ34
PIN34	GND	GND	—	—
PIN36	VSYNC_TE_MIPITX/VO1120_DATA13	MIPI interface frame synchronization signal / VOBT.1120 Output data 13	1.8	AL4
PIN38	AL15_1V8_I2S_WS	I2S left and right sound channel selection signal, or PCM 0 frame synchronization signal	1.8	AL15
PIN40	AL14_1V8_I2S_SD_TX	I2S or PCM interface data output	1.8	AL14

3.6.14 Power supply interface

The pin arrangement of this section is shown in the following figure: