

## Team Details

Team Name:

**Wafer Minds**

SR. NO	ROLE	NAME	ACADEMIC YEAR
1	Team Leader	Ebinesh K	3
2	Member 1	Kaviya Dharshini G	2
3	Member 2	Abishek J	2

 **COLLEGE NAME**

Chennai Institute of Technology

 **TEAM LEADER CONTACT NUMBER**

+91 7845887115

 **TEAM LEADER EMAIL ADDRESS**

ebineshk.vlsi2023@citchennai.net

# Problem Statement Addressed

Edge AI-Based Defect Classification System for Semiconductor Wafer/Die Images.

Semiconductor defect inspection currently relies on cloud processing or manual review, causing high latency, scalability issues, and delayed quality decisions.



High inspection latency



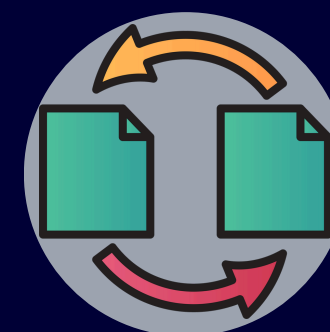
Cloud-based analysis delays real-time defect detection on production lines.



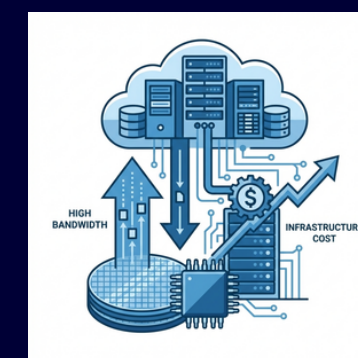
Manual Inspection Limitations



Human review is slow, subjective, and not scalable for high-volume manufacturing.



Bandwidth and infrastructure cost



Continuous transfer of high-resolution wafer images increases network load and operational expense.

# Idea Description



A deep learning-based automated visual inspection system for wafer surface defect classification using transfer learning. The approach leverages a pretrained EfficientNet-B0 model fine-tuned on the Carinthia wafer defect dataset, enabling accurate multi-class defect identification with minimal training overhead and high generalization capability.

## KEY CONCEPT & APPROACH

A transfer-learning based deep learning system using **EfficientNet-B0** for automated multi-class wafer defect classification.

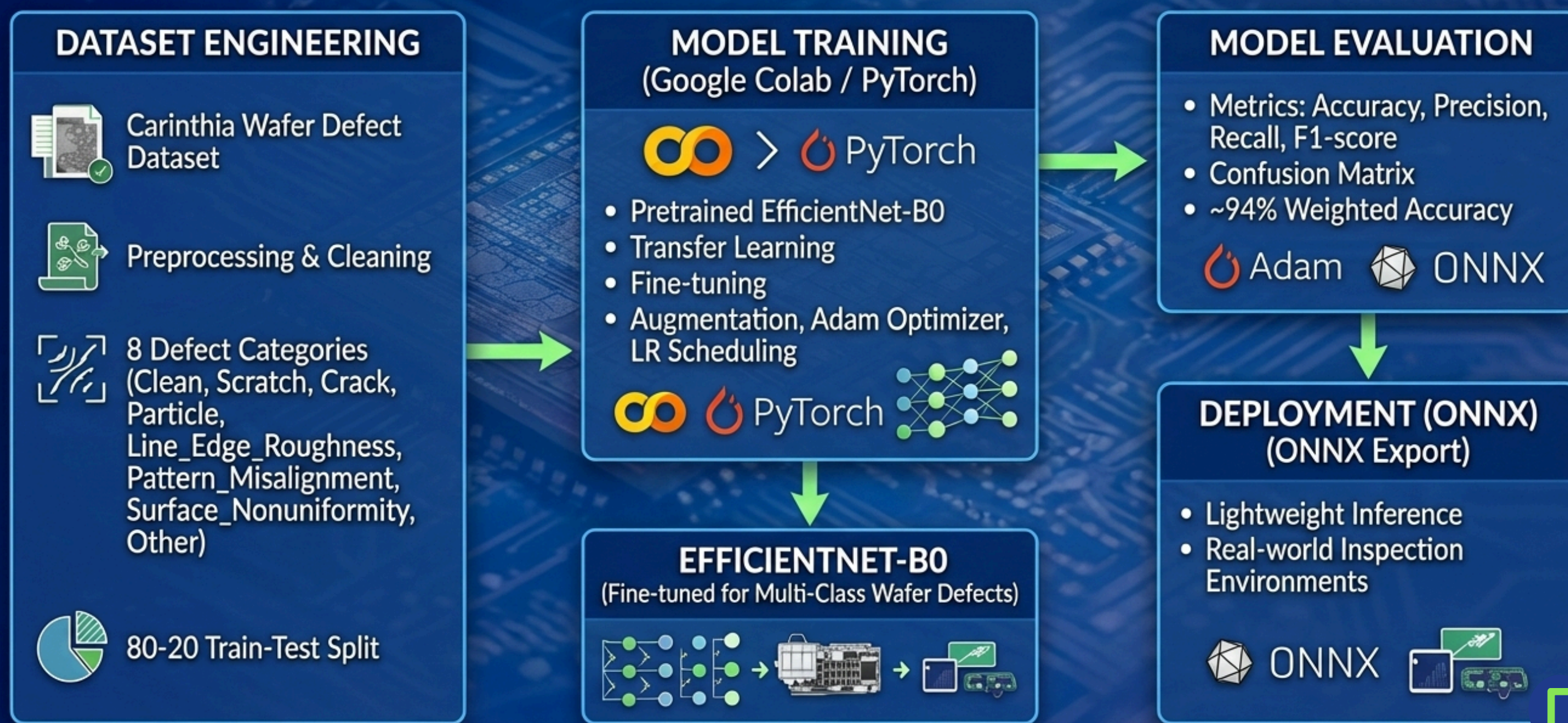
## SOLUTION OVERVIEW

A fine-tuned EfficientNet-B0 classifies wafer images into **8 classes**: Clean, Scratch, Crack, Particle, Line\_Edge\_Roughness, Pattern\_Misalignment, Surface\_Nonuniformity, and Other for fast, automated quality inspection



## Proposed Solution

### AUTOMATED DEEP LEARNING-BASED VISUAL INSPECTION PIPELINE FOR WAFER DEFECT CLASSIFICATION







# Dataset Plan & Class Design

## **Carinthia dataset**

← [click here for dataset](#)

Class List	Training Set	Testing Set
Clean	180	40
Crack	181	46
Line_Edge_Roughness	801	201
Pattern_Misalignment	801	201
Surface_Nonuniformity	801	201
Particle	231	58
Scratch	44	11
Other	810	204

**Total images: 4,591 images**

**No. of classes: 8 (6 defect classes + Clean + Other)**

**Train/Validation/Test split: 80 / 10 / 10**

**Image type: Grayscale wafer inspection images (preferred for defect visibility and reduced computation)**

**Labeling method: Manual**

## Results (Phase 1)

### Model Details

- **Architecture:** EfficientNet-B0 (lightweight CNN backbone)
- **Training approach:** Transfer Learning (ImageNet pretraining + fine-tuning)
- **Input size:** 224 × 224 (grayscale replicated to 3 channels)
- **Model size:** ~ 20 MB (ONNX-ready compact variant)
- **Framework:** PyTorch (trained in Google Colab)

**ONNX File Link**

### Training Strategy

- **Optimizer:** Adam
- **Learning rate:** Scheduled (StepLR decay)
- **Loss:** Cross-Entropy Loss
- **Data Augmentation:** Random rotation, horizontal/vertical flip, normalization
- **Train/Test split:** 80/20

### Metrics on Test Split (962 images)

- **Overall Accuracy:** 94.3%
- **Weighted Precision:** 0.9464
- **Weighted Recall:** 0.9428
- **Weighted F1-score:** 0.9437

# GitHub & Video Link



## GitHub Repository

[https://github.com/Ebiinesh/wafer\\_minds\\_deeptech\\_hackathon2026](https://github.com/Ebiinesh/wafer_minds_deeptech_hackathon2026)



## Prototype / Simulation Video

<https://drive.google.com/file/d/1m2CR6tNh1pl29nN5pMSDvudTbNMbTQoC/view?usp=sharing>

# Research and References



## Research Background & Methodology

Deep learning-based automated wafer defect inspection offers higher accuracy, consistency, and scalability compared to traditional manual and rule-based methods. In our work, we adopted a transfer learning approach by fine-tuning a pretrained EfficientNet-B0 model on the Carinthia wafer defect dataset, applying systematic data preprocessing and augmentation, and evaluating performance using accuracy, precision, recall, F1-score, and a confusion matrix to ensure reliable multi-class defect classification.



## References & Citations

List key papers, articles, or data sources.

[Ref 1] Carinthia Wafer Surface Defect Database – Public Dataset Repository / <https://zenodo.org/records/10715190>

[Ref 2] Tan, M., & Le, Q. (2019). EfficientNet: Rethinking Model Scaling for Convolutional Neural Networks / <https://arxiv.org/abs/1905.11946>

[Ref 3] He, K., Zhang, X., Ren, S., & Sun, J. (2016). Deep Residual Learning for Image Recognition / <https://arxiv.org/abs/1512.03385>