

PSoC® Creator™ Project Datasheet for LM502

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Table of Contents

1 Overview	
2 Pins	3
2.1 Hardware Pins	4
2.2 Hardware Ports	6
2.3 Software Pins	8
3 System Settings	10
3.1 System Configuration	10
3.2 System Debug Settings	
3.3 System Operating Conditions	
4 Clocks	
4.1 System Clocks	
4.2 Local and Design Wide Clocks	12
5 Interrupts	14
5.1 Interrupts	14
6 Flash Memory	15
7 Bootloader and Bootloadable	16
7.1 Bootloadable Application	16
7.2 Bootloader Application	16
8 Design Contents	18
8.1 Schematic Sheet: Page 1	18
9 Components	19
9.1 Component type: Bootloadable [v1.60]	19
9.1.1 Instance Bootloadable_1	19
9.2 Component type: SCB_P4 [v4.0]	19
9.2.1 Instance SPI_1	
9.2.2 Instance UART_1	
9.2.3 Instance UART_2	49
10 Other Resources.	



1 Overview

PSoC 4200S family is one of the smaller members of the PSoC 4 family of devices and is upward compatible with larger members of PSoC 4.

- High-performance, 32-bit single cycle Cortex-M0 CPU core
- Capacitive touch sensing (CapSense®)
- Configurable Timer/Counter/PWM block
- Two current sourcing/sinking DACs (IDACs)
- Comparator with 1.2 V reference
- · Configurable I2C block with master, slave, and multi-master operating modes
- Low-power operating modes including Sleep and Deep-Sleep

Figure 1 shows the major components of a typical <u>PSoC 4100S Plus</u> series member PSoC 4 device. For details on all the systems listed above, please refer to the <u>PSoC 4 Technical Reference Manual</u>.

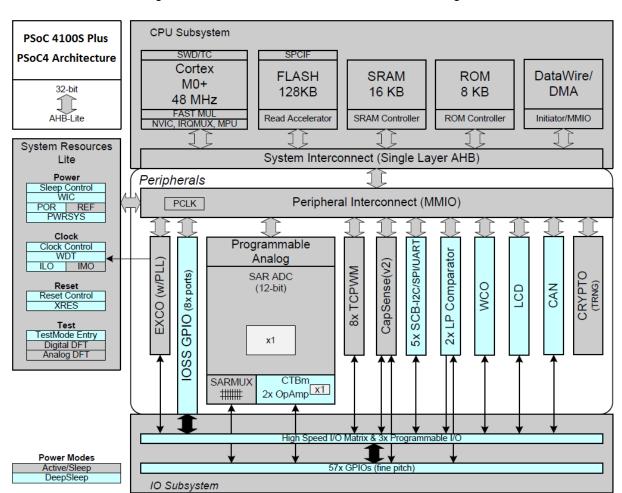


Figure 1. PSoC 4100S Plus Device Series Block Diagram



Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C4147AZI-S445
Package Name	64-TQFP
Family	PSoC 4
Series	PSoC 4100S Plus
Max CPU speed (MHz)	48
Flash size (kB)	128
SRAM size (kB)	16
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by HFCLK, listed in the <u>System Clocks</u> section below.

Table 2 lists the device resources that this design uses:

Table 2. Device Resources

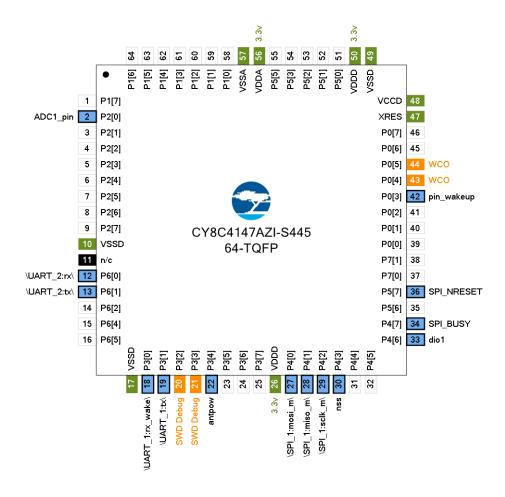
Resource Type	Used	Free	Max	% Used
Interrupts	4	24	28	14.29 %
10	18	36	54	33.33 %
Segment LCD	0	1	1	0.00 %
CapSense	0	1	1	0.00 %
Die Temp	0	1	1	0.00 %
Serial Communication (SCB)	3	2	5	60.00 %
DMA Channels	0	8	8	0.00 %
Timer/Counter/PWM	0	8	8	0.00 %
Crypto	0	1	1	0.00 %
Smart IO Ports	0	3	3	0.00 %
Comparator/Opamp	0	2	2	0.00 %
Comparator	0	1	1	0.00 %
LP Comparator	0	2	2	0.00 %
SAR ADC	0	1	1	0.00 %
DAC				
7-bit IDAC	0	2	2	0.00 %



2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout





2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

P1[7] GPIO [unused] Analog HiZ analog	Pin	Port	Name	Туре	Drive Mode
3	1	P1[7]	GPIO [unused]		
4 P2[2] GPIO [unused] 5 P2[3] GPIO [unused] 6 P2[4] GPIO [unused] 7 P2[5] GPIO [unused] 8 P2[6] GPIO [unused] 9 P2[7] GPIO [unused] 10 VSSD VSSD 12 P6[0] \UART_2:rx\ Dgtl In 13 P6[1] \UART_2:rx\ Dgtl Out 14 P6[2] GPIO [unused] 15 P6[4] GPIO [unused] 16 P6[5] GPIO [unused] 17 VSSD VSSD VSSD Power 18 P3[0] \UART_1:rx_wake\ Dgtl In 19 P3[1] \UART_1:rx_wake\ Dgtl Out 20 P3[2] Debug:SWD_CK Reserved 21 P3[3] Debug:SWD_CK Reserved 22 P3[4] antpow Software 23 P3[5] GPIO [unused] GPIO [unused] 25	2	P2[0]	ADC1_pin	Analog	HiZ analog
5 P2[3] GPIO [unused]	3	P2[1]	GPIO [unused]		
5 P2[3] GPIO [unused] 6 P2[4] GPIO [unused] 7 P2[5] GPIO [unused] 8 P2[6] GPIO [unused] 9 P2[7] GPIO [unused] 10 VSSD VSSD 12 P6[0] \UART_2:rx\ Dgtl In 13 P6[1] \UART_2:rx\ Dgtl In 14 P6[2] GPIO [unused] 15 P6[4] GPIO [unused] 16 P6[5] GPIO [unused] 17 VSSD VSSD VSSD VSSD Power 18 P3[0] \UART_1:rx_wake\ Dgtl In HiZ digital 19 P3[1] \UART_1:rx_wake\ Dgtl Out Strong drive 20 P3[2] Debug:SWD_CK Reserved 21 P3[3] Debug:SWD_CK Reserved 22 P3[4] antpow Software In/Out 23 P3[5] GPIO [unused] Strong drive 25	4	P2[2]	GPIO [unused]		
6 P2[4] GPIO [unused] 7 P2[5] GPIO [unused] 8 P2[6] GPIO [unused] 9 P2[7] GPIO [unused] 10 VSSD Power 12 P6[0] \UART_2:rx\ Dgtl In HiZ digital 13 P6[1] \UART_2:rx\ Dgtl Out Strong drive 14 P6[2] GPIO [unused] Feld GPIO [unused] Feld 15 P6[4] GPIO [unused] Feld Strong drive Strong drive Feld GPIO [unused] Feld GPIO [unused] G	5		GPIO [unused]		
7 P2[5] GPIO [unused] 9 8 P2[6] GPIO [unused] 9 9 P2[7] GPIO [unused] 9 10 VSSD VSSD Power 11 P6[0] \UART_2:rx\ Dgtl In HiZ digital 13 P6[1] \UART_2:rx\ Dgtl Out Strong drive 14 P6[2] GPIO [unused] 9 9 15 P6[4] GPIO [unused] 9 <td>6</td> <td></td> <td>GPIO [unused]</td> <td></td> <td></td>	6		GPIO [unused]		
8 P2[6] GPIO [unused] 9 P2[7] GPIO [unused] 10 VSSD VSSD 12 P6[0] \UART_2:rx\ Dgtl In 13 P6[1] \UART_2:rx\ Dgtl Out 14 P6[2] GPIO [unused] 15 P6[4] GPIO [unused] 16 P6[5] GPIO [unused] 17 VSSD VSSD VSSD VSSD Power 18 P3[0] \UART_1:rx_wake\ Dgtl In HiZ digital 19 P3[1] \UART_1:rx_wake\ Dgtl Out Strong drive 20 P3[2] Debug:SWD_IO Reserved 21 P3[3] Debug:SWD_CK Reserved 22 P3[4] antpow Software In/Out Strong drive 24 P3[6] GPIO [unused] GPIO [unused] Served 24 P3[6] GPIO [unused] GPIO [unused] Servered 25 P3[7] GPIO [unused] GPIO [unused] <td>7</td> <td>P2[5]</td> <td>GPIO [unused]</td> <td></td> <td></td>	7	P2[5]	GPIO [unused]		
10	8		GPIO [unused]		
10	9	P2[7]	GPIO [unused]		
13	10		VSSD	Power	
14	12	P6[0]	\UART_2:rx\	Dgtl In	HiZ digital
14 P6[2] GPIO [unused] 15 P6[4] GPIO [unused] 16 P6[5] GPIO [unused] 17 VSSD VSSD Power 18 P3[0] \UART_1:rx_wake\ Dgtl In HiZ digital 19 P3[1] \UART_1:rx_wake\ Dgtl Out Strong drive 20 P3[2] Debug:SWD_IO Reserved 21 P3[3] Debug:SWD_CK Reserved 22 P3[4] antpow Software In/Out 23 P3[5] GPIO [unused] Software In/Out 24 P3[6] GPIO [unused] GPIO [unused] 25 P3[7] GPIO [unused] Strong drive 26 VDDD VDDD Power 27 P4[0] \SPI_1:miso_m\ Dgtl Out Strong drive 28 P4[1] \SPI_1:scik_m\ Dgtl Out Strong drive 30 P4[3] nss Software In/Out Software 31 P4[4] GPIO [unused] <td>13</td> <td>P6[1]</td> <td>\UART_2:tx\</td> <td>Dgtl Out</td> <td>Strong drive</td>	13	P6[1]	\UART_2:tx\	Dgtl Out	Strong drive
15	14		GPIO [unused]		J
16	15		GPIO [unused]		
17 VSSD VSSD Power 18 P3[0] \UART_1:rx_wake\ Dgtl In HiZ digital 19 P3[1] \UART_1:rx_wake\ Dgtl Out Strong drive 20 P3[2] Debug:SWD_IO Reserved 21 P3[3] Debug:SWD_CK Reserved 22 P3[4] antpow Software In/Out 23 P3[5] GPIO [unused] Software In/Out 24 P3[6] GPIO [unused] GPIO [unused] 25 P3[7] GPIO [unused] GPIO [unused] 26 VDDD VDDD Power 27 P4[0] \SPI_1:mosi_m\ Dgtl Out Strong drive 28 P4[1] \SPI_1:scik_m\ Dgtl Out Strong drive 30 P4[3] nss Software In/Out Strong drive 31 P4[4] GPIO [unused] GPIO [unused] HIZ digital 32 P4[6] dio1 Software In/Out Software In/Out 34 P4[7]	16		GPIO [unused]		
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19 P3[1] \UART_1:tx\ Dgtl Out Strong drive 20 P3[2] Debug:SWD_IO Reserved 21 P3[3] Debug:SWD_CK Reserved 22 P3[4] antpow Software In/Out 23 P3[5] GPIO [unused] GPIO [unused] 24 P3[6] GPIO [unused] GPIO [unused] 25 P3[7] GPIO [unused] GPIO [unused] 26 VDDD VDDD Power 27 P4[0] \SPI_1:mosi_m\ Dgtl Out Strong drive 28 P4[1] \SPI_1:miso_m\ Dgtl In HiZ digital 29 P4[2] \SPI_1:sclk_m\ Dgtl Out Strong drive 30 P4[3] nss Software In/Out Strong drive 31 P4[4] GPIO [unused] GPIO [unused] Software In/Out HiZ digital 34 P4[7] SPI_BUSY Software In/Out Strong drive In/Out 35 P5[6] GPIO [unused] Software In/Out <t< td=""><td>18</td><td></td><td>\UART 1:rx wake\</td><td>Dgtl In</td><td>HiZ digital</td></t<>	18		\UART 1:rx wake\	Dgtl In	HiZ digital
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30 P4[3] nss Software In/Out Strong drive 31 P4[4] GPIO [unused] 32 P4[5] GPIO [unused] 40	$\overline{}$				
In/Out					
32 P4[5] GPIO [unused] 33 P4[6] dio1 Software In/Out down 34 P4[7] SPI_BUSY Software In/Out HiZ digital 35 P5[6] GPIO [unused] Software In/Out 36 P5[7] SPI_NRESET Software In/Out 37 P7[0] GPIO [unused] GPIO [unused] 38 P7[1] GPIO [unused] GPIO [unused] 40 P0[1] GPIO [unused] GPIO [unused]	30	P4[3]	nss		Strong arive
33 P4[6] dio1 Software In/Out down Res pull down 34 P4[7] SPI_BUSY Software In/Out HiZ digital HiZ digital In/Out 35 P5[6] GPIO [unused] Software In/Out Strong drive 36 P5[7] SPI_NRESET Software In/Out Strong drive 37 P7[0] GPIO [unused] GPIO [unused] 38 P7[1] GPIO [unused] GPIO [unused] 40 P0[1] GPIO [unused]	31	P4[4]	GPIO [unused]		
In/Out down	32	P4[5]	GPIO [unused]		
34 P4[7] SPI_BUSY Software In/Out HiZ digital 35 P5[6] GPIO [unused] Strong drive 36 P5[7] SPI_NRESET Software In/Out 37 P7[0] GPIO [unused] GPIO [unused] 38 P7[1] GPIO [unused] GPIO [unused] 39 P0[0] GPIO [unused] GPIO [unused] 40 P0[1] GPIO [unused] GPIO [unused]	33	P4[6]	dio1	I	
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36 P5[7] SPI_NRESET Software In/Out Strong drive 37 P7[0] GPIO [unused] 9	35	P5[6]	GPIO [unused]	104	
37 P7[0] GPIO [unused] 38 P7[1] GPIO [unused] 39 P0[0] GPIO [unused] 40 P0[1] GPIO [unused]					Strong drive
38 P7[1] GPIO [unused] 39 P0[0] GPIO [unused] 40 P0[1] GPIO [unused]	37	P7[0]	GPIO [unused]	1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	
39 P0[0] GPIO [unused] 40 P0[1] GPIO [unused]					
40 P0[1] GPIO [unused]					
			•		
	41	P0[2]	GPIO [unused]	1	



Pin	Port	Name	Туре	Drive Mode
42	P0[3]	pin_wakeup	Software	Res pull
			In/Out	down
43	P0[4]	XTAL 32kHz:Xi	Reserved	
44	P0[5]	XTAL 32kHz:Xo	Reserved	
45	P0[6]	GPIO [unused]		
46	P0[7]	GPIO [unused]		
47	XRES	XRES	Dedicated	
48	VCCD	VCCD	Power	
49	VSSD	VSSD	Power	
50	VDDD	VDDD	Power	
51	P5[0]	GPIO [unused]		
52	P5[1]	GPIO [unused]		
53	P5[2]	GPIO [unused]		
54	P5[3]	GPIO [unused]		
55	P5[5]	GPIO [unused]		
56	VDDA	VDDA	Power	
57	VSSA	VSSA	Power	
58	P1[0]	GPIO [unused]		
59	P1[1]	GPIO [unused]		
60	P1[2]	GPIO [unused]		
61	P1[3]	GPIO [unused]		
62	P1[4]	GPIO [unused]		
63	P1[5]	GPIO [unused]		
64	P1[6]	GPIO [unused]		

Abbreviations used in Table 3 have the following meanings:

- HiZ analog = High impedance analog
- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- Dgtl Out = Digital Output
- Res pull down = Resistive pull down



2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode
P0[0]	39	GPIO [unused]		
P0[1]	40	GPIO [unused]		
P0[2]	41	GPIO [unused]		
P0[3]	42	pin_wakeup	Software In/Out	Res pull down
P0[4]	43	XTAL 32kHz:Xi	Reserved	
P0[5]	44	XTAL 32kHz:Xo	Reserved	
P0[6]	45	GPIO [unused]		
P0[7]	46	GPIO [unused]		
P1[0]	58	GPIO [unused]		
P1[1]	59	GPIO [unused]		
P1[2]	60	GPIO [unused]		
P1[3]	61	GPIO [unused]		
P1[4]	62	GPIO [unused]		
P1[5]	63	GPIO [unused]		
P1[6]	64	GPIO [unused]		
P1[7]	1	GPIO [unused]		
P2[0]	2	ADC1_pin	Analog	HiZ analog
P2[1]	3	GPIO [unused]		
P2[2]	4	GPIO [unused]		
P2[3]	5	GPIO [unused]		
P2[4]	6	GPIO [unused]		
P2[5]	7	GPIO [unused]		
P2[6]	8	GPIO [unused]		
P2[7]	9	GPIO [unused]	D.:41.1:	1117 11 114 1
P3[0]	18	\UART_1:rx_wake\	Dgtl In	HiZ digital
P3[1]	19	\UART_1:tx\	Dgtl Out	Strong drive
P3[2]	20	Debug:SWD_IO	Reserved	
P3[3]	21	Debug:SWD_CK	Reserved	04
P3[4]	22	antpow	Software In/Out	Strong drive
P3[5]	23	GPIO [unused]		
P3[6]	24	GPIO [unused]		
P3[7]	25	GPIO [unused]		
P4[0]	27	\SPI_1:mosi_m\	Dgtl Out	Strong drive
P4[1]	28	\SPI_1:miso_m\	Dgtl In	HiZ digital
P4[2]	29	\SPI_1:sclk_m\	Dgtl Out	Strong drive
P4[3]	30	nss	Software In/Out	Strong drive
P4[4]	31	GPIO [unused]		
P4[5]	32	GPIO [unused]		
P4[6]	33	dio1	Software In/Out	Res pull down
P4[7]	34	SPI_BUSY	Software In/Out	HiZ digital
P5[0]	51	GPIO [unused]		



Port	Pin	Name	Type	Drive Mode
P5[1]	52	GPIO [unused]		
P5[2]	53	GPIO [unused]		
P5[3]	54	GPIO [unused]		
P5[5]	55	GPIO [unused]		
P5[6]	35	GPIO [unused]		
P5[7]	36	SPI_NRESET	Software In/Out	Strong drive
P6[0]	12	\UART_2:rx\	Dgtl In	HiZ digital
P6[1]	13	\UART_2:tx\	Dgtl Out	Strong drive
P6[2]	14	GPIO [unused]		
P6[4]	15	GPIO [unused]		
P6[5]	16	GPIO [unused]		
P7[0]	37	GPIO [unused]		
P7[1]	38	GPIO [unused]	·	

Abbreviations used in Table 4 have the following meanings:

- Res pull down = Resistive pull down
- HiZ analog = High impedance analog
- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- Dgtl Out = Digital Output



2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type
\SPI_1:miso_m\	P4[1]	Dgtl In
\SPI_1:mosi_m\	P4[0]	Dgtl Out
\SPI_1:sclk_m\	P4[2]	Dgtl Out
\UART_1:rx_wake\	P3[0]	Dgtl In
\UART_1:tx\	P3[1]	Dgtl Out
\UART_2:rx\	P6[0]	Dgtl In
\UART_2:tx\	P6[1]	Dgtl Out
ADC1_pin	P2[0]	Analog
antpow	P3[4]	Software In/Out
Debug:SWD_CK	P3[3]	Reserved
Debug:SWD_IO	P3[2]	Reserved
dio1	P4[6]	Software In/Out
GPIO [unused]	P0[0]	
GPIO [unused]	P5[6]	
GPIO [unused]	P0[7]	
GPIO [unused]	P7[0]	
GPIO [unused]	P7[1]	
GPIO [unused]	P0[1]	
GPIO [unused]	P0[6]	
GPIO [unused]	P0[2]	
GPIO [unused]	P1[2]	
GPIO [unused]	P1[1]	
GPIO [unused]	P1[0]	
GPIO [unused]	P1[5]	
GPIO [unused]	P1[4]	
GPIO [unused]	P1[3]	
GPIO [unused]	P5[1]	
GPIO [unused]	P5[0]	
GPIO [unused]	P1[6]	
GPIO [unused]	P5[5]	
GPIO [unused]	P5[3]	
GPIO [unused]	P5[2]	
GPIO [unused]	P3[5]	
GPIO [unused]	P2[5]	
GPIO [unused]	P2[4]	
GPIO [unused]	P3[6]	
GPIO [unused]	P2[6]	
GPIO [unused]	P6[2]	
GPIO [unused]	P2[7]	
GPIO [unused]	P6[5]	
GPIO [unused]	P6[4]	
GPIO [unused]	P4[4]	
GPIO [unused]	P1[7]	
GPIO [unused]	P2[1]	



Name	Port	Туре
GPIO [unused]	P4[5]	
GPIO [unused]	P2[3]	
GPIO [unused]	P2[2]	
GPIO [unused]	P3[7]	
nss	P4[3]	Software In/Out
pin_wakeup	P0[3]	Software In/Out
SPI_BUSY	P4[7]	Software In/Out
SPI_NRESET	P5[7]	Software In/Out
XTAL 32kHz:Xi	P0[4]	Reserved
XTAL 32kHz:Xo	P0[5]	Reserved

Abbreviations used in Table 5 have the following meanings:

- Dgtl In = Digital Input
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the <u>System Reference Guide</u>
 CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet



3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Unused Bonded IO	Disallowed
Heap Size (bytes)	0x1800
Stack Size (bytes)	0x0100
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD (serial wire debug)
Chip Protection	Open

3.3 System Operating Conditions

Table 8. System Operating Conditions

Name	Value
VDDA (V)	3.3
VDDD (V)	3.3
Variable VDDA	True

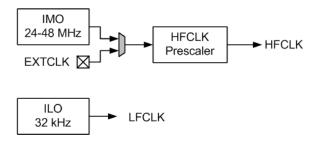


4 Clocks

The clock system includes these clock resources:

- Two internal clock sources:
 - o 24 to 48 MHz Internal Main Oscillator (IMO) ±2% at all frequencies with trim
 - o 32 kHz Internal Low Speed Oscillator (ILO)
- External clock (EXTCLK) generated using a signal from an I/O pin
- High-frequency clock (HFCLK) of up to 48 MHz selected from IMO or external clock
- Dedicated prescaler for HFCLK
- Low-frequency clock (LFCLK sourced by ILO
 - o Dedicated prescaler for system clock (SYSCLK) of up to 48 MHz sourced by HFCLK
- 24 to 48 MHz Internal Main Oscillator (IMO) ±2%

Figure 3. System Clock Configuration





4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired	Nominal	Accuracy	Start	Enabled
			Freq	Freq	(%)	at	
						Reset	
SysClk	NONE	HFClk	? MHz	24 MHz	±2	True	True
PLL0_Sel	NONE	IMO	24 MHz	24 MHz	±2	True	True
IMO	NONE		24 MHz	24 MHz	±2	True	True
HFClk	NONE	IMO	24 MHz	24 MHz	±2	True	True
ILO	NONE		40 kHz	40 kHz	-50,+100	True	True
LFClk	NONE	ILO	? MHz	40 kHz	-50,+100	True	True
Timer_Sel	NONE	WCO	32.768	32.768	±0.015	True	True
			kHz	kHz			
WCO	NONE		32.768	32.768	±0.015	False	True
			kHz	kHz			
RTC_Sel	NONE		? MHz	? MHz	±0	True	True
Timer1	NONE	Timer_Sel	? MHz	? MHz	±0	False	False
Timer2	NONE	Timer_Sel	? MHz	? MHz	±0	False	False
ExtClk	NONE		16 MHz	? MHz	±0	False	False
Timer (WDT)	NONE	LFClk	? MHz	? MHz	±0	False	False
PLL0	NONE	PLL0_Sel	24 MHz	? MHz	±2	False	False
Timer0	NONE	Timer_Sel	? MHz	? MHz	±0.015	False	False
ECO	NONE		24 MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

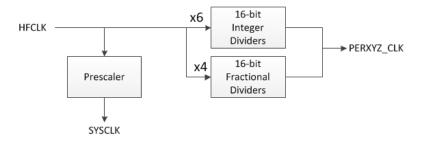


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
SPI_1_SCBCLK	FIXED FUNCT- ION	HFClk	48 MHz	24 MHz	±2	True	True



Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
UART_1 SCBCLK	FIXED FUNCT- ION	HFClk	1.498 MHz	1.5 MHz	±2	True	True
UART_2 SCBCLK	FIXED FUNCT- ION	HFCIk	1.382 MHz	1.412 MHz	±2	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 4 Technical Reference Manual
- - CySysClkPll0 API routines
 - CySysClkEco API routines
 - CySysClkWco API routines
 - o CySysClkWrite API routines



5 Interrupts

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	Vector	Priority
wakeup_irq	0	0	3
UART_1_RX_WAKEUP_IRQ	3	3	3
global_irq	4	4	2
UART_1_SCB_IRQ	8	8	0

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 4 Technical Reference Manual
- Interrupts chapter in the <u>System Reference Guide</u>
 Cylnt API routines and related registers
- Datasheet for cy isr component



6 Flash Memory

PSoC 4 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x1FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U Unprotected
- W Full Protection

For more information on Flash memory and protection, please refer to:

- Flash Protection chapter in the <u>PSoC 4 Technical Reference Manual</u>
- Flash and EEPROM chapter in the **System Reference Guide**
 - CySysFlash API routines

LM502 Datasheet 09/16/2019 13:40 15



7 Bootloader and Bootloadable

Figure 5 details the Flash memory map for the bootloader and/or bootloadable application(s) included in this design.

Figure 5. Bootloader Memory Map

Bootloadable application

Start Address 1

Bootloader application

7.1 Bootloadable Application

Table 13. Bootloadable Settings

Name	Value
Application Version	0x0000
Application ID	0x0000
Application Custom ID	0x0
Application Image 1 Start Address	0x1600
Application Image 1 End Address	0x1FFFF
Manual Application Image Placement	False

Address 0

7.2 Bootloader Application

Table 14. Bootloader Settings

3	
Name	Value
Checksum Type	BasicChecksum
Supports Multiple Application Images	False
Application Version	0x0000
Bootloader Start Address	0x0
Bootloader End Address	0x15B5

For more information on the bootloader and startup please refer to:

• Startup and Linking chapter in the <u>System Reference Guide</u>



• Datasheet for Bootloader and Bootloadable component

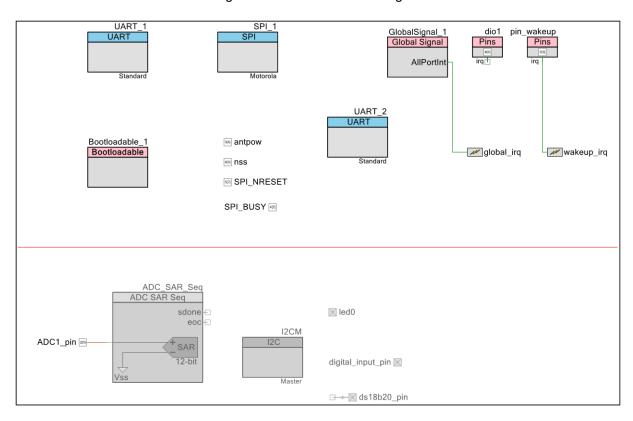


8 Design Contents

This design's schematic content consists of the following schematic sheet:

8.1 Schematic Sheet: Page 1

Figure 6. Schematic Sheet: Page 1



This schematic sheet contains the following component instances:

- Instance Bootloadable_v1_60)
- Instance SPI_1 (type: SCB_P4_v4_0)
- Instance <u>UART_1</u> (type: SCB_P4_v4_0)
- Instance <u>UART_2</u> (type: SCB_P4_v4_0)



9 Components

9.1 Component type: Bootloadable [v1.60]

9.1.1 Instance Bootloadable_1

Description: Provides bootloadable application functionality.

Instance type: Bootloadable [v1.60]

Datasheet: online component datasheet for Bootloadable

Table 15. Component Parameters for Bootloadable_1

Parameter Name	Value	Description
appCustomID	0	Provides a 4 byte custom ID
		number to represent anything in
		the Bootloadable application.
appID	0	Provides a 2 byte number to
		represent the ID of the
		bootloadable application.
appVersion	0	Provides a 2 byte number to
		represent the version of the
		bootloadable application.
autoPlacement	true	Provides a method for PSoC
		Creator to place a Bootloadable
		application image at a specified location. If true, the image will
		be placed automatically. If false,
		the image will be placed at an
		address specified by the
		Placement Address option.
checksumExcludeSize	0	Provides a size in bytes of
		checksum exclude section
elfFilePath	.\bootloader.cydsn\C-	Provides a reference to the
	ortexM0p\ARM_GCC	Bootloader application (.elf) that
	541\Debug\bootloader.elf	is associated with this
		Bootloadable application.
hexFilePath	.\bootloader.cydsn\C-	Provides a reference to the
	ortexM0p\ARM_GCC	Bootloader application (.hex)
	541\Debug\bootloader.hex	that is associated with this
		Bootloadable application.
placementAddress	0	Allows specifying an address
		where the bootloadable
		application will be placed in the
		memory. Available only if the
		Automatic Application Image Placement option is true.
User Comments		Instance-specific comments.
USEI CUIIIIEIIIS		matance-specific comments.

9.2 Component type: SCB_P4 [v4.0]

9.2.1 Instance SPI_1

Description: Serial Communication Block (SCB)

Instance type: SCB_P4 [v4.0]

Datasheet: online component datasheet for SCB_P4

Table 16. Component Parameters for SPI_1

LM502 Datasheet 09/16/2019 13:40 19



Parameter Name	Value	Description
Ezl2cByteModeEnable	false	When the SCB mode is EZI2C,
		this parameter specifies the
		number of bits per FIFO data
		element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO
		depth is 8 entries. The byte mode – true: an 8-bit
		FIFO data element. The FIFO
		depth is 16 entries.
		·
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
Ezl2cClockFromTerm	false	When the SCB mode is EZI2C,
		this parameter provides a clock terminal to connect a clock
		outside the component.
Ezl2cClockStretching	true	When the SCB mode is EZI2C,
LZIZGOIOGROTI etci ii i ig	lide	this parameter specifies
		whether the SCL is stretched
		while in EZI2C operation.
Ezl2cDataRate	100	When the SCB mode is EZI2C,
		this parameter defines EZI2C
		Data rate in kbps. The standard
		data rates are: 100, 400 and
E-10 Ni i Off A Live		1000 kbps.
Ezl2cNumberOfAddresses	1	When the SCB mode is EZI2C, this parameter defines the
		number of I2C slave addresses
		that device respond to.
Ezl2cPrimarySlaveAddress	8	When the SCB mode is EZI2C,
,		this parameter specifies EZI2C
		primary 7-bits slave address
		(MSB ignored).
Ezl2cSecondarySlaveAddress	9	When the SCB mode is EZI2C,
		this parameter specifies EZI2C
		secondary 7-bits slave address
		(MSB ignored). Only applicable when EZI2C
		clock stretching option is set.
Ezl2cSubAddressSize	8	When the SCB mode is EZI2C,
EZIZOGUM (GGIOGOZIZO		this parameter specifies the
		maximum size of the slave
		buffer that is exposed to the
		master: 8bits – maximum buffer
		size is 256 bytes, 16 bits –
		maximum buffer size is 65535
F-IO-)Walta Frankla	£.1	bytes.
Ezl2cWakeEnable	false	When the SCB mode is EZI2C,
		this parameter enables wakeup from Deep Sleep on I2C
		address match event.
		address materies



Parameter Name	Value	Description
I2C Bus Voltage	3.3	When the SCB mode is I2C, this parameter specifies the voltage applied to the pull-up resistors on the I2C bus.
		Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2C Bus Voltage	3.3	When the SCB mode is EZI2C, this parameter specifies the voltage applied to the pull-up resistors on the I2C bus. Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2cAcceptAddress	false	When the SCB mode is I2C, this parameter specifies whether to accept the match slave address in RX FIFO or not. All slave matched addresses are ACKed. The user has to register the callback function to handle accepted addresses. This feature has to be used when more than one address support is required.
I2cAcceptGeneralCall	false	When the SCB mode is I2C, this parameter specifies whether to accept the general call address. The general call address is ACKed when accepted and NAKed otherwise. The user has to register the callback function to handle the general call address.
I2cByteModeEnable	false	When the SCB mode is I2C, this parameter specifies the number of bits per FIFO data element. The byte mode – false: a 16-bit FIFO data element. The FIFO depth is 8 entries. The byte mode – true: an 8-bit FIFO data element. The FIFO depth is 16 entries. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2cClockFromTerm	false	When the SCB mode is I2C, this parameter provides a clock terminal to connect a clock outside the component.
I2cDataRate	100	When the SCB mode is I2C, this parameter specifies the data rate in kbps. The standard data rates are: 100, 400 and 1000 kbps.



Parameter Name	Value	Description
I2cExternIntrHandler	false	When the SCB mode is I2C, this parameter specifies whether the I2C interrupt handler is configured in SCB_I2CInit(). This parameter is intended to be used by the PM/SM bus component. The modification parameter default value causes I2C mode failures.
I2cManualOversampleControl	true	When the SCB mode is I2C, this parameter specifies the method of calculating the oversampling as manual or automatic.
I2cMode	Slave	When the SCB mode is I2C, this parameter defines the I2C operation mode as: Slave, Master, Multi-Master or Multi-Master-Slave.
I2cOvsFactor	16	When the SCB mode is I2C, this parameter defines the oversampling factor of SCBCLK.
I2cOvsFactorHigh	8	When the SCB mode is I2C, this parameter defines the high oversampling factor of SCBCLK. Only applicable for I2C Master modes.
I2cOvsFactorLow	8	When the SCB mode is I2C, this parameter defines the low oversampling factor of SCBCLK. Only applicable for I2C Master modes.
I2cSlaveAddress	8	When the SCB mode is I2C, this parameter specifies the I2C 7-bits slave address (MSB ignored).
I2cSlaveAddressMask	254	When the SCB mode is I2C, this parameter specifies the I2C Slave address mask. Bit value 0 – excludes bit from address comparison. Bit value 1 – the bit needs to match with the corresponding bit of the I2C slave address.
I2cWakeEnable	false	When the SCB mode is I2C, this parameter enables wakeup from Deep Sleep on an I2C address match event.
ScbMisoSdaTxEnable	true	This parameter defines the availability of the spi_miso_i2csda_uart_tx pin.
ScbMode	SPI	This parameter defines the mode of operation for the SCB component.
ScbMosiSclRxEnable	true	This parameter defines the availability of the spi_mosi_i2cscl_uart_rx pin.



Parameter Name	Value	Description
ScbRxWakeIrqEnable	false	This parameter defines the
		availability of the spi_mosi_i2c
		scl_uart_rx_wake pin.
ScbSclkEnable	false	This parameter defines the
		availability of the sclk pin.
ScbSs0Enable	false	This parameter defines the
		availability of the ss0 pin.
ScbSs1Enable	false	This parameter defines the
		availability of the ss1 pin.
ScbSs2Enable	false	This parameter defines the
		availability of the ss2 pin.
ScbSs3Enable	false	This parameter defines the
		availability of the ss3 pin.
Show EZI2C Terminals	false	When the SCB mode is EZI2C,
		this parameter removes internal
		pins and expose signals to
		terminals. The exposed
		terminals must be connected to
		the pins.
Show I2C Terminals	false	When the SCB mode is I2C, this
		parameter removes internal pins
		and expose signals to terminals.
		The exposed terminals must be
OL OBLE		connected to the pins.
Show SPI Terminals	false	When the SCB mode is SPI,
		this parameter removes internal
		pins and expose signals to terminals. The exposed
		terminals must be connected to
		the pins or SmartIO component.
Show UART Terminals	false	When the SCB mode is UART,
Show OART Terminals	laise	this parameter removes internal
		pins and expose signals to
		terminals. The exposed
		terminals must be connected to
		the pins or SmartIO component.
Slew Rate	Fast	When the SCB mode is EZI2C,
		this parameter specifies the
		slew rate settings of the I2C
		pins.
		For devices supporting GPIO
		Over-Voltage Tolerance
		(GPIO_OVT) pins, I2C FM+
		options should be used when
		I2C data rate is greater than
		400 kbps. This option also
		requires the I2C bus voltage to
		be defined.Refer to the Device
		Datasheet to determine which
		pins are GPIO_OVT capable.



Parameter Name	Value	Description EMBEDDED IN TO
Slew Rate	Fast	When the SCB mode is I2C, this
Ciew itale	1 431	parameter specifies the slew
		rate settings of the I2C pins.
		For devices supporting GPIO
		Over-Voltage Tolerance
		(GPIO_OVT) pins, I2C FM+
		options should be used when
		I2C data rate is greater than
		400 kbps. This option also
		requires the I2C bus voltage to
		be defined. Refer to the Device
		Datasheet to determine which
		pins are GPIO_OVT capable.
CmiDitData	0000	
SpiBitRate	8000	When the SCB mode is SPI,
		this parameter specifies the Bit
		rate in kbps (up to 8000 kbps);
		the actual rate may differ based
		on available clock frequency
		and component settings. This
		parameter has no effect if the
		Clock from terminal parameter
		is enabled.
SpiBitsOrder	MSB First	When the SCB mode is SPI,
		this parameter defines the bit
		order as: MSB first or LSB first.
SpiByteModeEnable	false	When the SCB mode is SPI,
		this parameter specifies the
		number of bits per FIFO data
		element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO
		depth is 8 entries.
		The byte mode – true: an 8-bit
		FIFO data element. The FIFO
		depth is 16 entries.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
SpiClockFromTerm	false	When the SCB mode is SPI,
		this parameter provides a clock
		terminal to connect a clock
		outside the component.
SpiFreeRunningSclk	false	When the SCB mode is SPI,
		this parameter specifies the
		SCLK generation by the master
		as: gated or free running
		(continuous).
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.



Parameter Name	Value	Description
SpilnterruptMode	None	When the SCB mode is SPI, this parameter specifies the interrupt mode. None: Removes all interrupt support. Internal: Leaves the interrupt SCBIRQ inside the component - the interrupt terminal becomes invisible. External: Provides an interrupt terminal to connect an interrupt outside the component.
SpilntrMasterSpiDone	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_M. SPI_DONE interrupt source. SCB.INTR_M. SPI_DONE: all data are sent into TX FIFO and the TX FIFO and the shifter register are emptied. Only applicable for SPI Master mode.
SpiIntrRxFull	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.FULL interrupt source. SCB.INTR_RX.FULL trigger condition: RX FIFO is full.
SpiIntrRxNotEmpty	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.NOT_EMPTY interrupt source. SCB.INTR_RX.NOT_EMPTY trigger condition: RX FIFO is not empty. There is at least one entry to get data from.
SpiIntrRxOverflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to write to a full RX FIFO.
SpiIntrRxTrigger	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.TRIGGER interrupt source. SCB.INTR_RX.TRIGGER trigger condition: remains active until RX FIFO has more entries than the value specified by SpiRxTriggerLevel.
SpiIntrRxUnderflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.UNDERFLOW interrupt source. SCB.INTR_RX.UNDERFLOW trigger condition: attempt to read from an empty RX FIFO.



TODILLI OLAYODUSELLOL I MILEL LINE SC	Cription CB mode is SPI,
	ter enables the
	SLAVE.BUS
	errupt source.
SCB.INTR_	SLAVE.BUS
	r condition: slave
	deselected at an
· ·	time in the SPI
	nsfer.
	ole for SPI Slave
	ode.
	CB mode is SPI,
	ter enables the
	EMPTY interrupt
	urce. X.EMPTY trigger
	FIFO is empty.
	CB mode is SPI,
'	ter enables the
	TX.NOT_FULL
	ot source.
	TX.NOT_FULL
trigger conditio	n: TX FIFO is not
	at least one entry
·	ut data.
· ·	CB mode is SPI,
	ter enables the
	X.OVERFLOW
	ot source.
	X.OVERFLOW tion: attempt to
	full TX FIFO.
	CB mode is SPI,
	ter enables the
	TX.TRIGGER
	ot source.
SCB.INTR_	TX.TRIGGER
	n: remains active
	has fewer entries
	ue specified by
·	iggerLevel.
	CB mode is SPI,
	ter enables the
	X.UNDERFLOW ot source.
	X.UNDERFLOW
	tion: attempt to
	empty TX FIFO.
	CB mode is SPI,
· · · · · · · · · · · · · · · · · · ·	ter enables late
	he MISO line by
the r	master.
'	CB mode is SPI,
	r applies a digital
· · · · · · · · · · · · · · · · · · ·	filter to the SPI
inpu	ut line.



Parameter Name	Value	Description
SpiMode	Master	When the SCB mode is SPI, this parameter selects SPI mode of operation as: Slave or Master.
SpiNumberOfRxDataBits	8	When the SCB mode is SPI, this parameter specifies the number of data bits inside the SPI byte/word for RX direction.
SpiNumberOfSelectLines	0	When the SCB mode is SPI, this parameter defines the number of slave select lines. The SPI Slave has only one slave select line. The SPI Master has up to 4 lines.
SpiNumberOfTxDataBits	8	When the SCB mode is SPI, this parameter define the number of data bits inside the SPI byte/word for TX direction.
SpiOvsFactor	8	When the SCB mode is SPI, this parameter defines the oversampling factor of SCBCLK.
SpiRemoveMiso	false	When the SCB mode is SPI, this parameter removes the MISO pin.
SpiRemoveMosi	false	When the SCB mode is SPI, this parameter removes the MOSI pin.
SpiRemoveSclk	false	When the SCB mode is SPI, this parameter removes the SCLK pin.
SpiRxBufferSize	8	When the SCB mode is SPI, this parameter defines the size of the RX buffer.
SpiRxOutputEnable	false	When the SCB mode is SPI, this parameter enables the RX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.
SpiRxTriggerLevel	7	When the SCB mode is SPI, this parameter defines the number of entries in the RX FIFO to control the SCB.INTRRX.TRIGGER interrupt event or RX DMA trigger output.
SpiSclkMode	CPHA = 0, CPOL = 0	When the SCB mode is SPI, this parameter defines the serial clock phase (CPHA) and polarity (CPOL).
SpiSs0Polarity	Active Low	When the SCB mode is SPI, this parameter specifies active polarity of slave select 0. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.

LM502 Datasheet 09/16/2019 13:40 27



Parameter Name	Value	Description
SpiSs1Polarity	Active Low	When the SCB mode is SPI,
Opios ir dianty	Active Low	this parameter specifies active
		polarity of slave select 1.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
SpiSs2Polarity	Active Low	When the SCB mode is SPI,
		this parameter specifies active polarity of slave select 2.
		Applicable only for devices
		other than PSoC 4000/PSoC 4100/PSoC 4200.
SpiSs3Polarity	Active Low	When the SCB mode is SPI,
opiessi siamy	7,6475 254	this parameter specifies active polarity of slave select 3.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
SpiSubMode	Motorola	When the SCB mode is SPI,
		this parameter defines the sub
		mode of the SPI as: Motorola,
		TI(Start Coincides), TI(Start Precedes), or National
		Semiconductor.
SpiTransferSeparation	Continuous	When the SCB mode is SPI,
'		this parameter defines the type
		of SPI transfers separation as:
		continuous or separated.
SpiTxBufferSize	8	When the SCB mode is SPI,
		this parameter defines the size
SpiTxOutputEnable	false	of the TX buffer. When the SCB mode is SPI,
SpirkOdiputEnable	laise	this parameter enables the TX
		trigger output terminal of the
		component. This terminal must
		be connected to the DMA input
		trigger or left unconnected. Only
		applicable for devices which
SpiTyTriggorl syst		have a DMA controller.
SpiTxTriggerLevel	0	When the SCB mode is SPI, this parameter defines the
		number of entries in the TX
		FIFO to control the SCB.INTR
		TX.TRIGGER interrupt event or
		TX DMA trigger output.
SpiWakeEnable	false	When the SCB mode is SPI,
		this parameter enables wakeup
		from Deep Sleep on slave select event.
		Select event.



Parameter Name	Value	Description
UartByteModeEnable	false	When the SCB mode is UART,
		this parameter specifies the
		number of bits per FIFO data element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO depth is 8 entries.
		The byte mode – true: an 8-bit
		FIFO data element. The FIFO depth is 16 entries.
		Applicable only for devices
		other than PSoC 4000/PSoC 4100/PSoC 4200.
UartClockFromTerm	false	When the SCB mode is UART,
		this parameter provides a clock terminal to connect a clock
UartCtsEnable	false	outside the component. When the SCB mode is UART,
CartotsEriable	laise	this parameter enables the cts input.
		Only applicable for devices other than PSoC 4000/PSoC
		4100/PSoC 4200.
UartCtsPolarity	Active Low	When the SCB mode is UART,
		this parameter specifies active polarity of an input cts signal.
		Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartDataRate	115200	When the SCB mode is UART,
		this parameter specifies the
		Baud rate in bps (up to 1000
		kbps); the actual rate may differ based on available clock
		frequency and component
		settings. This parameter has no
		effect if the Clock from terminal
		parameter is enabled.
UartDirection	TX + RX	When the SCB mode is UART,
		this parameter enables RX or TX direction or both
		simultaneously.
UartDropOnFrameErr	false	When the SCB mode is UART,
·		this parameter defines whether
		the data is dropped from RX
Lieut Due vo Ora De vita (Fur	£.1	FIFO on a frame error event.
UartDropOnParityErr	false	When the SCB mode is UART, this parameter determines
		whether the data is dropped
		from RX FIFO on a parity error
		event.



Parameter Name Value Description UartInterruptMode None When the SCB mode is UART, this parameter specifies the interrupt mode. None: Removes all interrupt support. Internal: Leaves the interrupt SCBIRQ inside the component - the interrupt terminal becomes invisible. External: Provides an interrupt terminal to connect an interrupt outside component. UartIntrRxBreakDetected false This parameter enables the RX break detection interrupt source to trigger the interrupt output. UartIntrRxFrameErr false When the SCB mode is UART, this parameter enables the SCB.INTR_RX.FRAMEERROR interrupt source. UartIntrRxFull false When the SCB mode is UART, this parameter enables the SCB.INTR_RX.FULL interrupt source. UartIntrRxFull false When the SCB mode is UART, this parameter enables the SCB.INTR_RX.FULL interrupt source. UartIntrRxNotEmpty false When the SCB mode is UART, this parameter enables the SCB.INTR_RX.NOT_EMPTY interrupt source. UartIntrRxNotEmpty false When the SCB mode is UART, this parameter enables the SCB.INTR_RX.NOT_EMPTY interrupt source. UartIntrRxOverflow false When the SCB mode is UART, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. UartIntrRxOverflow false When the SCB mode is UART, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source.
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Condition: RX FIFO is full. UartIntrRxNotEmpty false When the SCB mode is UART, this parameter enables the SCB.INTR_RX.NOT_EMPTY interrupt source. SCB.INTR_RX.NOT_EMPTY trigger condition: RX FIFO is not empty. There is at least one entry to get data from. UartIntrRxOverflow false When the SCB mode is UART, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to
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SCB.INTR_RX.NOT_EMPTY trigger condition: RX FIFO is not empty. There is at least one entry to get data from. UartIntrRxOverflow false When the SCB mode is UART, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to
trigger condition: RX FIFO is not empty. There is at least one entry to get data from. UartIntrRxOverflow false When the SCB mode is UART, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to
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SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to
interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to
SCB.INTR_RX.OVERFLOW trigger condition: attempt to
trigger condition: attempt to
UartIntrRxParityErr false When the SCB mode is UART,
this parameter enables the
SCB.INTR_RX.PARITY
ERROR interrupt source.
SCB.INTR_RX.PARITY
ERROR trigger condition: parity
error in received data frame.
UartIntrRxTrigger false When the SCB mode is UART,
this parameter enables the
SCB.INTR_RX.TRIGGER
interrupt source.
SCB.INTR_RX.TRIGGER
trigger condition: remains active
until RX FIFO has more entries
than the value specified by
UartRxTriggerLevel.



Parameter Name	Value	Description
UartIntrRxUnderflow	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_RX.UNDERFLOW
		interrupt source.
		SCB.INTR_RX.UNDERFLOW
		trigger condition: attempt to read from an empty RX FIFO.
UartIntrTxEmpty	false	When the SCB mode is UART,
Garana i Xempty	laise	this parameter enables the
		SCB.INTR_TX.EMPTY interrupt
		source.
		SCB.INTR_TX.EMPTY trigger
		condition: TX FIFO is empty.
UartIntrTxNotFull	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.NOT_FULL interrupt source.
		SCB.INTR_TX.NOT_FULL
		trigger condition: TX FIFO is not
		full. There is at least one entry
		to put data.
UartIntrTxOverflow	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.OVERFLOW
		interrupt source. SCB.INTR_TX.OVERFLOW
		trigger condition: attempt to
		write to a full TX FIFO.
UartIntrTxTrigger	false	When the SCB mode is UART,
3		this parameter enables the
		SCB.INTR_TX.TRIGGER
		interrupt source.
		SCB.INTR_TX.TRIGGER
		trigger condition: remains active until TX FIFO has fewer entries
		than the value specified by
		UartTxTriggerLevel.
UartIntrTxUartDone	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.UART_DONE
		interrupt source.
		SCB.INTR_TX.UART_DONE
		trigger condition: all data are sent in to TX FIFO and the
		transmit FIFO and the shifter
		register are emptied.
UartIntrTxUartLostArb	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.UART_ARB
		LOST interrupt source.
		SCB.INTR_TX.UART_ARB
		LOST trigger condition: UART lost arbitration, the value driven
		on the TX line is not the same
		as the value observed on the
		RX line. This event is useful
		when the transmitter and the
		receiver share a TX/RX line.
		Only applicable for UART
	00/40/0040 40:40	SmartCard mode.



	Description
	SCB mode is UART,
	ameter enables the
SCB.INTI	R_TX.UART_NACK
	errupt source.
	R_TX.UART_NACK
	condition: UART
	r received a negative
	nowledgement.
	oplicable for UART artCard mode.
	SCB mode is UART,
	ameter enables the
	R TX.UNDERFLOW
	errupt source.
	R_TX.UNDERFLOW
	ondition: attempt to
	an empty TX FIFO.
	SCB mode is UART,
· ·	neter enables the low
· ·	r receiver option.
Only appli	icable for UART IrDA
Lieutindo Delevity	mode.
,	SCB mode is UART, rameter inverts the
· · · · · · · · · · · · · · · · · · ·	ng RX line signal.
	icable for UART IrDA
Siny appir	mode.
UartMedianFilterEnable false When the	SCB mode is UART,
	neter applies a digital
	ian filter to the UART
	input line.
· ·	SCB mode is UART,
· · · · · · · · · · · · · · · · · · ·	ameter enables the
	ulti-processor mode.
	oplicable for UART
	andard mode.
	SCB mode is UART, eter define whether to
	tched UART address
1	ito RX FIFO.
	cable for UART multi-
	cessor mode.
UartMpRxAddress 2 When the	SCB mode is UART,
this para	ameter defines the
	ART address.
1	cable for UART multi-
·	cessor mode.
	SCB mode is UART,
	ameter defines the
	ss mask in multi- or operation mode.
	0 – excludes bit from
	ess comparison.
	1 – the bit needs to
	th the corresponding
	ne UART address.
	cable for UART multi-
pro	cessor mode.



Parameter Name	Value	Description
UartNumberOfDataBits	8 bits	When the SCB mode is UART, this parameter defines the number of data bits inside the UART byte/word.
UartNumberOfStopBits	1 bit	When the SCB mode is UART, this parameter defines the number of Stop bits.
UartOvsFactor	12	When the SCB mode is UART, this parameter defines the oversampling factor of SCBCLK.
UartParityType	None	When the SCB mode is UART, this parameter applies UART parity check as Odd or Even or discards the parity entirely.
UartRtsEnable	false	When the SCB mode is UART, this parameter enables the rts output. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRtsPolarity	Active Low	When the SCB mode is UART, this parameter specifies active polarity of the output rts signal. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRtsTriggerLevel	4	When the SCB mode is UART, this parameter specifies the number of entries in the RX FIFO to activate the rts output signal. When the receiver FIFO has fewer entries than the UartRtsTriggerLevel, an rts output signal is activated. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRxBreakWidth	11	This parameter specifies the break width in bits.
UartRxBufferSize	8	When the SCB mode is UART, this parameter defines the size of the RX buffer.
UartRxOutputEnable	false	When the SCB mode is UART, this parameter enables the RX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.



Davamatar Nama	Value	EMBEDDED IN TO
Parameter Name	Value	Description
UartRxTriggerLevel	/	When the SCB mode is UART,
		this parameter defines the
		number of entries in the RX
		FIFO to trigger control the
		SCB.INTR_RX.TRIGGER
		interrupt event or RX DMA
		trigger output.
UartSmCardRetryOnNack	false	When the SCB mode is UART,
		this parameter defines whether
		to send a message again when
		a NACK response is received.
		Only applicable for UART
		SmartCard mode.
UartSubMode	Standard	When the SCB mode is UART,
		this parameter defines the sub
		mode of UART as: Standard,
		SmartCard or IrDA.
UartTxBufferSize	8	When the SCB mode is UART,
GaittyBalloroi20		this parameter defines the size
		of the TX buffer.
UartTxOutputEnable	false	When the SCB mode is UART,
OartixOdiputEnable	laise	this parameter enables the TX
		trigger output terminal of the
		component. This terminal must
		be connected to the DMA input
		trigger or left unconnected. Only
		applicable for devices which
		have a DMA controller.
UartTxTriggerLevel	0	When the SCB mode is UART,
OarrixinggerLevel	0	
		this parameter defines the
		number of entries in the TX
		FIFO to control the SCB.INTR
		TX.TRIGGER interrupt event or
LL AVA/ - L E L L		TX DMA trigger output.
UartWakeEnable	false	When the SCB mode is UART,
		this parameter enables the
		wakeup from Deep Sleep on
		start bit event. The actual
		wakeup source is RX GPIO.
		The skip start UART feature
		allows it to continue receiving
		bytes.
User Comments	1	Instance-specific comments.

9.2.2 Instance UART_1

Description: Serial Communication Block (SCB)

Instance type: SCB_P4 [v4.0]

Datasheet: online component datasheet for SCB_P4

Table 17. Component Parameters for UART_1



Parameter Name	Value	Description
Ezl2cByteModeEnable	false	When the SCB mode is EZI2C,
		this parameter specifies the
		number of bits per FIFO data
		element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO
		depth is 8 entries.
		The byte mode – true: an 8-bit
		FIFO data element. The FIFO
		depth is 16 entries.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
Ezl2cClockFromTerm	false	When the SCB mode is EZI2C,
		this parameter provides a clock
		terminal to connect a clock
		outside the component.
Ezl2cClockStretching	true	When the SCB mode is EZI2C,
		this parameter specifies
		whether the SCL is stretched
		while in EZI2C operation.
Ezl2cDataRate	100	When the SCB mode is EZI2C,
		this parameter defines EZI2C
		Data rate in kbps. The standard
		data rates are: 100, 400 and
		1000 kbps.
Ezl2cNumberOfAddresses	1	When the SCB mode is EZI2C,
		this parameter defines the
		number of I2C slave addresses
		that device respond to.
Ezl2cPrimarySlaveAddress	8	When the SCB mode is EZI2C,
•		this parameter specifies EZI2C
		primary 7-bits slave address
		(MSB ignored).
Ezl2cSecondarySlaveAddress	9	When the SCB mode is EZI2C,
,		this parameter specifies EZI2C
		secondary 7-bits slave address
		(MSB ignored).
		Only applicable when EZI2C
		clock stretching option is set.
Ezl2cSubAddressSize	8	When the SCB mode is EZI2C,
		this parameter specifies the
		maximum size of the slave
		buffer that is exposed to the
		master: 8bits – maximum buffer
		size is 256 bytes, 16 bits –
		maximum buffer size is 65535
		bytes.
Ezl2cWakeEnable	false	When the SCB mode is EZI2C,
		this parameter enables wakeup
		from Deep Sleep on I2C
		address match event.



Parameter Name	Value	Description
I2C Bus Voltage	3.3	When the SCB mode is I2C, this parameter specifies the voltage applied to the pull-up resistors on the I2C bus.
		Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2C Bus Voltage	3.3	When the SCB mode is EZI2C, this parameter specifies the voltage applied to the pull-up resistors on the I2C bus. Only applicable for devices other than PSoC 4000/PSoC
I2cAcceptAddress	false	4100/PSoC 4200. When the SCB mode is I2C, this parameter specifies whether to accept the match slave address in RX FIFO or not. All slave matched addresses are ACKed. The user has to register the callback function to handle accepted addresses. This feature has to be used when more than one address support is required.
I2cAcceptGeneralCall	false	When the SCB mode is I2C, this parameter specifies whether to accept the general call address. The general call address is ACKed when accepted and NAKed otherwise. The user has to register the callback function to handle the general call address.
I2cByteModeEnable	false	When the SCB mode is I2C, this parameter specifies the number of bits per FIFO data element. The byte mode – false: a 16-bit FIFO data element. The FIFO depth is 8 entries. The byte mode – true: an 8-bit FIFO data element. The FIFO depth is 16 entries. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2cClockFromTerm	false	When the SCB mode is I2C, this parameter provides a clock terminal to connect a clock outside the component.
I2cDataRate	100	When the SCB mode is I2C, this parameter specifies the data rate in kbps. The standard data rates are: 100, 400 and 1000 kbps.



Parameter Name	Value	Description
I2cExternIntrHandler	false	When the SCB mode is I2C, this parameter specifies whether the I2C interrupt handler is
		configured in SCB_I2CInit(). This parameter is intended to be used by the PM/SM bus component. The modification
10 M 10	4	parameter default value causes I2C mode failures.
I2cManualOversampleControl	true	When the SCB mode is I2C, this parameter specifies the method of calculating the oversampling as manual or automatic.
I2cMode	Slave	When the SCB mode is I2C, this parameter defines the I2C operation mode as: Slave, Master, Multi-Master or Multi-Master-Slave.
I2cOvsFactor	16	When the SCB mode is I2C, this parameter defines the oversampling factor of SCBCLK.
I2cOvsFactorHigh	8	When the SCB mode is I2C, this parameter defines the high oversampling factor of SCBCLK. Only applicable for I2C Master modes.
I2cOvsFactorLow	8	When the SCB mode is I2C, this parameter defines the low oversampling factor of SCBCLK. Only applicable for I2C Master modes.
I2cSlaveAddress	8	When the SCB mode is I2C, this parameter specifies the I2C 7-bits slave address (MSB ignored).
I2cSlaveAddressMask	254	When the SCB mode is I2C, this parameter specifies the I2C Slave address mask. Bit value 0 – excludes bit from address comparison. Bit value 1 – the bit needs to match with the corresponding bit of the I2C slave address.
I2cWakeEnable	false	When the SCB mode is I2C, this parameter enables wakeup from Deep Sleep on an I2C address match event.
ScbMisoSdaTxEnable	true	This parameter defines the availability of the spi_miso_i2csda_uart_tx pin.
ScbMode	UART	This parameter defines the mode of operation for the SCB component.
ScbMosiSclRxEnable	true	This parameter defines the availability of the spi_mosi_i2cscl_uart_rx pin.



Parameter Name	Value	Description
ScbRxWakeIrqEnable	false	This parameter defines the
- Cost attraction quitable	laio	availability of the spi_mosi_i2c
		scl_uart_rx_wake pin.
ScbSclkEnable	false	This parameter defines the
CODCORLINGBIO	laise	availability of the sclk pin.
ScbSs0Enable	false	This parameter defines the
SCDOSULTIABLE	laise	availability of the ss0 pin.
ScbSs1Enable	false	This parameter defines the
Schostellable	laise	availability of the ss1 pin.
ScbSs2Enable	false	
SCDSSZENADIE	laise	This parameter defines the
0.1.0.0511.	f.1.	availability of the ss2 pin.
ScbSs3Enable	false	This parameter defines the
		availability of the ss3 pin.
Show EZI2C Terminals	false	When the SCB mode is EZI2C,
		this parameter removes internal
		pins and expose signals to
		terminals. The exposed
		terminals must be connected to
OL 100 T : 1		the pins.
Show I2C Terminals	false	When the SCB mode is I2C, this
		parameter removes internal pins
		and expose signals to terminals.
		The exposed terminals must be
01 001 7 1		connected to the pins.
Show SPI Terminals	false	When the SCB mode is SPI,
		this parameter removes internal
		pins and expose signals to
		terminals. The exposed
		terminals must be connected to
Observation II	6.1.	the pins or SmartIO component.
Show UART Terminals	false	When the SCB mode is UART,
		this parameter removes internal
		pins and expose signals to terminals. The exposed
		terminals. The exposed
		the pins or SmartIO component.
Slew Rate	Fast	
Siew Rate	rasi	When the SCB mode is EZI2C, this parameter specifies the
		slew rate settings of the I2C
		pins.
		For devices supporting GPIO
		Over-Voltage Tolerance
		(GPIO_OVT) pins, I2C FM+
		options should be used when
		I2C data rate is greater than
		400 kbps. This option also
		requires the I2C bus voltage to
		be defined.Refer to the Device
		Datasheet to determine which
		pins are GPIO_OVT capable.



Parameter Name	Value	Description
Slew Rate	Fast	When the SCB mode is I2C, this
		parameter specifies the slew
		rate settings of the I2C pins.
		For devices supporting GPIO
		Over-Voltage Tolerance
		(GPIO_OVT) pins, I2C FM+
		options should be used when
		I2C data rate is greater than
		400 kbps. This option also
		requires the I2C bus voltage to
		be defined. Refer to the Device
		Datasheet to determine which
		pins are GPIO_OVT capable.
SpiBitRate	1000	When the SCB mode is SPI,
Opibilitate	1000	this parameter specifies the Bit
		rate in kbps (up to 8000 kbps);
		the actual rate may differ based
		on available clock frequency
		and component settings. This
		parameter has no effect if the
		Clock from terminal parameter
		is enabled.
CniDitaOrdar	MSB First	When the SCB mode is SPI,
SpiBitsOrder	MSB FIISI	· 1
		this parameter defines the bit
0.10 + 14 + 5 + 14		order as: MSB first or LSB first.
SpiByteModeEnable	false	When the SCB mode is SPI,
		this parameter specifies the
		number of bits per FIFO data
		element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO
		depth is 8 entries.
		The byte mode – true: an 8-bit
		FIFO data element. The FIFO
		depth is 16 entries.
		Ameliaahla amkufan dayisaa
		Applicable only for devices
		other than PSoC 4000/PSoC
0.:0115	6.1	4100/PSoC 4200.
SpiClockFromTerm	false	When the SCB mode is SPI,
		this parameter provides a clock
		terminal to connect a clock
	1	outside the component.
SpiFreeRunningSclk	false	When the SCB mode is SPI,
		this parameter specifies the
		SCLK generation by the master
		as: gated or free running
		(continuous).
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.



Parameter Name	Value	Description
SpiInterruptMode	None	When the SCB mode is SPI, this parameter specifies the interrupt mode. None: Removes all interrupt support. Internal: Leaves the interrupt SCBIRQ inside the component - the interrupt terminal becomes invisible. External: Provides an interrupt terminal to connect an interrupt outside the component.
SpiIntrMasterSpiDone	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_M. SPI_DONE interrupt source. SCB.INTR_M. SPI_DONE: all data are sent into TX FIFO and the TX FIFO and the shifter register are emptied. Only applicable for SPI Master mode.
SpiIntrRxFull	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.FULL interrupt source. SCB.INTR_RX.FULL trigger condition: RX FIFO is full.
SpiIntrRxNotEmpty	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.NOT_EMPTY interrupt source. SCB.INTR_RX.NOT_EMPTY trigger condition: RX FIFO is not empty. There is at least one entry to get data from.
SpiIntrRxOverflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to write to a full RX FIFO.
SpilntrRxTrigger	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.TRIGGER interrupt source. SCB.INTR_RX.TRIGGER trigger condition: remains active until RX FIFO has more entries than the value specified by SpiRxTriggerLevel.
SpiIntrRxUnderflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.UNDERFLOW interrupt source. SCB.INTR_RX.UNDERFLOW trigger condition: attempt to read from an empty RX FIFO.



Parameter Name	Value	Description
SpiIntrSlaveBusError	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_SLAVE.BUS ERROR interrupt source.
		SCB.INTR_SLAVE.BUS
		ERROR trigger condition: slave
		select line is deselected at an
		unexpected time in the SPI
		transfer.
		Only applicable for SPI Slave mode.
SpiIntrTxEmpty	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_TX.EMPTY interrupt
		source. SCB.INTR_TX.EMPTY trigger
		condition: TX FIFO is empty.
SpilntrTxNotFull	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_TX.NOT_FULL
		interrupt source. SCB.INTR TX.NOT FULL
		trigger condition: TX FIFO is not
		full. There is at least one entry
		to put data.
SpiIntrTxOverflow	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_TX.OVERFLOW interrupt source.
		SCB.INTR_TX.OVERFLOW
		trigger condition: attempt to
		write to a full TX FIFO.
SpiIntrTxTrigger	false	When the SCB mode is SPI,
		this parameter enables the SCB.INTR_TX.TRIGGER
		interrupt source.
		SCB.INTR_TX.TRIGGER
		trigger condition: remains active
		until TX FIFO has fewer entries than the value specified by
		SpiTxTriggerLevel.
SpiIntrTxUnderflow	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_TX.UNDERFLOW
		interrupt source.
		SCB.INTR_TX.UNDERFLOW trigger condition: attempt to
		read from an empty TX FIFO.
SpiLateMisoSampleEnable	false	When the SCB mode is SPI,
		this parameter enables late
		sampling of the MISO line by
SpiMedianFilterEnable	false	the master. When the SCB mode is SPI,
	เลเจษ	this parameter applies a digital
		3 tap median filter to the SPI
		input line.



		EMBEDDED IN T
Parameter Name	Value	Description
SpiMode	Slave	When the SCB mode is SPI,
		this parameter selects SPI
		mode of operation as: Slave or
		Master.
SpiNumberOfRxDataBits	8	When the SCB mode is SPI,
'		this parameter specifies the
		number of data bits inside the
		SPI byte/word for RX direction.
SpiNumberOfSelectLines	1	When the SCB mode is SPI,
Opirumber OrderectEnies	'	this parameter defines the
		number of slave select lines.
		The SPI Slave has only one
		slave select line. The SPI
0.31 1.05 0.4 0.4		Master has up to 4 lines.
SpiNumberOfTxDataBits	8	When the SCB mode is SPI,
		this parameter define the
		number of data bits inside the
		SPI byte/word for TX direction.
SpiOvsFactor	16	When the SCB mode is SPI,
		this parameter defines the
		oversampling factor of
		SCBCLK.
SpiRemoveMiso	false	When the SCB mode is SPI,
' ·		this parameter removes the
		MISO pin.
SpiRemoveMosi	false	When the SCB mode is SPI,
Opii terrio vervicor	laise	this parameter removes the
		MOSI pin.
SpiRemoveSclk	false	When the SCB mode is SPI,
SpirteilloveScik	laise	
		this parameter removes the
0 :0 0 %		SCLK pin.
SpiRxBufferSize	8	When the SCB mode is SPI,
		this parameter defines the size
		of the RX buffer.
SpiRxOutputEnable	false	When the SCB mode is SPI,
		this parameter enables the RX
		trigger output terminal of the
		component. This terminal must
		be connected to the DMA input
		trigger or left unconnected. Only
		applicable for devices which
		have a DMA controller.
SpiRxTriggerLevel	7	When the SCB mode is SPI,
		this parameter defines the
		number of entries in the RX
		FIFO to control the SCB.INTR -
		RX.TRIGGER interrupt event or
		RX DMA trigger output.
SpiSclkMode	CPHA = 0, CPOL	When the SCB mode is SPI,
- Opioontivious	= 0	this parameter defines the serial
	- 0	clock phase (CPHA) and
		polarity (CPOL).
SpiCoODolority	A =4ix = 1 =	
SpiSs0Polarity	Active Low	When the SCB mode is SPI,
		this parameter specifies active
		polarity of slave select 0.
		Annalis and Control
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.



Parameter Name	Value	Description
SpiSs1Polarity	Active Low	When the SCB mode is SPI,
		this parameter specifies active
		polarity of slave select 1.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
SpiSs2Polarity	Active Low	When the SCB mode is SPI,
		this parameter specifies active
		polarity of slave select 2.
		Applicable only for devices
		other than PSoC 4000/PSoC
0.10.00.1.11	A .: 1	4100/PSoC 4200.
SpiSs3Polarity	Active Low	When the SCB mode is SPI,
		this parameter specifies active polarity of slave select 3.
		polarity of slave select 3.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
SpiSubMode	Motorola	When the SCB mode is SPI,
		this parameter defines the sub
		mode of the SPI as: Motorola, TI(Start Coincides), TI(Start
		Precedes), or National
		Semiconductor.
SpiTransferSeparation	Continuous	When the SCB mode is SPI,
		this parameter defines the type
		of SPI transfers separation as:
		continuous or separated.
SpiTxBufferSize	8	When the SCB mode is SPI,
		this parameter defines the size of the TX buffer.
SpiTxOutputEnable	false	When the SCB mode is SPI,
OprixOutputEriable	laise	this parameter enables the TX
		trigger output terminal of the
		component. This terminal must
		be connected to the DMA input
		trigger or left unconnected. Only
		applicable for devices which
Ou iT: Triangel		have a DMA controller.
SpiTxTriggerLevel	0	When the SCB mode is SPI,
		this parameter defines the number of entries in the TX
		FIFO to control the SCB.INTR -
		TX.TRIGGER interrupt event or
		TX DMA trigger output.
SpiWakeEnable	false	When the SCB mode is SPI,
		this parameter enables wakeup
		from Deep Sleep on slave
		select event.



Dougnates No.	Value	EMBEDDED IN TO
Parameter Name	Value	Description
UartByteModeEnable	false	When the SCB mode is UART,
		this parameter specifies the
		number of bits per FIFO data element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO
		depth is 8 entries.
		The byte mode – true: an 8-bit
		FIFO data element. The FIFO depth is 16 entries.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
UartClockFromTerm	false	When the SCB mode is UART,
		this parameter provides a clock
		terminal to connect a clock
		outside the component.
UartCtsEnable	false	When the SCB mode is UART,
		this parameter enables the cts
		input.
		Only applicable for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
UartCtsPolarity	Active Low	When the SCB mode is UART,
		this parameter specifies active
		polarity of an input cts signal.
		Only applicable for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
UartDataRate	115200	When the SCB mode is UART,
		this parameter specifies the
		Baud rate in bps (up to 1000
		kbps); the actual rate may differ
		based on available clock
		frequency and component
		settings. This parameter has no effect if the Clock from terminal
		parameter is enabled.
UartDirection	TX + RX	When the SCB mode is UART,
	17.17	this parameter enables RX or
		TX direction or both
		simultaneously.
UartDropOnFrameErr	false	When the SCB mode is UART,
·		this parameter defines whether
		the data is dropped from RX
	_	FIFO on a frame error event.
UartDropOnParityErr	false	When the SCB mode is UART,
		this parameter determines
		whether the data is dropped
		from RX FIFO on a parity error event.
		event.



Parameter Name	Value	Description
UartInterruptMode	Internal	When the SCB mode is UART, this parameter specifies the interrupt mode. None: Removes all interrupt support. Internal: Leaves the interrupt SCBIRQ inside the component - the interrupt terminal becomes invisible. External: Provides an interrupt terminal to connect an
UartIntrRxBreakDetected	false	interrupt outside component. This parameter enables the RX break detection interrupt source to trigger the interrupt output.
UartIntrRxFrameErr	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.FRAME ERROR interrupt source. SCB.INTR_RX.FRAME ERROR trigger condition: frame error in received data frame.
UartIntrRxFull	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.FULL interrupt source. SCB.INTR_RX.FULL trigger condition: RX FIFO is full.
UartIntrRxNotEmpty	true	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.NOT_EMPTY interrupt source. SCB.INTR_RX.NOT_EMPTY trigger condition: RX FIFO is not empty. There is at least one entry to get data from.
UartIntrRxOverflow	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to write to a full RX FIFO.
UartIntrRxParityErr	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.PARITY ERROR interrupt source. SCB.INTR_RX.PARITY ERROR trigger condition: parity error in received data frame.
UartIntrRxTrigger	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.TRIGGER interrupt source. SCB.INTR_RX.TRIGGER trigger condition: remains active until RX FIFO has more entries than the value specified by UartRxTriggerLevel.



46

		EMBEDDED IN TO
Parameter Name	Value	Description
UartIntrRxUnderflow	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_RX.UNDERFLOW
		interrupt source.
		SCB.INTR_RX.UNDERFLOW
		trigger condition: attempt to
I loublish Tro Chants	foloo	read from an empty RX FIFO.
UartIntrTxEmpty	false	When the SCB mode is UART, this parameter enables the
		SCB.INTR_TX.EMPTY interrupt
		source.
		SCB.INTR_TX.EMPTY trigger
		condition: TX FIFO is empty.
UartIntrTxNotFull	false	When the SCB mode is UART,
	13.15	this parameter enables the
		SCB.INTR TX.NOT FULL
		interrupt source.
		SCB.INTR TX.NOT FULL
		trigger condition: TX FIFO is not
		full. There is at least one entry
		to put data.
UartIntrTxOverflow	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.OVERFLOW
		interrupt source.
		SCB.INTR_TX.OVERFLOW
		trigger condition: attempt to
		write to a full TX FIFO.
UartIntrTxTrigger	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.TRIGGER interrupt source.
		SCB.INTR_TX.TRIGGER
		trigger condition: remains active
		until TX FIFO has fewer entries
		than the value specified by
		UartTxTriggerLevel.
UartIntrTxUartDone	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.UART_DONE
		interrupt source.
		SCB.INTR_TX.UART_DONE
		trigger condition: all data are
		sent in to TX FIFO and the
		transmit FIFO and the shifter
LlorthetrTvl lorth octArb	foloo	register are emptied.
UartIntrTxUartLostArb	false	When the SCB mode is UART, this parameter enables the
		SCB.INTR_TX.UART_ARB
		LOST interrupt source.
		SCB.INTR_TX.UART_ARB
		LOST trigger condition: UART
		lost arbitration, the value driven
		on the TX line is not the same
		as the value observed on the
		RX line. This event is useful
		when the transmitter and the
		receiver share a TX/RX line.
		Only applicable for UART
	00/40/0040 40:40	SmartCard mode.



Parameter Name	Value	Description
UartIntrTxUartNack	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.UART_NACK
		interrupt source.
		SCB.INTR_TX.UART_NACK
		trigger condition: UART transmitter received a negative
		acknowledgement.
		Only applicable for UART
		SmartCard mode.
UartIntrTxUnderflow	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.UNDERFLOW
		interrupt source.
		SCB.INTR_TX.UNDERFLOW
		trigger condition: attempt to read from an empty TX FIFO.
UartIrdaLowPower	false	When the SCB mode is UART,
	14,50	this parameter enables the low
		power receiver option.
		Only applicable for UART IrDA
		mode.
UartIrdaPolarity	Non-Inverting	When the SCB mode is UART,
		this parameter inverts the
		incoming RX line signal.
		Only applicable for UART IrDA mode.
UartMedianFilterEnable	false	When the SCB mode is UART,
Garawedian morenasio	laide	this parameter applies a digital
		3 tap median filter to the UART
		input line.
UartMpEnable	false	When the SCB mode is UART,
		this parameter enables the
		UART multi-processor mode.
		Only applicable for UART Standard mode.
UartMpRxAcceptAddress	false	When the SCB mode is UART,
OartimproxAcceptAddress	laise	this parameter define whether to
		put the matched UART address
		into RX FIFO.
		Only applicable for UART multi-
		processor mode.
UartMpRxAddress	2	When the SCB mode is UART,
		this parameter defines the
		UART address. Only applicable for UART multi-
		processor mode.
UartMpRxAddressMask	255	When the SCB mode is UART,
	200	this parameter defines the
		address mask in multi-
		processor operation mode.
		Bit value 0 – excludes bit from
		address comparison.
		Bit value 1 – the bit needs to
		match with the corresponding bit of the UART address.
		Only applicable for UART multi-
		processor mode.



Parameter Name	Value	Description
UartNumberOfDataBits	8 bits	When the SCB mode is UART, this parameter defines the number of data bits inside the UART byte/word.
UartNumberOfStopBits	1 bit	When the SCB mode is UART, this parameter defines the number of Stop bits.
UartOvsFactor	13	When the SCB mode is UART, this parameter defines the oversampling factor of SCBCLK.
UartParityType	None	When the SCB mode is UART, this parameter applies UART parity check as Odd or Even or discards the parity entirely.
UartRtsEnable	false	When the SCB mode is UART, this parameter enables the rts output. Applicable only for devices
		other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRtsPolarity	Active Low	When the SCB mode is UART, this parameter specifies active polarity of the output rts signal. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRtsTriggerLevel	4	When the SCB mode is UART, this parameter specifies the number of entries in the RX FIFO to activate the rts output signal. When the receiver FIFO has fewer entries than the UartRtsTriggerLevel, an rts output signal is activated. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRxBreakWidth	11	This parameter specifies the break width in bits.
UartRxBufferSize	8	When the SCB mode is UART, this parameter defines the size of the RX buffer.
UartRxOutputEnable	false	When the SCB mode is UART, this parameter enables the RX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.



Parameter Name	Value	Description
UartRxTriggerLevel	7	When the SCB mode is UART, this parameter defines the number of entries in the RX FIFO to trigger control the SCB.INTR_RX.TRIGGER interrupt event or RX DMA trigger output.
UartSmCardRetryOnNack	false	When the SCB mode is UART, this parameter defines whether to send a message again when a NACK response is received. Only applicable for UART SmartCard mode.
UartSubMode	Standard	When the SCB mode is UART, this parameter defines the sub mode of UART as: Standard, SmartCard or IrDA.
UartTxBufferSize	8	When the SCB mode is UART, this parameter defines the size of the TX buffer.
UartTxOutputEnable	false	When the SCB mode is UART, this parameter enables the TX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.
UartTxTriggerLevel	0	When the SCB mode is UART, this parameter defines the number of entries in the TX FIFO to control the SCB.INTRTX.TRIGGER interrupt event or TX DMA trigger output.
UartWakeEnable User Comments	true	When the SCB mode is UART, this parameter enables the wakeup from Deep Sleep on start bit event. The actual wakeup source is RX GPIO. The skip start UART feature allows it to continue receiving bytes. Instance-specific comments.
User Comments		instance-specific comments.

9.2.3 Instance UART_2

Description: Serial Communication Block (SCB)

Instance type: SCB_P4 [v4.0]

Datasheet: online component datasheet for SCB_P4

Table 18. Component Parameters for UART_2

LM502 Datasheet 09/16/2019 13:40 49



Parameter Name	Value	Description
Ezl2cByteModeEnable	false	When the SCB mode is EZI2C,
LZIZCDYtelWodeLflable	laise	this parameter specifies the
		number of bits per FIFO data
		element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO
		depth is 8 entries.
		The byte mode – true: an 8-bit
		FIFO data element. The FIFO
		depth is 16 entries.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
C=10 oCloskCroseTorres	foloo	
Ezl2cClockFromTerm	false	When the SCB mode is EZI2C,
		this parameter provides a clock
		terminal to connect a clock
5 10 0L 10: 11:		outside the component.
Ezl2cClockStretching	true	When the SCB mode is EZI2C,
		this parameter specifies
		whether the SCL is stretched
		while in EZI2C operation.
Ezl2cDataRate	100	When the SCB mode is EZI2C,
		this parameter defines EZI2C
		Data rate in kbps. The standard
		data rates are: 100, 400 and
		1000 kbps.
Ezl2cNumberOfAddresses	1	When the SCB mode is EZI2C,
		this parameter defines the
		number of I2C slave addresses
		that device respond to.
Ezl2cPrimarySlaveAddress	8	When the SCB mode is EZI2C,
		this parameter specifies EZI2C
		primary 7-bits slave address
		(MSB ignored).
Ezl2cSecondarySlaveAddress	9	When the SCB mode is EZI2C,
		this parameter specifies EZI2C
		secondary 7-bits slave address
		(MSB ignored).
		Only applicable when EZI2C
		clock stretching option is set.
Ezl2cSubAddressSize	8	When the SCB mode is EZI2C,
		this parameter specifies the
		maximum size of the slave
		buffer that is exposed to the
		master: 8bits – maximum buffer
		size is 256 bytes, 16 bits –
		maximum buffer size is 65535
		bytes.
Ezl2cWakeEnable	false	When the SCB mode is EZI2C,
	.5.75	this parameter enables wakeup
		from Deep Sleep on I2C
		address match event.
	1	2.2.2.222



Parameter Name	Value	Description
I2C Bus Voltage	3.3	When the SCB mode is I2C, this parameter specifies the voltage applied to the pull-up resistors on the I2C bus.
		Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2C Bus Voltage	3.3	When the SCB mode is EZI2C, this parameter specifies the voltage applied to the pull-up resistors on the I2C bus. Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2cAcceptAddress	false	When the SCB mode is I2C, this parameter specifies whether to accept the match slave address in RX FIFO or not. All slave matched addresses are ACKed. The user has to register the callback function to handle accepted addresses. This feature has to be used when more than one address support is required.
I2cAcceptGeneralCall	false	When the SCB mode is I2C, this parameter specifies whether to accept the general call address. The general call address is ACKed when accepted and NAKed otherwise. The user has to register the callback function to handle the general call address.
I2cByteModeEnable	false	When the SCB mode is I2C, this parameter specifies the number of bits per FIFO data element. The byte mode – false: a 16-bit FIFO data element. The FIFO depth is 8 entries. The byte mode – true: an 8-bit FIFO data element. The FIFO depth is 16 entries. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2cClockFromTerm	false	When the SCB mode is I2C, this parameter provides a clock terminal to connect a clock outside the component.
I2cDataRate	100	When the SCB mode is I2C, this parameter specifies the data rate in kbps. The standard data rates are: 100, 400 and 1000 kbps.



Parameter Name	Value	Description
I2cExternIntrHandler	false	When the SCB mode is I2C, this parameter specifies whether the I2C interrupt handler is configured in SCB_I2CInit(). This parameter is intended to be used by the PM/SM bus component. The modification parameter default value causes I2C mode failures.
I2cManualOversampleControl	true	When the SCB mode is I2C, this parameter specifies the method of calculating the oversampling as manual or automatic.
I2cMode	Slave	When the SCB mode is I2C, this parameter defines the I2C operation mode as: Slave, Master, Multi-Master or Multi-Master-Slave.
I2cOvsFactor	16	When the SCB mode is I2C, this parameter defines the oversampling factor of SCBCLK.
I2cOvsFactorHigh	8	When the SCB mode is I2C, this parameter defines the high oversampling factor of SCBCLK. Only applicable for I2C Master modes.
I2cOvsFactorLow	8	When the SCB mode is I2C, this parameter defines the low oversampling factor of SCBCLK. Only applicable for I2C Master modes.
I2cSlaveAddress	8	When the SCB mode is I2C, this parameter specifies the I2C 7-bits slave address (MSB ignored).
I2cSlaveAddressMask	254	When the SCB mode is I2C, this parameter specifies the I2C Slave address mask. Bit value 0 – excludes bit from address comparison. Bit value 1 – the bit needs to match with the corresponding bit of the I2C slave address.
I2cWakeEnable	false	When the SCB mode is I2C, this parameter enables wakeup from Deep Sleep on an I2C address match event.
ScbMisoSdaTxEnable	true	This parameter defines the availability of the spi_miso_i2csda_uart_tx pin.
ScbMode	UART	This parameter defines the mode of operation for the SCB component.
ScbMosiSclRxEnable	true	This parameter defines the availability of the spi_mosi_i2cscl_uart_rx pin.



Parameter Name	Value	Description
ScbRxWakeIrqEnable	false	This parameter defines the
		availability of the spi_mosi_i2c
		scl_uart_rx_wake pin.
ScbSclkEnable	false	This parameter defines the
		availability of the sclk pin.
ScbSs0Enable	false	This parameter defines the
		availability of the ss0 pin.
ScbSs1Enable	false	This parameter defines the
		availability of the ss1 pin.
ScbSs2Enable	false	This parameter defines the
		availability of the ss2 pin.
ScbSs3Enable	false	This parameter defines the
		availability of the ss3 pin.
Show EZI2C Terminals	false	When the SCB mode is EZI2C,
		this parameter removes internal
		pins and expose signals to
		terminals. The exposed
		terminals must be connected to
		the pins.
Show I2C Terminals	false	When the SCB mode is I2C, this
		parameter removes internal pins
		and expose signals to terminals.
		The exposed terminals must be
OL OBLE		connected to the pins.
Show SPI Terminals	false	When the SCB mode is SPI,
		this parameter removes internal
		pins and expose signals to terminals. The exposed
		terminals must be connected to
		the pins or SmartIO component.
Show UART Terminals	false	When the SCB mode is UART,
Show OART Terminals	laise	this parameter removes internal
		pins and expose signals to
		terminals. The exposed
		terminals must be connected to
		the pins or SmartIO component.
Slew Rate	Fast	When the SCB mode is EZI2C,
		this parameter specifies the
		slew rate settings of the I2C
		pins.
		For devices supporting GPIO
		Over-Voltage Tolerance
		(GPIO_OVT) pins, I2C FM+
		options should be used when
		I2C data rate is greater than
		400 kbps. This option also
		requires the I2C bus voltage to
		be defined.Refer to the Device
		Datasheet to determine which
		pins are GPIO_OVT capable.



Parameter Name	Value	Description
Slew Rate	Fast	When the SCB mode is I2C, this
Olew Itale	1 431	parameter specifies the slew
		rate settings of the I2C pins.
		For devices supporting GPIO
		Over-Voltage Tolerance
		(GPIO_OVT) pins, I2C FM+
		options should be used when
		I2C data rate is greater than
		400 kbps. This option also
		requires the I2C bus voltage to
		be defined. Refer to the Device
		Datasheet to determine which
CmiDitData	1000	pins are GPIO_OVT capable.
SpiBitRate	1000	When the SCB mode is SPI,
		this parameter specifies the Bit
		rate in kbps (up to 8000 kbps);
		the actual rate may differ based
		on available clock frequency
		and component settings. This
		parameter has no effect if the
		Clock from terminal parameter
		is enabled.
SpiBitsOrder	MSB First	When the SCB mode is SPI,
		this parameter defines the bit
		order as: MSB first or LSB first.
SpiByteModeEnable	false	When the SCB mode is SPI,
		this parameter specifies the
		number of bits per FIFO data
		element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO
		depth is 8 entries.
		The byte mode – true: an 8-bit
		FIFO data element. The FIFO
		depth is 16 entries.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
SpiClockFromTerm	false	When the SCB mode is SPI,
		this parameter provides a clock
		terminal to connect a clock
		outside the component.
SpiFreeRunningSclk	false	When the SCB mode is SPI,
_		this parameter specifies the
		SCLK generation by the master
		as: gated or free running
		(continuous).
		·
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.



Parameter Name	Value	Description
SpilnterruptMode	None	When the SCB mode is SPI, this parameter specifies the interrupt mode. None: Removes all interrupt support. Internal: Leaves the interrupt SCBIRQ inside the component - the interrupt terminal becomes invisible. External: Provides an interrupt terminal to connect an interrupt outside the component.
SpilntrMasterSpiDone	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_M. SPI_DONE interrupt source. SCB.INTR_M. SPI_DONE: all data are sent into TX FIFO and the TX FIFO and the shifter register are emptied. Only applicable for SPI Master mode.
SpiIntrRxFull	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.FULL interrupt source. SCB.INTR_RX.FULL trigger condition: RX FIFO is full.
SpiIntrRxNotEmpty	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.NOT_EMPTY interrupt source. SCB.INTR_RX.NOT_EMPTY trigger condition: RX FIFO is not empty. There is at least one entry to get data from.
SpilntrRxOverflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to write to a full RX FIFO.
SpiIntrRxTrigger	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.TRIGGER interrupt source. SCB.INTR_RX.TRIGGER trigger condition: remains active until RX FIFO has more entries than the value specified by SpiRxTriggerLevel.
SpilntrRxUnderflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.UNDERFLOW interrupt source. SCB.INTR_RX.UNDERFLOW trigger condition: attempt to read from an empty RX FIFO.



Parameter Name	Value	Description
SpiIntrSlaveBusError	false	When the SCB mode is SPI,
'		this parameter enables the
		SCB.INTR_SLAVE.BUS
		ERROR interrupt source.
		SCB.INTR_SLAVE.BUS
		ERROR trigger condition: slave
		select line is deselected at an
		unexpected time in the SPI
		transfer.
		Only applicable for SPI Slave mode.
SpiIntrTxEmpty	false	When the SCB mode is SPI,
Spiriti TXETTIPITY	laise	this parameter enables the
		SCB.INTR_TX.EMPTY interrupt
		source.
		SCB.INTR_TX.EMPTY trigger
		condition: TX FIFO is empty.
SpiIntrTxNotFull	false	When the SCB mode is SPI,
,		this parameter enables the
		SCB.INTR_TX.NOT_FULL
		interrupt source.
		SCB.INTR_TX.NOT_FULL
		trigger condition: TX FIFO is not
		full. There is at least one entry
		to put data.
SpiIntrTxOverflow	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_TX.OVERFLOW interrupt source.
		SCB.INTR_TX.OVERFLOW
		trigger condition: attempt to
		write to a full TX FIFO.
SpilntrTxTrigger	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_TX.TRIGGER
		interrupt source.
		SCB.INTR_TX.TRIGGER
		trigger condition: remains active
		until TX FIFO has fewer entries
		than the value specified by
SpiIntrTxUnderflow	false	SpiTxTriggerLevel. When the SCB mode is SPI,
Opiniu i xondernow	Idioc	this parameter enables the
		SCB.INTR TX.UNDERFLOW
		interrupt source.
		SCB.INTR_TX.UNDERFLOW
		trigger condition: attempt to
		read from an empty TX FIFO.
SpiLateMisoSampleEnable	false	When the SCB mode is SPI,
		this parameter enables late
		sampling of the MISO line by
		the master.
SpiMedianFilterEnable	false	When the SCB mode is SPI,
		this parameter applies a digital
		3 tap median filter to the SPI
		input line.



Parameter Name	Value	Description
SpiMode	Slave	When the SCB mode is SPI, this parameter selects SPI mode of operation as: Slave or Master.
SpiNumberOfRxDataBits	8	When the SCB mode is SPI, this parameter specifies the number of data bits inside the SPI byte/word for RX direction.
SpiNumberOfSelectLines	1	When the SCB mode is SPI, this parameter defines the number of slave select lines. The SPI Slave has only one slave select line. The SPI Master has up to 4 lines.
SpiNumberOfTxDataBits	8	When the SCB mode is SPI, this parameter define the number of data bits inside the SPI byte/word for TX direction.
SpiOvsFactor	16	When the SCB mode is SPI, this parameter defines the oversampling factor of SCBCLK.
SpiRemoveMiso	false	When the SCB mode is SPI, this parameter removes the MISO pin.
SpiRemoveMosi	false	When the SCB mode is SPI, this parameter removes the MOSI pin.
SpiRemoveSclk	false	When the SCB mode is SPI, this parameter removes the SCLK pin.
SpiRxBufferSize	8	When the SCB mode is SPI, this parameter defines the size of the RX buffer.
SpiRxOutputEnable	false	When the SCB mode is SPI, this parameter enables the RX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.
SpiRxTriggerLevel	7	When the SCB mode is SPI, this parameter defines the number of entries in the RX FIFO to control the SCB.INTRRX.TRIGGER interrupt event or RX DMA trigger output.
SpiSclkMode	CPHA = 0, CPOL = 0	When the SCB mode is SPI, this parameter defines the serial clock phase (CPHA) and polarity (CPOL).
SpiSs0Polarity	Active Low	When the SCB mode is SPI, this parameter specifies active polarity of slave select 0. Applicable only for devices other than PSoC 4000/PSoC
		4100/PSoC 4200.

LM502 Datasheet 09/16/2019 13:40 57



Parameter Name	Value	Description
SpiSs1Polarity	Active Low	When the SCB mode is SPI,
Opios ir cianty	Active Low	this parameter specifies active
		polarity of slave select 1.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
SpiSs2Polarity	Active Low	When the SCB mode is SPI,
		this parameter specifies active polarity of slave select 2.
		Applicable only for devices
		other than PSoC 4000/PSoC 4100/PSoC 4200.
SpiSs3Polarity	Active Low	When the SCB mode is SPI,
		this parameter specifies active polarity of slave select 3.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
SpiSubMode	Motorola	When the SCB mode is SPI,
		this parameter defines the sub
		mode of the SPI as: Motorola,
		TI(Start Coincides), TI(Start Precedes), or National
		Semiconductor.
SpiTransferSeparation	Continuous	When the SCB mode is SPI,
·		this parameter defines the type
		of SPI transfers separation as:
		continuous or separated.
SpiTxBufferSize	8	When the SCB mode is SPI,
		this parameter defines the size of the TX buffer.
SpiTxOutputEnable	false	When the SCB mode is SPI,
Opi i Xodipate nabio	laioc	this parameter enables the TX
		trigger output terminal of the
		component. This terminal must
		be connected to the DMA input
		trigger or left unconnected. Only
		applicable for devices which have a DMA controller.
SpiTxTriggerLevel	0	When the SCB mode is SPI,
		this parameter defines the
		number of entries in the TX
		FIFO to control the SCB.INTR
		TX.TRIGGER interrupt event or
SpiWakoEpablo	false	TX DMA trigger output. When the SCB mode is SPI,
SpiWakeEnable	IdiSe	this parameter enables wakeup
		from Deep Sleep on slave
		select event.



Parameter Name	Value	Description
UartByteModeEnable	false	When the SCB mode is UART,
		this parameter specifies the
		number of bits per FIFO data element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO depth is 8 entries.
		The byte mode – true: an 8-bit
		FIFO data element. The FIFO depth is 16 entries.
		Applicable only for devices
		other than PSoC 4000/PSoC 4100/PSoC 4200.
UartClockFromTerm	false	When the SCB mode is UART,
		this parameter provides a clock terminal to connect a clock
UartCtsEnable	false	outside the component. When the SCB mode is UART,
Odi (OtsEriable	iaise	this parameter enables the cts input.
		Only applicable for devices other than PSoC 4000/PSoC
		4100/PSoC 4200.
UartCtsPolarity	Active Low	When the SCB mode is UART,
		this parameter specifies active polarity of an input cts signal.
		Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartDataRate	115200	When the SCB mode is UART,
		this parameter specifies the
		Baud rate in bps (up to 1000
		kbps); the actual rate may differ based on available clock
		frequency and component
		settings. This parameter has no
		effect if the Clock from terminal
11. 12: 6	TV 51	parameter is enabled.
UartDirection	TX + RX	When the SCB mode is UART,
		this parameter enables RX or TX direction or both
		simultaneously.
UartDropOnFrameErr	false	When the SCB mode is UART,
		this parameter defines whether
		the data is dropped from RX
	false	FIFO on a frame error event. When the SCB mode is UART,
UartDropOnParityErr	iaise	this parameter determines
		whether the data is dropped
		from RX FIFO on a parity error
		event.



Parameter Name	Value	Description
UartInterruptMode	None	When the SCB mode is UART, this parameter specifies the interrupt mode. None: Removes all interrupt support. Internal: Leaves the interrupt SCBIRQ inside the component - the interrupt terminal becomes invisible. External: Provides an interrupt terminal to connect an interrupt outside component.
UartIntrRxBreakDetected	false	This parameter enables the RX break detection interrupt source to trigger the interrupt output.
UartIntrRxFrameErr	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.FRAME ERROR interrupt source. SCB.INTR_RX.FRAME ERROR trigger condition: frame error in received data frame.
UartIntrRxFull	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.FULL interrupt source. SCB.INTR_RX.FULL trigger condition: RX FIFO is full.
UartIntrRxNotEmpty	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.NOT_EMPTY interrupt source. SCB.INTR_RX.NOT_EMPTY trigger condition: RX FIFO is not empty. There is at least one entry to get data from.
UartIntrRxOverflow	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to write to a full RX FIFO.
UartIntrRxParityErr	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.PARITY ERROR interrupt source. SCB.INTR_RX.PARITY ERROR trigger condition: parity error in received data frame.
UartIntrRxTrigger	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.TRIGGER interrupt source. SCB.INTR_RX.TRIGGER trigger condition: remains active until RX FIFO has more entries than the value specified by UartRxTriggerLevel.



UartIntrTxUnderflow false When the SCB mode is UART this parameter enables the SCB.INTR RX UNDERFLOW interrupt source. SCB.INTR RX UNDERFLOW trigger condition: attempt to read from an empty RX FIFO. UartIntrTxEmpty false When the SCB mode is UART, this parameter enables the SCB.INTR_TX.EMPTY integer condition: TX FIFO is empty. UartIntrTxNotFull false When the SCB mode is UART, this parameter enables the SCB.INTR_TX.MOT_FULL interrupt source. SCB.INTR_TX.MOT_FULL interrupt source. SCB.INTR_TX.NOT_FULL trigger condition: TX FIFO is not full. There is at least one entry to put data. When the SCB mode is UART, this parameter enables the SCB.INTR_TX.NOT_FULL interrupt source. SCB.INTR_TX.OVERFLOW interrupt source. SCB.INTR_TX.OVERFLOW trigger condition: attempt to write to a full TX FIFO. UartIntrTxTrigger false When the SCB mode is UART, this parameter enables the SCB.INTR_TX.TX GREER interrupt source. SCB.INTR_TX.TX GREER interrup	Parameter Name	Value	Description
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LM502 Datasheet 09/16/2019 13:40 61



Parameter Name	Value	Description
UartIntrTxUartNack	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.UART_NACK
		interrupt source.
		SCB.INTR_TX.UART_NACK
		trigger condition: UART
		transmitter received a negative acknowledgement.
		Only applicable for UART
		SmartCard mode.
UartIntrTxUnderflow	false	When the SCB mode is UART.
		this parameter enables the
		SCB.INTR_TX.UNDERFLOW
		interrupt source.
		SCB.INTR_TX.UNDERFLOW
		trigger condition: attempt to
UartIrdaLowPower	foloo	read from an empty TX FIFO. When the SCB mode is UART.
UartifdaLowPower	false	this parameter enables the low
		power receiver option.
		Only applicable for UART IrDA
		mode.
UartIrdaPolarity	Non-Inverting	When the SCB mode is UART,
		this parameter inverts the
		incoming RX line signal.
		Only applicable for UART IrDA
		mode.
UartMedianFilterEnable	false	When the SCB mode is UART,
		this parameter applies a digital 3 tap median filter to the UART
		input line.
UartMpEnable	false	When the SCB mode is UART,
	1-11-2	this parameter enables the
		UART multi-processor mode.
		Only applicable for UART
		Standard mode.
UartMpRxAcceptAddress	false	When the SCB mode is UART,
		this parameter define whether to
		put the matched UART address into RX FIFO.
		Only applicable for UART multi-
		processor mode.
UartMpRxAddress	2	When the SCB mode is UART,
'		this parameter defines the
		UART address.
		Only applicable for UART multi-
		processor mode.
UartMpRxAddressMask	255	When the SCB mode is UART,
		this parameter defines the address mask in multi-
		processor operation mode.
		Bit value 0 – excludes bit from
		address comparison.
		Bit value 1 – the bit needs to
		match with the corresponding
		bit of the UART address.
		Only applicable for UART multi-
		processor mode.



Parameter Name	Value	Description
UartNumberOfDataBits	8 bits	When the SCB mode is UART, this parameter defines the number of data bits inside the UART byte/word.
UartNumberOfStopBits	1 bit	When the SCB mode is UART, this parameter defines the number of Stop bits.
UartOvsFactor	12	When the SCB mode is UART, this parameter defines the oversampling factor of SCBCLK.
UartParityType	None	When the SCB mode is UART, this parameter applies UART parity check as Odd or Even or discards the parity entirely.
UartRtsEnable	false	When the SCB mode is UART, this parameter enables the rts output. Applicable only for devices
		other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRtsPolarity	Active Low	When the SCB mode is UART, this parameter specifies active polarity of the output rts signal. Applicable only for devices
		other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRtsTriggerLevel	4	When the SCB mode is UART, this parameter specifies the number of entries in the RX FIFO to activate the rts output signal. When the receiver FIFO has fewer entries than the UartRtsTriggerLevel, an rts output signal is activated. Applicable only for devices
		other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRxBreakWidth	11	This parameter specifies the break width in bits.
UartRxBufferSize	8	When the SCB mode is UART, this parameter defines the size of the RX buffer.
UartRxOutputEnable	false	When the SCB mode is UART, this parameter enables the RX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.



Parameter Name	Value	Description
	Value	
UartRxTriggerLevel	/	When the SCB mode is UART,
		this parameter defines the
		number of entries in the RX
		FIFO to trigger control the
		SCB.INTR_RX.TRIGGER
		interrupt event or RX DMA
		trigger output.
UartSmCardRetryOnNack	false	When the SCB mode is UART,
		this parameter defines whether
		to send a message again when
		a NACK response is received.
		Only applicable for UART
		SmartCard mode.
UartSubMode	Standard	When the SCB mode is UART,
		this parameter defines the sub
		mode of UART as: Standard,
		SmartCard or IrDA.
UartTxBufferSize	8	When the SCB mode is UART,
GUITTABUITOTOIZO		this parameter defines the size
		of the TX buffer.
UartTxOutputEnable	false	When the SCB mode is UART,
Oart i xOutputEnable	laise	
		this parameter enables the TX
		trigger output terminal of the
		component. This terminal must
		be connected to the DMA input
		trigger or left unconnected. Only
		applicable for devices which
		have a DMA controller.
UartTxTriggerLevel	0	When the SCB mode is UART,
		this parameter defines the
		number of entries in the TX
		FIFO to control the SCB.INTR
		TX.TRIGGER interrupt event or
		TX DMA trigger output.
UartWakeEnable	false	When the SCB mode is UART,
		this parameter enables the
		wakeup from Deep Sleep on
		start bit event. The actual
		wakeup source is RX GPIO.
		The skip start UART feature
		allows it to continue receiving
		bytes.
User Comments		Instance-specific comments.
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10 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
 - Software base types
 - Hardware register types
 - Compiler defines
 - o Cypress API return codes
 - Interrupt types and macros
- Registers
 - o The full PSoC 4 register map is covered in the PSoC 4 Registers Technical Reference
 - o Register Access chapter in the System Reference Guide

 - § CY_GET API routines§ CY_SET API routines
- System Functions chapter in the **System Reference Guide**
 - o General API routines
 - o CyDelay API routines
 - o CyVd Voltage Detect API routines
- Power Management
 - o Power Supply and Monitoring chapter in the PSoC 4 Technical Reference Manual
 - o Low Power Modes chapter in the PSoC 4 Technical Reference Manual
 - o Power Management chapter in the System Reference Guide
 - § CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
 - CyWdť API routinės