

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI**B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering****NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)**

(Effective from the academic year 2021 – 22)

VII Semester

Advanced VLSI			
Course Code	21EC71	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Learn overview of VLSI design flow
- Emphasise on Back end VLSI design flow
- Learn basics of verification with reference to System Verilog

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. CMOS Logic: Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers. Text Book 1

Teaching-Learning Process	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3
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Module-2

Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.

Routing: Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back annotation. Text Book 1

Teaching-Learning Process	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3
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Module-3	
Verification Guidelines: The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components, layered testbench.	
Data Types: Built in Data types, fixed and dynamic arrays, Queues, associative arrays, linked lists, array methods, choosing a type, creating new types with type def, creating user defined structures, type conversion, Enumerated types, constants and strings, Expression width.	
Text Book 2	
Teaching-Learning Process	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3
Module-4	
Procedural Statements and Routines: Procedural statements, Tasks, Functions and void functions, Task and function overview, Routine arguments, returning from a routine, Local data storage, time values.	
Connecting the test bench and design: Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions.	
Text Book 2	
Teaching-Learning Process	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3
Module-5	
Randomization: Introduction, What to randomize? , Randomization in System Verilog, Random number functions, Common randomization problems, Random Number Generators.	
Functional Coverage: Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation.	
Text Book 2	
Teaching-Learning Process	Chalk and talk method, Power point presentation RBT Level: L1, L2, L3
Course outcomes (Course Skill Set)	
At the end of the course the student will be able to:	
<ol style="list-style-type: none"> 1. Understand VLSI design flow 2. Describe the concepts of ASIC design methodology 3. Create floor plan including partition and routing with the use of CAD algorithms 4. Will have better insights into VLSI back-end design flow 5. Learn verification basics and System Verilog 	
Assessment Details (both CIE and SEE)	
The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.	
Continuous Internal Evaluation:	
Three Unit Tests each of 20 Marks (duration 01 hour)	
<ol style="list-style-type: none"> 1. First test at the end of 5th week of the semester 2. Second test at the end of the 10th week of the semester 3. Third test at the end of the 15th week of the semester 	
Two assignments each of 10 Marks	
<ol style="list-style-type: none"> 4. First assignment at the end of 4th week of the semester 5. Second assignment at the end of 9th week of the semester 	

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20**

Marks (duration 01 hours)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Michael John Sebastian Smith, Application - Specific Integrated Circuits, Addison-Wesley Professional, 2005.
2. Chris Spear, System Verilog for Verification – A guide to learning the Test bench language features, Springer Publications, Second Edition, 2010.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Use EDA tool to design basic Analog blocks like amplifiers and 4-bit RAM
- Prepare a white paper on ASIC design flow referring to literatures of Cadence and Synopsys EDA tools
- Mini project using System Verilog