

RTL8211F(D)(I) UTP <=> RGMII QFN-40 Pin Reference Schematic

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Ethernet PHY

REVISION HISTORY


RTL8211F(D)(I) UTP <=> RGMII QFN-40 Pin Reference Schematic V1.0

RTL8211F(D)(I) UTP <=> RGMII QFN-40 Pin Reference Schematic V1.01

* Change the value of C5/C6 for RTL8211FDI/FI application.

RTL8211F(D)(I) UTP <=> RGMII QFN-40 Pin Reference Schematic V1.02

* Fix the name of the path.

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[illegible]

A circuit diagram showing a resistor labeled R7 with a value of 2.49K 1%. One end of the resistor is connected to a ground symbol, and the other end is connected to a node labeled RSET.

Pull-up to disable PLL @ ALDPS mode.

Pull-up for additional 2ns delay to TXC/RXC for data latching.

A circuit diagram showing a horizontal line representing a signal path. On the left, the text "MDIO" is written in red. The line continues to the right, passing through a resistor symbol (a zigzag line) labeled "R11" above it. To the right of the resistor, the value "1.5K" is written. The line then terminates at a small circle, with the text "DVDDRG" written in red above it.

Pinout diagram of the RTL8211F(D)(I) Ethernet controller. The diagram shows a central chip with pins numbered 1 to 30. Pins 1-10 are on the left, 11-20 on the bottom, and 21-30 on the right. A ground symbol is connected to pin 41, labeled 'EGND'. The chip is labeled 'RTL8211F(D)(I)'.

Pin	Signal	Pin	Signal	Pin	Signal
1	MDIO+	11	AVDD33	21	REG_OUT
2	MDIO-	12	PHYRSTB	22	DVDD33
3	AVDD10	13	MDIO	23	DVDDRG
4	MDIO+	14	MDIO	24	RXC(PHYAD1)
5	MDIO-	15	MDIO	25	RXC(LPHYAD2)
6	MDIO+	16	TXD0	26	RXC(LPHYAD3)
7	MDIO-	17	TXD1	27	RXC(RDLY)
8	AVDD10	18	TXD0	28	RXC1(TXDLY)
9	MDIO+	19	TXD1	29	RXC2(PLOFF)
10	MDIO-	20	TXD0	30	RXC3(PHYAD0)
					DVDD10

VDD33

AVDD33

DVDD33

Reserved for EMI. (optional)

Close to PHY PIN11 and PIN40 for Analog Power

Close to PHY PIN29 for Digital Power & SWR

LED0/CFG_EXT

R16 4.7K (NC) R17 4.7K

R18 4.7K LED0/CFG_EXT0 R19 4.7K (NC)

R20 4.7K LED0/CFG_EXT0 R21 4.7K (NC)

DVDD33

RGMMI Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V (default)	1'b1	2'b00
External 2.5V	1'b1	2'b01
External 1.8V	1'b1	2'b10
External 1.5V	1'b1	2'b11
Internal 2.5V	1'b0	2'b01
Internal 1.8V	1'b0	2'b10
Internal 1.5V	1'b0	2'b11

DVDDDRG

R22 4.7K (NC) RXD3/PHYAD0 R23 4.7K

R26 4.7K RXC2/PHYA1 R27 4.7K (NC)

R26 4.7K RXCTL/PHYAD2

PHY Address	PHYAD[2:0]
0	3'b000
1 (default)	3'b001
2	3'b010
3	3'b011
4	3'b100
5	3'b101
6	3'b110
7	3'b111

PHY Interface

RXC_N (Close to PHY. Reserved for EMI. (optional))

RXC_N

R47

0

C27

22pF (NC)

R48

0

R49

0

R50

0

R51

0

R52

0

RXD0_N

RXD1_N

RXD2_N

RXD3_N

RXCTL_N

DVDD33

DVDDR33

R6
0

C12
0.1uF

C13
4.7uF

Note 1: R6 is not needed for ONLY 3.3V RGMII application, and DVDDR33 can be connected directly to DVDD33.

Note 2: DVDDR33 must be short (or R6 be mounted) to DVDD33 if the external RGMII 3.3V is selected.

Note 3: R6 must be removed if the internal or external 2.5V/1.8V/1.5V RGMII is selected.

Note 4: CAPs must be closed to pin28 for EMI consideration.

For LDO mode

For SWR mode

Note 1: The Trace length between L1 and PHY Pin 30 must be within 0.5 cm, C6 and C7 to L1 must be within 0.5cm.

Note 2: Bypass CAPs close to PHY DVDD10/AVDD10 power pins.

Note 3: Any inductance or bead except L1 is not allowed on the path from REGOUT to DVDD10/AVDD10.

Note 4: R3 is reserved to change the DVDD10/AVDD10 supply source to LDO mode (RTL8211FD).

Note 5: No design change of PCB model is needed if R3 is reserved. If only RTL8211FD used for particular PCB model, directly short REGOUT to DVDD10/AVDD10.

Note 6: If RTL8211FI is selected, the C6 should be replaced as 10uF X7R capacitor for industrial grade application. Please refer to the datasheet for other industrial grade information.

Note 7: If RTL8211FDI is selected, the C5 should be replaced for industrial grade application and the value is still under testing.