Software Product Lines with Unbounded Parametric Real-Time Constraints



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Integrated Model-based Testing of Continuously Evolving Software Product Lines

ES Real-Time Systems Lab

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Dept. of Computer Science (adjunct Professor)

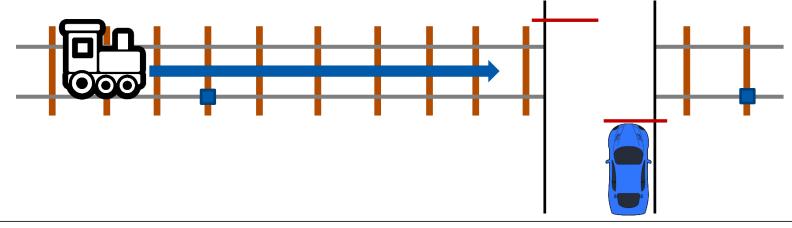
www.es.tu-darmstadt.de

Running Example

[Alur et al. (1993): Parametric Real-time Reasoning]

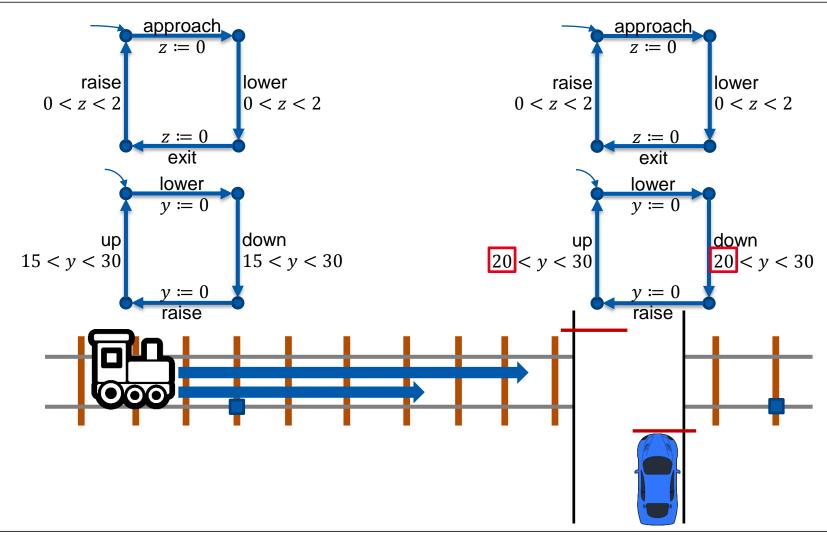


Controller Gate approach, lower Location z = 0Clock **Clock Reset Clock Constraint** down raise lower 0 < z < 215 < y < 3015 < y < 300 < z < 2 $z \coloneqq 0$ raise exit **Switch**



Product Line of TA

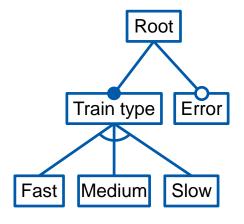




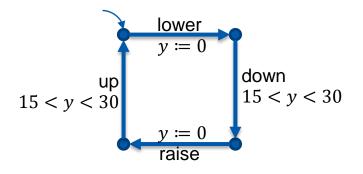
Featured Timed Automata (FTA)

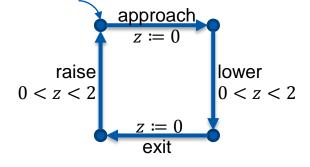
[Cordy et al. (2012): Behavioural Modelling and Verification of Real-Time Software Product Lines]





Presence conditions for clock constraints and switches

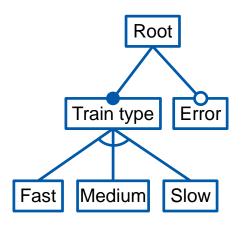


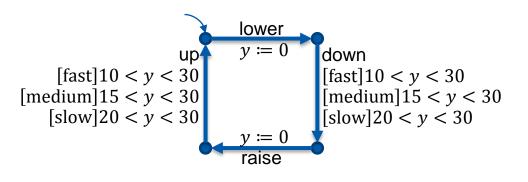


Featured Timed Automata (FTA)

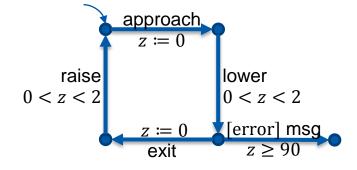
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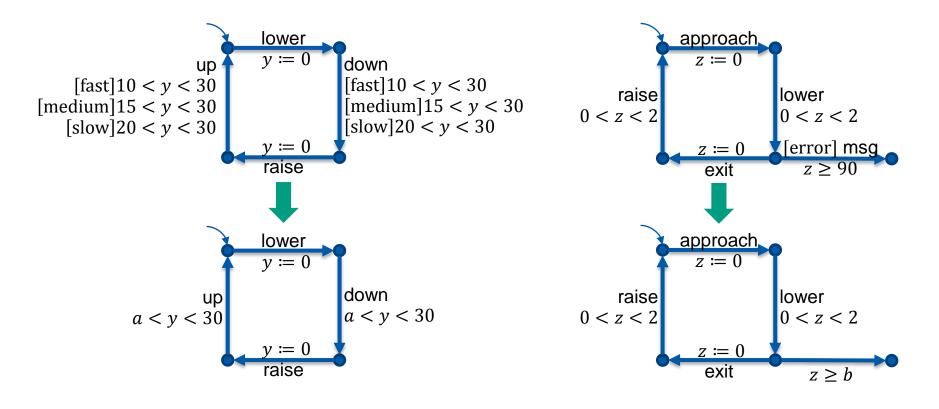
Presence conditions for clock constraints and switches



Parametric Timed Automata (PTA)

[Alur et al. (1993): Parametric Real-time Reasoning]



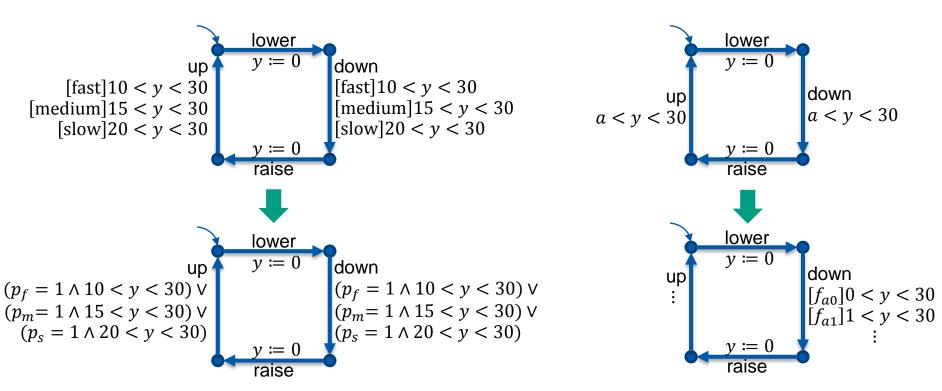


- Unbounded numeric parameters instead of Boolean features
- Results in (potentially) infinite number of configurations



Mutual encoding of FTA and PTA



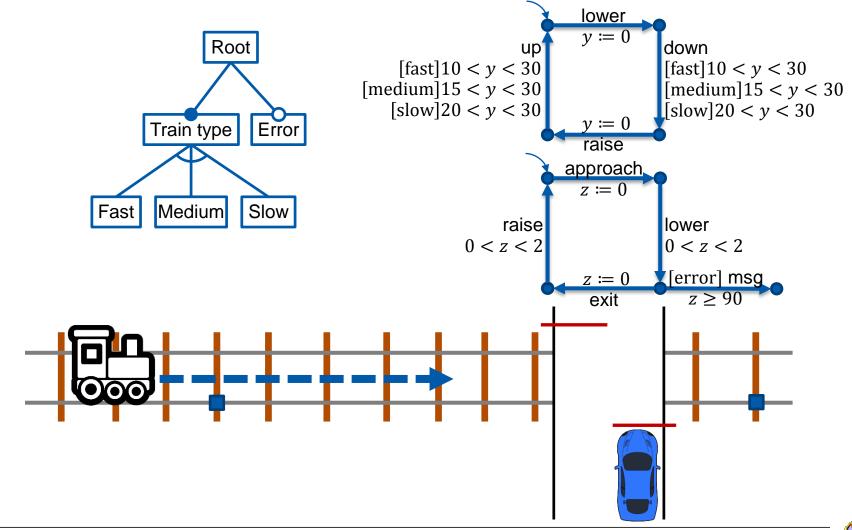


- FTA → PTA: one parameter for each feature
- (Bounded) PTA → FTA: one feature for each parameter valuation
- Restriction: Unbounded parameter domains cannot be mapped



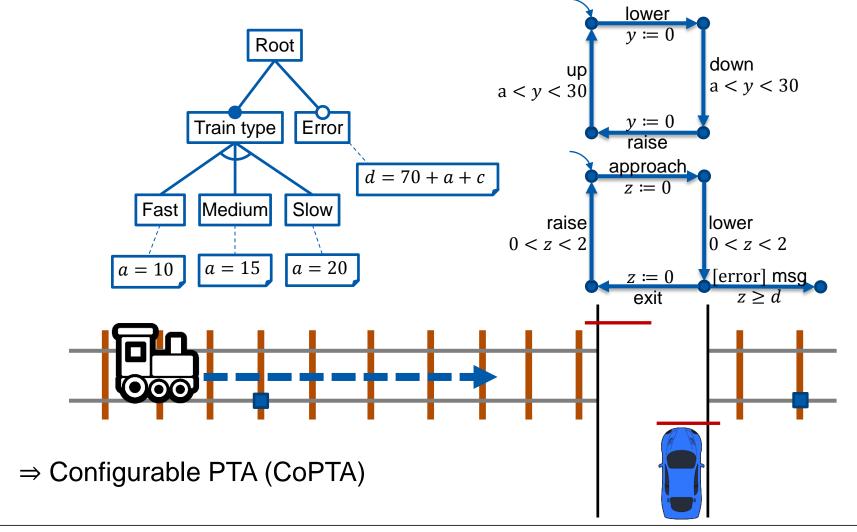
Unbounded Real-Time Constraints





Unbounded Real-Time Constraints

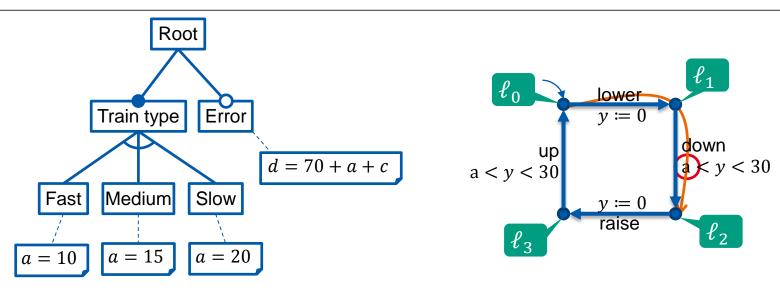




Test-Case Generation

[Bürdek et al. (2015): Facilitating Reuse in Multi-goal Test-Suite Generation for Software Product Lines] [André (2009): IMITATOR: A Tool for Synthesizing Constraints on Timing Bounds of Timed Automata]





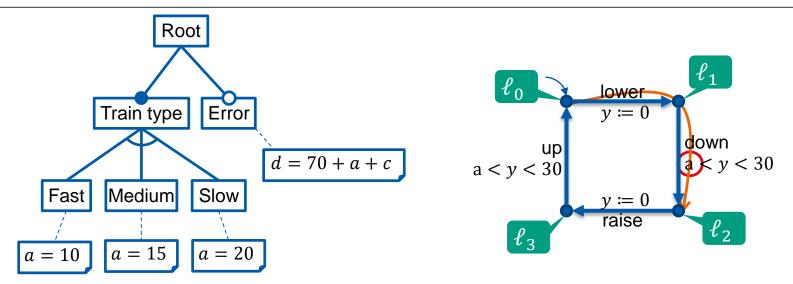
- Test case for ℓ_2 : $\ell_0 \xrightarrow{(7,lower)} \ell_1 \xrightarrow{(12,down)} \ell_2$
- May be reused for ℓ_1 [Bürdek et al., 2015]
- May be reused for configurations with feature fast [Bürdek et al., 2015]
- Implementation based on Imitator [André, 2009]



Test-Case Generation

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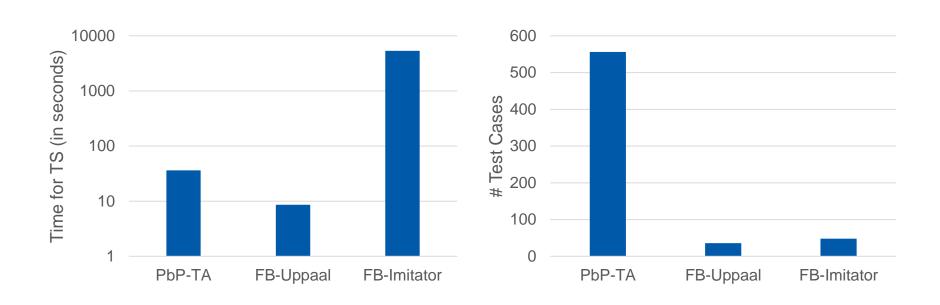


HeliC*PTA



Evaluation (Gear Control)





- Can we reduce computational effort and the test suite size?
- 66 locations
- 22 Variants
- No unbounded parametric variability



Conclusion



- Family-based approach with FTA:
 - Smaller test suite
 - Faster test-suite generation
- Family-based parametric approach with CoPTA:
 - Slower test-suite generation
 - Potentially unlimited amount of variants

 Generate CoPTA models from source code



 $[https://commons.wikimedia.org/wiki/File:Future_plate_blue.svg] \\$



Decidability Properties for PTA

[André (2008): What's decidable about parametric timed automata?]



- \mathcal{P} -emptiness: Is a property satisfiable with a given parameter valuation?
- \mathcal{P} -universality: Is a property satisfiable for all parameter valuations?
- P-finiteness: Is the set which satisfies a given property finite?

Decidability Results for PTA

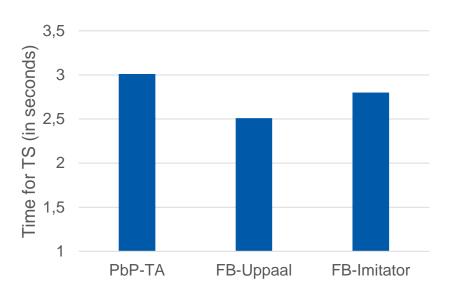
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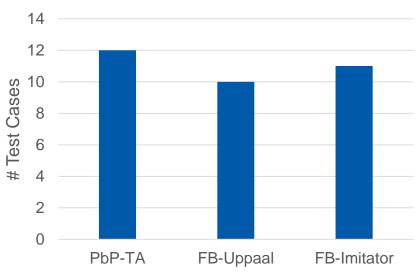


Time Domain	Parameter Domain	P-Clocks	NP-Clocks	Params	Decidable?
\mathbb{N}_0	\mathbb{N}_0	3	0	1	No
\mathbb{R}_+	\mathbb{N}_0	2	any	1	Yes
\mathbb{R}_+	\mathbb{N}_0	3	0	1	No
\mathbb{R}_+	\mathbb{N}_0 (bounded)	any	any	any	Yes
\mathbb{R}_+	\mathbb{Q}_+	1	0	any	Yes
\mathbb{R}_+	\mathbb{R}_+	1	3	1	No

Evaluation (Train-Gate-Controller)







- 12 locations
- 2 Variants
- No unbounded parametric variability

