Evan Lee | elee301@calpoly.edu | github.com/Eclypsee | linkedin.com/in/evan-l-0186302ab

Personal Website

EDUCATION

California Polytechnic State University- *Computer Engineering: GPA: 3.9, 2023-2026*

EXPERIENCE

Frontend and Integration Lead for CodeDay.io

- **Tools used: Javascript, React.js, Pinecone, Vercel, OpenAI API, Fly.io**
- Developed and optimized a custom AI model using Pinecone databases for real-time debugging assistance, improving code error detection accuracy by 15%.
- Collaborated with a diverse engineering team to build a responsive React.js frontend for a web-based debugging platform.
- Integrated and deployed the application on Fly.io, ensuring high availability and continuous uptime.
- Partnered with **CodeDay**, **serving over 70,000 users**, to deliver accessible AI-powered debugging tools, reducing student error-resolution time.

Convolutional Neural Network Developer for Inspirit AI

- **Tools used: Python, Sklearn, Tensorflow, Seaborn**
- Led a team of engineers in developing computer vision software to detect pneumonia from X-ray images.
- Spearheaded the computer vision effort, utilizing TensorFlow and Sklearn to train and deploy a Convolutional Neural Network achieving 90.8% accuracy in pneumonia detection.
- Collaborated cross-functionally to create and present a comprehensive report showcasing the project's success.

Underwater Robotics Embedded Systems Engineer for CalPoly UROV

- **Tools used: STM32, C, Blue Robotics ESC, USART, Fusion 360**
- Developed Thrust Vectoring code using a Moore Penrose pseudo-inverse algorithm for a fully vectored underwater craft.
- Developed a PWM driver utilizing the STM32 Cube IDE that allows for proper control of the T200 thruster using the Blue Robotics BASIC ESC.
- Designed and tested a working 48V to 12V DC/DC converter in Autodesk Fusion 360 that converts and regulates voltage for our manipulator and servos.

PROJECTS

RISC-V MCU on Artix 7 FPGA board

- **Tools used: System Verilog, Basys3 Artix-7 FPGA, Xilinx Vivado, RISC-V Assembly**
- Developing a RISC-V MCU on an Artix-7 Basys3 board using Xilinx Vivado for simulation and synthesis.
- Implemented core components including ALU, registers, memory, control unit, and branch condition generator.
- Integrated a custom CSR for Interrupt Service Routine handling.
- Designed and tested data paths for fetch, decode, execution, memory access, and write-back stages.

Snake Game in RISC-V Assembly

- **Tools used: System Verilog, Basys3 Artix-7 FPGA, Xilinx Vivado, RISC-V Assembly**
- Developed the game snake in a Basys3 FPGA board that displays to a VGA capable display
- Designed the game entirely in RISC-V Assembly utilizing the MMIO system for display, an Interrupt Service Routine for button presses, and a VGA driver that reads from MMIO.

Artix 7 FPGA Memory Recall Puzzle

- **Tools used: System Verilog, Basys3 Artix-7 FPGA, Xilinx Vivado**
- Designed and implemented a memory game on a Basys3 FPGA using Verilog.
- Developed an FSM to control game states (pattern display, user input, pattern comparison).
- Utilized an LFSR for random pattern generation and an accumulator for score tracking.
- Integrated LED and seven-segment displays via a multiplexer, ensuring accurate output.
- Performed functional simulations and timing analysis to validate performance.

TECHNICAL SKILLS

Python, Tensorflow, Seaborn, Sklearn, Solidworks, Java, Javascript, HTML, CSS, Soldering, Onshape, Git, FPGA programming, Pinecone Vector Databases, Vercel, Fly.io, React.js, RISC-V, System Verilog, C, STM32